CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX7032
AIS Rx Data Processor NMEA 0183-HS Output

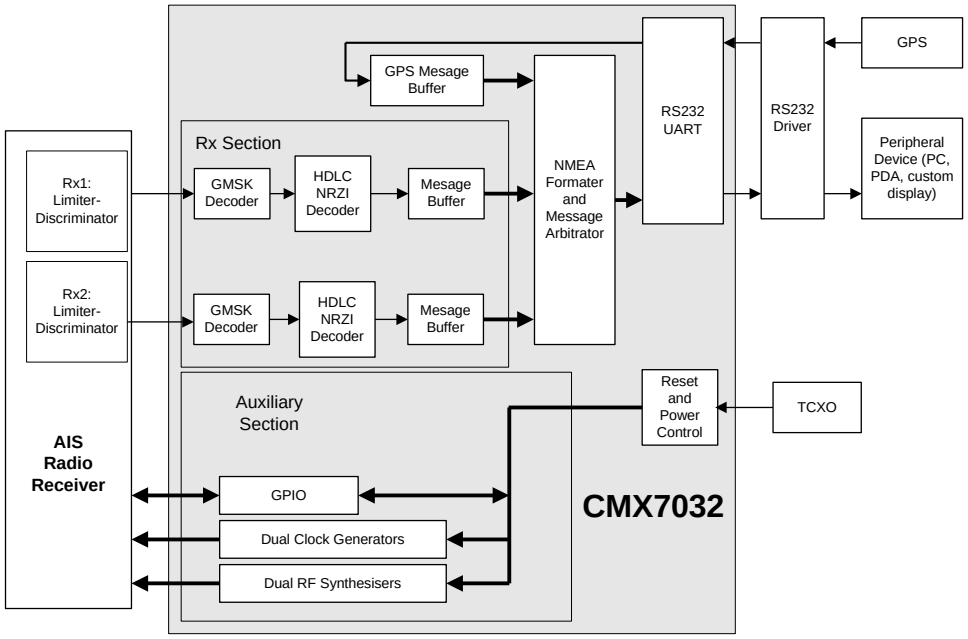
D/7032_FI2.0/9 October 2013

DATASHEET

CMX7032FI-2.x: Marine AIS Rx-only data processor designed for Limiter-Discriminator based RF systems

Features:

- Dual GMSK Demodulators
- AIS Data Output in RS232 – NMEA 0183 Format
- Optimum Rx Co-channel Performance
- Low Profile 64 Pin Leadless VQFN and LQFP Packages
- Configurable by Function Image™ (FI)
- Two RF Synthesisers
- Two Auxiliary System Clock Generators
- Low-Power (3.0V to 3.6V) Operation
- Limiter-Discriminator Rx Interface
- Automatic FI Loading from EEPROM for Host-less Operation
- Automatic Identification System (AIS) for Marine Safety
- Compatible with PE0201 Kit
- Compatible with DE70321 Kit
- For AIS Rx-only Modules



1 Brief Description

A highly integrated Baseband Signalling Processor IC, the CMX7032 used with 7032FI-2.x fulfils the requirements of the Rx-only Marine Automatic Identification System (AIS) receiver market.

The AIS system allows ships and base stations to communicate their position and other data to each other without the need for a centralised controller. This allows vessels to “see” each other and take appropriate action to avoid collision and so improve marine safety. The system uses a GMSK 9600 baud data link in the Marine VHF radio band. The system requirements are defined in ITU-M 1371-4.

When used with the 7032FI-2.x the device operates in a Rx-only mode and comprises two parallel Limiter-Discriminator Rx paths and an RS232 style/NMEA 0183-HS compatible output (38400 baud). The device performs signal demodulation with associated AIS functions, such as training sequence detection, NRZI conversion and HDLC processing (flags, bit de-stuffing, CRC check). Integrated Rx data buffers are also provided which removes the need for a host µC. Provision of a number of user-programmable areas in the FI allows the RF synthesisers of the CMX7032 to be programmed directly, which simplifies the system hardware design, reducing the overall equipment cost and size. Allowance is made in the RS232 interface for an external GPS device to be connected to reduce the proliferation of interface connections in the final product design.7032FI-2.0 is compatible with CMX7032 devices with batch code 67228 or later. Devices from earlier batch codes may be used with care, but are not recommended for production.

The CMX7032 device utilises CML’s proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™: this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external EEPROM or from a host µController over the built-in RS232 serial interface. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

This Datasheet is the first part of a two-part document comprising Datasheet and User Manual: the User Manual can be obtained by registering your interest in this product with your local CML representative. These documents refer specifically to the features provided by Function Image™ 2.x.

CONTENTS

TABLES

FIGURES

1.1 History

Version	Changes	Date
9	• Update which allows GPS baud rate to be set by the state of pin 56 • Update to reflect that pins 15 and 16 will be set low or high at the start or end respectively of a received burst to provide channel status indication • References to ITU-R M.1371-1 changed to '-4' to reflect the latest version of the specification	11/9/13
8	• Update to RF Synthesiser parameters, following evaluation.	29/7/11
7	• Addition of operating voltage range clarification (3.0V to 3.6V) into History files • Reference to "thickstub" tools being removed from section 7.4.2 added into History files. Contact CML for further help on EEPROM in-circuit programming. • Corrected typographical errors in section 9 (V_{DD}, etc). • Function Image™ flowchart (Fig 5) revised to show "$PCML CMX7032-20nn<cr><lf>" as the data string output after successfully loading the FI.	18/9/09
6	• Corrections to BOOTEN pin states, Table 4 • Other minor typographical and stylistic updates • GPS pass-through sentences updated • Power-on reset response updated to include version identification	9/9/09

5	• Correction of FI reference to 2.0 • Correction to signal flow direction on SPI bus and addition of C-BUS Mode connection to Block Diagram (Figure 1) • Emphasis of unused pins which need to be connected to Vss or Vdd, section 3 • Correction to signal flow of Burst_Det and RFVss signals in Figure 3 • Reference to potential FI upgrades and version number reporting added to sections 7.3.3 and 7.4 • Clarification of required clock frequency for operation of CMX7032 with FI-2.0 in section 9.1.2 • Correction of Rx input impedance in parametric specification, section 9.1.3 • Correction of N and R division ratio limits in section 9.1.3 • Clarification of typical and maximum current consumption in section 9.1.3 • Addition/correction of notes 23, 24 and 34 to section 9.1.3 • Clarification of operation of b13 in System CLK 1 and 2 registers, section 11.1.3 • Change status of FI-2.0.0.2 to full release in section 13 • minor editorial changes and clarifications	6/10/08
4	• Text references to SYSCLK1 and 2 corrected in section 11.	22/9/08
3	• EEPROM registers for RF PLL N/R corrected in Table 4 • References to CMX7042 removed • Section 11.1.3, default SYSCLK states and operation of b13 corrected • EEPROM (not C_BUS) locations - Figure 9 corrected • Text regarding HEX files added in section 11	3/9/08
2	• Pin 57 now connected to DVdd. This is required to guarantee reliable operation • Pin 29 now connected to AVss. This is required to guarantee reliable operation • Pin 56 now connected to DVss. This is required to guarantee reliable operation • Information on the Q1 package exposed metal pad added • AIS Channel Number added to Table 2 • Notes 6 and 7 added to Table 1 • Loop filter example changed to coincide with that on DE70321 • CLK, RxIN, PLL, Charge Pump parameters updated • Tcch parameter updated • minor editorial changes and clarifications	31/1/08
1	• Original document	23/7/07

2 Block Diagram

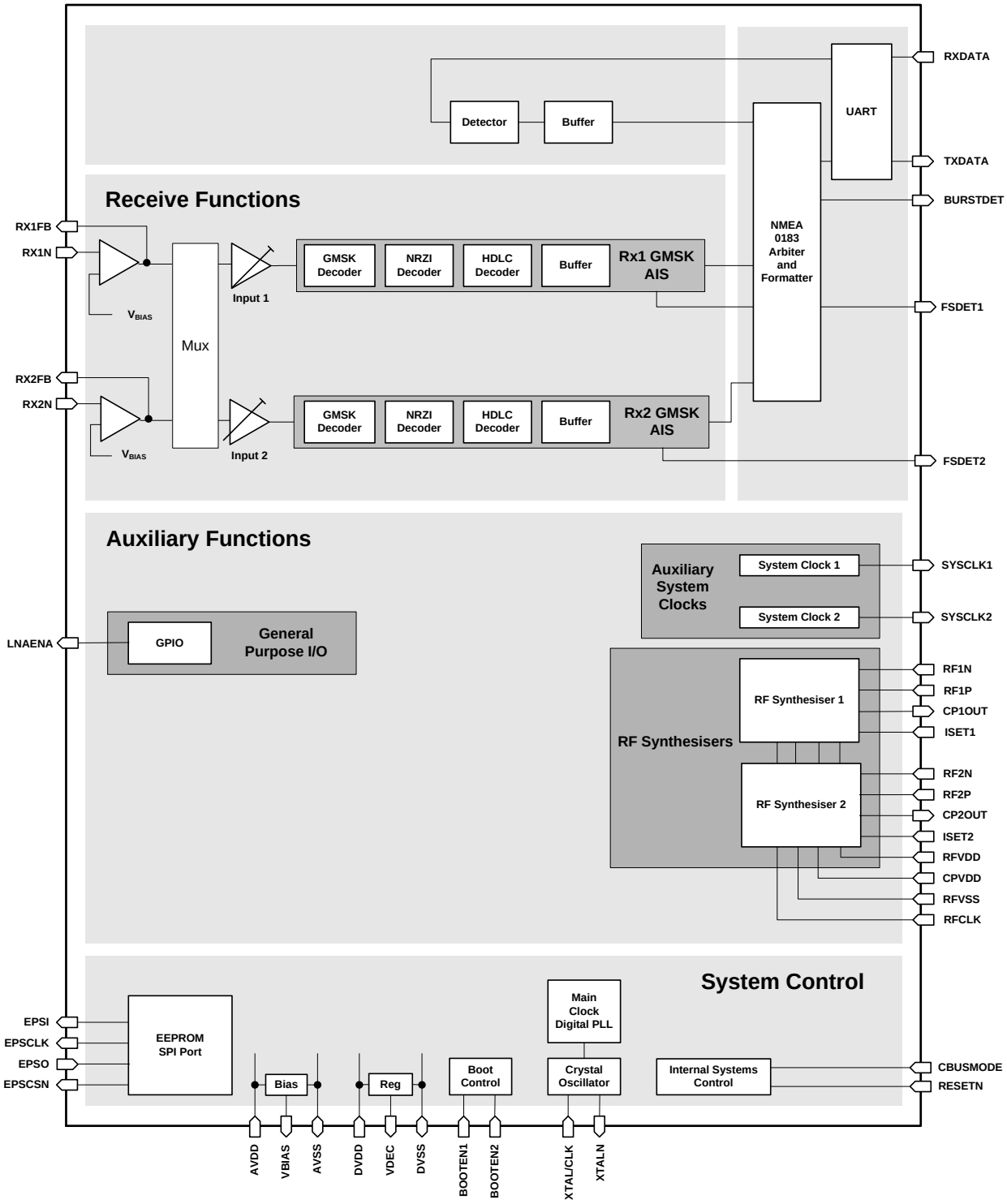


Figure 1 CMX7032 FI-2.x Block Diagram

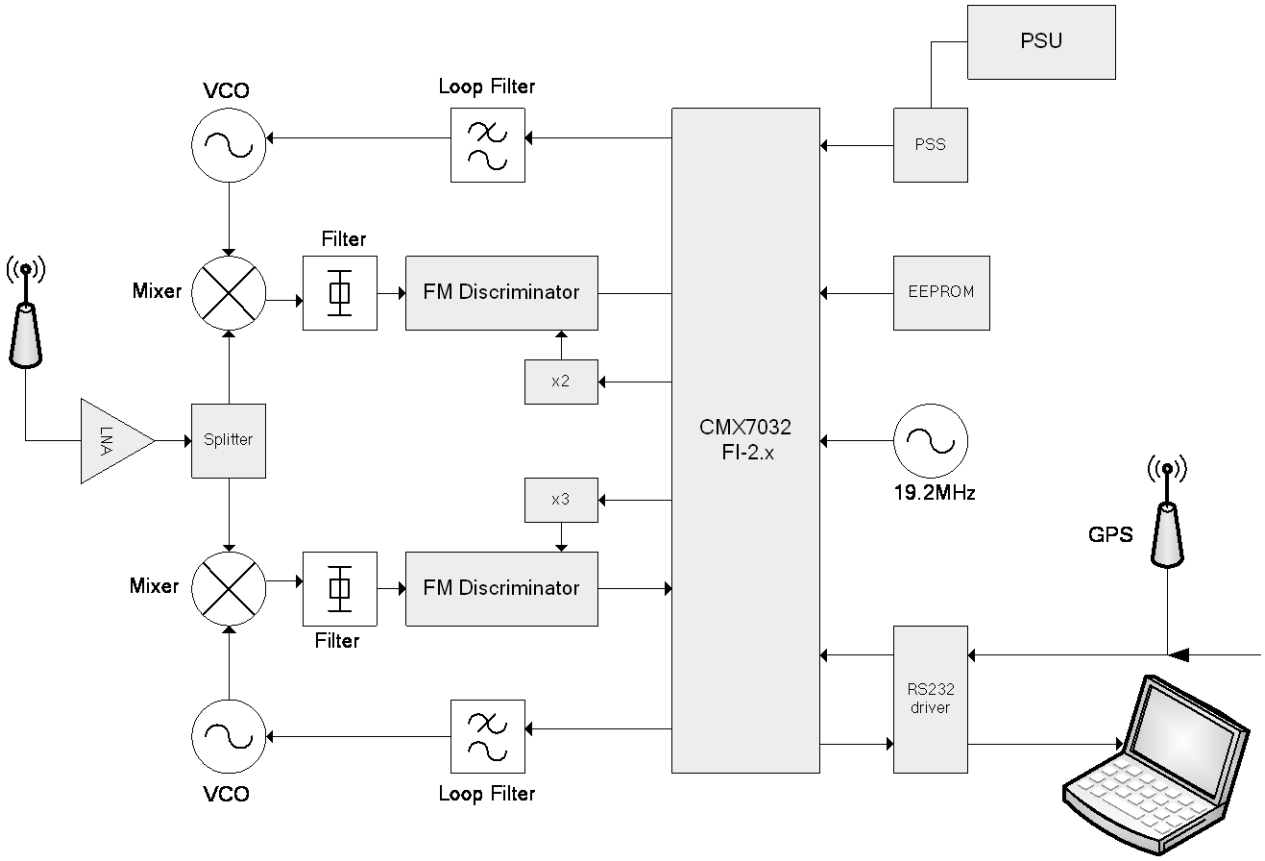


Figure 2 Typical System Block Diagram

3 Signal List

CMX7032 64-pin Q1/L9	Pin Name	Type	Description
1	-	OP	***reserved: connect to DV_{DD} with a 100kΩ resistor***
2	RF1N	IP	RF Synthesiser #1 Negative Input
3	RF1P	IP	RF Synthesiser #1 Positive Input
4	RFVSS	PWR	The negative supply rail (ground) for the RF synthesisers
5	CP1OUT	OP	1st Charge Pump output
6	ISET1	IP	1st Charge Pump Current Set input
7	RFVDD	PWR	The 2.5V positive supply rail for the RF synthesisers. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
8	RF2N	IP	RF Synthesiser #2 Negative Input
9	RF2P	IP	RF Synthesiser #2 Positive Input
10	RFVSS	PWR	The negative supply rail (ground) for the 2nd RF synthesiser
11	CP2OUT	OP	2nd Charge Pump output
12	ISET2	IP	2nd Charge Pump Current Set input
13	CPVDD	PWR	The 3.3V positive supply rail for the RF charge pumps. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins
14	RFCLK	IP	RF Clock Input (common to both synthesisers)[1]
15	FSDET1	OP	Frame Sync Detect 1 – goes low upon detecting the start flag of a received burst on Channel 1 and high at the end of the burst[2]
16	FSDET2	OP	Frame Sync Detect 2 – goes low upon detecting the start flag of a received burst on Channel 2 and high at the end of the burst[2]
17	-	NC	*reserved* – do not connect this pin
18	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for optional connection to RFV_{DD}.
19	-	NC	*reserved* – do not connect this pin
20	SYSCLK1	OP	Synthesized Digital System Clock Output 1
21	DVSS	PWR	Digital Ground
22	-	NC	*reserved* – do not connect this pin
23	LNAENA	OP	LNA_enable: active lo when demodulator is running
24	RX1N	IP	Rx1 inverting input
25	RX1FB	OP	Rx1 input amplifier feedback
26	RX2N	IP	Rx2 inverting input
27	RX2FB	OP	Rx2 input amplifier feedback

[1] To minimise crosstalk, this signal should be connected to the same clock source as XTAL/CLK input. By default, this is connected internally at power-on, alternatively, this may be achieved by connecting the pin to the XTALN output when a 19.2MHz source is in use.

[2] Internal filtering and processing delays should be taken into account when evaluating timings.

CMX7032 64-pin Q1/L9	Pin Name	Type	Description
28	-	NC	*reserved* – do not connect this pin
29	-	IP	***reserved: connect to AV_{SS}***
30	AVSS	PWR	Analogue Ground
31	-	NC	*reserved* – do not connect this pin
32	-	NC	*reserved* – do not connect this pin
33	VBIAS	OP	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.
34	-	NC	*reserved* – do not connect this pin
35	-	NC	*reserved* – do not connect this pin
36	-	NC	*reserved* – do not connect this pin
37	-	NC	*reserved* – do not connect this pin
38	-	NC	*reserved* – do not connect this pin
39	AVDD	PWR	Analogue +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.
40	-	NC	*reserved* – do not connect this pin
41	-	NC	*reserved* – do not connect this pin
42	AVSS	PWR	Analogue Ground
43	-	NC	*reserved* – do not connect this pin
44	-	NC	*reserved* – do not connect this pin
45	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for the optional connection to RFV_{DD}.
46	XTAL/CLK	IP	19.2MHz input from the external clock source
47	XTALN	OP	The output of the on-chip Xtal oscillator inverter. NC as a 19.2MHz Clock source is used
48	DVDD	PWR	Digital +3.3V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins
49	RXDATA	IP	RS232: Serial data input from the µC/GPS
50	TXDATA	TS OP	RS232: Serial data output in NMEA 0183-HS format
51	RESETN	IP+PU	Reset Input
52	DVSS	PWR	Digital Ground
53	-	NC	*reserved* – do not connect this pin
54	BURSTDET	OP	AIS Burst detected – active lo
55	SYSCLK2	OP	Synthesised Digital System Clock Output 2
56	GPSRATE	IP	Determines the GPS baud rate. For 4800 baud connect to DV_{SS}, for 38400 baud connect to DV_{DD} via a 47kΩ resistor.

CMX7032 64-pin Q1/L9	Pin Name	Type	Description
57	CBUSMODE	IP+PD	Connect to DV_{DD}
58	EPSI	OP	EEPROM Serial Interface: SPI bus Output
59	EPSCLK	OP	EEPROM Serial Interface: SPI bus Clock
60	EPSO	IP+PD	EEPROM Serial Interface: SPI bus Input
61	EPSCSN	OP	EEPROM Serial Interface: SPI bus Chip Select
62	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program
63	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program
64	DVSS	PWR	Digital Ground
EXPOSED METAL PAD	SUB	~	On Q1 packages only : the central metal pad may be connected to Analogue Ground (AV_{SS}) or left unconnected. **No other electrical connection is permitted.**

Notes:

IP = Input (+PU/PD = internal pullup/pulldown resistor)
OP = Output
TS OP = 3-state Output
PWR = Power Supply Connection
NC = No Connection

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
RFV_{DD}	RFVDD	Power supply for RF synthesiser circuits
CPV_{DD}	CPVDD	Power supply for RF charge pump
V_{DEC}	VDEC	Power supply for core logic, derived from DV_{DD} by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits
RFV_{SS}	RFVSS	Ground for all RF circuits

4 Recommended External Components

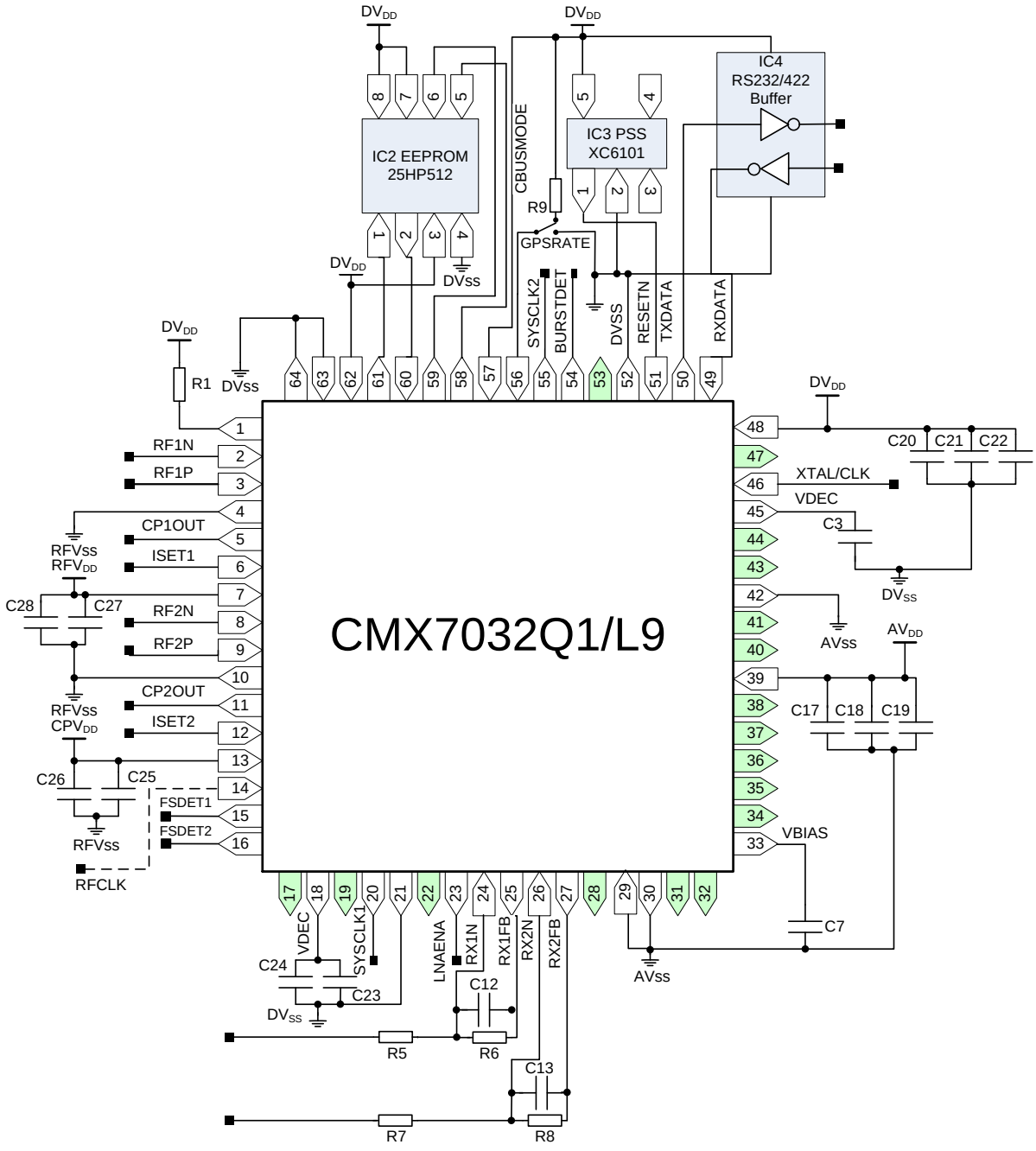


Figure 3 CMX7032 FI-2 Recommended External Components

Table 2 Component Values

R1	100kΩ	C3	10nF	C21	10nF	IC2	25HP512
R5	100kΩ - note 2	C4	not fitted	C22	10nF	IC3	XC6101
R6	100kΩ	C7	100nF	C23	10nF	IC4	ADM1385
R7	100kΩ - note 3	C12	47pF	C24	10µF		
R8	100kΩ	C13	47pF	C25	10nF		
R9	47kΩ - note 8	C17	10µF	C26	10µF		
		C18	10nF	C27	10nF	XTAL/CLK	19.2MHz
		C19	10nF	C28	10µF		See note 1
		C20	10µF				

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. CLK is a 19.2MHz external clock generator.
2. R5 should be selected to provide the desired dc gain of the input, as follows:

$$|GAIN_{RX1N}| = 100k\Omega / R5$$

   The gain should be such that the resultant output at the RX1FB pin is within the input signal range specified in 9.1.3.
3. R7 should be selected to provide the desired dc gain of the input as follows:

$$|GAIN_{RX2N}| = 100k\Omega / R7$$

   The gain should be such that the resultant output at the RX2FB pin is within the input signal range specified in 9.1.3.
4. Care should be taken in connecting the output of the Limiter-Discriminator device to the Rx input pins of the CMX7032. The format of the GMSK signal requires that the frequency response of the input circuits extends to below 10Hz, however the variations in the incoming AIS signals from many different stations require that the input must rapidly follow the changes in dc and signal levels without de-grading the signal seen at the Rx input pins.
5. C12 and C13 should be chosen to minimise the phase distortion of the input signal and provide a flat amplitude response up to at least 4800Hz.
6. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both V_{DEC} pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each V_{DEC} pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both V_{DEC} pins.
7. The BOOTEN pins (pins 62 and 63) are configured in this diagram for loading from EEPROM, other loading modes are available see section 7.4.
8. Pin 56 (GPSRATE) – connect to DV_{SS} or pull high to DV_{DD} via R9.

5 PCB Layout Guidelines and Power Supply Decoupling

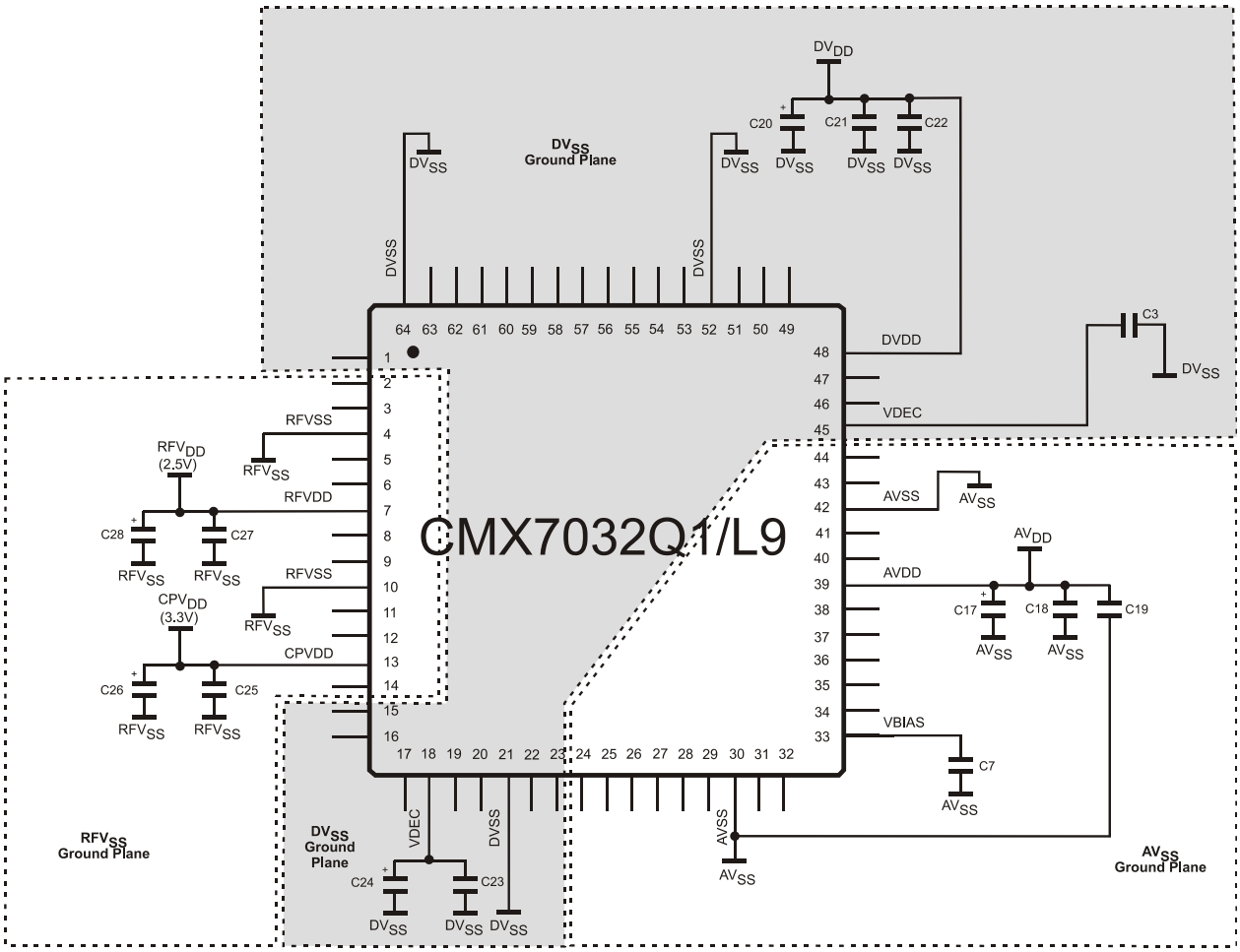


Figure 4 CMX7032 Power Supply Connections and De-coupling

Component Values as per Table 2.

Notes**:**

1. It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX7032 and the supply and bias de-coupling capacitors. The supply decoupling capacitors should be as close as possible to the CMX7032. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS}, RFV_{SS} and DV_{SS} supplies in the area of the CMX7032, with provision to make links between them close to the CMX7032. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

2. The central metal pad (which is exposed on Q1 package only) may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AV_{SS}). **No other electrical connection is permitted.**

3. V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled to ensure its integrity so, apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with an external high input impedance buffer.

4. The 2.5V V_{DEC} output can be used to supply the 2.5V RFV_{DD}, to remove the need for an external 2.5V regulated supply. VDEC can be directly connected to RFVDD.

6 General Description

6.1 Overview

Rx Modem Functions

- Fixed modulation format:
  - AIS 25kHz channel (GMSK, 9600bps, 2.4kHz deviation, BT=0.4)
- Simultaneous reception of two AIS channels
- AIS Burst mode with full AIS frame formatting (HDLC-type)
  - Frame sync recognition
  - Bit de-stuffing
  - NRZI decoding
  - Training sequence and start/stop flag detection
  - CRC checking
- Four 160 byte Rx data buffers can automatically store up to four 5-slot AIS bursts (2 per Rx channel)
- Rx signal input gain

100 - 600 MHz RF Synthesisers

- Two Integer-N synthesisers
- Flexible design minimizes reference spurs for low phase noise results
- Charge pump
  - High/low soft selectable current setting to speed large frequency channel changes
  - Nominal current user defined by external resistor value

I/O Functions

- Output port to enable external LNA circuit
- Output port to indicate valid AIS burst received

System Functions

- All internal subsystems are controlled from the Function Image™ so removing the need for a host µC
- Internal system clocks derived from RF synthesiser reference oscillator eliminate the need for additional clock oscillator(s)
- User clock synthesisers generate two clocks for external use
- Function Image™ loads and executes directly from low-cost EEPROM
- Integrated 2.5V regulator can develop 2.5V from required 3.3V supply
- RS232 interface allows external GPS input to be connected and the data passed-through to the peripheral device. The GPS baud rate is selectable to either 4800 or 38400 baud.

6.2 AIS System Formats

The AIS system uses two basic channel access mechanisms – Self Organising Time Division Multiple Access (SOTDMA) and Carrier-Sensing Time Division Multiple Access (CSTDMA). The 7032FI-2.0 is compatible with both systems. The SOTDMA system is detailed in ITU-R M.1371-4 and IEC 61993-2 while the CSTDMA is detailed in IEC 62287.

The CSTDMA system is used in the implementation of the Class B-CS AIS. This requires the Receiver to monitor the first part of a slot for an existing AIS transmission from another station before deciding to use the slot for its own transmission or aborting and selecting a different slot.

The SOTDMA system is used in the Class A and Base Station AIS as well as the Class B-SOTDMA AIS standard.

The device will transfer all currently known AIS messages and formats, it is the peripheral device that must convert them into the relevant format for the user.

The relevant International standards are:

[0]	ITU-R M.1371-4
[1]	IEC 61993-2 Class A
[2]	IEC 62287-1 Class B CSTDMA
[3]	IEC 62287-2 Class B SOTDMA
[4]	IEC 62320-1 Base Station
[5]	IEC 62320-2 Aids to Navigation
[6]	IEC 61162 NMEA data format

7 Detailed Descriptions

7.1 Clock Source

The 7032FI-2.x must be used with a 19.2MHz oscillator. The RFCLK on the CMX7032 should also be derived from this source to avoid the generation of unwanted spurious signals. The default settings route the RFCLK directly from the XTAL/CLK pin internally, so no external connection is required in this configuration.

7.2 Power Supply

The CMX7032 is designed to function using the V_{DD} values shown in section 9.1.2. To achieve the published performance figures it is necessary to ensure that all power supplies are adequately de-coupled to remove spurious signals or noise. The CMX7032 stores the Function Image™ internally in static RAM, therefore it is imperative that DV_{DD} is maintained at all times to ensure the correct operation of the device. It is recommended that an external power supply supervisor is connected to the RESETN pin so that the device can be reset to its default state in the event of the power supply voltage being outside the specified levels (brown-out protection).

Care should be taken in the design of the power supply circuits to ensure that DV_{DD} power-on rise time characteristic allows the BOOTEN pins to achieve their correct state before the device becomes active.

7.3 Peripheral Interface

This section provides a general description of the RS232 serial interface protocol used to transfer data between the CMX7032, used with 7032FI-2.x, and the peripheral device.

7.3.1 Interface Hardware

The 7032FI-2.x receives AIS data bursts and after extracting the information from them, re-formats them into the NMEA 0183 format as defined in IEC 62287, IEC 61993 and IEC 61162 and outputs them on the TXDATA pin of the RS232 UART at 38400 baud, 8 bits, no parity. No hardware or software handshaking is implemented. A suitable level shifter/inverter/buffer should be used to interface this signal to the peripheral device for true RS232 or RS422 compatibility.

7.3.2 Interface Format

The 7032FI-2.x will only output data if the AIS burst has been correctly decoded with a valid CRC field. All bursts that have detected errors will be discarded. All error-free bursts will be presented at the TXDATA pin, irrespective of their data content, up to the maximal length of the data buffer, therefore it is the responsibility of the peripheral device to decode the NMEA 0183 data message as appropriate. This ensures that any changes or additions to the AIS messages or structures will not adversely affect the operation of the 7032FI-2.x. The 7032FI-2.x has been successfully tested with a number of commercial PC-based and PDA software packages[3].

The NMEA message structure is defined in IEC 61162 for AIS applications using the “encapsulated message” format, as shown in Table 3.

[3] See www.shipplotter.com for a suitable PC-based software package. Others are available.

Table 3 Message Structure

!AIVDM,x1,x2,x3,a,c--c,x4*hh<CR><LF>

ASCII	HEX	Description
!	21	Start of Sentence: starting delimiter.
AIVDM		Address Field: identifying type of talker and sentence format.
,	2C	Field Delimiter: starts each field except address and checksum fields.
x1		Total Number of Sentences field: encapsulated information often requires more than one sentence.
x2		Sentence Number Field: identifies which sentence of the total number of sentences this is.
x3		Sequential Message Identifier Field: field is incremented each time an encapsulated message is generated with the same formatter as a previously encapsulated message.
a		AIS Channel (A or B)
c--c		Data Sentence Block: AIS data coded as 6-bit fields.
x4		Fill Bits Field: represents the number of fill bits added to complete the last six-bit coded character.
*	2A	Checksum Delimiter: indicates that the following two alphanumeric characters show the HEX value of the checksum.
hh		Checksum Field: calculated by exclusive-OR'ing the 8 data bits (no start bits or stop bits) of each character in the sentence, between, but excluding "!" and "*". The hexadecimal value of the most significant and least significant 4 bits of the result are converted to two ASCII characters (0-9, A-F (upper case)) for transmission.
cr	0D	Carriage return.
lf	0A	Line feed.

The message has a maximum length of 80 characters, which can be easily exceeded by an AIS message, so the multi-sentence feature is used in most cases. Some peripheral equipment is available which can handle messages in excess of the standard limit, in which case a bit in the User Configuration register can be used to instruct the CMX7032 to ignore the limit and produce a single sentence. This feature can increase the efficiency of the RS232 interface but should be used with caution.

7.3.3 Operational Mode

The 7032FI-2.x has no user selectable modes of operation. It is entirely autonomous in its operation and if the device is configured to load the FI from EEPROM, then there is no host or µcontroller interaction required.

Once the device has powered up, it will check the BOOTEN pins for their status, and if set for EEPROM mode, will load the FI automatically. Once successfully loaded, it will output the proprietary NMEA 0183 data string:

$PCML CMX7032-2010<cr><lf>

to indicate that it is now operating. The User Configuration registers will then be read and the SYSCLKs and RF PLLs set up accordingly. (Note: FI version 2.0.0.2 does not report the version number in the data string).

As soon as the start of a burst is detected on either channel at the RX1N and RX2N inputs, the FSDET1 or FSDET2 pin will be set low until the end of the received burst. These pins therefore act as channel status indicators and will behave in the same way regardless of the message type (valid, invalid or corrupt). The device will then begin to attempt to decode the signal and once a valid preamble and start flag has been detected, place the received data into its internal buffer. On reception of a stop flag it will then decode the data and check the received checksum field. If the checksum indicates that the message has been received with no errors, it will then be passed to the NMEA formatter and placed in the output buffer. The device will automatically return to decoding signals at its input. Note that should a stop flag not be detected within the maximum allowed AIS message length, then the decode process will be reset and restarted automatically. The conditions that result in a message being discarded are:

- **Message too long or missing end flag**
  This indicates that the received message, after bit de-stuffing, is too long to fit into the internal message buffer. This condition could be caused by a missing or corrupted end flag.
- **CRC mismatch**
  This indicates that the received frame checksum does not match that calculated by the CMX7032, most probably as the result of one or more message bits being corrupted.
- **New frame header found when message buffer full**
  This happens if the internal message buffers are still in use when another message arrives.
- **End flag not on byte boundary**
  This indicates that the received message, after bit de-stuffing, is not a multiple of 8 bits. Assuming that the message was transmitted correctly, probably caused by an end flag being missed due to noise, and a subsequent message's start flag being mis-identified as the expected end flag or a bit error causing the bit de-stuffer to fail.

This process is performed on both Rx channels in parallel, but the NMEA data formatter will present the first decoded message to the RS232 UART while holding the second message in its internal buffer so that no data is lost. As there is no provision for handshaking on the UART, the peripheral device must be capable of reading the data back at the full 38400 baud rate, otherwise some data may be lost or the message corrupted. An active low pulse will be output on the BURSTDET pin when an AIS message is being transmitted over the RS232 port.

7.3.4 GPS Pass Through

Many applications (eg: chart plotter) also require an input from a positioning device. This is usually accomplished using a GPS unit. If the peripheral device has a limited number of communications ports, it is possible to attach the GPS sensor to the CMX7032 RS232 input, where it is turned round, so as to present both GPS and AIS data to the peripheral device on the IC's RS232 output.

Whenever the device is not actively outputting received AIS data, it will monitor the RXDATA pin for a valid GPS NMEA sentence (at either 4800 or 38400 baud, depending on the setting of pin 56). If a message with a valid GPS identifier is found, it will be placed in the buffer and be output on the TXDATA pin at 38400 baud. Note that while the 7032FI-2.x is receiving data on the RXDATA pin it cannot output AIS data on the TXDATA pin at the same time due to the difference in baud rates. For this reason, the GPS sentences are checked for a valid header so that the 7032FI-2.x can return to AIS output mode as soon as possible, so as to avoid buffer over-runs and potential loss of AIS data on a busy channel.

The valid GPS identifiers that are checked for are:

- $--GGA
- $--GLL
- $--GSA
- $--GSV
- $--RMC
- $--VTG
- $--DSC
- $--DSE

All other messages are discarded

Once a message from the GPS has been received by the device, it will check the AIS buffers for data. This means that if the GPS sends multiple messages in quick succession, some may be ignored in preference to the AIS data.

7.4 Function Image™ Load

The Function Image™ (FI) file, which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software or an Intel HEX file which can be programmed into an external EEPROM. The maximum possible size of Function Image™ is 46kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or after the RESETN pin returns high and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored by the CMX7032 until the next power-up.

Each time the device is powered up its Function Image™ must first be loaded. This assigns internal device resources and determines all device features. The device does not operate until the Function Image™ is loaded.

The BOOTEN pins are both fitted with internal 100k (approx.) pull down resistors.

For EEPROM load, only BOOTEN1 needs to be pulled high, however, if it is required to program the EEPROM in-situ from the host, either jumpers to V_{DD} or links to host I/O pins should be provided (see Table 4). Note that the BOOTEN pins MUST be in a valid state at power-up.

Once the FI has been loaded, the CMX7032 performs these actions:

(1) the product identification code and FI version number is reported e.g $PCML CMX7032-2010. (The 2.0.0.2 release does not include the version number).
(2) LNAENA output pin is cleared to 0.

If an invalid device is detected, the device will become unresponsive and a power-on reset is required to recover from this state.

Table 4 BOOTEN Pin States

	BOOTEN2	BOOTEN1
RS232 Host load	1	1
reserved	1	0
EEPROM load	0	1
No FI load	0	0

Note: DV_{DD} MUST be maintained at all times to preserve the Function Image™ data. If DV_{DD} is suspected of exceeding the specification limits, then a full power-on reset and an FI re-load should be performed to maintain the integrity of the device.

7.4.1 FI Loading from EEPROM

If the ‘C’ header file is used then the FI must be converted into a format suitable for the EEPROM programmer (normally Intel Hex) and loaded into the EEPROM either by a host or an external programmer. Alternatively, the CML Technical Portal also holds an Intel HEX file of the same FI. Any changes to the User Configuration registers must be completed before programming the EEPROM, either by changing the ‘C’ header file or the data in the EEPROM programmer’s buffer. The CMX7032 needs to have the BOOTEN pins set to EEPROM load, and then on power-on, the CMX7032 will automatically load the data from the EEPROM.

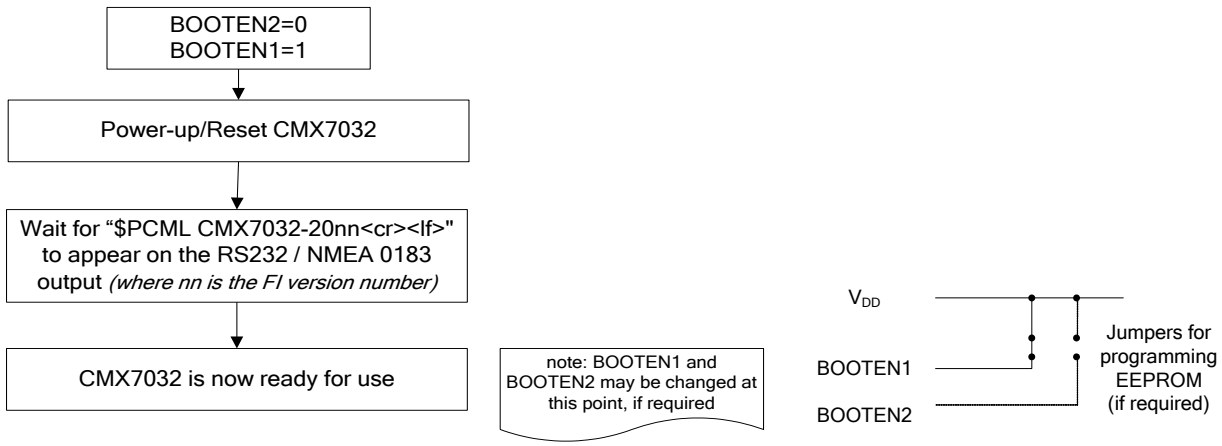


Figure 5 FI Loading from EEPROM

The CMX7032 has been designed to function with Atmel AT25HP512 serial EEPROM and the ATF512 flash EEPROM devices[4], however other manufacturers' parts may also be suitable. The time taken to load the FI is dependant on the XTAL/CLK source frequency, but should be less than 500ms.

7.4.2 FI Loading from Host Controller

The FI can be included into a host controller software build and downloaded into the CMX7032 at power-up over the RS232 interface. The BOOTEN pins must be set to the RS232 load configuration, the XTAL/CLK source set to 6.144MHz and the CMX7032 powered up. The data can then be sent directly over the RS232 to the CMX7032 at 115200baud. Following a successful FI load, the XTAL/CLK source should be returned to 19.2MHz to ensure correct operation. Further details of the data format and process are available through the CML Technical Portal.

[4] Note that these two memory devices have slightly different addressing schemes. FI-2.x is compatible with both schemes.

8 System Description and Tasks

This section describes the operation of main sections of the 7032FI-2.x and the interface provided to the external device(s).

8.1.1 Signal Routing

The 7032FI-2.x provides processing capability for two simultaneous AIS receive channels which are allocated to the RX1N and RX2N pins of the device. Both of these inputs are configured around an inverting op-amp stage to facilitate gain and filtering adjustments.

8.1.2 Operating Modes

The 7032FI-2.x automatically enters into its Operating mode when the Function Image™ has been successfully loaded. If the 7032FI-2.x does not load correctly the device will not operate.

8.1.3 Modem and Data Units

The 7032FI-2.x is logically divided into two main units, each of which can accept and perform tasks separately:

- Modem Unit
- Data Unit

The Modem Unit is primarily responsible for processing the Rx input signals to recover the Rx data they represent and storing that data in the internal Rx data buffers.

The Data Unit is primarily responsible for transferring and arbitrating data from the internal data buffers (including the external GPS input) to the RS232 interface and converting the data into NMEA 0183 format.

8.1.4 Rx Operation

Typical stages of Rx task operation are depicted in Figure 6 and occur as follows:

1. A Modem task is automatically started on power up and continues to run indefinitely. This instructs the IC to transfer any received data from the Rx1/2 Modems to the Rx1/2 Data Buffers.
2. The RxBRDY flags indicate to the Data Arbiter that data is ready and outputs it to the RS232 UART in NMEA 0183 format.
3. After the data has been sent, the Data Arbiter will re-check the Rx1/2 Data Buffers for valid data and output it as in Step 2.
4. If there is no data in Rx1/2 data buffers, the Data Arbiter will re-set the RS232 UART to 4800 baud and check for valid GPS data. If valid GPS data is detected, it will be loaded into the GPS data buffer and when complete, will be re-output at 38400baud.

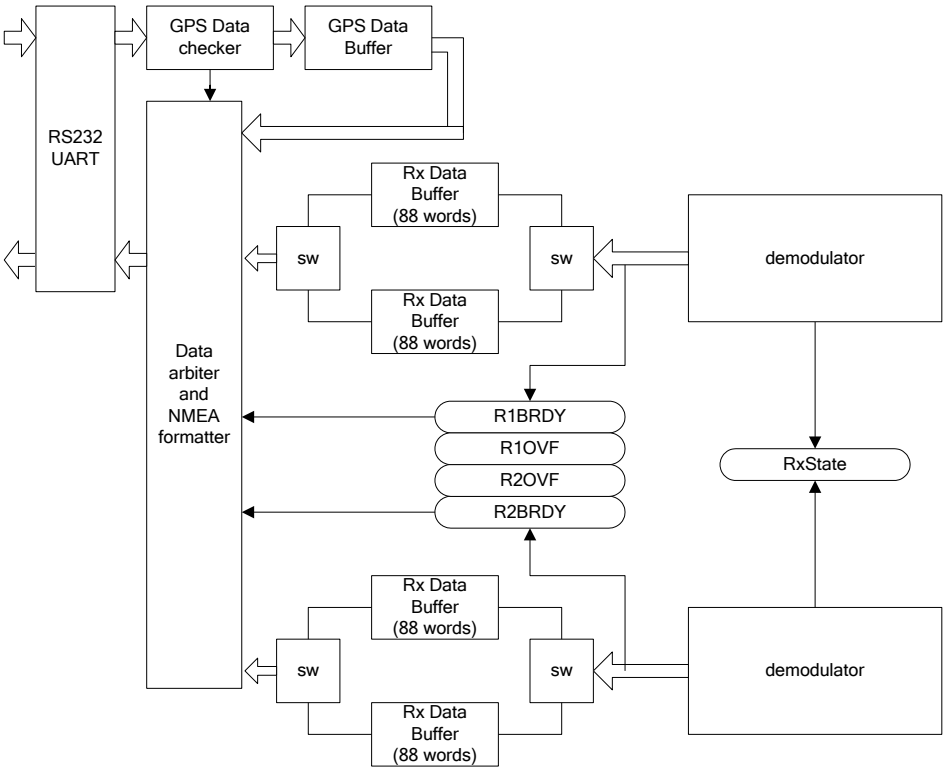


Figure 6 Rx Task Operation

8.2 Configuration Options

The device allows some of its parameters to be configured to a particular target application by changing the values of the User Configuration register locations of the FI (see User Manual section 10).

- RF PLL 1
- RF PLL 2
- SysCLK1
- SysCLK2
- NMEA 0183 sentence mode

8.3 RF Synthesiser

The CMX7032 includes two Integer-N RF synthesisers, each comprising a divider, phase comparator and charge pump. The divider has two sets of N and R registers: one set can be used for transmit and the other for receive. The division ratios can be set up by means of the User Configuration registers in the FI.

External RF components are needed to complete the synthesiser circuit. A typical schematic for one synthesiser, with external components, is shown in Figure 7.

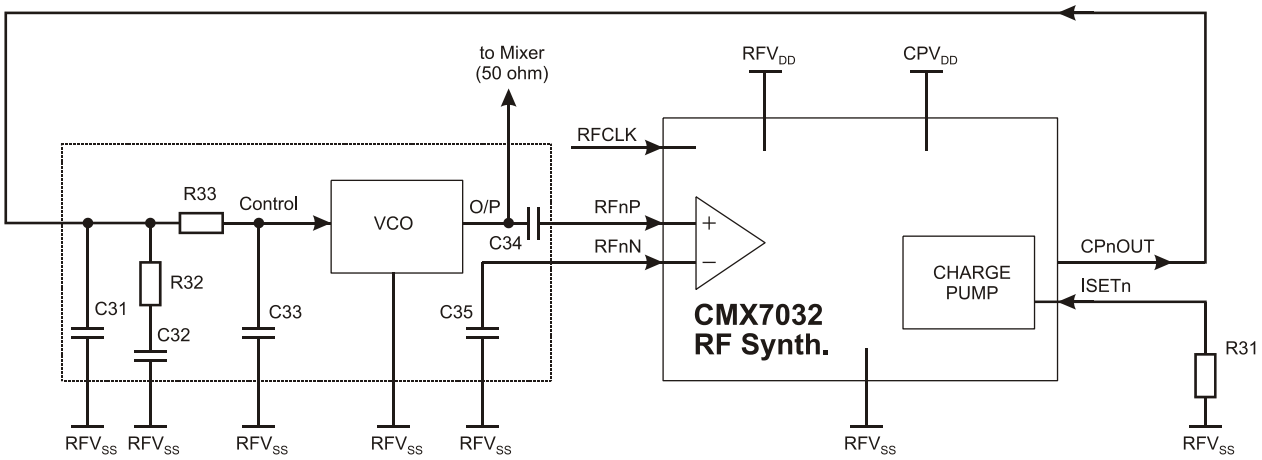


Figure 7 Example RF Synthesiser Components

R31	0Ω	C31	68nF
R32	820R	C32	470nF
R33	0Ω	C33	Not Fitted
		C34	1nF
		C35	1nF

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Note: R31 is chosen within the range 0Ω to 30kΩ and selects the nominal charge pump current.

It is recommended that C34 and C35 are kept close to the VCO and that the stub from the VCO to the CMX7032 is kept as short as possible. The loop filter components should be placed close to the VCO.

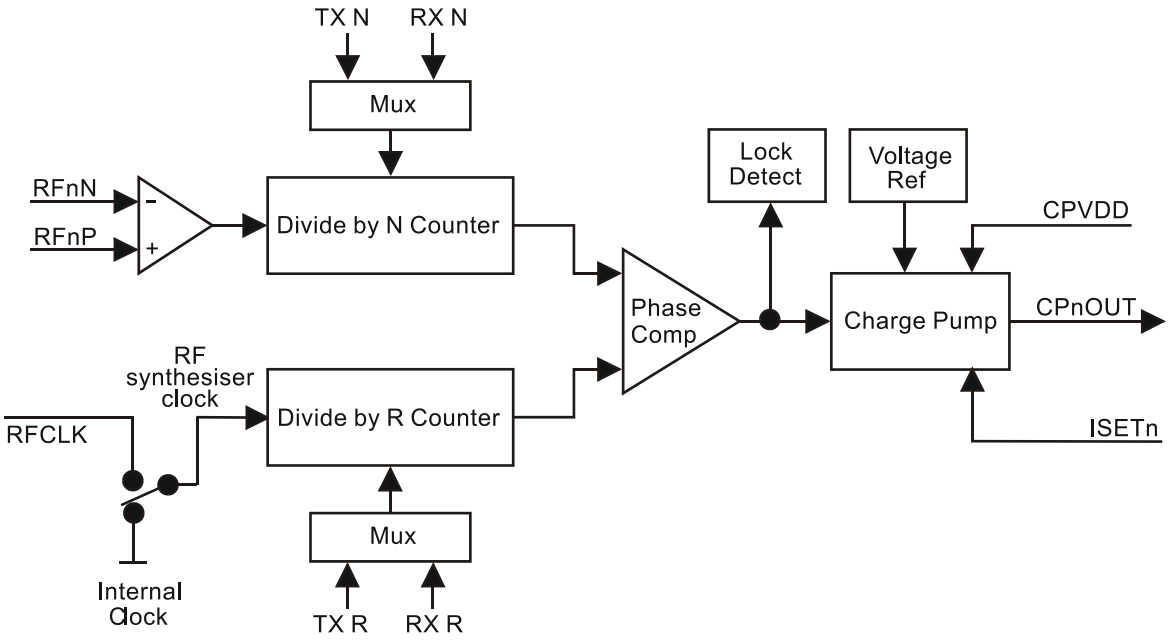


Figure 8 Single RF Synthesiser Block Diagram

The two RF synthesisers are programmable to any frequency in the range 100MHz to 600MHz. Figure 8 is a block diagram of one synthesiser channel. The RF synthesiser clock is the same 19.2MHz clock as is used by the baseband circuitry. The RF synthesiser clock is common to both channels. The charge pump supply (CPV_{DD}) is also common to both channels. The RF input pins (RFnN and RFnP), CPnOUT, ISETn and RFV_{SS} pins are channel specific and designated as either RF1P, RF1N, CP1OUT, ISET1, RFV_{SS} or RF2P, RF2N, CP2OUT, ISET2, RFV_{SS} on the Signal List in section 3. The N and R values for Tx and Rx modes are channel specific. The divide by N counter is 20 bits; the R counter is 13 bits. Typical external components are shown in Figure 7.

Both synthesisers are phase locked loops (PLLs) of the same design, utilising external VCOs and loop filters. The VCOs need to have good phase noise performance although it is likely that the high division ratios used will result in the dominant noise source being the reference oscillator. The phase detectors are of the phase-frequency type with a high impedance charge pump output requiring just passive components in the loop filter.

Two levels of charge pump gain are available to the user, to facilitate the possibility of locking at different rates under program control. A current setting resistor (R31) is connected between the ISETn pin (one for each PLL system) and the respective RFV_{SS}. This resistor will have an internally generated band gap voltage expressed across it and may have a value of 0Ω to 30kΩ, which (in conjunction with the on-chip series resistor of 9.6kΩ) will give charge pump current settings over a range of 2.5mA down to 230µA (including the control bit variation of 4 to 1). The value of the current setting resistor (R31) is determined in accordance with the following formulae:

gain bit set to 1: R31 (in Ω) = (24/Icp) – 9600
gain bit cleared to 0: R31 (in Ω) = (6/Icp) – 9600
where Icp is the charge pump current (in mA).

Note that the charge pump current should always be set to at least 230µA. The 'gain bit' refers to either bit 3 or bit 11 in the RF Synthesiser Control register.
The step size (comparison frequency) is programmable; to minimise the effects of phase noise this should be kept as high as possible. This can be set as low as 2.5kHz (for a reference input of 20MHz or less), or up to 200kHz – limited only by the performance of the phase comparator.

The frequency for each synthesiser is set by using two registers: an 'R' register that sets the division value of the input reference frequency to the comparison frequency (step size), and an 'N' register that sets the division of the required synthesized frequency from the external VCO to the comparison frequency. This yields the required synthesized frequency (Fs), such that:

$$Fs = (N / R) \times F_{REF}$$ where F_{REF} is the selected reference frequency

Other parameters for the synthesisers are the charge pump setting (high or low)

- Since the set-up for the PLLs takes 4 x "RF Synthesiser Data register" writes it follows that, while updating the PLL settings, the registers may contain unwanted or intermediate values of bits. These will persist until the last register is written. The names "Tx" and "Rx" are arbitrary and may be assigned to other functions as required. They are independent sets of registers, one of which is selected to command each PLL by changing the settings in the RF Synthesiser Control register.

For optimum performance, a common master clock should be used for the RF synthesisers (RFCLK) and the baseband sections (Main and Auxiliary System Clocks). Using unsynchronised clocks can result in spurious products being generated in the synthesiser output and in some cases difficulty may be experienced with obtaining lock in the RF synthesisers. The 7032FI-2.x is configured to use the internal clock for both RF synthesisers by default.

Lock Status

The lock status is not available on this FI.

RF Inputs

The RF inputs are differential and self-biased (when not powersaved). They are intended to be capacitively coupled to the RF signal. The signal should be in the range 0dBm to –20dBm (not necessarily balanced). To ensure an accurate input signal the RF should be terminated with 50Ω as close to the chip as possible and with the "P" and "N" inputs capacitively coupled to the input and ground, keeping these connections as short as possible. The RF input impedance is almost purely capacitive and is dominated by package and printed circuit board parasitics.

Guidelines for using the RF Synthesisers

- RF input slew rate (dv/dt) should be 14 V/µs minimum.
- The RF Synthesiser 2.5V digital supply (RFVDD) can be powered from the VDEC output pin.
- RF clock sources and other, different clock sources must not share common IC components, as this may introduce coupling into the RF. Unused ac-coupled clock buffer circuits should be tied to a dc supply, to prevent them oscillating. By default the RF clock source is routed to the XTAL/CLK input internally.
- It is recommended that the RF Synthesisers are operated with maximum gain Iset (ie. ISETn tied to RFV_{SS}).
- The loop components should be optimised for each VCO.

8.4 System Clock Synthesisers

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are phase locked loop (PLL) clocks that can be programmed via the System Clock registers in the User Configuration block of the FI. The System Clock PLL Configuration registers control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configuration registers control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a comparison frequency of 96kHz.

The System Clock output divider stages are designed so that they have a 1:1 Mark-to-Space ratio when an even divide number is selected.

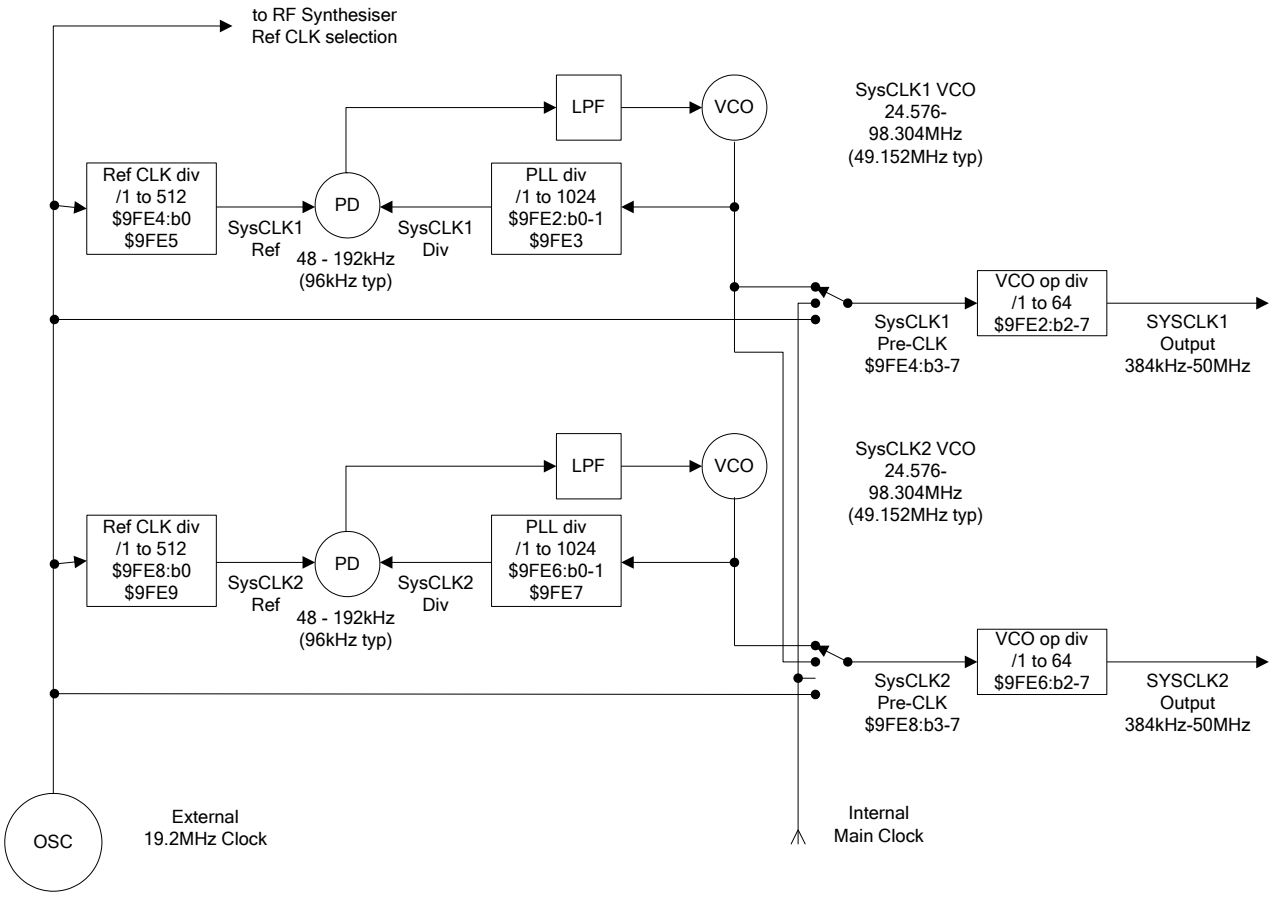


Figure 9 System Clock Generation

The 7032FI-2.x XTAL/CLK input should be driven by an externally generated 19.2MHz clock, in which case the default settings following FI load will provide 9.6MHz and 19.2MHz clock sources.

9 Performance Specification

9.1 Electrical Performance

9.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	–0.3	4.5	V
AV_{DD}- AV_{SS}	–0.3	4.5	V
RFV_{DD}- RFV_{SS}	–0.3	4.5	V
CPV_{DD}- RFV_{SS}	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Voltage on any pin to RFV_{SS} (excluding CPV_{DD})	–0.3	RFV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding V_{BIAS}) (i.e. V_{DEC}, AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS}, CPV_{DD}, RFV_{DD} or RFV_{SS})	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD} or CPV_{DD}	0	0.3	V
AV_{DD} and CPV_{DD}	0	0.3	V
DV_{SS} and AV_{SS} or RFV_{SS}	0	50	mV
AV_{SS} and RFV_{SS}	0	50	mV

All Packages	**Min.**	**Max.**	**Unit**
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q1 Package (64-pad VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	3500	mW
... Derating	–	35	mW/°C
L9 Package (64-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1690	mW
... Derating	–	16.9	mW/°C

9.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
$DV_{DD} – DV_{SS}$		3.0	3.6	V
$AV_{DD} – AV_{SS}$		3.0	3.6	V
$CPV_{DD} – RFV_{SS}$		3.0	3.6	V
$RFV_{DD} – DV_{SS}$	1	2.25	2.75	V
$V_{DEC} – DV_{SS}$	2	2.25	2.75	V
Operating Temperature		–40	+85	°C
Clock Frequency (CMX7032 device with FI-2.0 loaded)	3	19.2MHz - 20ppm	19.2MHz + 20ppm	
Function Image size	4	0	46	kBytes

Notes:
1 The V_{DEC} supply is automatically created from DV_{DD} by the on-chip voltage regulator.
2 The RFV_{DD} supply can be supplied from the V_{DEC} supply, if preferred.
3 The CMX7032 hardware limits for clock frequency (without an FI loaded) are 3.0MHz to 24.576MHz. These limits are then restricted by the FI which is loaded.
4 The current Function Image size (FI-2.0.1.0) is 28kBytes

9.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 3.
Maximum load on digital outputs = 30pF.
Clock Frequency = 19.2MHz (±20ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = CPV_{DD} = 3.0V to 3.6V; RFV_{DD} = 2.25V to 2.75V.
Reference Signal Level = 300mV pk-pk with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
Rx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)	23	–	14.4	22.0	mA
AI_{DD} (AV_{DD} = 3.3V)	23	–	5.8	9.0	mA
Additional current for one RF Synthesiser	24				
RFI_{DD} (CPV_{DD} = 3.3V, RFV_{DD} = 2.5V)		–	2.5	4.5	mA
Additional current for one Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	250	–	µA
AI_{DD} (AV_{DD} = 3.3V)		–	300	–	µA
CLK	25				
Input Logic ‘1’		70%	–	–	DV_{DD}
Input Logic ‘0’		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
RS232 Interface and Logic Inputs					
Input Logic ‘1’		70%	–	–	DV_{DD}
Input Logic ‘0’		–	–	30%	DV_{DD}
Input Leakage Current (Logic ‘1’ or ‘0’)		–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
RS232 Interface and Logic Outputs					
Output Logic ‘1’, (I_{OH} = 120µA)		90%	–	–	DV_{DD}
Output Logic ‘1’, (I_{OH} = 1mA)		80%	–	–	DV_{DD}
Output Logic ‘0’, (I_{OL} = 360µA)		–	–	10%	DV_{DD}
Output Logic ‘0’, (I_{OL} = -1.5mA)		–	–	15%	DV_{DD}
“Off” State Leakage Current	21	–	–	10	µA
V_{BIAS}	26				
Output Voltage Offset wrt AV_{DD}/2 (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

AC Parameters		Notes	Min.	Typ.	Max.	Unit
CLK Input						
'High' Pulse Width		31	15	–	–	ns
'Low' Pulse Width		31	15	–	–	ns
Input Impedance (at 19.2MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Clock Frequency			-	19.2	–	MHz
Clock Stability/Accuracy			–	–	±20	ppm
Clock Start Up (from powersave)			–	20	–	ms
System Clk 1/2 Outputs						
XTAL/CLK Input to CLOCK_OUT Timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' Pulse Width		33	76	81.38	87	ns
'Low' Pulse Width		33	76	81.38	87	ns
V_{BIAS}						
Start Up Time (from powersave)			–	30	–	ms
RxIN Input						
Input Impedance		34	–	> 10	–	MΩ
Input Signal Range		35	10	–	90	$\%V_{DD}$
Input Signal Envelope			0.3		2.7	Vp-p
Load Resistance (feedback pins)			80	–	–	kΩ
Amplifier Open Loop Voltage Gain (I/P = 1mV rms at 100Hz)			–	80	–	dB
Unity Gain Bandwidth			–	1.0	–	MHz
RF Synthesiser – Phase Locked Loops						
Reference Clock Input						
Frequency		64, 66	5.0	19.2	40.0	MHz
Input Logic '1'		61	70%	–	–	RFV_{DD}
Input Logic '0'		61	–	–	30%	RFV_{DD}
Divide Ratios (R)		62	2	–	8191	
RF Synthesiser		67				
Comparison Frequency			–	–	500	kHz
Input Frequency Range		65	100	–	600	MHz
Input Level (at 600MHz)			-15	–	0	dBm
Input Slew Rate			14	–	–	V/µs
Divide Ratios (N)			1088	–	1048575	
1Hz Normalised Phase Noise Floor		68	–	−197	–	dBc/Hz
Charge Pump Current (high)		63	±1.88	±2.5	±3.3	mA
Charge Pump Current (low)		63	±470	±625	±820	µA
Charge Pump Current - voltage variation			–	10%	–	per V
Charge Pump Current - sink to source match			–	5%	–	of ISET

Notes:

21 Tamb = 25°C, not including any current drawn from the device pins by external circuitry.
22 RF and auxiliary circuits disabled.
23 Nominal voltage only, maximum figure is extrapolated from that obtained under test conditions.
24 When using the external components shown in Figure 3 and Figure 7 and when supplying the current for RFV_{DD} from the regulated 2.5V digital (V_{DEC}) supply.
25 Characteristics when driving the XTAL/CLK pin with an external clock source.
26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 4.
31 Timing for an external input to the XTAL/CLK pin.
32 XTAL/CLK input driven by an external source.
33 6.144MHz XTAL fitted and 6.144MHz output selected.
34 With no external components connected, and measured at dc.
35 After multiplying by gain of input circuit, with external components connected.
36 Gain applied to signal at output of buffer amplifier: RX1FB or RX2FB.
37 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB.
41 Power-up refers to issuing an RS232 message. These limits apply only if V_{BIAS} is on and stable.
42 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.
43 With respect to the signal at the feedback pin of the selected input port.
44 With the output driving a 20kΩ load to $AV_{DD}/2$.
51 Denotes output impedance of the driver of the auxiliary input signal, to ensure <1 bit additional error under nominal conditions.
53 Guaranteed monotonic with no missing codes.
61 Square wave input.
62 Separate dividers provided for each PLL.
63 External ISET resistor (R31) = 0Ω (Internal ISET resistor = 9k6Ω nominally).
64 For optimum performance of the synthesiser subsystems, a common master clock should be used for the RF Synthesisers and the baseband sections. Using unsynchronised clocks is likely to result in spurious products being generated in the synthesiser outputs and in some cases difficulty may be experienced in obtaining lock in the RF Synthesisers.
65 Operation outside these frequency limits is possible, but not guaranteed. Below 150MHz, a square wave input may be required to provide an acceptable slew rate.
66 Lower input frequencies may be used subject to division ratio requirements being maintained.
67 It is recommended that RF Synthesiser 1 be used for higher frequency use (eg: RF 1st LO) and RF Synthesiser 2 be used for lower frequency use (eg: IF LO).
68 1Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop by: Phase Noise (in band) = PN1Hz + 20 $\log_{10}(N)$ + 10$\log_{10}(f_{comparison})$.

9.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 3.
Maximum load on digital outputs = 30pF.
CLK Frequency = 19.2MHz (±20ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = CPV_{DD} = 3.0V to 3.6V; RFV_{DD} = 2.25V to 2.75V.
Reference Signal Level = 300mV pk-pk with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.

Receive Parameters	Notes	Min.	Typ.	Max.	Unit
AIS (GMSK 9600bps), 25kHz channel					
Bit rate Accuracy		–	–	±50	ppm
BT		–	0.4	–	
Storage Time	1	–	8	–	bits
Packet Error Rate (PER) limit		–	–	20%	
PER with –10dB Co-channel Interference	2	–	–	20%	
PER with 10dB SNR	3	–	–	20%	
Rx Buffer Size (burst mode)		–	–	2 x176	bytes

Notes:
1. Through GMSK/FSK receive filters.
2. Measured at baseband to IEC 62287-1.
3. Measured at baseband with simulated FM channel noise.

9.2 SPI Timing

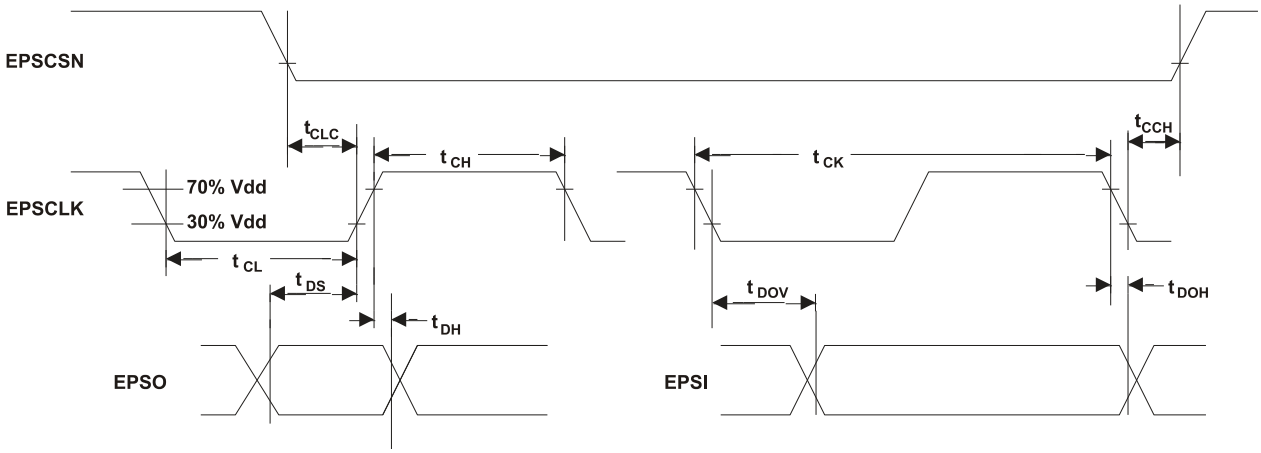
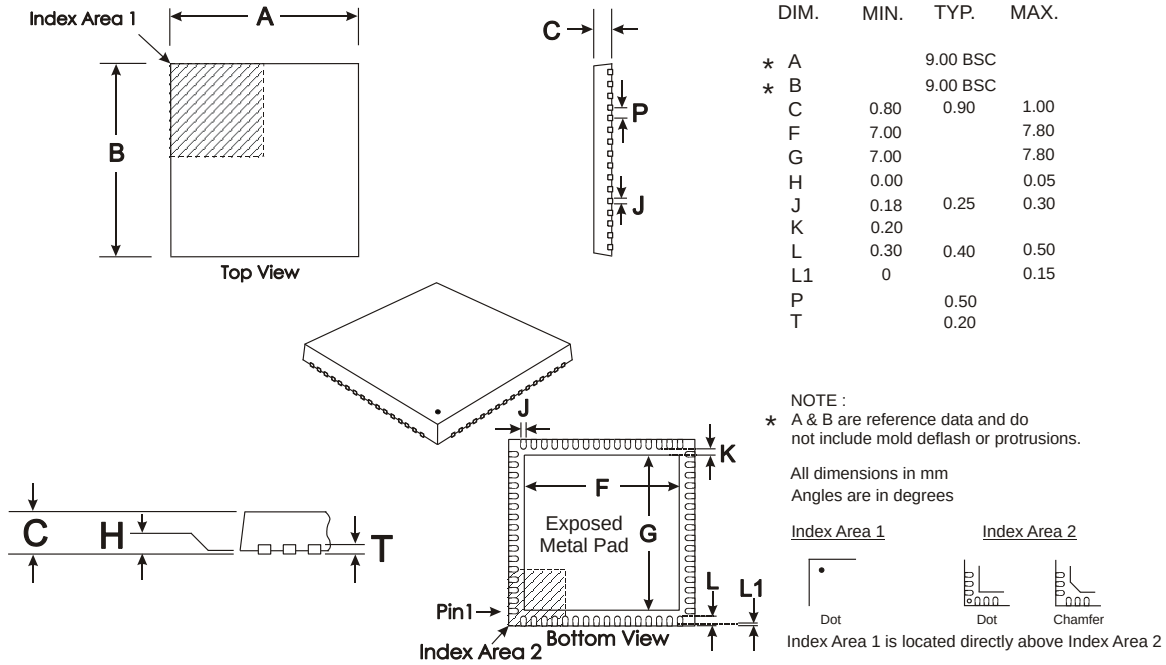


Figure 10 SPI Interface Timing

Serial (SPI) Bus Interface Timing		Notes	Min.	Typ.	Max.	Unit
T_{CK}	Clock cycle time		–	16	–	Xtal Clock Periods
T_{CL}	Clock 'low' pulse width		–	8	–	Xtal Clock Periods
T_{CH}	Clock 'high' pulse width		–	8	–	Xtal Clock Periods
t_{DOV}	Out data valid time		–	10	80	ns
t_{DOH}	Out data hold time		0	–	–	ns
T_{DS}	In data set up time		20	–	–	ns
T_{DH}	In data hold time		20	–	–	ns
t_{CLC}	Chip select low to clock rising edge		–	4	–	Xtal Clock Periods
t_{CCH}	Clock falling edge to chip select high		–	4	–	Xtal Clock Periods

Notes: 1. The serial (SPI) bus clock frequency is the CMX7032 internal (Main Clock ÷ 16) frequency. At power-on, the internal Main Clock is connected directly to the XTAL/CLK pin. An EEPROM should be chosen which is compatible with these timings.
2. Maximum 30pF load on each serial bus interface line.



DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

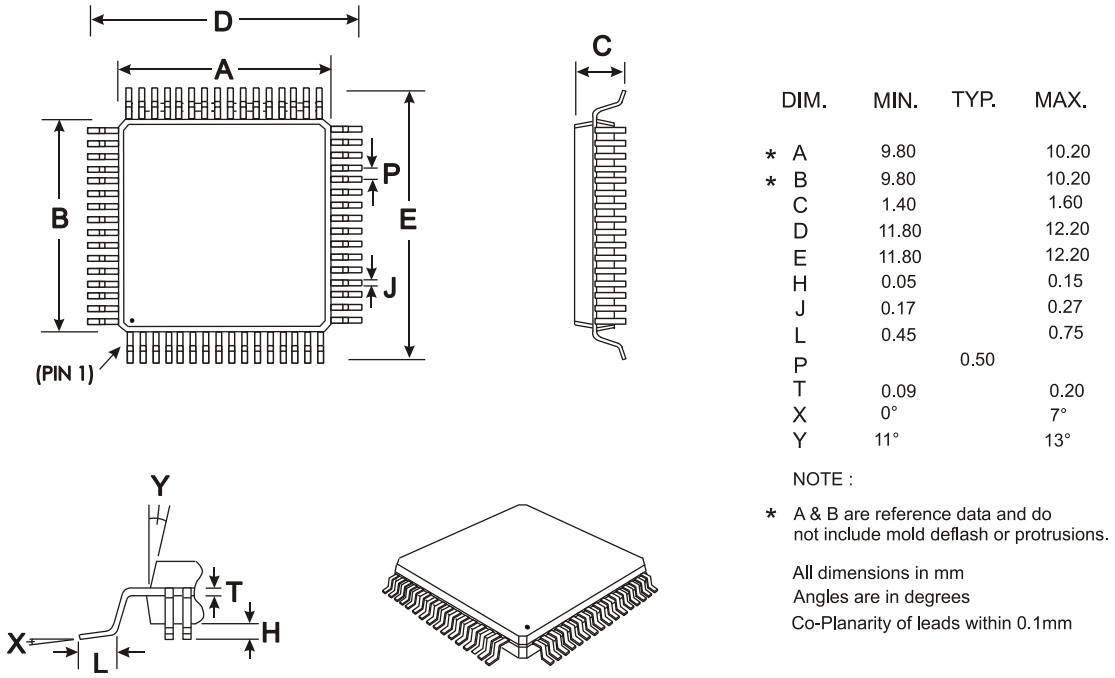
All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 11 Mechanical outline for 64-pad VQFN package (Q1)

Order as CMX7032Q1



DIM.	MIN.	TYP.	MAX.
* A	9.80		10.20
* B	9.80		10.20
C	1.40		1.60
D	11.80		12.20
E	11.80		12.20
H	0.05		0.15
J	0.17		0.27
L	0.45		0.75
P		0.50	
T	0.09		0.20
X	0°		7°
Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 12 Mechanical outline for 64-pin LQFP (leaded) package (L9)

Order as CMX7032L9

Infinite Capabilities . . .
FirmASIC®
. . . Maximum Flexibility

About *FirmASIC*®

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

CML Microcircuits (UK) Ltd COMMUNICATION SEMICONDUCTORS	CML Microcircuits (USA) Inc. COMMUNICATION SEMICONDUCTORS	CML Microcircuits (Singapore) Pte Ltd COMMUNICATION SEMICONDUCTORS
Tel: +44 (0)1621 875500 **Fax:** +44 (0)1621 875600 **Sales:** sales@cmlmicro.com **Tech Support:** techsupport@cmlmicro.com	**Tel:** +1 336 744 5050 800 638 5577 **Fax:** +1 336 744 5054 **Sales:** us.sales@cmlmicro.com **Tech Support:** us.techsupport@cmlmicro.com	**Tel:** +65 62 888129 **Fax:** +65 62 888230 **Sales:** sg.sales@cmlmicro.com **Tech Support:** sg.techsupport@cmlmicro.com
- www.cmlmicro.com -		