CS2841B

Automotive Current Mode PWM Control Circuit

The CS2841B provides all the necessary features to implement off−line fixed frequency current−mode control with a minimum number of external components.

The CS2841B (a variation of the CS2843A) is designed specifically for use in automotive operation. The low start threshold voltage of 8.0 V (typ), and the ability to survive 40 V automotive load dump transients are important for automotive subsystem designs. The CS2841 series has a history of quality and reliability in automotive applications.

The CS2841B incorporates a precision temperature−controlled oscillator with an internally trimmed discharge current to minimize variations in frequency. Duty−cycles greater than 50% are also possible. On board logic ensures that V_{REF} is stabilized before the output stage is enabled. Ion implant resistors provide tighter control of undervoltage lockout.
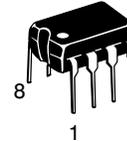
Features

- Optimized for Off−Line Control
- Internally Trimmed Temperature Compensated Oscillator
- Maximum Duty−Cycle Clamp
- V_{REF} Stabilized Before Output Stage Enabled
- Low Start−Up Current
- Pulse−By−Pulse Current Limiting
- Improved Undervoltage Lockout
- Double Pulse Suppression
- 1.0 % Trimmed Bandgap Reference
- High Current Totem Pole Output
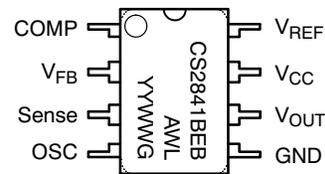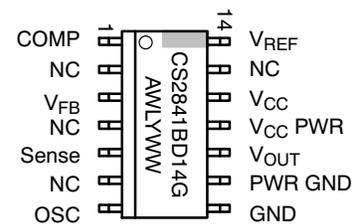- Pb−Free Packages are Available*

ON Semiconductor®

http://onsemi.com

PDIP−8
N SUFFIX
CASE 626

8
1

SOIC−14
D SUFFIX
CASE 751A

14
1

PIN CONNECTIONS AND MARKING DIAGRAM

PDIP−8

COMP — | — V_{REF}
V_{FB} — | — V_{CC}
Sense — | — V_{OUT}
OSC — | — GND

CS2841BEB
AWL
YYWWG

SOIC−14

COMP — | — V_{REF}
NC — | — NC
V_{FB} — | — V_{CC}
NC — | — V_{CC} PWR
Sense — | — V_{OUT}
NC — | — PWR GND
OSC — | — GND

CS2841BD14G
AWLYWW

CS2841B	= Device Code
A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

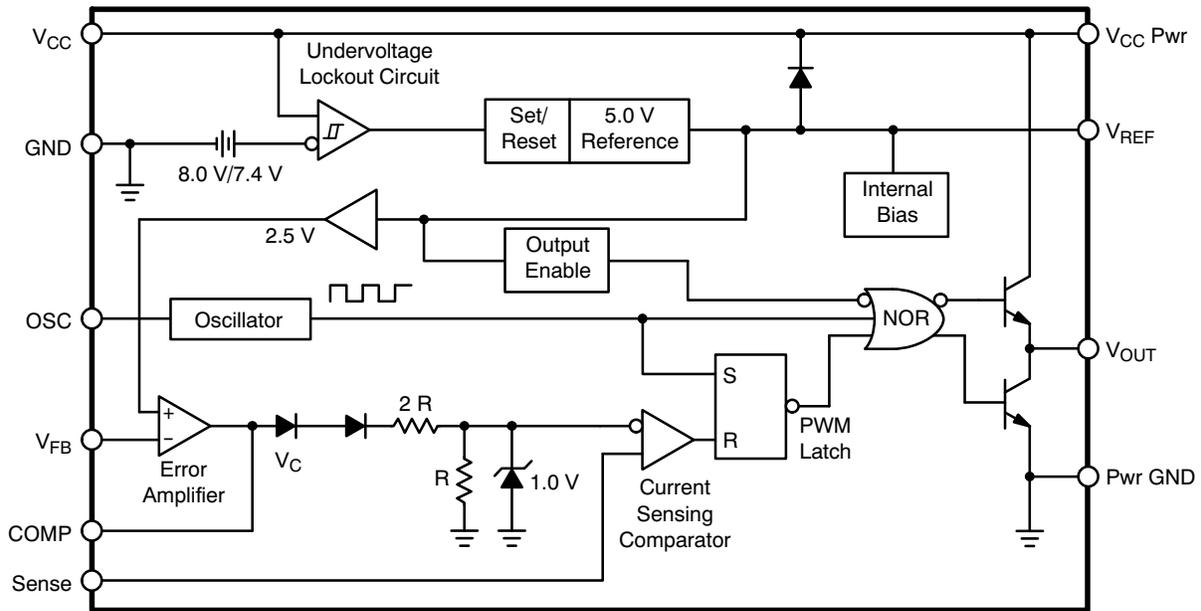See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

CS2841B

Figure 1. Block Diagram

MAXIMUM RATINGS

Rating		Value	Unit
Supply Voltage (Low Impedance Source)		40	V
Output Current		±1.0	A
Output Energy (Capacitive Load)		5.0	μJ
Analog Inputs (V_{FB}, Sense)		−0.3 to 5.5	V
Error Amp Output Sink Current		10	mA
Lead Temperature Soldering	Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2	260 peak 230 peak	°C °C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. 10 seconds max
2. 60 seconds max above 183°C

ORDERING INFORMATION

Device	Package	Shipping†
CS2841BEBN8	PDIP–8	50 Units / Rail
CS2841BEBN8G	PDIP–8 (Pb–Free)	50 Units / Rail
CS2841BED14	SOIC–14	55 Units / Rail
CS2841BED14G	SOIC–14 (Pb–Free)	55 Units / Rail
CS2841BEDR14	SOIC–14	2500 / Tape & Reel
CS2841BEDR14G	SOIC–14 (Pb–Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($-40°C \leq T_A \leq 85°C$, $R_T = 680$ kΩ, $C_T = 0.022$ µF for Triangular Mode, $V_{CC} = 15$ V (Note 3), $R_T = 10$ kΩ, $C_T = 3.3$ nF for Sawtooth Mode (see Figure 7); unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Reference Section					
Output Voltage	$T_J = 25°C$, $I_{OUT} = 1.0$ mA	4.9	5.0	5.1	V
Line Regulation	$8.4 \leq V_{CC} \leq 16$ V	–	6.0	20	mV
Load Regulation	$1.0 \leq I_{OUT} \leq 20$ mA	–	6.0	25	mV
Temperature Stability	Note 4	–	0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. Note 4	4.82	–	5.18	V
Output Noise Voltage	10 Hz $\leq f \leq 10$ kHz, $T_J = 25°C$. Note 4	–	50	–	µV
Long Term Stability	$T_A = 125°C$, 1000 Hrs. Note 4	–	5.0	25	mV
Output Short Circuit	$T_A = 25°C$	–30	–100	–180	mA
Oscillator Section					
Initial Accuracy	Sawtooth Mode: $T_J = 25°C$. See Figure 7. Sawtooth Mode: $-40°C \leq T_A \leq +85°C$ Triangular Mode: $T_J = 25°C$. See Figure 7.	47 44 44	52 52 52	57 60 60	kHz kHz kHz
Voltage Stability	$8.4 \leq V_{CC} \leq 16$ V	–	0.2	1.0	%
Temperature Stability	Sawtooth Mode: $T_{MIN} \leq T_A \leq T_{MAX}$. Note 4 Triangular Mode: $T_{MIN} \leq T_A \leq T_{MAX}$. Note 4	– –	5.0 8.0	– –	% %
Amplitude	V_{OSC} (Peak to Peak)	–	1.7	–	V
Discharge Current	$T_J = 25°C$ $T_{MIN} \leq T_A \leq T_{MAX}$	7.4 7.2	8.3 –	9.2 9.4	mA mA
Error Amp Section					
Input Voltage	$V_{COMP} = 2.5$ V	2.42	2.5	2.58	V
Input Bias Current	$V_{FB} = 0$ V	–	–0.3	–2.0	µA
A_{VOL}	$2.0 \leq V_{OUT} \leq 4.0$ V	65	90	–	dB
Unity Gain Bandwidth	Note 4	0.7	1.0	–	MHz
PSRR	8.4 V $\leq V_{CC} \leq 16$ V	60	70	–	dB
Output Sink Current	$V_{FB} = 2.7$ V, $V_{COMP} = 1.1$ V	2.0	6.0	–	mA
Output Source Current	$V_{FB} = 2.3$ V, $V_{COMP} = 5.0$ V	–0.5	–0.8	–	mA
V_{OUT} High	$V_{FB} = 2.3$ V, $R_L = 15$ kΩ to Ground	5.0	6.0	–	V
V_{OUT} Low	$V_{FB} = 2.7$ V, $R_L = 15$ kΩ to V_{REF}	–	0.7	1.1	V
Current Sense Section					
Gain	Notes 5 and 6	2.85	3.0	3.15	V/V
Maximum Input Signal	$V_{COMP} = 5.0$ V. Note 5	0.9	1.0	1.1	V
PSRR	12 V $\leq V_{CC} \leq 25$ V. Note 5	–	70	–	dB
Input Bias Current	$V_{Sense} = 0$ V	–	–2.0	–10	µA
Delay to Output	$T_J = 25°C$. Note 4	–	150	300	ns

3. Adjust V_{CC} above the start threshold before setting at 15 V
4. These parameters, although guaranteed, are not 100% tested in production
5. Parameter measured at trip point of latch with $V_{FB} = 0$
6. Gain defined as:

$$A = \frac{\Delta V_{COMP}}{\Delta V_{Sense}}; \ 0 \leq V_{Sense} \leq 0.8 \text{ V.}$$

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ELECTRICAL CHARACTERISTICS ($-40°C \leq T_A \leq 85°C$, $R_T = 680$ kΩ, $C_T = 0.022$ μF for Triangular Mode, $V_{CC} = 15$ V (Note 3), $R_T = 10$ kΩ, $C_T = 3.3$ nF for Sawtooth Mode (see Figure 7); unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Section					
Output Low Level	$I_{SINK} = 20$ mA $I_{SINK} = 200$ mA	– –	0.1 1.5	0.4 2.2	V V
Output High Level	$I_{SOURCE} = 20$ mA $I_{SOURCE} = 200$ mA	13 12	13.5 13.5	– –	V V
Rise Time	$T_J = 25°C$, $C_L = 1.0$ nF. Note 7	–	50	150	ns
Fall Time	$T_J = 25°C$, $C_L = 1.0$ nF. Note 7	–	50	150	ns
Output Leakage	Undervoltage Active, $V_{OUT} = 0$	–	–0.01	–10	μA
Total Standby Current					
Startup Current	–	–	0.5	1.0	mA
Operating Supply Current I_{CC}	$V_{FB} = V_{Sense} = 0$ V, $R_T = 10$ kΩ, $C_T = 3.3$ nF	–	11	17	mA
Undervoltage Lockout Section					
Start Threshold	–	7.6	8.0	8.4	V
Min. Operating Voltage	After Turn On	7.0	7.4	7.8	V

7. These parameters, although guaranteed, are not 100% tested in production.

PACKAGE PIN DESCRIPTION

PACKAGE PIN #		PIN SYMBOL	FUNCTION
PDIP–8	SOIC–14		
1	1	COMP	Error Amp Output, Used to Compensate Error Amplifier
2	3	V_{FB}	Error Amp Inverting Input
3	5	Sense	Noninverting Input to Current Sense Comparator
4	7	OSC	Oscillator Timing Network with Capacitor to Ground, Resistor to V_{REF}
5	8	GND	Ground
	9	Pwr GND	Output Driver Ground
6	10	V_{OUT}	Output Drive Pin
	11	V_{CC} Pwr	Output Driver Positive Supply
7	12	V_{CC}	Positive Power Supply
8	14	V_{REF}	Output of 5.0 V Internal Reference
	2, 4, 6, 13	NC	No Connection

CS2841B

TYPICAL PERFORMANCE CHARACTERISTICS
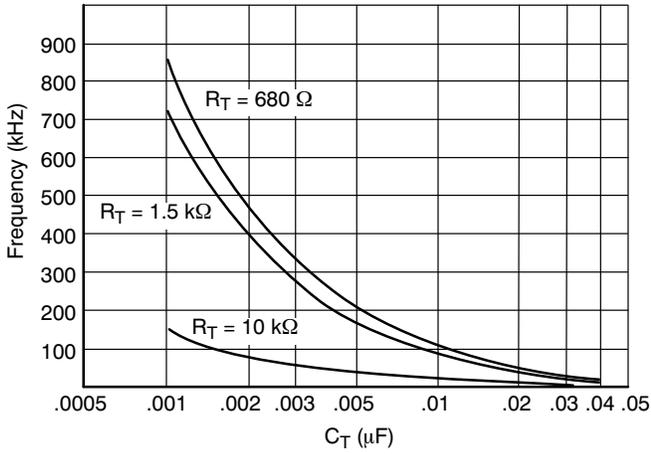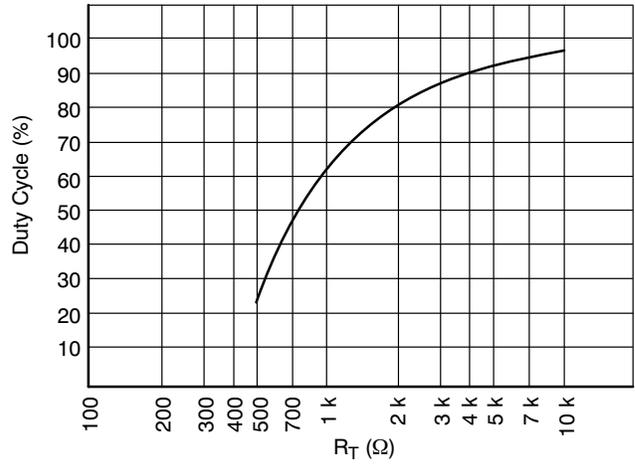

Figure 2. Oscillator Frequency vs. C_T

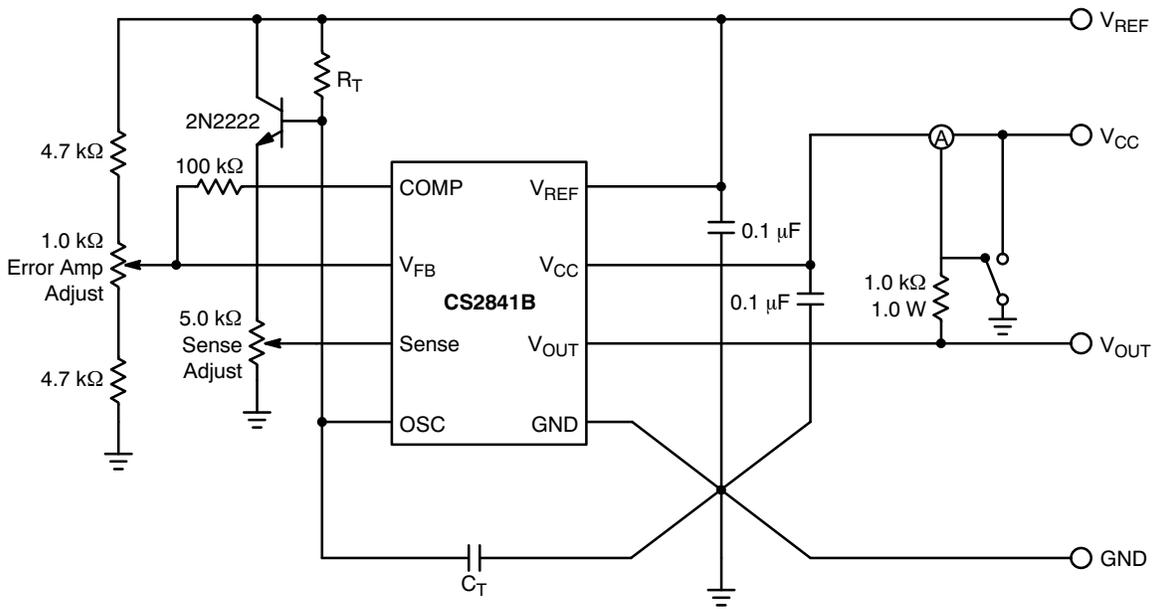Figure 3. Oscillator Duty Cycle vs. R_T

Figure 4. Test Circuit

CIRCUIT DESCRIPTION

Undervoltage Lockout

During Undervoltage Lockout (Figure 5), the output driver is biased to a high impedance state. The output should be shunted to ground with a resistor to prevent output leakage current from activating the power switch.
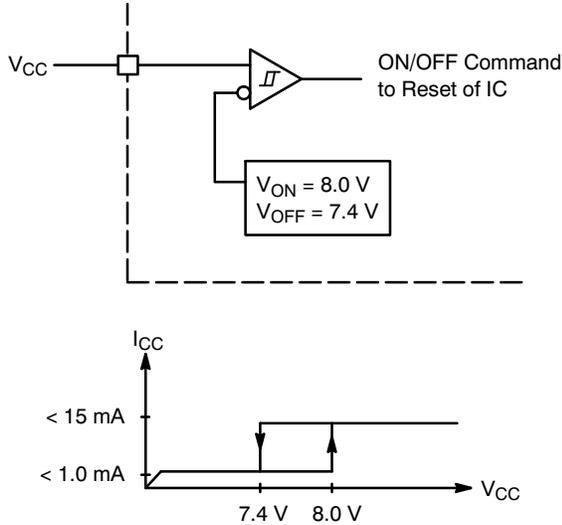

Figure 5. Typical Undervoltage Characteristics

PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal representing the peak output inductor current (Figure 6). An increase in V_{CC} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed–forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.
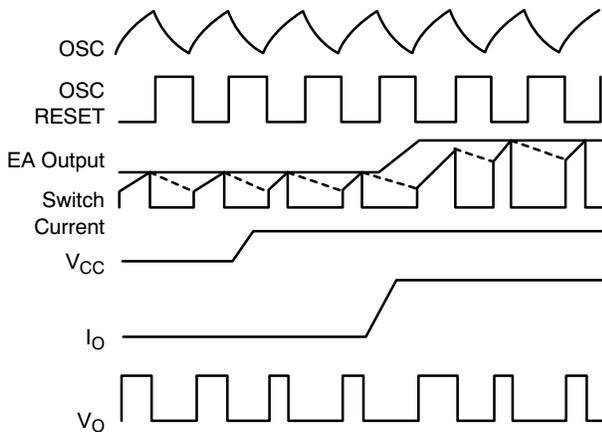
Figure 6. Timing Diagram for Key CS2841B Parameters

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of OSC components.
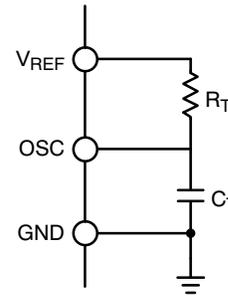
Timing Parameters
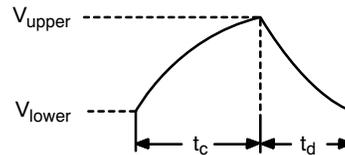
Sawtooth Mode
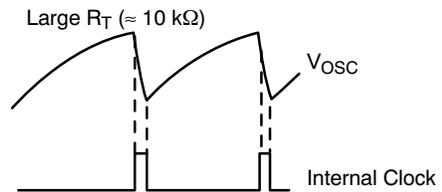
Triangular Mode
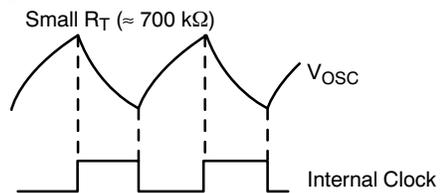
Figure 7. Oscillator Timing Network and Parameters

Setting the Oscillator

Oscillator timing capacitor, C_T, is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks out the output to the Low state, thus providing a user selected maximum duty cycle clamp. Charge and discharge times are determined by the general formulas:

$$t_c = R_T C_T \ln\left(\frac{V_{REF} - V_{lower}}{V_{REF} - V_{upper}}\right)$$

$$t_d = R_T C_T \ln\left(\frac{V_{REF} - I_d R_T - V_{upper}}{V_{REF} - I_d R_T - V_{lower}}\right)$$

Substituting in typical values for the parameters in the above formulas:

$V_{REF} = 5.0\,V$
$V_{upper} = 2.7\,V$
$V_{lower} = 1.0\,V$
$I_d = 8.3\,mA$
$t_c \approx 0.5534 R_T C_T$

$$t_d = R_T C_T \ln\left(\frac{2.3 - 0.0083 R_T}{4.0 - 0.0083 R_T}\right)$$

The frequency and maximum duty cycle can be determined from the Typical Performance Characteristic graphs.

Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to GND pin in a single point ground.

The transistor and 5.0 kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Sense.

Figure 8. Flyback Application

CS2841B

Input Voltage Range: 8.0 V to 16 V
Output Voltage: 17 V @ 100 mA > 300 mA
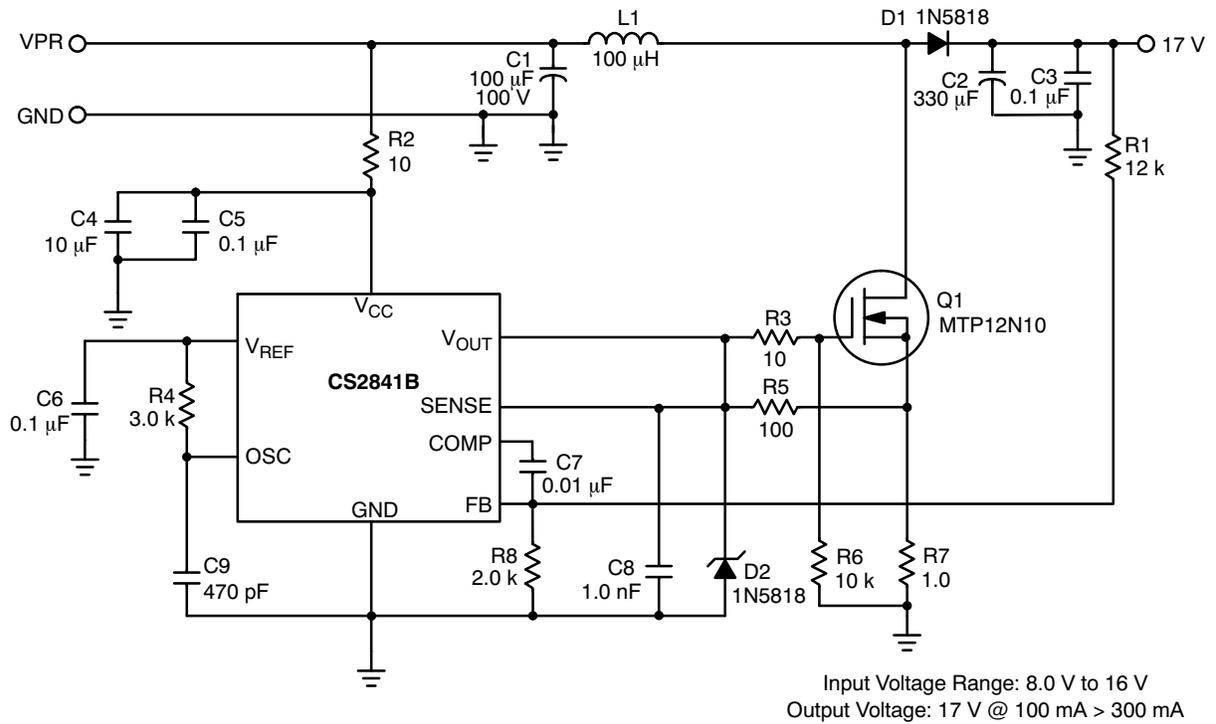
Figure 9. Boost Application

PACKAGE THERMAL DATA

Parameter		PDIP−8	SOIC−14	Unit
$R_{\theta JC}$	Typical	52	30	°C/W
$R_{\theta JA}$	Typical	100	125	°C/W

PACKAGE DIMENSIONS

PDIP−8
CASE 626−05
ISSUE L
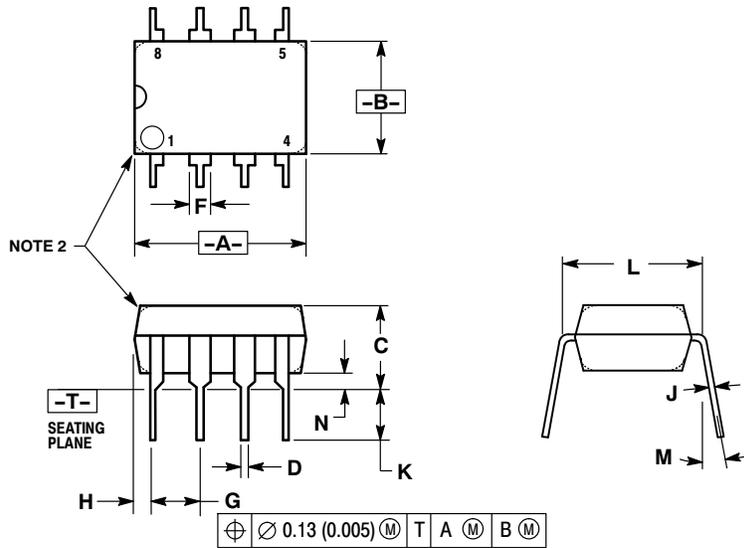
NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

NOTE 2

−B−

−A−

F

C

−T−
SEATING PLANE

N

D

K

H

G

L

J

M

⊕ | ∅ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ

CS2841B

PACKAGE DIMENSIONS

SOIC–14
CASE 751A–03
ISSUE J
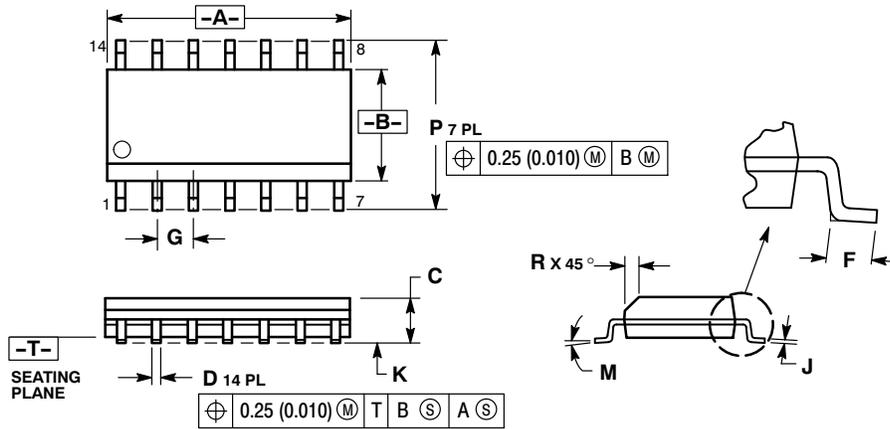
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS

CS2841B/D