CY2291

Three-PLL General Purpose EPROM Programmable Clock Generator

Features

- Three integrated phase-locked loops
- EPROM programmability
- Factory-programmable (CY2291) or field-programmable (CY2291F) device options
- Low-skew, low-jitter, high-accuracy outputs
- Power-management options (Shutdown, OE, Suspend)
- Frequency select option
- Smooth slewing on CPUCLK
- Configurable 3.3 V or 5 V operation
- 20-pin SOIC Package

Functional Description

The CY2291 is a third-generation family of clock generators. The CY2291 is upwardly compatible with the industry standard ICD2023 and ICD2028 and continues their tradition by providing a high level of customizable features to meet the diverse clock synchoronous systems.

All parts provide a highly configurable set of close for PC motherboard applications. Each of four configurable clock outputs (CLKA-CLKD) can be assigned 1 of 30 frequencies in any combination. Multiple outputs configured for the same or related[3] frequencies have low (<500 ps) skew, in effect providing on-chip buffering for heavily loaded signals.

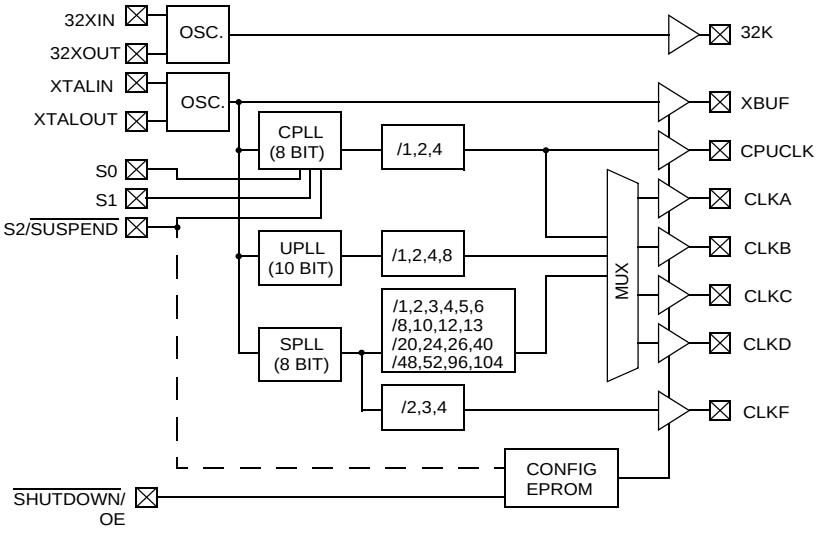
The CY2291 can be configured for either 5 V or 3.3 V operation. The internal ROM tables use EPROM technology, allowing full customization of output frequencies. The reference oscillator has been designed for 10 MHz to 25 MHz crystals, providing additional flexibility. No external components are required with this crystal. Alternatively, an external reference clock of frequency between 1 MHZ to 30 MHz can be used. Customers using the 32 kHz oscillator must connect a 10-MΩ resistor in parallel with the 32 kHz crystal.

For a complete list of related documentation, click here.

Selection Guide

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2291	8	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–100 MHz (5 V) 76.923 kHz–80 MHz (3.3 V)	Factory programmable Commercial temperature
CY2291I	8	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–90 MHz (5 V) 76.923 kHz–66.6 MHz (3.3 V)	Factory programmable Industrial temperature
CY2291F	8	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–90 MHz (5 V) 76.923 kHz–66.6 MHz (3.3 V)	Field programmable Commercial temperature
CY2291FI	8	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–80 MHz (5 V) 76.923 kHz–60.0 MHz (3.3 V)	Field programmable Industrial temperature

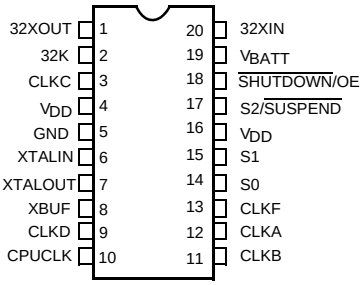
Logic Block Diagram



Contents

Pinouts

Figure 1. 20-pin SOIC pinout



Pin Definitions

Name	Pin Number	Description
32XOUT[1]	1	32.768-kHz crystal feedback.
32K	2	32.768-kHz output (always active if VBATT is present).
CLKC	3	Configurable clock output C.
VDD	4, 16	Voltage supply.
GND	5	Ground.
XTALIN[2]	6	Reference crystal input or external reference clock input.
XTALOUT[2, 3]	7	Reference crystal feedback.
XBUF	8	Buffered reference clock output.
CLKD	9	Configurable clock output D.
CPUCLK	10	CPU frequency clock output.
CLKB	11	Configurable clock output B.
CLKA	12	Configurable clock output A.
CLKF	13	Configurable clock output F.
S0	14	CPU clock select input, bit 0.
S1	15	CPU clock select input, bit 1.
S2/SUSPEND	17	CPU clock select input, bit 2. Optionally enables suspend feature when LOW.
SHUTDOWN/OE	18	Places outputs in three-state[4] condition and shuts down chip when LOW. Optionally, only places outputs in three-state[4] condition and does not shut down chip when LOW.
VBATT[1]	19	Battery supply for 32.768-kHz circuit.
32XIN[1]	20	32.768 kHz crystal input.

Notes
1. If power is applied to VBATT, then a watch crystal (32.768 KHz) must be connected to the 32XIN and 32XOUT pins.
2. For best accuracy, use a parallel-resonant crystal, $C_{LOAD} \approx 17$ pF or 18 pF.
3. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to crystal).
4. The CY2291 has weak pull downs on all outputs (except 32K). Hence, when a three-state condition is forced on the outputs, the output pins are pulled LOW.

Functional Overview

Output Configuration

The CY2291 has five independent frequency sources on-chip. These are the 32-kHz oscillator, the reference oscillator, and three Phase-locked loops (PLLs). Each PLL has a specific function. The System PLL (SPLL) drives the CLKF output and provides fixed output frequencies on the configurable outputs. The SPLL offers the most output frequency divider options. The CPU PLL (CPLL) is controlled by the select inputs (S0–S2) to provide eight user-selectable frequencies with smooth slewing between frequencies. The Utility PLL (UPLL) provides the most accurate clock. It is often used for miscellaneous frequencies not provided by the other frequency sources.

All configurations are EPROM programmable, providing short sample and production lead times.

Power Saving Features

The $\overline{\text{SHUTDOWN}}$/OE input three-states the outputs when pulled LOW (the 32-kHz clock output is not affected). If system shutdown is enabled, a LOW on this pin also shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the V_{DD} pins are less than 50 μA (for Commercial Temp. or 100 μA for Industrial Temp.) plus 15 μA max. for the 32-kHz subsystem and is typically 10 μA. After leaving shutdown mode, the PLLs have to re-lock. All outputs except 32K have a weak pull down so that the outputs do not float when three-stated.[4]

The S2/$\overline{\text{SUSPEND}}$ input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs except 32K can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a three-state condition.[3]

The CPUCLK can slew (transition) smoothly between 8 MHz and the maximum output frequency (100 MHz at 5V/80 MHz at 3.3 V for commercial temp. parts or 90 MHz at 5V/66.6 MHz at 3.3 V for industrial temp. and for field-programmed parts). This feature is extremely useful in “Green” PC and laptop applications, where reducing the frequency of operation can result in considerable power savings. This feature meets all 486 and Pentium® processor slewing requirements.

CyClocks Software

CyClocks™ is an easy-to-use application that allows you to configure any one of the EPROM programmable clocks offered by Cypress. You may specify the input frequency, PLL and output frequencies, and different functional options. Please note the output frequency ranges in this data sheet when specifying them in CyClocks to ensure that you stay within the limits. CyClocks also has a power calculation feature that allows you to see the power consumption of your specific configuration. CyClocks is a sub-application within the CyberClocks™ software. You can download a copy of CyberClocks for free on Cypress’s web site at www.cypress.com.

Cypress FTG Programmer

The Cypress frequency timing generator (FTG) Programmers is a portable programmer designed to custom program our family of EPROM field programmable clock devices. The FTG programmers connect to a PC serial port and allow users of CyClocks software to quickly and easily program any of the CY2291F, CY2292F, CY2071AF, and CY2907F devices. The ordering code for the Cypress FTG Programmer is CY3670.

Custom Configuration Request Procedure

The CY229x are EPROM-programmable devices that may be configured in the factory or in the field by a Cypress Field Application Engineer (FAE). The output frequencies requested are matched as closely as the internal PLL divider and multiplier options allow. All custom requests must be submitted to your local Cypress FAE or sales representative. The method to use to request custom configurations is:

Use CyClocks™ software. This software automatically calculates the output frequencies that can be generated by the CY229x devices and provides a print-out of final pinout which can be submitted (in electronic or print format) to your local FAE or sales representative. The CyClocks software is available free of charge from the Cypress web site (http://www.cypress.com) or from your local sales representative.

Once the custom request has been processed you receive a part number with a 3-digit extension (for example, CY2292SC-128) specific to the frequencies and pinout of your device. This is the part number used for samples requests and production orders.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Supply voltage .....–0.5 V to + 7.0 V

DC input voltage .....–0.5 V to + 7.0 V

Storage temperature ..... –65 °C to +150 °C

Maximum soldering temperature (10 sec) ..... 260 °C

Junction temperature ..... 150 °C

Package power dissipation ..... 750 mW

Static discharge voltage
(per MIL-STD-883, Method 3015) ..... ≥ 2000 V

Operating Conditions

Parameter [5]	Description	Part Numbers	Min	Max	Unit
V_{DD}	Supply voltage, 5.0 V operation	All	4.5	5.5	V
V_{DD}	Supply voltage, 3.3 V operation	All	3.0	3.6	V
$V_{BATT[1]}$	Battery backup voltage	All	2.0	5.5	V
T_A	Commercial operating temperature, ambient	CY2291/CY2291F	0	+70	°C
	Industrial operating temperature, ambient	CY2291I/CY2291FI	–40	+85	°C
C_{LOAD}	Max. load capacitance 5.0 V operation	All	–	25	pF
C_{LOAD}	Max. load capacitance 3.3 V operation	All	–	15	pF
f_{REF}	External reference crystal	All	10.0	25.0	MHz
	External reference clock [6, 7, 8]	All	1	30	MHz
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)		0.05	50	ms

Notes

5. Electrical parameters are guaranteed by design with these operating conditions, unless otherwise noted.
6. External input reference clock must have a duty cycle between 40% and 60%, measured at $V_{DD}/2$.
7. Please refer to Whitepaper "Crystal Parameters Recommendation for Cypress Frequency Synthesizers" for information on AC-coupling the external input reference clock.
8. The oscillator circuit is optimized for a crystal reference and for external reference clocks up to 20 MHz. For external reference clocks above 20 MHz, it is recommended that a 150Ω pull up resistor to V_{DD} be connected to the Xout pin.

Electrical Characteristics, Commercial 5.0 V

Parameter	Description	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = 4.0 mA		2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 4.0 mA		–	–	0.4	V
$V_{OH–32}$	32.768-kHz HIGH-level output voltage	I_{OH} = 0.5 mA		V_{BATT} × 0.5	–	–	V
$V_{OL–32}$	32.768-kHz LOW-level output voltage	I_{OL} = 0.5 mA		–	–	0.4	V
V_{IH}	HIGH-level input voltage[9]	Except crystal pins		2.0	–	–	V
V_{IL}	LOW-level input voltage[9]	Except crystal pins		–	–	0.8	V
I_{IH}	Input HIGH current	V_{IN} = V_{DD} – 0.5 V		–	<1	10	µA
I_{IL}	Input LOW current	V_{IN} = +0.5 V		–	<1	10	µA
I_{OZ}	Output leakage current	Three-state outputs		–	–	250	µA
I_{DD}	V_{DD} supply current commercial[10]	V_{DD} = V_{DD} Max., 5 V operation		–	75	100	mA
I_{DDS}	V_{DD} power supply current in shutdown mode[10]	Shutdown active, excluding V_{BATT}	CY2291 / CY2291F	–	10	50	µA
I_{BATT}	V_{BATT} power supply current	V_{BATT} = 3.0 V		–	5	15	µA

Electrical Characteristics, Commercial 3.3 V

Parameter	Description	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = 4.0 mA		2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 4.0 mA		–	–	0.4	V
$V_{OH–32}$	32.768-kHz HIGH-level output voltage	I_{OH} = 0.5 mA		V_{BATT} 0.5	–	–	V
$V_{OL–32}$	32.768-kHz LOW-level output voltage	I_{OL} = 0.5 mA		–	–	0.4	V
V_{IH}	HIGH-level input voltage[9]	Except crystal pins		2.0	–	–	V
V_{IL}	LOW-level input voltage[9]	Except crystal pins		–	–	0.8	V
I_{IH}	Input HIGH current	V_{IN} = V_{DD} – 0.5 V		–	<1	10	µA
I_{IL}	Input LOW current	V_{IN} = +0.5 V		–	<1	10	µA
I_{OZ}	Output leakage current	Three-state outputs		–	–	250	µA
I_{DD}	V_{DD} supply current [10] commercial	V_{DD} = V_{DD} Max., 3.3 V operation		–	50	65	mA
I_{DDS}	V_{DD} power supply current in shutdown mode [10]	Shutdown active, excluding V_{BATT}	CY2291 / CY2291F	–	10	50	µA
I_{BATT}	V_{BATT} power supply current	V_{BATT} = 3.0 V		–	5	15	µA

Notes

9. Xtal inputs have CMOS thresholds.
10. Load = Max., V_{IN} = 0V or V_{DD}, Typical (–104) configuration, CPUCLK = 66 MHz. Other configurations vary. Power can be approximated by the following formula (multiply by 0.65 for 3V operation): $I_{DD}=10+0.06•(F_{CPLL}+F_{UPLL}+2•F_{SPLL})+0.27•(F_{CLKA}+F_{CLKB}+F_{CLKC}+F_{CLKD}+F_{CPUCLK}+F_{CLKF}+F_{XBUF})$.

Electrical Characteristics, Industrial 5.0 V

Parameter	Description	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = 4.0 mA		2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 4.0 mA		–	–	0.4	V
$V_{OH–32}$	32.768-kHz HIGH-level output voltage	I_{OH} = 0.5 mA		V_{BATT} 0.5	–	–	V
$V_{OL–32}$	32.768-kHz LOW-level output voltage	I_{OL} = 0.5 mA		–	–	0.4	V
V_{IH}	HIGH-level input voltage[11]	Except crystal pins		2.0	–	–	V
V_{IL}	LOW-level input voltage[11]	Except crystal pins		–	–	0.8	V
I_{IH}	Input HIGH current	V_{IN} = V_{DD} – 0.5 V		–	< 1	10	µA
I_{IL}	Input LOW current	V_{IN} = +0.5 V		–	< 1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs		–	–	250	µA
I_{DD}	V_{DD} supply current[12] industrial	V_{DD} = V_{DD} Max., 5 V operation		–	75	110	mA
I_{DDS}	V_{DD} power supply current in shutdown mode[12]	Shutdown active, excluding V_{BATT}	CY2291I / CY2291FI	–	10	100	µA
I_{BATT}	V_{BATT} power supply current	V_{BATT} = 3.0 V		–	5	15	µA

Electrical Characteristics, Industrial 3.3 V

Parameter	Description	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = 4.0 mA		2.4	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 4.0 mA		–	–	0.4	V
$V_{OH–32}$	32.768-kHz HIGH-level output voltage	I_{OH} = 0.5 mA		V_{BATT} × 0.5	–	–	V
$V_{OL–32}$	32.768-kHz LOW-Level Output Voltage	I_{OL} = 0.5 mA		–	–	0.4	V
V_{IH}	HIGH-level input voltage[11]	Except crystal pins		2.0	–	–	V
V_{IL}	LOW-level input voltage[11]	Except crystal pins		–	–	0.8	V
I_{IH}	Input HIGH current	V_{IN} = V_{DD} – 0.5 V		–	< 1	10	µA
I_{IL}	Input LOW current	V_{IN} = +0.5 V		–	< 1	10	µA
I_{OZ}	Output leakage current	Three-state outputs		–	–	250	µA
I_{DD}	V_{DD} supply current[12] industrial	V_{DD} = V_{DD} max., 3.3 V operation		–	50	70	mA
I_{DDS}	V_{DD} power supply current in shutdown mode[12]	Shutdown active, excluding V_{BATT}	CY2291I / CY2291FI	–	10	100	µA
I_{BATT}	V_{BATT} power supply current	V_{BATT} = 3.0 V		–	5	15	µA

Notes

11. Xtal inputs have CMOS thresholds.
12. Load = Max., V_{IN} = 0V or V_{DD}, Typical (–104) configuration, CPUCLK = 66 MHz. Other configurations vary. Power can be approximated by the following formula (multiply by 0.65 for 3V operation): $I_{DD}=10+0.06•(F_{CPLL}+F_{UPLL}+2•F_{SPLL})+0.27•(F_{CLKA}+F_{CLKB}+F_{CLKC}+F_{CLKD}+F_{CPUCLK}+F_{CLKF}+F_{XBUF})$.

Switching Characteristics, Commercial 5.0 V

Parameter	Name	Description		Min	Typ	Max	Unit
t_1	Output period	Clock output range, 5 V operation	CY2291	10 (100 MHz)	–	13000 (76.923 kHz)	ns
			CY2291F	11.1 (90 MHz)	–	13000 (76.923 kHz)	ns
	Output duty cycle[13]	Duty cycle for outputs, defined as $t_2 \div t_1$[14] $f_{OUT} \geq 66$ MHz		40%	50%	60%	–
		Duty cycle for outputs, defined as $t_2 \div t_1$[14] $f_{OUT} < 66$ MHz		45%	50%	55%	–
t_3	Rise time	Output clock rise time[15]		–	3	5	ns
t_4	Fall time	Output clock fall time[15]		–	2.5	4	ns
t_5	Output disable time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW		–	10	15	ns
t_6	Output enable time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH		–	10	15	ns
t_7	Skew	Skew delay between any identical or related outputs[14, 16]		–	< 0.25	0.5	ns
t_8	CPUCLK Slew	Frequency transition rate		1.0	–	20.0	MHz/ms
t_{9A}	Clock jitter[17]	Peak-to-peak period jitter (t_{9A} Max. – t_{9A} min.),% of clock period ($f_{OUT} \leq 4$ MHz)		–	< 0.5	1	%
t_{9B}	Clock jitter[17]	Peak-to-peak period jitter (t_{9B} Max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)		–	< 0.7	1	ns
t_{9C}	Clock jitter[17]	Peak-to-peak period jitter (16 MHz < $f_{OUT} \leq$ 50 MHz)		–	< 400	500	ps
t_{9D}	Clock jitter[17]	Peak-to-peak period jitter (f_{OUT} > 50 MHz)		–	< 250	350	ps
t_{10A}	Lock time for CPLL	Lock Time from Power-up		–	< 25	50	ms
t_{10B}	Locktime for UPLL and SPLL	Lock Time from Power-up		–	< 0.25	1	ms
	Slew limits	CPU PLL Slew limits	CY2291	8	–	100	MHz
			CY2291F	8	–	90	MHz

Notes
13. XBUF duty cycle depends on XTALIN duty cycle.
14. Measured at 1.4 V.
15. Measured between 0.4V and 2.4 V.
16. CLKF is not guaranteed to be in phase with CLKA-D, even if it is referenced off the same PLL.
17. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit. For more information on jitter, please refer to the WhitePaper: "Datasheet Jitter Specifications for Cypress Timing Products".

Switching Characteristics, Commercial 3.3 V

Parameter	Name	Description		Min	Typ	Max	Unit
t_1	Output period	Clock output range, 3.3 V operation	CY2291	12.5 (80 MHz)	–	13000 (76.923 kHz)	ns
			CY2291F	15 (66.6 MHz)	–	13000 (76.923 kHz)	ns
	Output duty cycle [18]	Duty cycle for outputs, defined as $t_2 \div t_1$[19] $f_{OUT} \geq 66$ MHZ		40%	50%	60%	–
		Duty cycle for outputs, defined as $t_2 \div t_1$[19] $f_{OUT} < 66$ MHZ		45%	50%	55%	–
t_3	Rise time	Output clock rise time[20]		–	3	5	ns
t_4	Fall time	Output clock fall time[20]		–	2.5	4	ns
t_5	Output disable time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW		–	10	15	ns
t_6	Output enable time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH		–	10	15	ns
t_7	Skew	Skew delay between any identical or related outputs [19, 21]		–	< 0.25	0.5	ns
t_8	CPUCLK Slew	Frequency transition rate		1.0	–	20.0	MHz/ms
t_{9A}	Clock jitter[22]	Peak-to-peak period jitter (t_{9A} Max. – t_{9A} min.), % of clock period ($f_{OUT} \leq 4$ MHz)		–	< 0.5	1	%
t_{9B}	Clock jitter[22]	Peak-to-peak period jitter (t_{9B} Max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)		–	< 0.7	1	ns
t_{9C}	Clock jitter[22]	Peak-to-peak period jitter (16 MHz $< f_{OUT} \leq$ 50 MHz)		–	< 400	500	ps
t_{9D}	Clock jitter[22]	Peak-to-peak period jitter ($f_{OUT} >$ 50 MHz)		–	< 250	350	ps
t_{10A}	Lock time for CPLL	Lock time from power-up		–	< 25	50	ms
t_{10B}	Lock time for UPLL and SPLL	Lock time from power-up		–	< 0.25	1	ms
	Slew limits	CPU PLL slew limits	CY2291	8	–	80	MHz
			CY2291F	8	–	66.6	MHz

Notes
18. XBUF duty cycle depends on XTALIN duty cycle.
19. Measured at 1.4 V.
20. Measured between 0.4 V and 2.4 V.
21. CLKF is not guaranteed to be in phase with CLKA-D, even if it is referenced off the same PLL.
22. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit. For more information on jitter, please refer to the WhitePaper: "Datasheet Jitter Specifications for Cypress Timing Products".

Switching Characteristics, Industrial 5.0 V

Parameter	Name	Description		Min	Typ	Max	Unit
t_1	Output period	Clock output range, 5 V operation	CY2291I	11.1 (90 MHz)	–	13000 (76.923 kHz)	ns
			CY2291FI	12.5 (80 MHz)	–	13000 (76.923 kHz)	ns
	Output duty cycle[23]	Duty cycle for outputs, defined as $t_2 \div t_1$[24] $f_{OUT} \geq 66$ MHz		40%	50%	60%	–
		Duty cycle for outputs, defined as $t_2 \div t_1$[24] $f_{OUT} < 66$ MHz		45%	50%	55%	–
t_3	Rise time	Output clock rise time[25]		–	3	5	ns
t_4	Fall time	Output clock fall time[25]		–	2.5	4	ns
t_5	Output disable time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW		–	10	15	ns
t_6	Output enable time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH		–	10	15	ns
t_7	Skew	Skew delay between any identical or related outputs [24, 26]		–	< 0.25	0.5	ns
t_8	CPUCLK Slew	Frequency transition rate		1.0	–	20.0	MHz/ms
t_{9A}	Clock Jitter[27]	Peak-to-peak period jitter (t_{9A} Max. – t_{9A} min.), % of clock period ($f_{OUT} \leq 4$ MHz)		–	< 0.5	1	%
t_{9B}	Clock jitter[27]	Peak-to-peak period jitter (t_{9B} Max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)		–	< 0.7	1	ns
t_{9C}	Clock jitter[27]	Peak-to-peak period jitter (16 MHz < $f_{OUT} \leq$ 50 MHz)		–	< 400	500	ps
t_{9D}	Clock jitter[27]	Peak-to-peak period jitter ($f_{OUT} > 50$ MHz)		–	< 250	350	ps
t_{10A}	Lock time for CPLL	Lock time from power-up		–	< 25	50	ms
t_{10B}	Lock time for UPLL and SPLL	Lock time from power-up		–	< 0.25	1	ms
	Slew limits	CPU PLL Slew limits	CY2291I	8	–	90	MHz
			CY2291FI	8	–	80	MHz

Notes
23. XBUF duty cycle depends on XTALIN duty cycle.
24. Measured at 1.4 V.
25. Measured between 0.4 V and 2.4 V.
26. CLKF is not guaranteed to be in phase with CLKA-D, even if it is referenced off the same PLL.
27. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit. For more information on jitter, please refer to the WhitePaper: "Datasheet Jitter Specifications for Cypress Timing Products".

Switching Characteristics, Industrial 3.3 V

Parameter	Name	Description		Min	Typ	Max	Unit
t_1	Output period	Clock output range, 3.3 V operation	CY2291I	15 (66.6 MHz)	–	13000 (76.923 kHz)	ns
			CY2291FI	16.66 (60 MHz)	–	13000 (76.923 kHz)	ns
	Output duty cycle[28]	Duty cycle for outputs, defined as $t_2 \div t_1$[29] $f_{OUT} \geq 66$ MHz		40%	50%	60%	–
		Duty cycle for outputs, defined as $t_2 \div t_1$[29] $f_{OUT} < 66$ MHZ		45%	50%	55%	–
t_3	Rise time	Output clock rise time [30]		–	3	5	ns
t_4	Fall time	Output clock fall time [30]		–	2.5	4	ns
t_5	Output disable time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW		–	10	15	ns
t_6	Output enable time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH		–	10	15	ns
t_7	Skew	Skew delay between any identical or related outputs [29, 31]		–	< 0.25	0.5	ns
t_8	CPUCLK slew	Frequency transition rate		1.0	–	20.0	MHz/ms
t_{9A}	Clock jitter[32]	Peak-to-peak period jitter (t_{9A} Max. – t_{9A} min.), % of clock period ($f_{OUT} \leq 4$ MHz)		–	< 0.5	1	%
t_{9B}	Clock jitter[32]	Peak-to-peak period jitter (t_{9B} Max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)		–	< 0.7	1	ns
t_{9C}	Clock jitter[32]	Peak-to-peak period jitter (16 MHz $< f_{OUT} \leq$ 50 MHz)		–	< 400	500	ps
t_{9D}	Clock jitter[32]	Peak-to-peak period jitter ($f_{OUT} >$ 50 MHz)		–	< 250	350	ps
t_{10A}	Lock time for CPLL	Lock time from power-up		–	< 25	50	ms
t_{10B}	Lock time for UPLL and SPLL	Lock time from power-up		–	< 0.25	1	ms
	Slew limits	CPU PLL slew limits	CY2291I	8	–	66.6	MHz
			CY2291FI	8	–	60	MHz

Notes
28. XBUF duty cycle depends on XTALIN duty cycle.
29. Measured at 1.4 V.
30. Measured between 0.4 V and 2.4 V.
31. CLKF is not guaranteed to be in phase with CLKA-D, even if it is referenced off the same PLL.
32. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit. For more information on jitter, please refer to the WhitePaper: "Datasheet Jitter Specifications for Cypress Timing Products".

Switching Waveforms

Figure 2. All Outputs, Duty Cycle and Rise/Fall Time

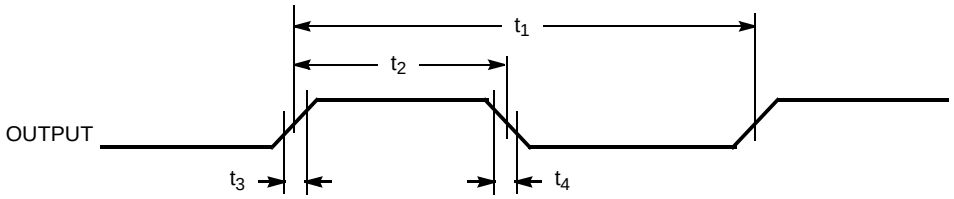


Figure 3. Output Three-State Timing [33]

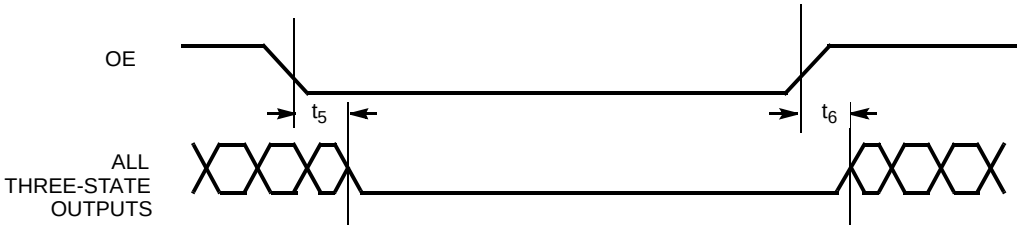


Figure 4. CLK Outputs Jitter and Skew

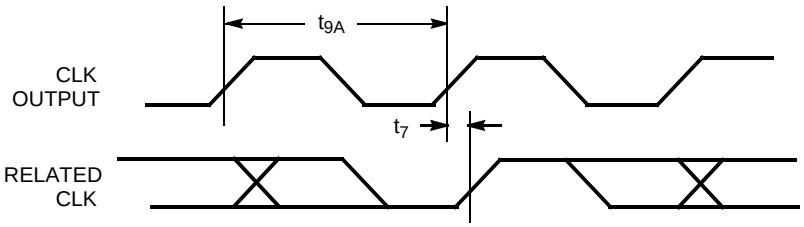
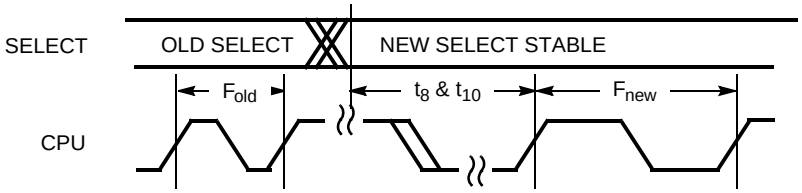
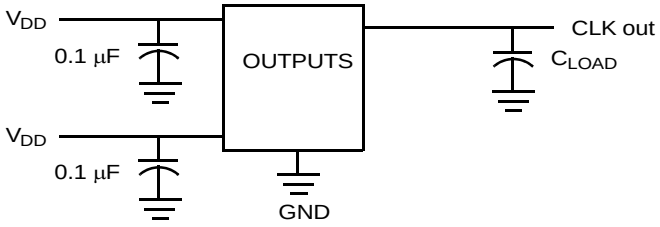


Figure 5. CPU Frequency Change



Test Circuit

Figure 6. Test Circuit



Note
33. The CY2291 has weak pull downs on all outputs (except 32K). Hence, when a three-state condition is forced on the outputs, the output pins are pulled LOW.

Ordering Information

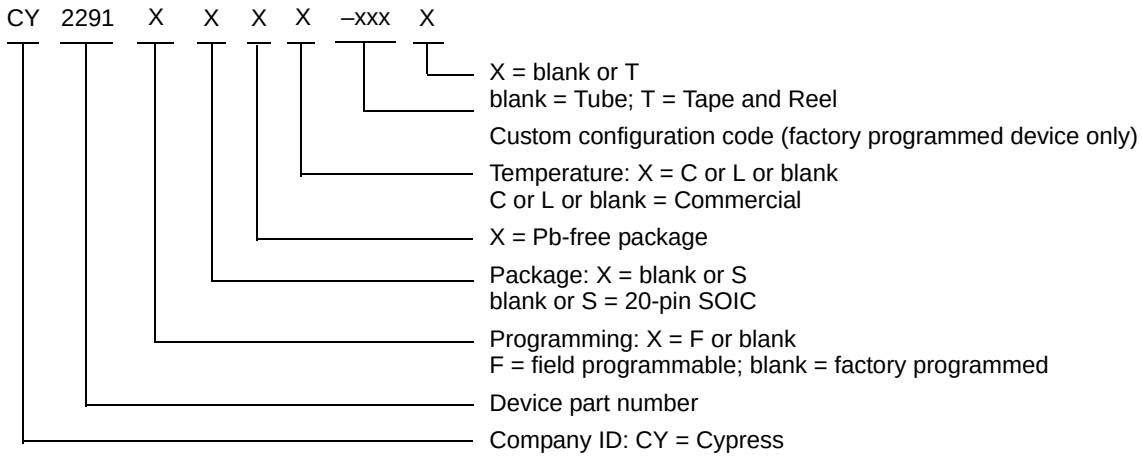
Ordering Code	Package Type	Operating Range	Operating Voltage
Pb-free			
CY2291FX	20-pin SOIC	Commercial	3.3 V or 5.0 V
CY2291FXT	20-pin SOIC – Tape and reel	Commercial	3.3 V or 5.0 V

Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE of Sales Representative for more information.

Possible Configurations

Ordering Code	Package Type	Operating Range	Operating Voltage
Pb-free			
CY2291SXC-XXX	20-pin SOIC	Commercial	5.0 V
CY2291SXC-XXXT	20-pin SOIC – Tape and reel	Commercial	5.0 V
CY2291SXL-XXX	20-pin SOIC	Commercial	3.3 V
CY2291SXL-XXXT	20-pin SOIC – Tape and reel	Commercial	3.3 V

Ordering Code Definitions



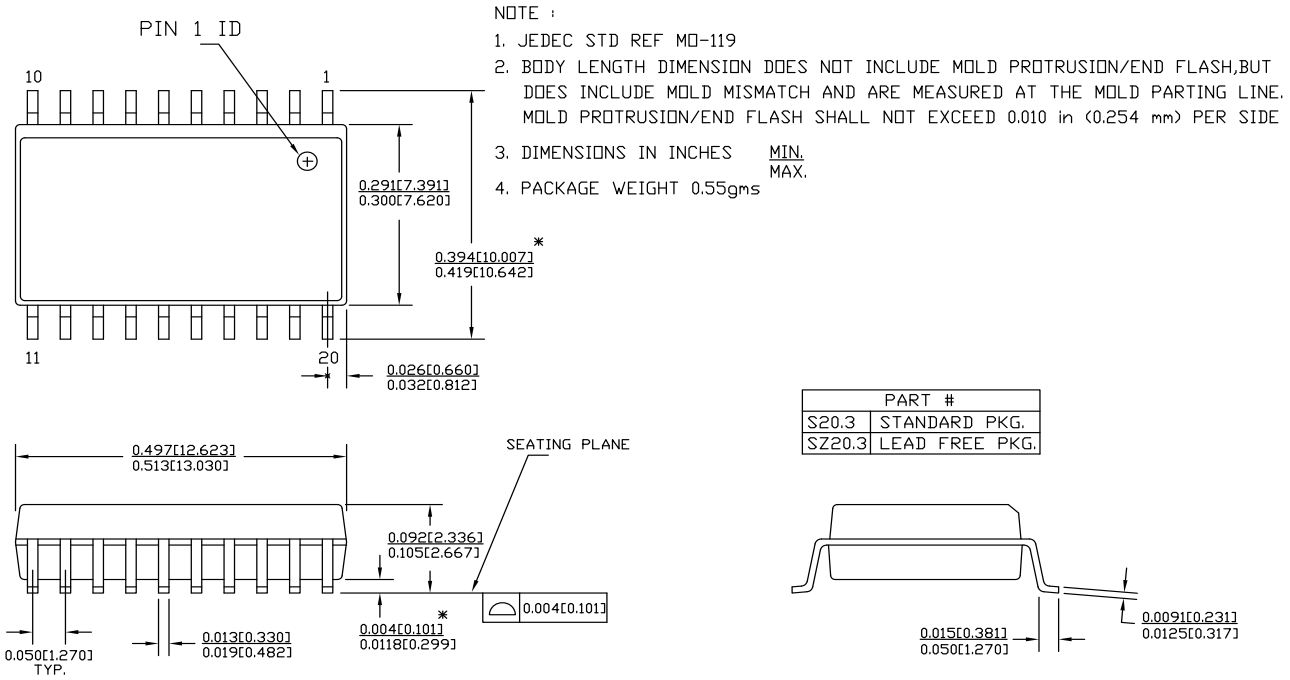
Packaging Information

Package Characteristics

Package	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Transistor Count
20-pin SOIC	70	46	9271

Package Diagram

Figure 7. 20-pin SOIC (0.513 × 0.300 × 0.0932 Inches) Package Outline, 51-85024



51-85024 *F

Acronyms

Acronym	Description	Acronym	Description
CLKIN	Clock Input	SPLL	System Phase Locked Loop
CMOS	complementary Metal Oxide Semiconductor	PPM	Parts Per Million
OE	Output Enable	FTG	Frequency Time Generator
PLL	Phase Locked Loop	FAE	Field Application Engineer

Document Conventions

Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degrees Celsius	µV	microvolt
fF	femtofarad	mA	milliampere
KB	1024 bytes	ms	millisecond
Kbit	1024 bits	nA	nanoampere
kHz	kilohertz	ns	nanosecond
MHz	megahertz	nV	nanovolt
M?	megaohm	pA	picoampere
µA	microampere	pF	picofarad
µF	microfarad	pp	peak-to-peak
µH	microhenry	ppm	parts per million
µs	microsecond	ps	picosecond

Document History Page

Document Title: CY2291, Three-PLL General Purpose EPROM Programmable Clock Generator Document Number: 38-07189				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110321	SZV	10/28/01	Change from Spec number: 38-00410 to 38-07189
*A	121836	RBI	12/14/02	Power up requirements added to Operating Conditions Information
*B	276756	RGL	10/18/04	Added Lead Free Devices
*C	2565316	AESA / KVM	09/16/08	Added Note “Not recommended for new designs.” Removed part number CY2291F, CY2291FT, CY2291SC-XXX, CY2291SC-XXXT, CY2291SI-XXX, CY2291SI-XXXT, CY2291SL-XXX, CY2291SL-XXXT, CY2291FIT, CY2291SXI-XXX, CY2291SXI-XXXT, CY2291FXI and CY2291FXIT. Changed CyClocks reference to include CyberClocks. Changed Lead-free to Pb-free. Updated Package diagram 51-85024 *B to 51-85024 *C. Updated template.
*D	2898985	KVM	03/25/2010	Updated Ordering Information. Added note regarding Possible Configurations in Ordering Information section. Added Possible Configurations (for “xxx’ parts). Updated Package Diagram
*E	3080949	BASH	11/10/2010	Removed Benefits. Added Functional Description content Removed Operation content from the data sheet. Added Acronyms and Units of Measure. Updated as per new template
*F	3450141	PURU	01/12/2011	Added note 1 regarding VBATT and Watch crystal Removed multiple occurrences of many notes Changed θ_{JA} and θ_{JC} values to 70 and 46 respectively under Package Characteristics section.
*G	3849272	PURU	12/21/2012	Removed “Understanding the CY2291 and CY2292” application note related information in all instances across the document.
*H	4201345	CINM	11/25/2013	Updated Packaging Information: Updated Package Diagram: spec 51-85024 – Changed revision from *D to *E. Updated in new template. Completing Sunset Review.
*I	4576237	XHT	11/21/2014	Added related documentation hyperlink in page 1. Updated Figure 7 (spec 51-85024 *E to *F) in Package Diagram .

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