CY2303

Phase-Aligned Clock Multiplier

Features

- 3-Multiplier configuration (1x, 2x, 4x ref)
- 10 MHz to 166.67 MHz operating range (reference input from 10 MHz to 41.67 MHz)
- Phase alignment
- 80 ps typical period jitter
- Output enable pin
- 3.3 V operation
- 5 V tolerant input
- 8-pin 150-mil small-outline integrated circuit (SOIC) package
- Commercial temperature range

Functional Description

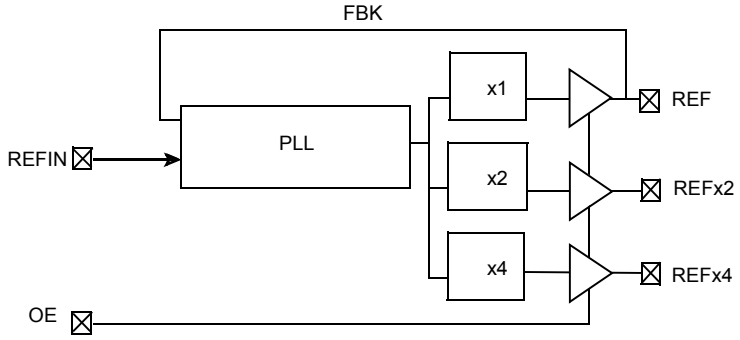
The CY2303 is a 3 output 3.3 V phase-aligned system clock designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

The part allows user to obtain 1x, 2x, and 4x REFIN output frequencies on respective output pins.

The CY2303 has an on-chip PLL, which locks to an input clock presented on the REFIN pin. The PLL feedback is internally connected to the REF output. The input-to-output is guaranteed to be less than ±200 ps, and output-to-output skew is guaranteed to be less than 200 ps.

Multiple CY2303 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 400 ps.

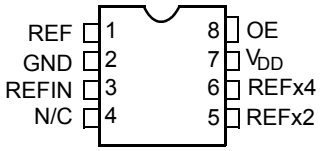
Logic Block Diagram



Contents

Pin Configurations

Figure 1. 8-pin SOIC pinout



Pin Description

Pin	Signal [1]	Description
1	REF	REF output (1x reference input)
2	GND	Ground
3	REFIN	Input reference frequency, 5 V tolerant input
4	N/C	No connect
5	REFx2	2x reference input
6	REFx4	4x reference input
7	V_{DD}	3.3 V supply
8	OE	Output enable (weak pull-up)

Note
1. Weak pull-down on all outputs.

Maximum Ratings

Supply voltage to ground potential ..... –0.5 V to +7.0 V
DC input voltage (except ref) ..... –0.5 V to V_{DD} + 0.5 V
DC input voltage REFIN ..... –0.5 V to 7 V

Storage temperature ..... –65 °C to +150 °C
Junction temperature ..... 150 °C
Static discharge voltage
(per MIL-STD-883, method 3015) ..... > 2000 V

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	0	70	°C
C_L	Load capacitance, 10 MHz < F_{OUT} < 133.33 MHz	–	18	pF
	Load capacitance, 133.33 MHz < F_{OUT} < 166.67 MHz	–	12	pF
C_{IN}	Input capacitance	–	7	pF
t_{PU}	Power-up time for all V_{DD}'s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage		–	0.8	V
V_{IH}	Input HIGH voltage		2.0	–	V
I_{IL}	Input LOW current	V_{IN} = 0 V	–	100	µA
I_{IH}	Input HIGH current	V_{IN} = V_{DD}	–	50	µA
V_{OL}	Output LOW voltage [2]	I_{OL} = 8 mA	–	0.4	V
V_{OH}	Output HIGH voltage [2]	I_{OH} = –8 mA	2.4	–	V
I_{DD}	Supply current	Unloaded outputs, REFIN = 41.67 MHz	–	45	mA
		Unloaded outputs, REFIN = 25 MHz	–	32	mA
		Unloaded outputs, REFIN = 10 MHz	–	18	mA

Note
2. Parameter is guaranteed by design and characterization. It is not 100% tested in production.

Switching Characteristics

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
$1/t_1$	Output frequency	18-pF load	10	–	133.33	MHz
		12-pF load	–	–	166.67	MHz
	Duty cycle [3] = $t_2 \div t_1$	Measured at $V_{DD}/2$	40	50	60	%
t_3	Rise time [3]	Measured between 0.8 V and 2.0 V	–	–	1.20	ns
t_4	Fall time [3]	Measured between 0.8 V and 2.0 V	–	–	1.20	ns
t_5	Output to output skew on rising edges [3]	All outputs equally loaded Measured at $V_{DD}/2$	–	–	200	ps
t_6	Delay, REFIN rising edge to REF rising edge [3]	Measured at $V_{DD}/2$ from REFIN to any output	–	–	±200	ps
t_7	Device to device skew [3]	Measured at $V_{DD}/2$ on the REF pin of the device (pin 1)	–	–	400	ps
t_J	Period jitter [3]	Measured at F_{OUT} < 133.33 MHz, loaded outputs, 18-pF load	–	±80	±175	ps
t_{LOCK}	PLL lock time [3]	Stable power supply, valid clocks presented on REFIN	–	–	1.0	ms

Note
3. All parameters are specified with loaded outputs.

Switching Waveforms

Figure 2. Duty Cycle Timing

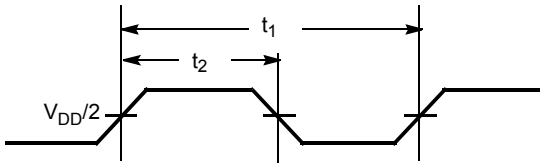


Figure 3. All Outputs Rise/Fall Time

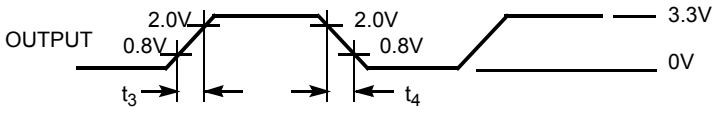


Figure 4. Output to Output Skew

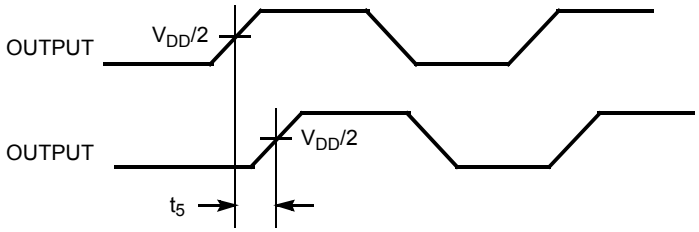


Figure 5. Input to Output Propagation Delay

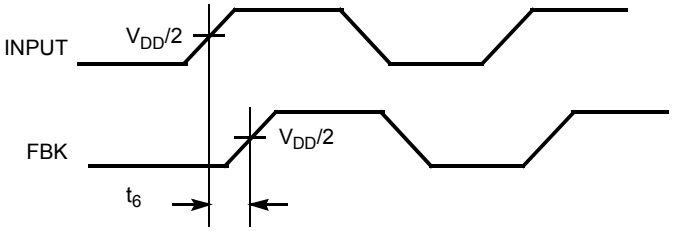
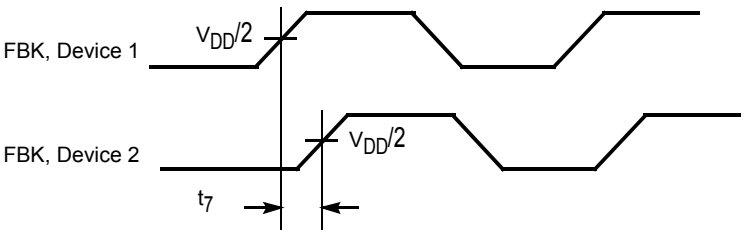
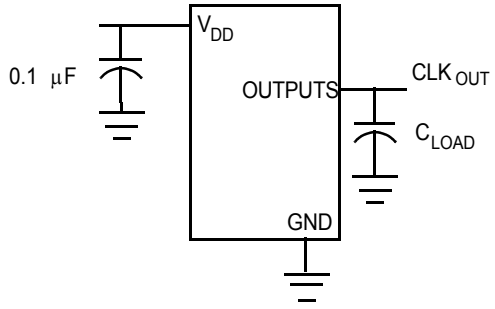


Figure 6. Device to Device Skew



Test Circuits

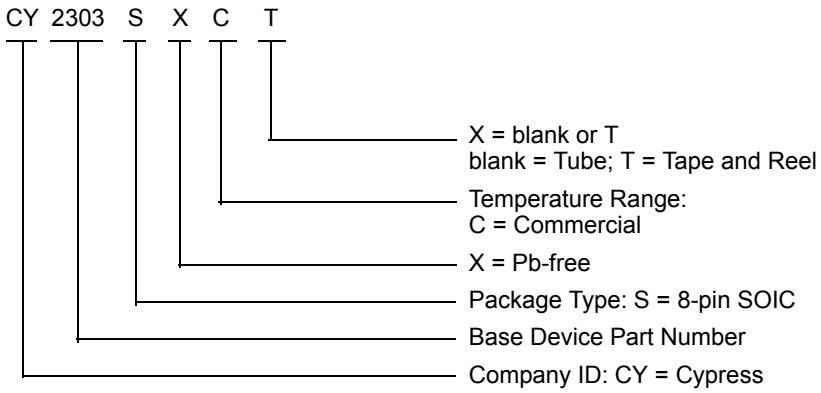
Figure 7. Test Circuit #1



Ordering Information

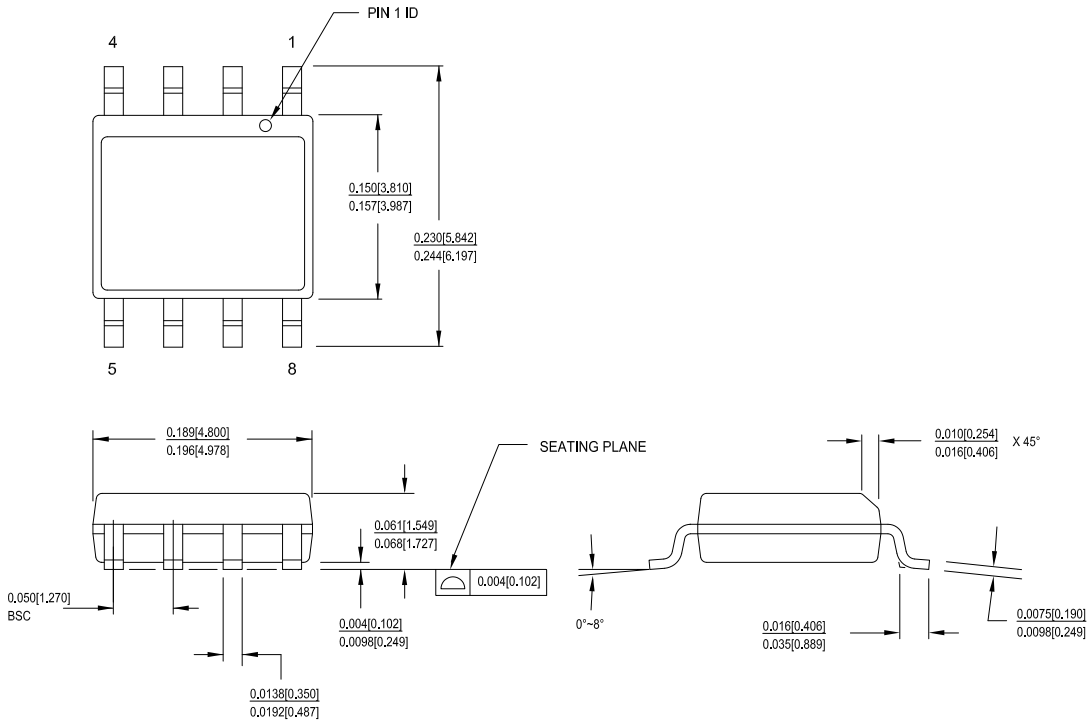
Ordering Code	Package Type	Operating Range
Pb-free		
CY2303SXC	8-pin SOIC (150 Mils)	Commercial (0 °C to 70 °C)
CY2303SXCT	8-pin SOIC (150 Mils) - Tape and Reel	Commercial (0 °C to 70 °C)

Ordering Code Definitions



Package Diagram

Figure 8. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066



51-85066 *F

Acronyms

Acronym	Description
FBK	Feedback
OE	Output Enable
PLL	Phase Locked Loop
REFIN	Reference Input

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
kHz	kilohertz
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
pA	picoampere
pF	picofarad
ps	picosecond
V	volt

Reference Documents

Reference documents are available through your local Cypress sales representative. You can also direct your requests to tsbusdev@cypress.com.

Document Number	Document Title	Description
NA	NA	NA

Errata

This section describes the errors, workaround solution and silicon design fixes for Cypress zero delay clock buffers belonging to the families CY2303. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Table 1. Part Numbers Affected

Part Number	Device Variants
CY2303SXC	All Variants
CY2303SXCT	All Variants

CY2303 Errata Summary

Items	Part Number	Fix Status
Start up lock time issue [CY2303]	All	Silicon fixed. New silicon available from WW 10 of 2013

CY2303 Qualification Status of fixed silicon

Product Status: In production

Qualification report last updated on 11/27/2012

http://www.cypress.com/?rID=72595

1. Start up lock time issue

■ **Problem Definition**

Output of CY2304 fails to locks within 1 ms upon power up (as per datasheet spec)

■ **Parameters Affected**

PLL lock time

■ **Trigger Condition(s)**

Start up

■ **Scope of Impact**

It can impact the performance of system and its throughput

■ **Workaround**

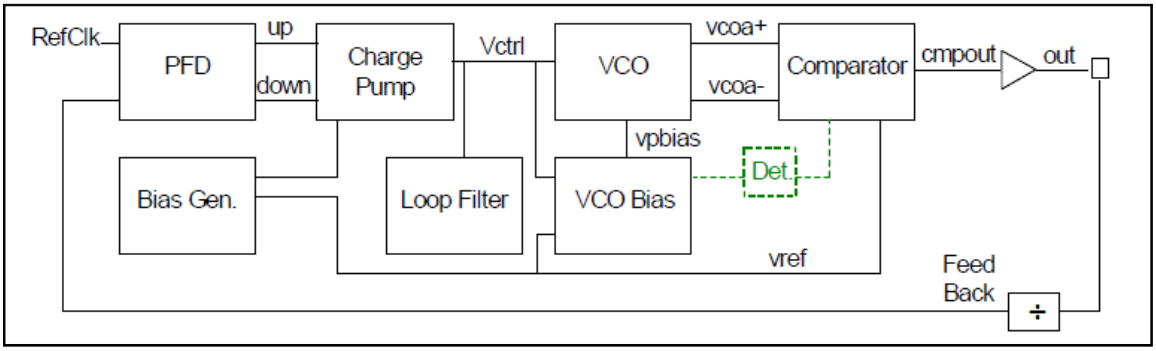
Apply reference input (RefClk) before power up (V_{DD}). If RefClk is applied after power up, noise gets coupled on the output and propagates back to the PLL causing it to take higher time to acquire lock. If reference input is present during power up, noise will not propagate to the PLL and device will start up normally without problems.

■ **Fix Status**

This issue is due to design marginality. Two minor design modifications have been made to address this problem.

a. Addition of VCO bias detector block as shown in the following figure keeps comparator power down till VCO bias is present and thereby eliminating the propagation of noise to feedback.

b. Bias generator enhancement for successful initialization.


RefClk
PFD
up
down
Charge Pump
Vctrl
VCO
vcoa+
vcoa-
Comparator
cmpout
out
vpbias
Det
Bias Gen.
Loop Filter
VCO Bias
vref
Feed Back
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Document History Page

Document Title: CY2303, Phase-Aligned Clock Multiplier Document Number: 38-07249				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110514	SZV	01/07/02	Change from Spec number: 38-01036 to 38-07249
*A	121852	RBI	12/14/02	Power up requirements added to Operating Conditions Information
*B	390413	RGL	08/10/05	Added Lead-free devices Added typical values for jitter
*C	2568533	AESA	09/23/08	Updated template. Removed part number CY2303SC and CY2303SI from Selector Guide table. Removed part number CY2303SC, CY2303SCT, CY2303SI, and CY2303SIT.
*D	2897294	KVM	03/22/10	Removed part numbers CY2303SXI and CY2303SXIT from ordering information table and related industrial temperature references. Updated package diagram. Updated copyright section.
*E	3026183	BASH	09/01/2010	Updated t_J from 80 ps to ±80 ps in Switching Characteristics on page 3. Added Ordering Code Definitions. Added Acronyms, Units of Measure and Reference Documents.
*F	4018186	CINM	06/10/2013	Updated Package Diagram: spec 51-85066 – Changed revision from *D to *F. Added Errata.
*G	4127379	CINM	10/23/2013	Updated in new template. Completing Sunset Review.

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