

Single-PLL General Purpose EPROM Programmable Clock Generator

Features

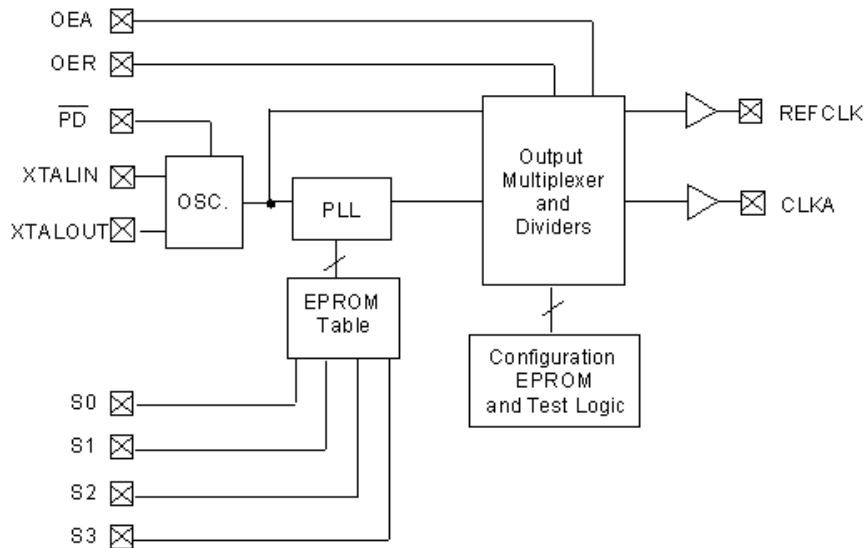
- Single phase locked loop (PLL) architecture
- EPROM programmability
- Factory programmable (CY2907) or field programmable (CY2907F) device options
- Up to two configurable outputs
- Low skew, low jitter, high accuracy outputs
- Power management (power-down, OE)
- Frequency select option
- Configurable 5 V or 3.3 V Operation
- 8-pin or 14-pin SOIC packages

Benefits

- Generates a custom frequency from an external source
- Easy customization and fast turnaround
- Programming support available for all opportunities
- Provides clocking requirements from a single device
- Meets critical industry standard timing requirements
- Supports low power applications
- Up to 16 user selectable frequencies
- Supports industry standard design platforms
- Industry standard packaging saves on board space

For a complete list of related documentation, click [here](#).

Logic Block Diagram



Contents

Pin Configurations	3	Ordering Information	10
Pin Description	3	Ordering Code Definitions	10
Functional Description	4	Package Characteristics	10
Device Programming	4	Package Diagrams	11
CyberClocks™ Software	4	Acronyms	13
Cypress CY3670 Programming Kit	4	Document Conventions	13
Maximum Ratings	5	Units of Measure	13
Operating Conditions	5	Document History Page	14
Electrical Characteristics	6	Sales, Solutions, and Legal Information	15
Electrical Characteristics	6	Worldwide Sales and Design Support	15
Switching Characteristics	7	Products	15
Switching Characteristics	8	PSoC® Solutions	15
Switching Waveforms	9	Cypress Developer Community	15
Test Circuit	9	Technical Support	15

Pin Configurations

Figure 1. 14-pin SOIC and 8-pin SOIC pinouts (Top View)



Pin Description

Name	Pin Number		Description
	14-pin SOIC	8-pin SOIC	
S1	1	5	Frequency select (CLKA) (internal pull-up resistor to V _{DD})
S2	2	NA	Frequency select (CLKA) (internal pull-up resistor to V _{DD})
S3	3	NA	Frequency select (CLKA) (internal pull-up resistor to V _{DD})
V _{SS}	4	2	Ground
V _{SS}	5	NA	Ground
$\overline{\text{PD}}$	6	NA	Power-down (active LOW) (internal pull-up resistor to V _{DD})
XTALIN ^[1]	7	3	Reference crystal input
XTALOUT ^[1, 2]	8	4	Reference crystal feedback
OER	9	NA	REFCLK output enable (active HIGH) (internal pull-up resistor to V _{DD})
OEA	10	NA	CLKA output enable (active HIGH) (internal pull-up resistor to V _{DD})
CLKA	11	6	Clock output
V _{DD}	12	7	Voltage supply
REFCLK	13	8	Reference clock output (default, can be driven by PLL if desired)
S0	14	1	Frequency select (CLKA) (internal pull-up resistor to V _{DD})

Notes

- For best accuracy, use a parallel resonant crystal, C_{LOAD} ≈ 17 pF.
- Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to crystal).

Functional Description

The CY2907 is a general purpose clock generator designed for use in a wide variety of applications — from graphics to PC peripherals to disk drives. It generates selectable system clock frequencies from a single reference input (crystal or reference clock). The CY2907 is configured with an EPROM array, similar to the other devices in the Cypress EPROM Programmable Clock family, making it easy to customize for any application. Furthermore, the CY2907 is compatible with all industry standard 9107 and 9108 clock synthesizers.

Device Programming

Two versions of the CY2907 are available - Field Programmable and Factory Programmable. Field programmable devices must be programmed before being installed in an application. They are one-time-programmable (OTP). Customers can program small quantities in-house using the Cypress CY3670 programmer. Production quantities are available through Cypress's value-added distribution partners, or by using third party programmers from BP Microsystems, Hi-Lo Systems, and others.

For high volume orders, devices can be factory programmed by Cypress. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, you receive a new part number, samples, and a data sheet with the programmed values. This part number is used for additional sample requests and production orders.

CyberClocks™ Software

CyberClocks is an easy-to-use software application that enables the user to configure any one of the EPROM Programmable Clocks offered by Cypress. You may specify the input frequency, PLL and output frequencies, and different functional options. Note the output frequency ranges in this data sheet when specifying them in CyberClocks to make sure that you stay within the limits. After a configuration is established, you can print the configuration and save programming files in ENT and JED formats.

CyberClocks runs on PCs running the Windows™ operating system, and is available for free download on the Cypress Semiconductor website at www.cypress.com.

Within the CyberClocks application, the CY2907 is found in the CyClocks™ section. Note that the standalone CyberClocks software should not be confused with the CyberClocks Online software, which is a web-based application that is used to configure other programmable clock devices.

Cypress CY3670 Programming Kit

Cypress's CY3670 is a portable programmer that connects to a PC serial port and enables users of CyClocks software to quickly and easily program any of the CY2291F, CY2292F, CY2071AF, and CY2907F devices. An adapter is also required and is ordered separately. The CY3097 is the adapter for the CY2907F8. For the CY2907F14, order adapter CY3098.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply voltage -0.5 to +7.0 V
 Input voltage -0.5 V to V_{DD} + 0.5 V

Storage temperature (non-condensing) ... -65 °C to +150 °C
 Max soldering temperature (10 sec) +260 °C
 Junction temperature +150 °C
 Static discharge voltage
 (per MIL-STD-883, method 3015) > 2000 V

Operating Conditions

Parameter ^[3]	Description	Min	Max	Unit
V _{DD}	Supply voltage, 5 V operation	4.5	5.5	V
	Supply voltage, 3.3 V operation	3.0	3.6	V
T _A	Commercial operating temperature, Ambient	0	70	°C
C _L	Maximum capacitive load	–	15	pF
f _{REF}	External reference crystal	10.0	25.0	MHz
	External reference clock ^[4, 5]	1.0	30.0	MHz

Notes

- 3. Electrical parameters are guaranteed with these operating conditions.
- 4. Guaranteed by design, not 100% tested in production.
- 5. Load = max typical configuration, f_{REF} = 14.318 MHz. Specific configurations may vary. A close approximation of I_{DD} can be derived by the following formula:
 $I_{DD} \text{ (mA)} = V_{DD} \times (6.25 + (0.055 \times f_{REF}) + (0.0017 \times C_{LOAD} \times (F_{CLKA} + REFCLK)))$. C_{LOAD} is specified in pF and F is specified in MHz.

Electrical Characteristics

At 5.0 V Commercial ($V_{DD} = 4.5 \text{ V to } 5.5 \text{ V}$, $T_A = 0 \text{ }^\circ\text{C to } +70 \text{ }^\circ\text{C}$)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	Except crystal inputs	2.0	–	V
V_{IL}	Low-level input voltage	Except crystal inputs	–	0.8	V
$V_{OH}^{[6]}$	High-level output voltage	$V_{DD} = V_{DD} \text{ Min.}$ $I_{OH} = -30 \text{ mA}$ CLKA	2.4	–	V
$V_{OL}^{[6]}$	Low-level output voltage	$V_{DD} = V_{DD} \text{ Min.}$ $I_{OL} = 10 \text{ mA}$ CLKA	–	0.4	V
$I_{OH}^{[6]}$	Output high current	$V_{OH} = 2.0 \text{ V}$	–	–35	mA
$I_{OL}^{[6]}$	Output low current	$V_{OL} = 0.8 \text{ V}$	22	–	mA
I_{IH}	Input high current	$V_{IH} = V_{DD}$	–2	2	μA
I_{IL}	Input low current	$V_{IL} = 0 \text{ V}$	–	20	μA
$I_{DD}^{[7]}$	Power supply current	$\overline{\text{PD}}$ HIGH, CLKA = 50 MHz	–	42	mA
I_{DD}	Power supply current	$\overline{\text{PD}}$ LOW, Logic inputs LOW	–	100	μA
I_{DD}	Power supply current	$\overline{\text{PD}}$ LOW, Logic inputs HIGH	–	40	μA
$R_{PU}^{[6]}$	Pull-up resistor	$V_{IN} = V_{DD} - 1.0 \text{ V}$	–	700	$\text{k}\Omega$

Electrical Characteristics

At 3.3 V Commercial ($V_{DD} = 3.0 \text{ V to } 3.6 \text{ V}$, $T_A = 0 \text{ }^\circ\text{C to } +70 \text{ }^\circ\text{C}$)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	Except crystal inputs	$0.7 \times V_{DD}$	–	V
V_{IL}	Low-level input voltage	Except crystal inputs	–	$0.2 \times V_{DD}$	V
$V_{OH}^{[8]}$	High-level output voltage	CLKA, $I_{OH} = -5 \text{ mA}$	$0.85 \times V_{DD}$	–	V
$V_{OL}^{[8]}$	Low-level output voltage	CLKA, $I_{OL} = 6 \text{ mA}$	–	$0.1 \times V_{DD}$	V
$I_{OH}^{[8]}$	Output high current	$V_{OH} = 0.7 \times V_{DD}$	–	–10	mA
$I_{OL}^{[8]}$	Output low current	$V_{OL} = 0.2 \times V_{DD}$	15	–	mA
I_{IH}	Input high current	$V_{IH} = V_{DD}$	–2	2	μA
I_{IL}	Input low current	$V_{IL} = 0 \text{ V}$	–	10	μA
$I_{DD}^{[9]}$	Power supply current	$\overline{\text{PD}}$ HIGH, CLKA = 50 MHz	–	40	mA
I_{DD}	Power supply current	$\overline{\text{PD}}$ LOW, Logic inputs LOW	–	40	μA
I_{DD}	Power supply current	$\overline{\text{PD}}$ LOW, Logic inputs HIGH	–	12	μA
$R_{PU}^{[8]}$	Pull-up resistor	$V_{IN} = V_{DD} - 0.5 \text{ V}$	–	900	$\text{k}\Omega$

Notes

6. Guaranteed by design, not 100% tested in production.

7. Load = max. typical configuration, $f_{REF} = 14.318 \text{ MHz}$. Specific configurations may vary. A close approximation of I_{DD} can be derived by the following formula:
 $I_{DD} \text{ (mA)} = V_{DD} \times (6.25 + (0.055 \times F_{REF}) + (0.0017 \times C_{LOAD} \times (F_{CLKA} + REFCLK)))$. C_{LOAD} is specified in pF and F is specified in MHz.

8. Guaranteed by design, not 100% tested in production.

9. Load = max. typical configuration, $f_{REF} = 14.318 \text{ MHz}$. Specific configurations may vary. A close approximation of I_{DD} can be derived by the following formula:
 $I_{DD} \text{ (mA)} = V_{DD} \times (6.25 + (0.055 \times F_{REF}) + (0.0017 \times C_{LOAD} \times (F_{CLKA} + REFCLK)))$. C_{LOAD} is specified in pF and F is specified in MHz.

Switching Characteristics

At 5.0 V Commercial

Parameter ^[10]	Output ^[11]	Description	Test Conditions	Min	Max	Unit
t _R	CLKA	Output rise time 0.8 V to 2.0 V	15 pF load	–	1.40	ns
t _F	CLKA	Output fall time 2.0 V to 0.8 V	15 pF load	–	1.00	ns
t _R	CLKA	Output rise time 20% to 80%	15 pF load	–	3.5	ns
t _F	CLKA	Output fall time 80% to 20%	15 pF load	–	2.5	ns
t _D	CLKA	Duty cycle	15 pF load at 1.4 V	45.0	55.0	%
F _I	XTALIN	Input frequency	Crystal oscillator	10	25	MHz
F _I	XTALIN	Input frequency	External input clock ^[12]	1	30	MHz
F _O	CLKA	Output frequency	CY2907, 15 pF load	0.5	130.0	MHz
			CY2907F, 15 pF load	0.5	100.0	MHz
t _{JIS}	CLKA	Jitter (one sigma)	20 MHz to 130 MHz	–	150	ps
t _{JIS}	CLKA	Jitter (one sigma)	14 MHz to 20 MHz	–	200	ps
t _{JIS}	CLKA	Jitter (one sigma)	Less than 14 MHz	–	1	%
t _{JAB}	CLKA	Jitter (absolute)	20 MHz to 130 MHz	–250	+ 250	ps
t _{JAB}	CLKA	Jitter (absolute)	14 MHz to 20 MHz	–500	+ 500	ps
t _{JAB}	CLKA	Jitter (absolute)	Less than 14 MHz	–	3	%
t _{PU}		Power-up time		–	18	ms
t _{FT}	CLKA	Transition time	8 MHz to 66.6 MHz	–	13	ms

Notes

10. Guaranteed by design, not 100% tested in production.

11. REFCLK output can also be configured to be driven by the PLL. In that case these characteristics are also valid.

12. Refer to the application note *Crystal Oscillator Topics* when using an external reference clock as an input frequency source.

Switching Characteristics

At 3.3 V Commercial

Parameter ^[13]	Output ^[14]	Description	Test Conditions	Min	Max	Unit
t _R	CLKA	Output rise time 20% to 80%	15 pF Load	–	3.5	ns
t _F	CLKA	Output fall time 80% to 20%	15 pF Load	–	2.5	ns
t _D	CLKA	Duty cycle	15 pF Load at 1.4 V	40.0	53.0	%
F _I	XTALIN	Input frequency	Crystal Oscillator	10	25	MHz
F _I	XTALIN	Input frequency	External Input Clock ^[15]	1	30	MHz
F _O	CLKA	Output frequency	CY2907, 15 pF Load	0.5	100.0	MHz
			CY2907F, 15 pF Load	0.5	80.0	MHz
t _{JIS}	CLKA	Jitter (one sigma)	25 MHz to 100 MHz	–	150	ps
t _{JIS}	CLKA	Jitter (one sigma)	14 MHz to 25 MHz	–	200	ps
t _{JIS}	CLKA	Jitter (one sigma)	Less than 14 MHz	–	1	%
t _{JAB}	CLKA	Jitter (absolute)	25 MHz to 120 MHz	–250	+250	ps
t _{JAB}	CLKA	Jitter (absolute)	14 MHz to 25 MHz	–500	+500	ps
t _{JAB}	CLKA	Jitter (absolute)	Less than 14 MHz	–	3	%
t _{PU}		Power-up time		–	18	ms
t _{FT}	CLKA	Transition time	8 MHz to 66.6 MHz	–	13	ms

Notes

13. Guaranteed by design, not 100% tested in production.

14. REFCLK output can also be configured to be driven by the PLL. In that case these characteristics are also valid.

15. Refer to the application note *Crystal Oscillator Topics* when using an external reference clock as an input frequency source.

Switching Waveforms

Figure 2. Frequency Select Change (Transition Time)

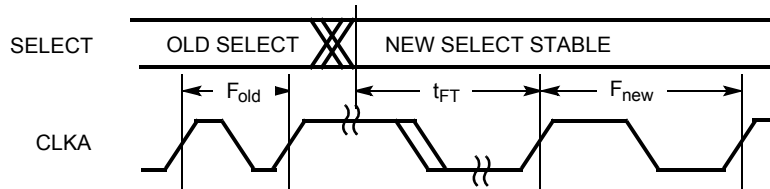


Figure 3. Duty Cycle Timing

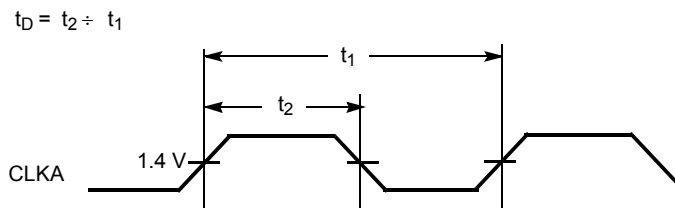
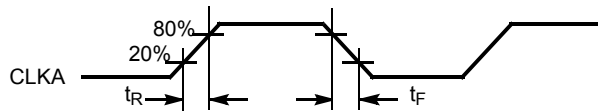
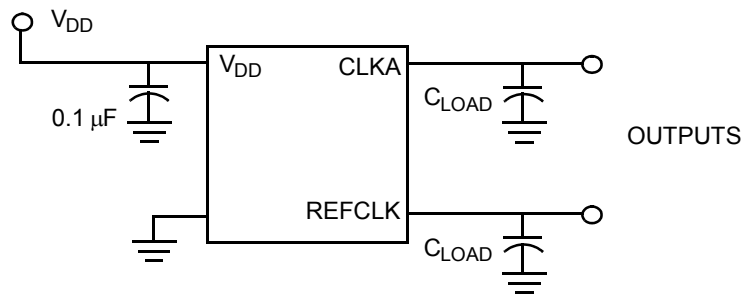


Figure 4. All Outputs Rise/Fall Time



Test Circuit

Figure 5. Test Circuit



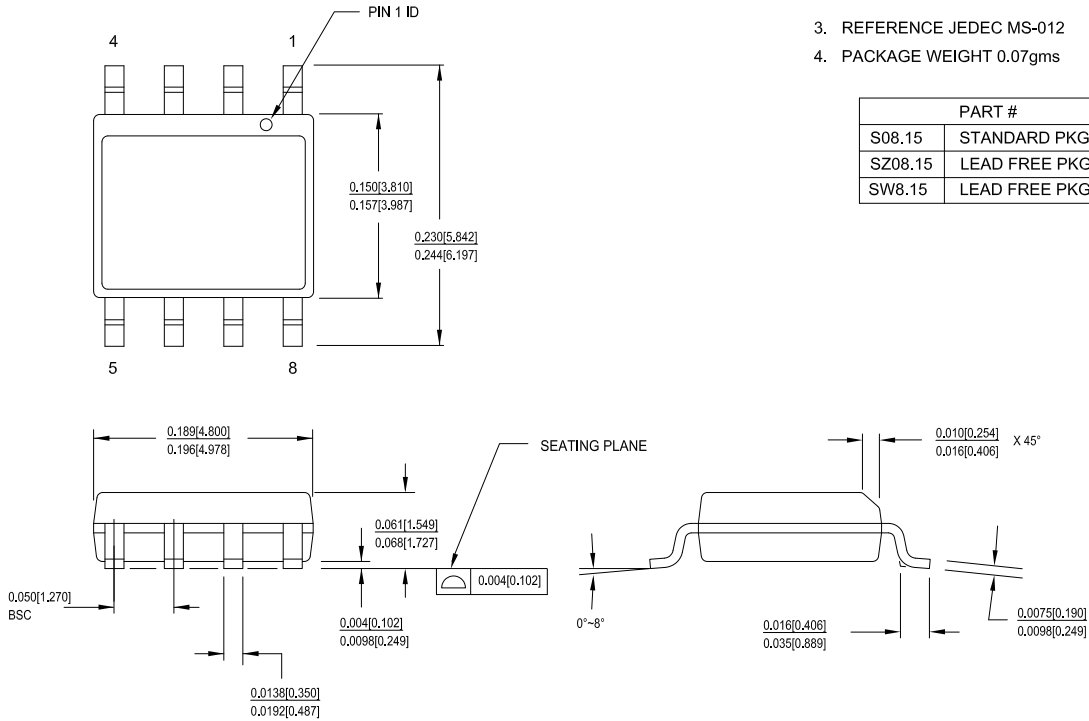
Note: All capacitors should be placed as close to each pin as possible.

Package Diagrams

Figure 6. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN.
MAX.
2. PIN 1 IS OPTIONAL,
ROUND ON SINGLE LEADFRAME
RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



51-85066 *F

Acronyms

Acronym	Description
EPROM	Erasable Programmable Read Only Memory
OE	Output Enable
PLL	Phase-Locked Loop
SOIC	Small-Outline Integrated Circuit
TSSOP	Thin-Shrink Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
ppm	parts per million
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY2907, Single-PLL General Purpose EPROM Programmable Clock Generator Document Number: 38-07137				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	110246	SZV	12/18/01	Change from Spec number: 38-00505 to 38-07137
*A	1088524	KVM / KKVTMP	See ECN	Added Pb-free for CY2907F8 and CY2907F14 field programmable devices Updated and added to text on page 2 Applied new template
*B	2715646	KVM / AESA	06/10/09	Removed industrial temperature references: page 1 features list, T _A spec, DC and AC electrical tables Removed Selector Guide table from page 1 Removed obsolete part numbers from the ordering information table: CY2907SC-xxx, CY2907SC-xxxT, CY2907SI-xxx, CY2907SI-xxxT, CY2907F8T, CY2907F8I, CY2907F8IT, CY2907F14T, CY2907F14I and CY2907F14IT Added note: "Not for new designs"
*C	2948496	KVM	06/09/10	Updated ordering information table. Updated package diagrams.
*D	3051170	BASH	10/07/2010	Updated Ordering Information and added Ordering Code Definitions . Added Acronyms and Units of Measure . Minor edits.
*E	3155189	BASH	01/27/2011	No technical updates.
*F	3402027	BASH	10/11/2011	Updated Ordering Information : Removed the following pruned parts CY2907SL-262 and CY2907SL-262T from the table. Updated package diagrams.
*G	4047640	CINM	07/02/2013	Updated Package Diagrams : spec 51-85066 – Changed revision from *E to *F. Completing Sunset Review.
*H	4399810	AJU	06/05/2014	Updated in new template. Added watermark "Not Recommended for New Designs".
*I	4587350	AJU	12/05/2014	Added related documentation hyperlink in page 1. Removed pruned parts CY2907FX14 and CY2907FX14T.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC[®] Solutions

[psoc.cypress.com/solutions](#)
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

[cypress.com/go/support](#)

© Cypress Semiconductor Corporation, 2001-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.