

## 2-Mbit (128K x 16) Static RAM

### Features

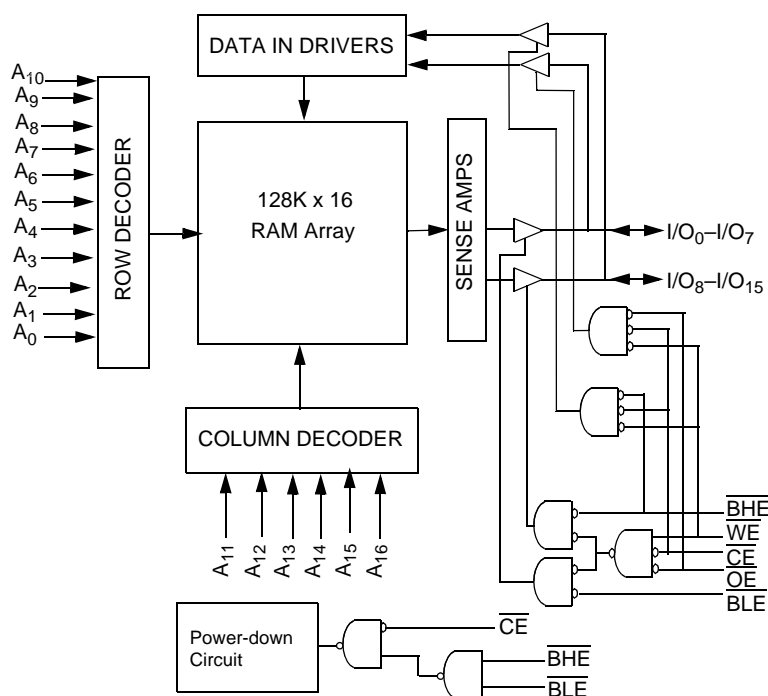
- **Temperature Ranges**
  - Industrial:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - Automotive-A:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - Automotive-E:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- **High Speed: 55 ns**
- **Wide voltage range: 2.7V–3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free 44-pin TSOP Type II package**

### Functional Description<sup>[1]</sup>

The CY62137VN is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in

portable applications such as cellular telephones. The device also has an automatic power-down feature that reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{\text{CE}}$  HIGH) or when  $\overline{\text{CE}}$  is LOW and both  $\overline{\text{BLE}}$  and  $\overline{\text{BHE}}$  are HIGH. The input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{\text{CE}}$  HIGH), outputs are disabled ( $\overline{\text{OE}}$  HIGH),  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$  are disabled ( $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW). Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ), is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{16}$ ). If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from I/O pins ( $\text{I/O}_8$  through  $\text{I/O}_{15}$ ) is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{16}$ ). Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing the Write Enable ( $\overline{\text{WE}}$ ) HIGH. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $\text{I/O}_0$  to  $\text{I/O}_7$ . If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from memory will appear on  $\text{I/O}_8$  to  $\text{I/O}_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

### Logic Block Diagram



#### Note:

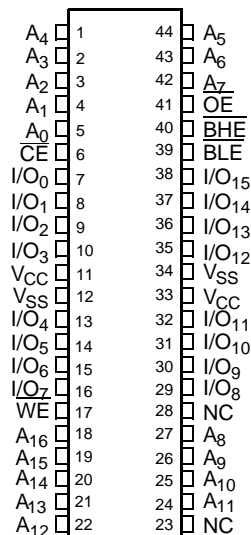
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

## Product Portfolio

Product		V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation			
						Operating, I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (μA)	
		Min.	Typ. <sup>[3]</sup>	Max.		Typ. <sup>[3]</sup>	Max.	Typ. <sup>[3]</sup>	Max.
CY62137VNLL	Industrial	2.7	3.0	3.6	55	7	20	1	15
CY62137VNLL					70	7	15	1	15
CY62137VNLL	Automotive-A				70	7	15	1	15
CY62137VNLL	Automotive-E				70	7	15	1	20

## Pin Configurations

TSOP II (Forward)  
Top View



## Pin Definitions

Pin Number	Type	Description
1–5, 18–22, 24–27, 42–45	Input	<b>A<sub>0</sub>–A<sub>16</sub>.</b> Address Inputs
7–10, 13–16, 29–32, 35–38	Input/Output	<b>I/O<sub>0</sub>–I/O<sub>15</sub>.</b> Data lines. Used as input or output lines depending on operation
23	No Connect	<b>NC.</b> This pin is not connected to the die
17	Input/Control	<b>WE.</b> When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
6	Input/Control	<b>CE.</b> When LOW, selects the chip. When HIGH, deselects the chip
40, 39	Input/Control	<b>Byte Write Select Inputs, active LOW.</b> <b>BHE</b> controls I/O <sub>15</sub> –I/O <sub>8</sub> , <b>BLE</b> controls I/O <sub>7</sub> –I/O <sub>0</sub> .
41	Input/Control	<b>OE.</b> Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins
12, 34	Ground	<b>V<sub>SS</sub>.</b> Ground for the device
11, 33	Power Supply	<b>V<sub>CC</sub>.</b> Power supply for the device

### Notes:

- NC pins are not connected on the die.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(TYP)</sub>, T<sub>A</sub> = 25°C.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.5V to +4.6V

DC Voltage Applied to Outputs

in High-Z State<sup>[4]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[4]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40°C to +85°C	2.7V to 3.6V
Automotive-A	-40°C to +85°C	
Automotive-E	-40°C to +125°C	

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-55			-70			Unit
			Min.	Typ. <sup>[3]</sup>	Max.	Min.	Typ. <sup>[3]</sup>	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 2.7V$ , $I_{OH} = -1.0$ mA	2.4			2.4			V
$V_{OL}$	Output LOW Voltage	$V_{CC} = 2.7V$ , $I_{OL} = 2.1$ mA			0.4			0.4	V
$V_{IH}$	Input HIGH Voltage		2.2		$V_{CC} + 0.5V$	2.2		$V_{CC} + 0.5V$	V
$V_{IL}$	Input LOW Voltage		-0.5		0.8	-0.5		0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-1		+1	μA
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1		+1	-1		+1	μA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$I_{OUT} = 0$ mA, $f = f_{MAX} = 1/t_{RC}$ , CMOS Levels	$V_{CC} = 3.6V$	Ind'l	7	20	7	15	mA
				Auto-A/ Auto-E			7	15	
		$I_{OUT} = 0$ mA, $f = 1$ MHz, CMOS Levels	$V_{CC} = 3.6V$	Ind'l	1	2	1	2	mA
				Auto-A/ Auto-E			1	2	
$I_{SB1}$	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = f_{MAX}$	$V_{CC} = 3.6V$	Ind'l		100		100	μA
				Auto-A/ Auto-E				100	
$I_{SB2}$	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = 0$	$V_{CC} = 3.6V$	Ind'l	1	15	1	15	μA
				Auto-A			1	15	
				Auto-E			1	20	

## Capacitance<sup>[5]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ C$ , $f = 1$ MHz, $V_{CC} = V_{CC(typ)}$	6	pF
$C_{OUT}$	Output Capacitance		8	pF

## Thermal Resistance<sup>[5]</sup>

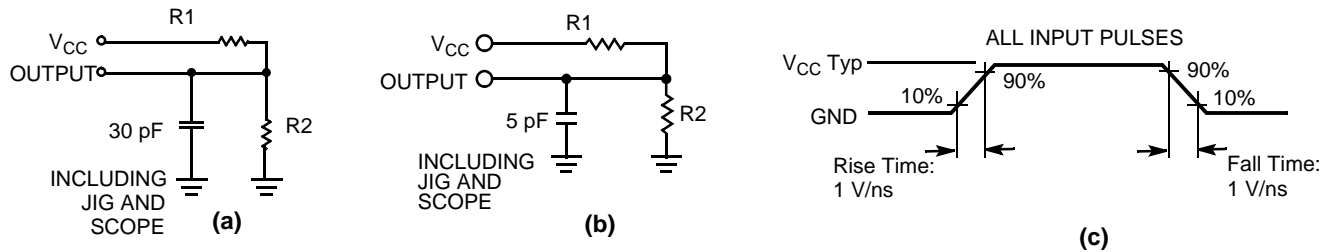
Parameter	Description	Test Conditions	TSOPII	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 2-layer printed circuit board	60	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		22	°C/W

### Notes:

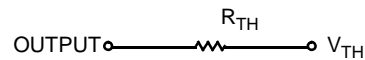
4.  $V_{IL(min.)} = -2.0V$  for pulse durations less than 20 ns.

5. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

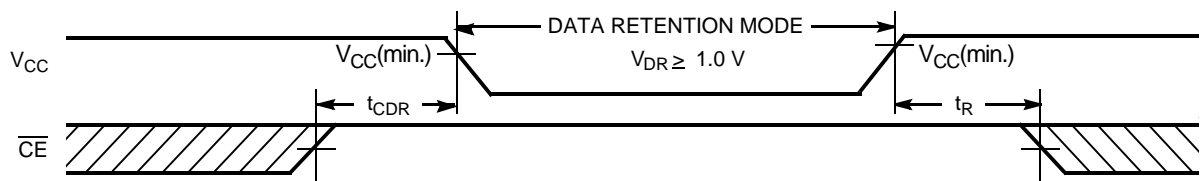


Parameters	Value	Unit
R1	1105	Ohms
R2	1550	Ohms
$R_{TH}$	645	Ohms
$V_{TH}$	1.75	Volts

## Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[3]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.0			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.0V$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ ; No input may exceed $V_{CC} + 0.3V$		0.5	7.5	$\mu A$
		Ind'I/Auto-A				
		Auto-E			10	
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns
$t_R$	Operation Recovery Time		$t_{RC}$			ns

## Data Retention Waveform



**Switching Characteristics** Over the Operating Range <sup>[6]</sup>

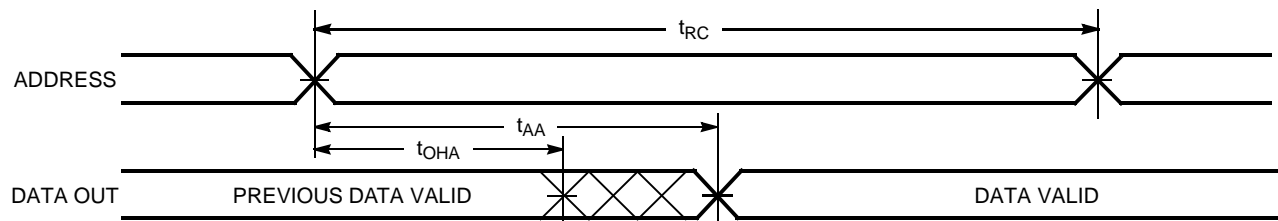
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z <sup>[7]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[7, 8]</sup>		25		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low-Z <sup>[7]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High-Z <sup>[7, 8]</sup>		25		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-down		55		70	ns
t <sub>DBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Data Valid		55		70	ns
t <sub>LZBE</sub> <sup>(9)</sup>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low-Z	5		5		ns
t <sub>HZBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High-Z		25		25	ns
Write Cycle <sup>[10, 11]</sup>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	45		60		ns
t <sub>AW</sub>	Address Set-up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	40		50		ns
t <sub>SD</sub>	Data Set-up to Write End	25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[7, 8]</sup>		20		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[7]</sup>	5		10		ns
t <sub>BW</sub>	$\overline{BHE}$ / $\overline{BLE}$ LOW to End of Write	50		60		ns

**Notes:**

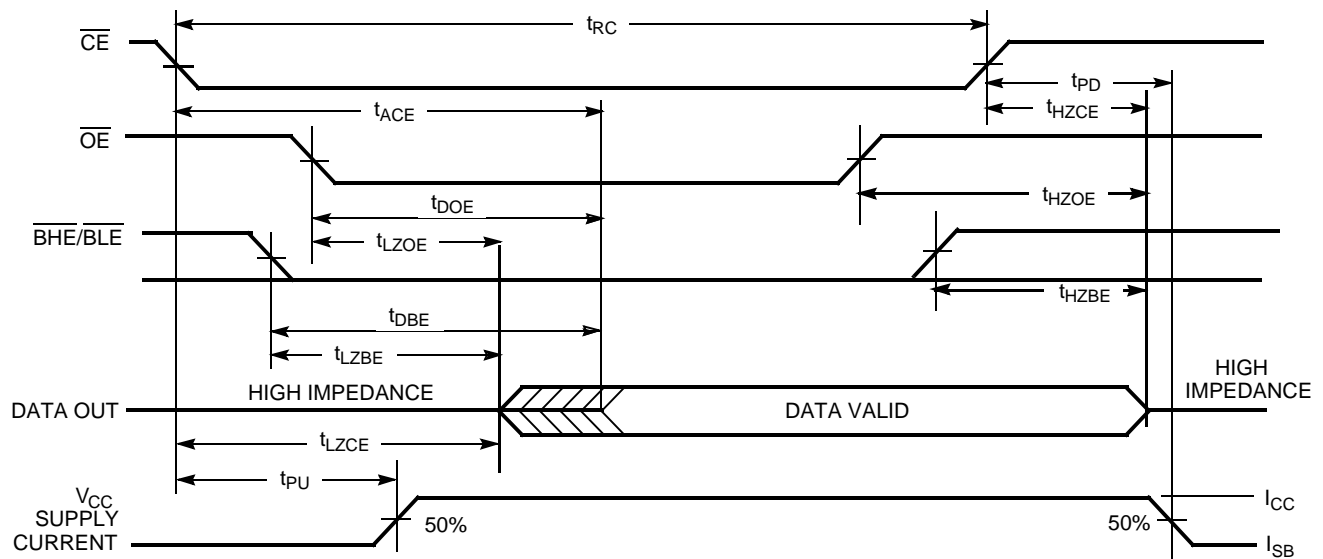
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to V<sub>CC</sub> typ., and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
7. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
8. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. If both byte enables are toggled together this value is 10 ns.
10. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

## Switching Waveforms

### Read Cycle No. 1<sup>[12, 13]</sup>



### Read Cycle No. 2<sup>[13, 14]</sup>

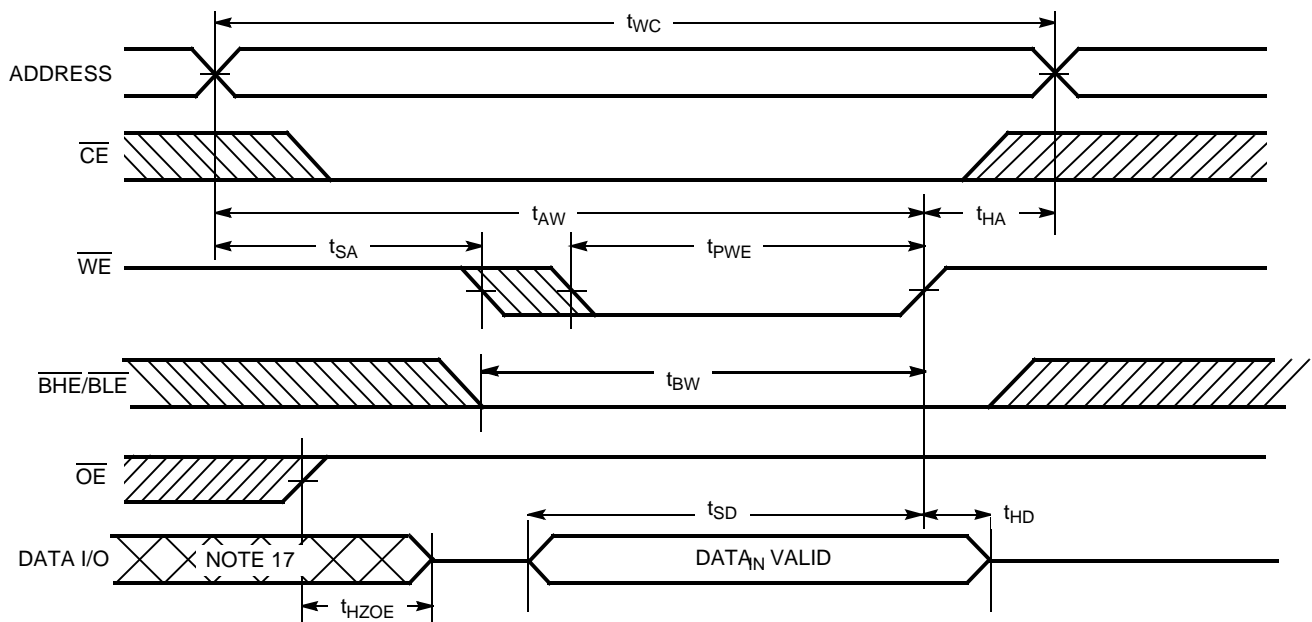


#### Notes:

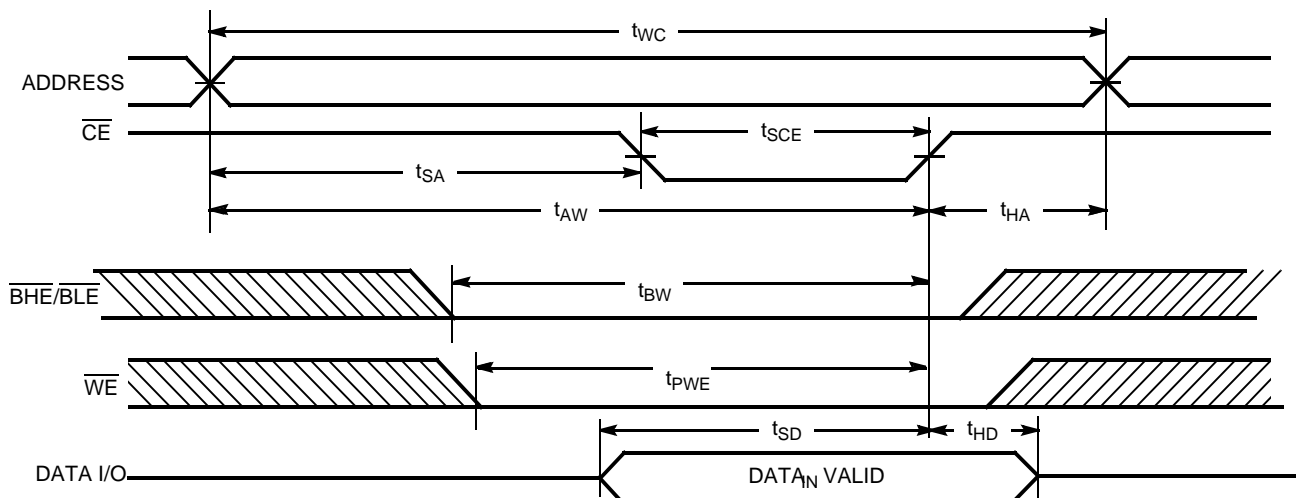
12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
13.  $\overline{WE}$  is HIGH for read cycle.
14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms (continued)

### Write Cycle No. 1 ( $\overline{\text{WE}}$ Controlled)<sup>[10, 15, 16]</sup>

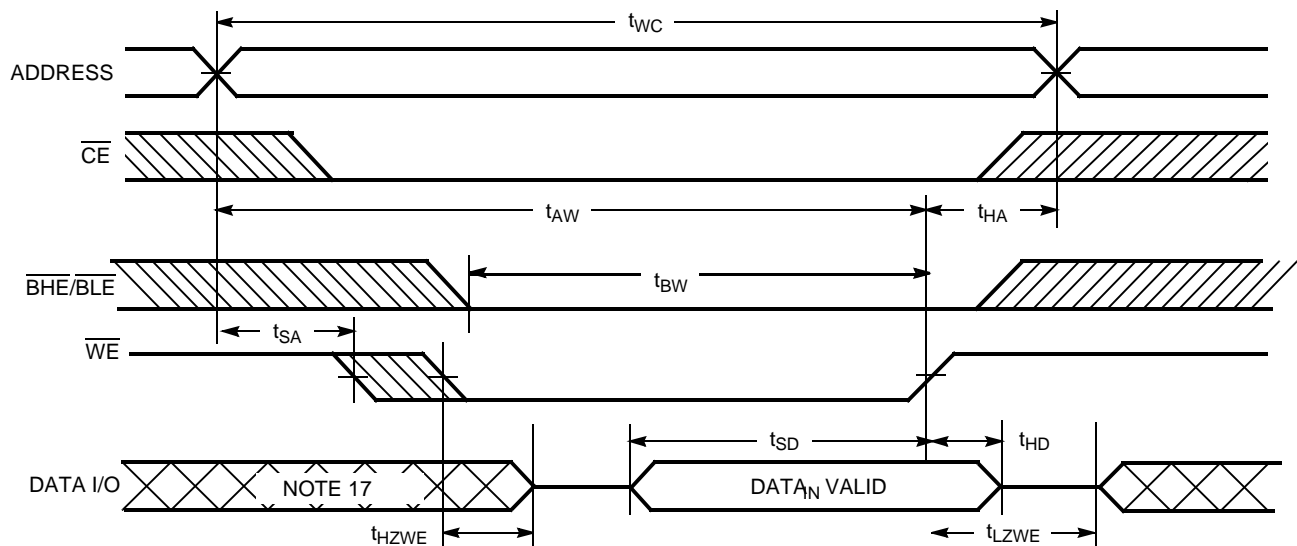
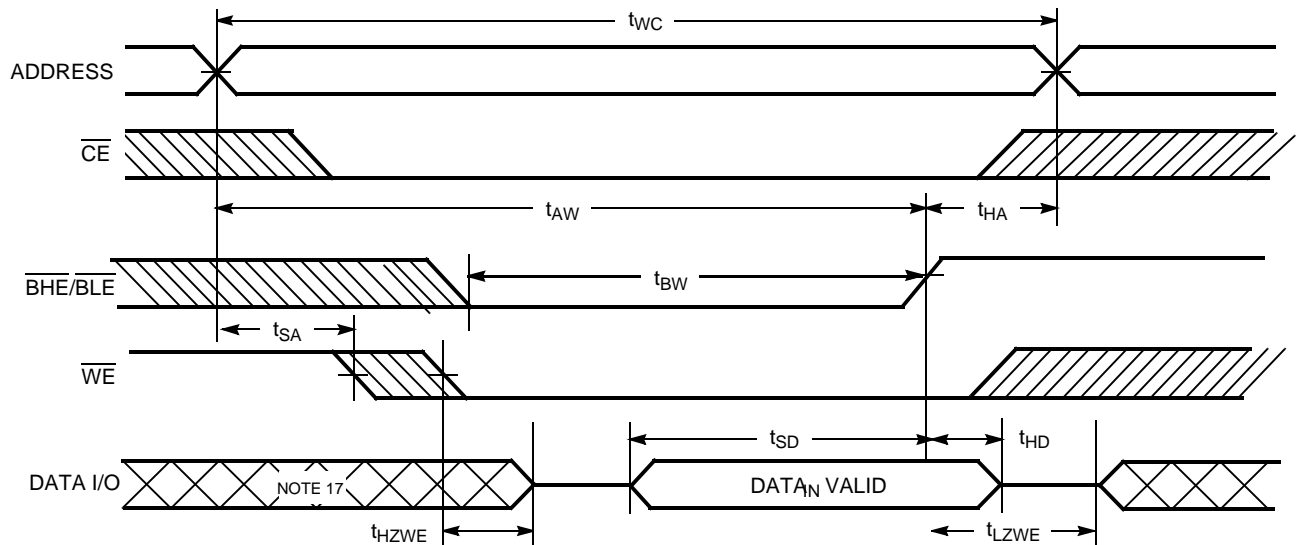


### Write Cycle No. 2 ( $\overline{\text{CE}}$ Controlled)<sup>[10, 15, 16]</sup>



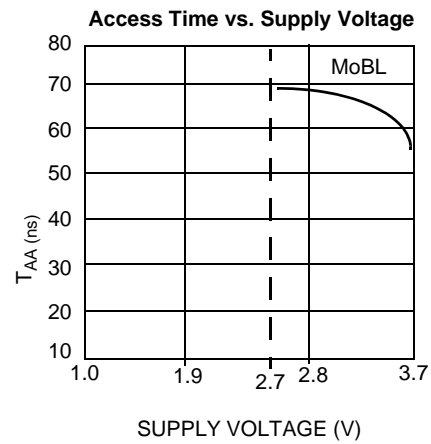
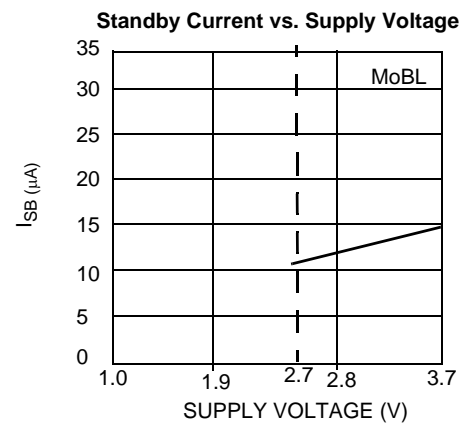
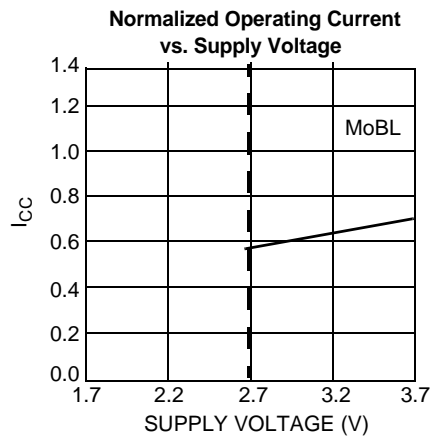
#### Notes:

15. Data I/O is high-impedance if  $\overline{\text{OE}} = V_{IH}$ .
16. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[11, 16]</sup>**

**Write Cycle No. 4 ( $\overline{\text{BHE/BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[17]</sup>**




## Typical DC and AC Characteristics



## Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	I/O <sub>8</sub> –I/O <sub>15</sub>	I/O <sub>0</sub> –I/O <sub>7</sub>	Mode	Power
H	X	X	X	X	High-Z	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X	X	X	H	H	High-Z	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out	Data Out	Read	Active ( $I_{CC}$ )
L	H	L	H	L	High-Z	Data Out	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out	High-Z	Read	Active ( $I_{CC}$ )
L	H	H	X	X	High-Z	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In	Data In	Write	Active ( $I_{CC}$ )
L	L	X	H	L	High-Z	Data In	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In	High-Z	Write	Active ( $I_{CC}$ )

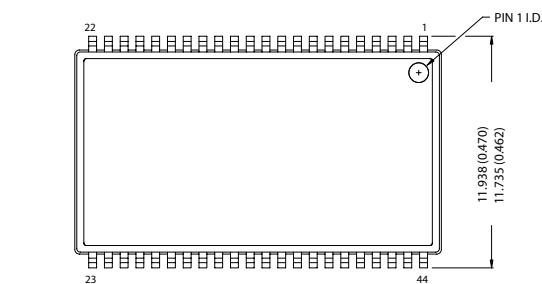
## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62137VNLL-55ZXI	51-85087	44-pin TSOP II (Pb-free)	Industrial
70	CY62137VNLL-70ZXI		44-pin TSOP II (Pb-free)	Industrial
	CY62137VNLL-70ZSXA		44-pin TSOP II (Pb-free)	Automotive-A
	CY62137VNLL-70ZSXE		44-pin TSOP II (Pb-free)	Automotive-E

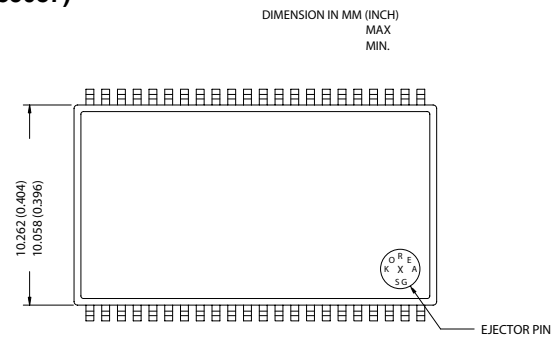
Please contact your local Cypress sales representative for availability of these parts

## Package Diagram

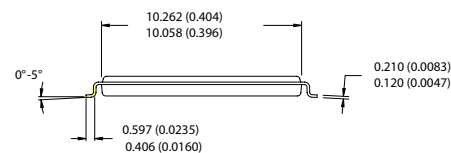
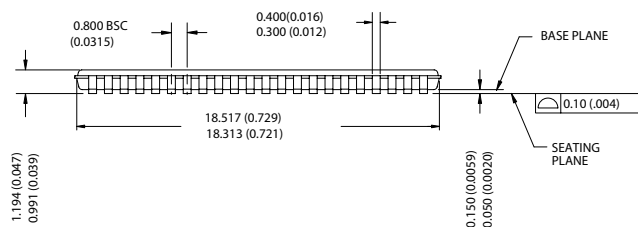
### 44-Pin TSOP II (51-85087)



TOP VIEW



BOTTOM VIEW



51-85087-\*A

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## Document History Page

Document Title: CY62137VN MoBL <sup>®</sup> 2-Mbit (128K x 16) Static RAM Document Number: 001-06497				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	426503	See ECN	NXR	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Updated Ordering Information table

# Mouser Electronics

Authorized Distributor

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