



## CY62146G MoBL<sup>®</sup> Automotive

# 4-Mbit (256K words × 16 bit) Static RAM with Error-Correcting Code (ECC)

## Features

- High speed: 45 ns
- Temperature Range
  - Automotive-A: -40 °C to +85 °C
- Ultra-low standby power
  - Typical standby current: 3.5  $\mu$ A
- Embedded ECC for single-bit error correction<sup>[1]</sup>
- Voltage range: 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 44-pin TSOP II package

## Functional Description

CY62146G is high-performance CMOS low-power (MoBL) SRAM devices with embedded ECC.

Device is accessed by asserting the chip enable ( $\overline{CE}$ ) input LOW.

Data writes are performed by asserting the Write Enable ( $\overline{WE}$ ) input LOW, while providing the data on I/O<sub>0</sub> through I/O<sub>15</sub> and address on A<sub>0</sub> through A<sub>17</sub> pins. The Byte High Enable (BHE) and Byte Low Enable (BLE) inputs control write operations to the upper and lower bytes of the specified memory location. BHE controls I/O<sub>8</sub> through I/O<sub>15</sub> and BLE controls I/O<sub>0</sub> through I/O<sub>7</sub>.

Data reads are performed by asserting the Output Enable ( $\overline{OE}$ ) input and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O<sub>0</sub> through I/O<sub>15</sub>). Byte accesses can be performed by asserting the required byte enable signal (BHE or BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a HI-Z state when the device is deselected ( $\overline{CE}$  HIGH), or control signals are de-asserted ( $\overline{OE}$ , BLE, BHE).

The logic block diagram is on page 2.

## Product Portfolio

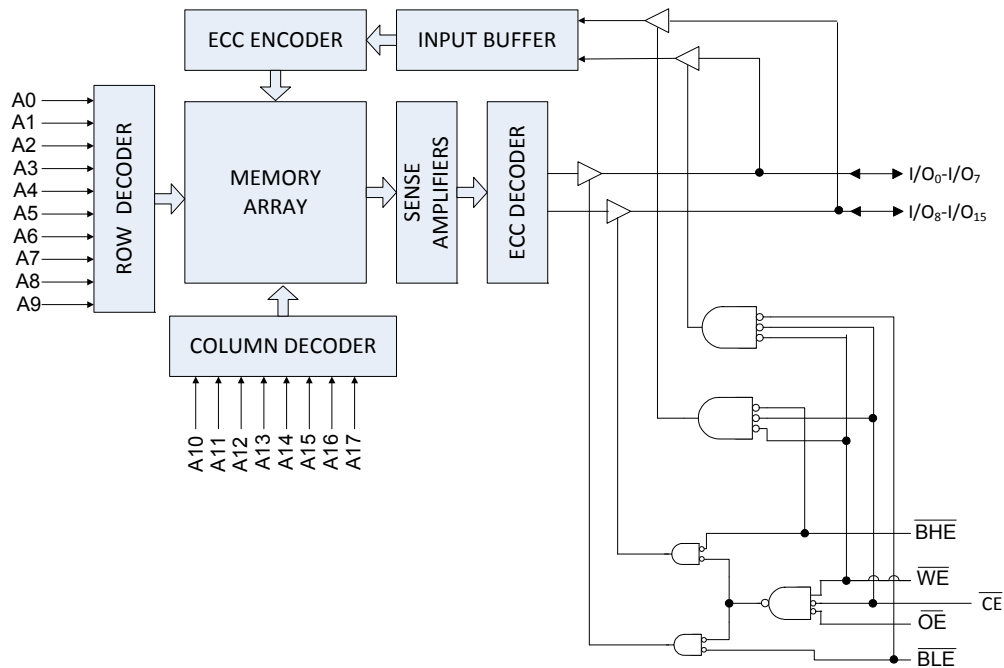
Product	Features and Options (see <a href="#">Pin Configuration – CY62146G</a> on page 4)	Range	V <sub>CC</sub> Range (V)	Speed (ns)	Power Dissipation			
					Operating I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> ( $\mu$ A)	
					f = f <sub>max</sub>			
					Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max
CY62146G30	Single Chip Enable	Automotive-A	2.2 V–3.6 V	45	15	20	3.5	8.7
CY62146G			4.5 V–5.5 V					

### Notes

1. This device does not support automatic write-back on error detection.

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 3 V (for V<sub>CC</sub> range of 2.2 V–3.6 V) and V<sub>CC</sub> = 5 V (for V<sub>CC</sub> range of 4.5 V–5.5 V), T<sub>A</sub> = 25 °C.

## Logic Block Diagram – CY62146G

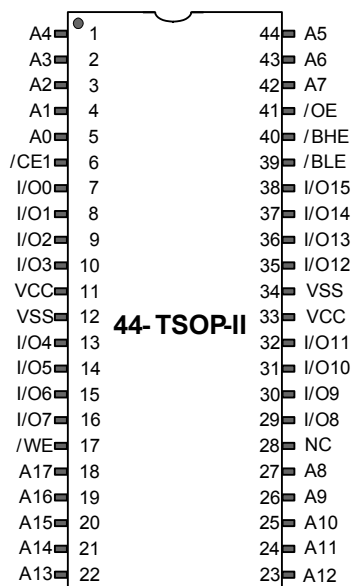


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## Pin Configuration – CY62146G

Figure 1. 44-pin TSOP II pinout – CY62146G <sup>[3]</sup>



### Note

3. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to + 150 °C

Ambient temperature  
with power applied ..... -55 °C to + 125 °C

Supply voltage  
to ground potential<sup>[4]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V

DC voltage applied to outputs  
in HI-Z state<sup>[4]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V

DC input voltage<sup>[4]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V

Output current into outputs (in low state) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >140 mA

## Operating Range

Grade	Ambient Temperature	$V_{CC}$
Automotive-A	-40 °C to +85 °C	2.2 V to 3.6 V
		4.5 V to 5.5 V

## DC Electrical Characteristics

Over the operating range

Parameter	Description		Test Conditions	45 ns (Automotive-A)			Unit
				Min	Typ	Max	
$V_{OH}$	Output HIGH voltage	2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	2	—	—	V
		2.7 V to 3.6 V	$V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2.2	—	—	
		4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2.4	—	—	
		4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	$V_{CC} - 0.5^{[5]}$	—	—	
$V_{OL}$	Output LOW voltage	2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$	—	—	0.4	V
		2.7 V to 3.6 V	$V_{CC} = \text{Min}, I_{OL} = 2.1 \text{ mA}$	—	—	0.4	
		4.5 V to 5.5 V	$V_{CC} = \text{Min}, I_{OL} = 2.1 \text{ mA}$	—	—	0.4	
$V_{IH}$	Input HIGH voltage	2.2 V to 2.7 V	—	2	—	$V_{CC} + 0.3^{[4]}$	V
		2.7 V to 3.6 V	—	2	—	$V_{CC} + 0.3^{[4]}$	
		4.5 V to 5.5 V	—	2.2	—	$V_{CC} + 0.5^{[4]}$	
$V_{IL}$	Input LOW voltage	2.2 V to 2.7 V	—	-0.3 <sup>[4]</sup>	—	0.6	V
		2.7 V to 3.6 V	—	-0.3 <sup>[4]</sup>	—	0.8	
		4.5 V to 5.5 V	—	-0.5 <sup>[4]</sup>	—	0.8	
$I_{IX}$	Input leakage current		$GND \leq V_{IN} \leq V_{CC}$	-1	—	+1	$\mu\text{A}$
$I_{OZ}$	Output leakage current		$GND \leq V_{OUT} \leq V_{CC}$ , Output disabled	-1	—	+1	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ operating supply current		Max $V_{CC}$ , $I_{OUT} = 0 \text{ mA}$ , CMOS levels	$f = f_{MAX}$	—	15	mA
				$f = 1 \text{ MHz}$	—	3.5	

### Note

4.  $V_{IL(\text{min})} = -2.0 \text{ V}$  and  $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$  for pulse durations of less than 2 ns.

5. This parameter is guaranteed by design and not tested.

**DC Electrical Characteristics** (continued)

Over the operating range

Parameter	Description	Test Conditions	45 ns (Automotive-A)			Unit
			Min	Typ	Max	
$I_{SB1}^{[6]}$	Automatic power down current – CMOS inputs; $V_{CC} = 2.2\text{ V to }3.6\text{ V and }4.5\text{ V to }5.5\text{ V}$	$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V or }CE_2 \leq 0.2\text{ V}$ $V_{IN} \geq V_{CC} - 0.2\text{ V or }V_{IN} \leq 0.2\text{ V},$ $f = f_{max}$ (address and data only), $f = 0$ ( $\overline{OE}$ , $\overline{WE}$ , $\overline{BHE}$ , and $\overline{BLE}$ ), Max $V_{CC}$	–	3.5	8.7	$\mu\text{A}$
$I_{SB2}^{[6]}$	Automatic power down current – CMOS inputs $V_{CC} = 2.2\text{ V to }3.6\text{ V and }4.5\text{ V to }5.5\text{ V}$	$\overline{CE}_1 \geq V_{CC} - 0.2\text{ V or }CE_2 \leq 0.2\text{ V}$ $V_{IN} \geq V_{CC} - 0.2\text{ V or }V_{IN} \leq 0.2\text{ V},$ $f = 0$ , Max $V_{CC}$	–	3.5	8.7	$\mu\text{A}$

**Notes**

 6. Chip enable ( $\overline{CE}$ ) must be tied to CMOS levels to meet the  $I_{SB1}/I_{SB2}/I_{CCDR}$  spec. Other inputs can be left floating.

## Capacitance

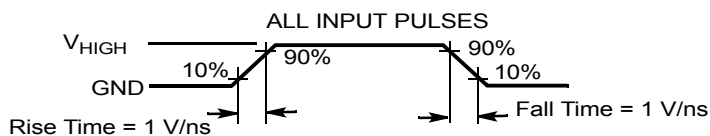
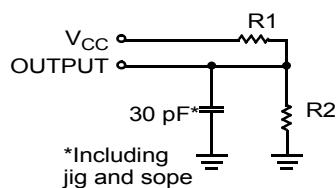
Parameter <sup>[7]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^{\circ}\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(\text{typ})}$	10	pF
$C_{OUT}$	Output capacitance		10	pF

## Thermal Resistance

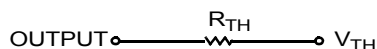
Parameter <sup>[7]</sup>	Description	Test Conditions	44-pin TSOP II	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board	66.82	$^{\circ}\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		15.97	$^{\circ}\text{C/W}$

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms<sup>[8]</sup>



Equivalent to: THÉVENIN EQUIVALENT



Parameters	2.5 V	3.0 V	Unit
$R1$	16667	1103	$\Omega$
$R2$	15385	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.20	1.75	V

### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ .

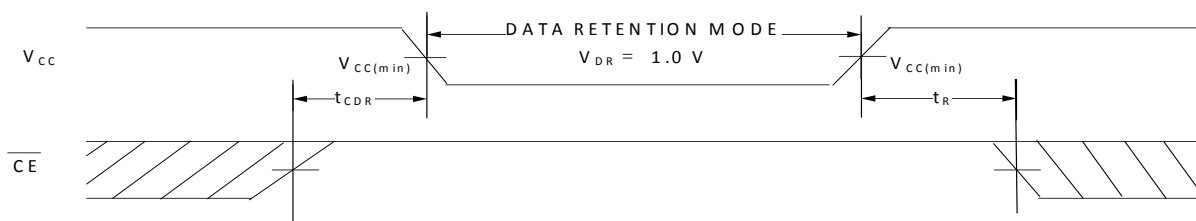
## Data Retention Characteristics

Over the Operating range

Parameter	Description	Conditions (Automotive-A)	Min	Typ <sup>[9]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention	—	1	—	—	V
$I_{CCDR}^{[10, 11]}$	Data retention current	$V_{CC} = 1.2 \text{ V}$ $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	—	—	13	$\mu\text{A}$
$t_{CDR}^{[12]}$	Chip deselect to data retention time	—	0	—	—	ns
$t_R^{[12, 13]}$	Operation recovery time	—	45	—	—	ns

## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 3 \text{ V}$  (for  $V_{CC}$  range of 2.2 V–3.6 V) and  $V_{CC} = 5 \text{ V}$  (for  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A = 25^\circ\text{C}$ .
10. Chip enable ( $\overline{CE}$ ) must be tied to CMOS levels to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
11.  $I_{CCDR}$  is guaranteed only after device is first powered up to  $V_{CC(min)}$  and then brought down to  $V_{DR}$ .
12. These parameters are guaranteed by design.
13. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100 \mu\text{s}$  or stable at  $V_{CC(min)} \geq 100 \mu\text{s}$ .



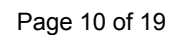
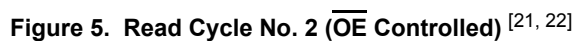
## AC Switching Characteristics

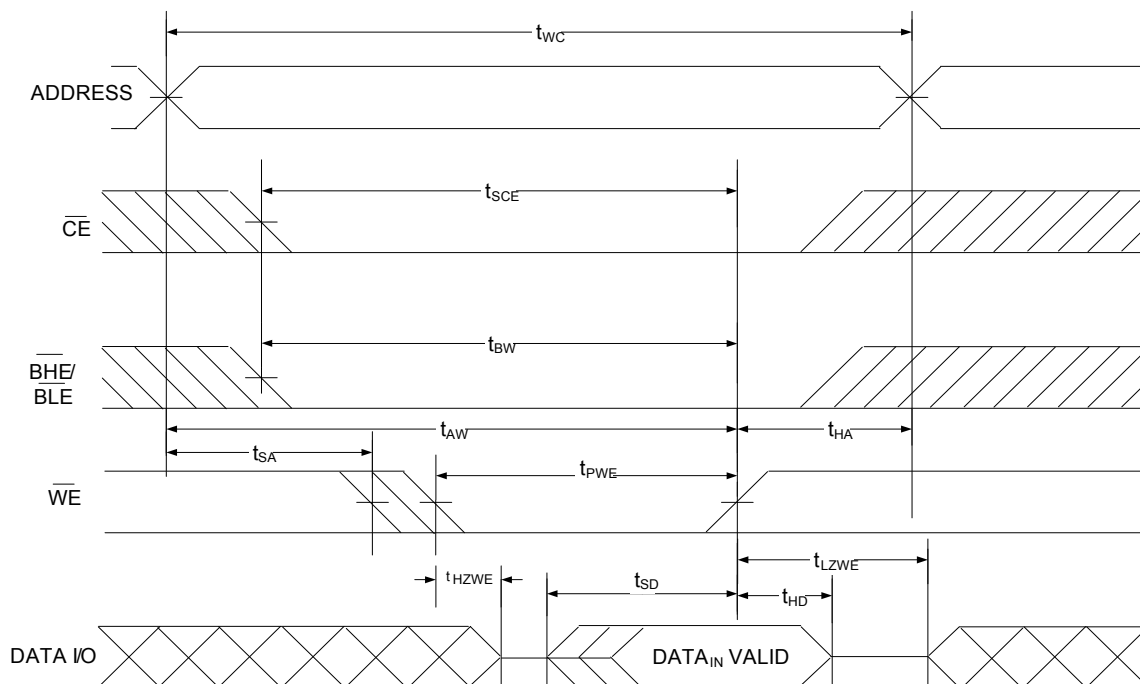
Parameter <sup>[14]</sup>	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t <sub>RC</sub>	Read cycle time	45	–	ns
t <sub>AA</sub>	Address to data valid	–	45	ns
t <sub>OHA</sub>	Data hold from address change	10	–	ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to data valid	–	45	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to data valid	–	22	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low impedance <sup>[15, 16]</sup>	5	–	ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to HI-Z <sup>[15, 16, 17]</sup>	–	18	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low impedance <sup>[15, 16]</sup>	10	–	ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to HI-Z <sup>[15, 16, 17]</sup>	–	18	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to power-up <sup>[16]</sup>	0	–	ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH and CE <sub>2</sub> LOW to power-down <sup>[16]</sup>	–	45	ns
t <sub>DBE</sub>	$\overline{BLE}$ / $\overline{BHE}$ LOW to data valid	–	22	ns
t <sub>LZBE</sub>	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low impedance <sup>[15, 16]</sup>	5	–	ns
t <sub>HZBE</sub>	$\overline{BLE}$ / $\overline{BHE}$ HIGH to HI-Z <sup>[15, 16, 17]</sup>	–	18	ns
Write Cycle <sup>[18, 19]</sup>				
t <sub>WC</sub>	Write cycle time	45	–	ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to write end	35	–	ns
t <sub>AW</sub>	Address setup to write end	35	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	35	–	ns
t <sub>BW</sub>	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	ns
t <sub>SD</sub>	Data setup to write end	25	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to HI-Z <sup>[15, 16, 17]</sup>	–	18	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low impedance <sup>[15, 16]</sup>	10	–	ns

### Notes

14. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{CC} \geq 3$  V) and  $V_{CC}/2$  (for  $V_{CC} < 3$  V), and input pulse levels of 0 to 3 V (for  $V_{CC} \geq 3$  V) and 0 to  $V_{CC}$  (for  $V_{CC} < 3$  V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
15. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.
16. These parameters are guaranteed by design.
17.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
18. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
19. The minimum pulse width in Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .

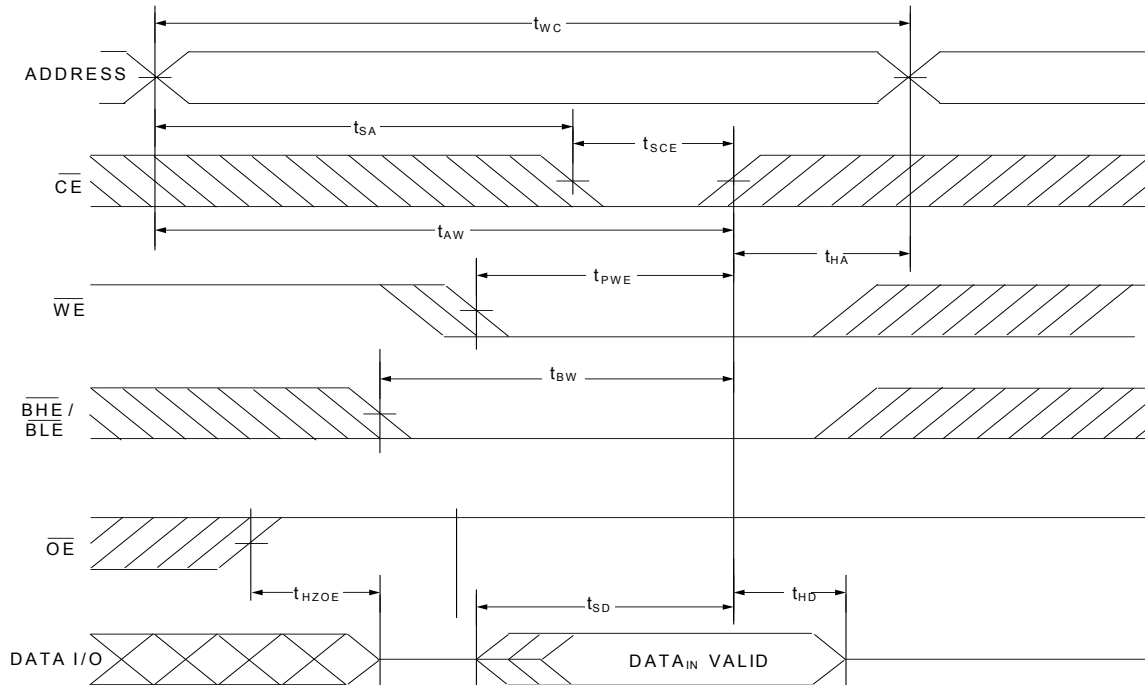
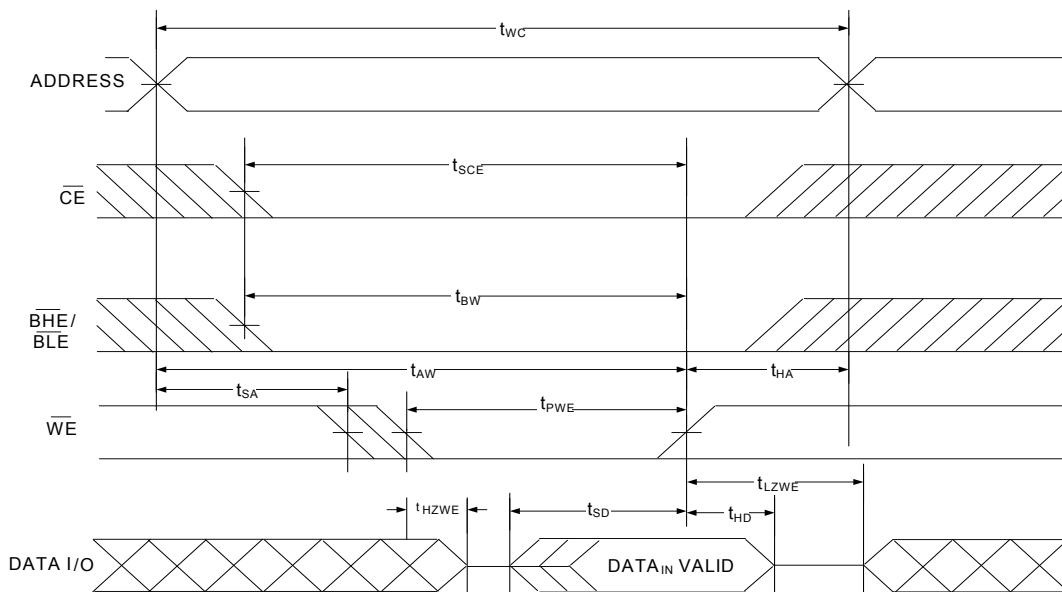
**Figure 4. Read Cycle No. 1 of CY62146G (Address Transition Controlled) [20]**



**Switching Waveforms (continued)**
**Figure 6. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled) [23, 24]**

**Notes**

23. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

24. Data I/O is in a HI-Z state if  $\overline{\text{CE}} = V_{\text{IH}}$ , or  $\overline{\text{OE}} = V_{\text{IH}}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .

**Switching Waveforms (continued)**
**Figure 7. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled) [25, 26]**

**Figure 8. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [25, 26, 27]**

**Notes**

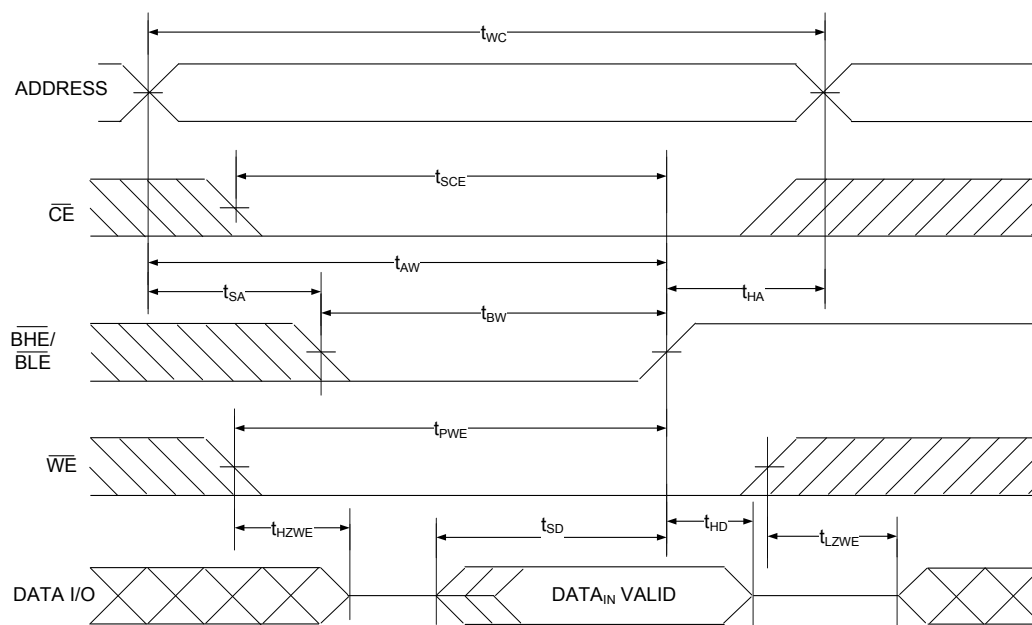
25. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}}_1 = V_{IL}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{IL}$ , and  $\text{CE}_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

26. Data I/O is in Hi-Z state if  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{OE}} = V_{IH}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

27. The minimum write pulse width for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) should be sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms (continued)

**Figure 9. Write Cycle No. 4 ( $\overline{\text{BHE}}/\overline{\text{BLE}}$  Controlled)** [28, 29]



### Notes

28. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{IL}$ ,  $\overline{\text{CE}}_1 = V_{IL}$ ,  $\overline{\text{BHE}}$  or  $\overline{\text{BLE}}$  or both =  $V_{IL}$ , and  $\text{CE}_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

29. Data I/O is in a HI-Z state if  $\overline{\text{CE}} = V_{IH}$ , or  $\overline{\text{OE}} = V_{IH}$  or  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{IH}$ .

**Truth Table – CY62146G**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	HI-Z	Deselect/Power-down	Standby ( $I_{\text{SB}}$ )
$X^{[30]}$	X	X	H	H	HI-Z	Output disabled	Active ( $I_{\text{CC}}$ )
L	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{\text{CC}}$ )
L	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); HI-Z ( $I/O_8$ – $I/O_{15}$ )	Read	Active ( $I_{\text{CC}}$ )
L	H	L	L	H	HI-Z ( $I/O_0$ – $I/O_7$ ); Data Out ( $I/O_8$ – $I/O_{15}$ )	Read	Active ( $I_{\text{CC}}$ )
L	H	H	X	X	HI-Z	Output disabled	Active ( $I_{\text{CC}}$ )
L	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{\text{CC}}$ )
L	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); HI-Z ( $I/O_8$ – $I/O_{15}$ )	Write	Active ( $I_{\text{CC}}$ )
L	L	X	L	H	HI-Z ( $I/O_0$ – $I/O_7$ ); Data In ( $I/O_8$ – $I/O_{15}$ )	Write	Active ( $I_{\text{CC}}$ )

**Notes**

30. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

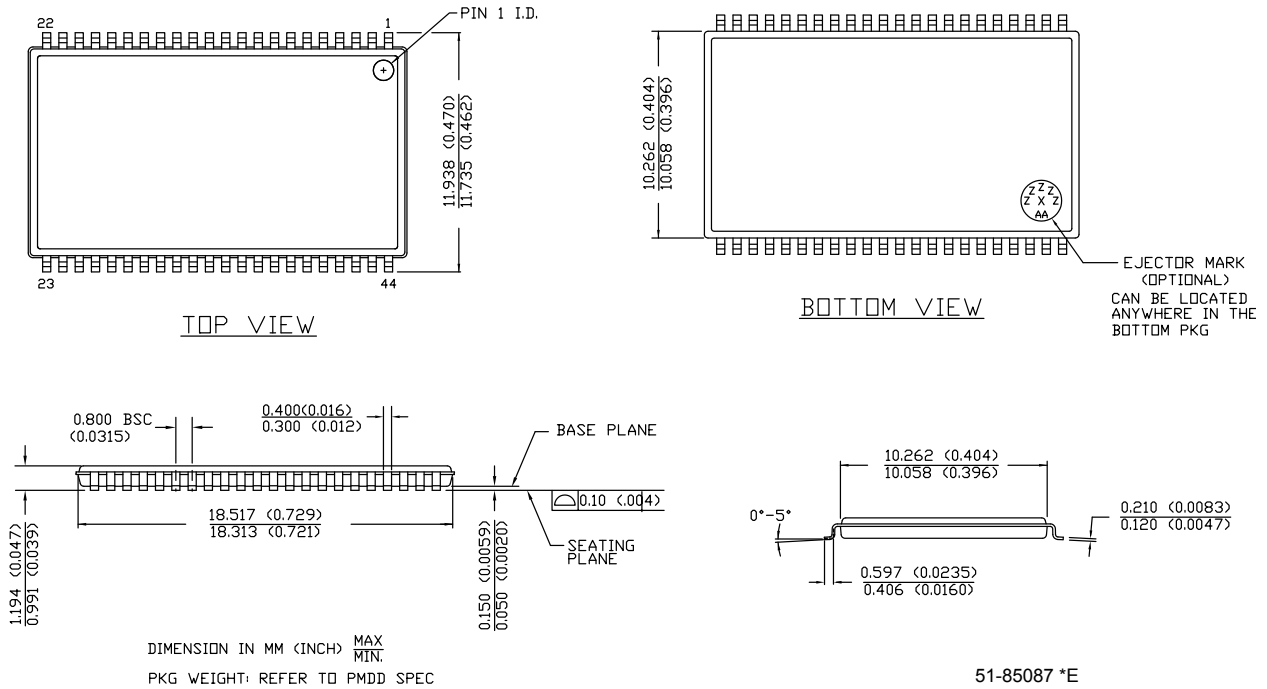
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62146G30-45ZSXA	51-85087	44-pin TSOP II	Automotive-A
	4.5 V–5.5 V	CY62146G-45ZSXA	51-85087	44-pin TSOP II	Automotive-A

## Ordering Code Definitions

CY	621	4	6	X	G	X	-	45	ZS	X	A	
												Temperature Grade: A = Automotive-A
												Pb-free
												Package Type: ZS = 44-pin TSOP II
												Speed Grade: 45 = 45 ns
												Voltage Range: X = 30 or blank 30 = 3 V typ; blank = 5 V typ
												Process Technology: G = 65 nm
												Chip Enable: X = blank or 2 blank = Single Chip Enable; 2 = Dual Chip Enable
												Bus Width: 6 = × 16
												Density: 4 = 4-Mbit
												Family Code: 621 = MoBL SRAM family
												Company ID: CY = Cypress

## Package Diagrams

**Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087**





## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

**Document History Page**

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