

# 16-Mbit (2M x 8) MoBL<sup>®</sup> Static RAM

## Features

- **Very high speed**
  - 55 ns
- **Wide voltage range**
  - 2.2V – 3.6V
- **Ultra-low active power**
  - Typical active current: 2 mA @ f = 1 MHz
  - Typical active current: 15 mA @ f = f<sub>Max</sub> (55 ns Speed)
- **Ultra-low standby power**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $\overline{CE}_2$  and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free and non Pb-free 48-ball VFBGA package**

## Functional Description<sup>[1]</sup>

The CY62168DV30 is a high-performance CMOS static RAMs organized as 2048Kbit words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly

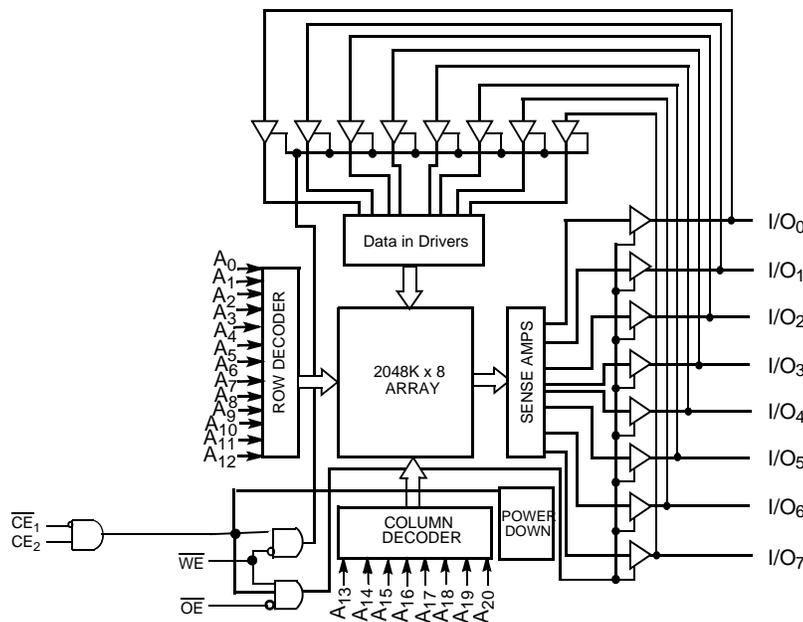
reduces power consumption. The device can be put into standby mode reducing power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected Chip Enable 1 ( $\overline{CE}_1$ ) HIGH or Chip Enable 2 ( $\overline{CE}_2$ ) LOW. The input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when: deselected Chip Enable 1 ( $\overline{CE}_1$ ) HIGH or Chip Enable 2 ( $\overline{CE}_2$ ) LOW, outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation (Chip Enable 1 ( $\overline{CE}_1$ ) LOW and Chip Enable 2 ( $\overline{CE}_2$ ) HIGH and WE LOW).

Writing to the device is accomplished by taking Chip Enable 1 ( $\overline{CE}_1$ ) LOW and Chip Enable 2 ( $\overline{CE}_2$ ) HIGH and Write Enable (WE) input LOW. Data on the eight I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>20</sub>).

Reading from the device is accomplished by taking Chip Enable 1 ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW and Chip Enable 2 ( $\overline{CE}_2$ ) HIGH while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

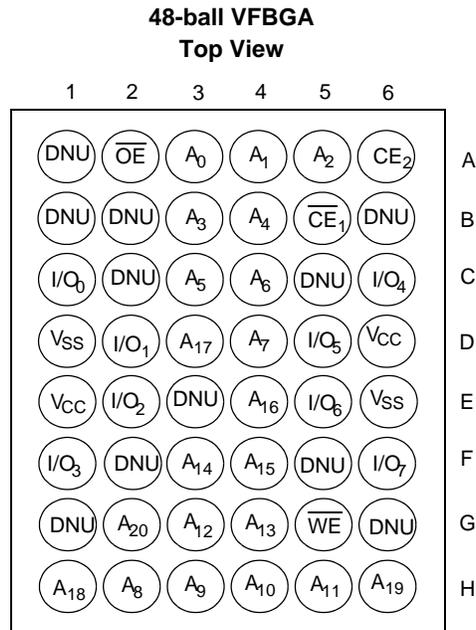
The eight input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH and WE LOW). See the truth table for a complete description of read and write modes.

## Logic Block Diagram



**Note:**

1. For best-practice recommendations, please refer to the Cypress application note entitled *System Design Guidelines*, available at <http://www.cypress.com>.

**Pin Configuration<sup>[2]</sup>**

**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> ( $\mu$ A)	
	f = 1 MHz		f = f <sub>Max</sub>							
	Min.	Typ. <sup>[3]</sup>	Max.				Typ. <sup>[3]</sup>	Max.	Typ. <sup>[3]</sup>	Max.
CY62168DV30LL	2.2	3.0	3.6	55	2	4	15	30	2.5	22

**Notes:**

2. DNU pins have to be left floating or tied to V<sub>SS</sub> to ensure proper operation.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.3V to  $V_{CC(max)}$  + 0.3V  
 DC Voltage Applied to Outputs in High-Z State<sup>[4, 5]</sup> ..... -0.3V to  $V_{CC(max)}$  + 0.3V

DC Input Voltage<sup>[4, 5]</sup> ..... -0.3V to  $V_{CC(max)}$  + 0.3V  
 Output Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)  
 Latch-up Current..... > 200 mA

**Operating Range**

Range	Ambient Temperature ( $T_A$ ) <sup>[6]</sup>	$V_{CC}$ <sup>[7]</sup>
Industrial	-40°C to +85°C	2.2V – 3.6V

**DC Electrical Characteristics (Over the Operating Range)**

Parameter	Description	Test Conditions	CY62168DV30-55			Unit	
			Min.	Typ. <sup>[3]</sup>	Max.		
$V_{OH}$	Output HIGH Voltage	$2.2V \leq V_{CC} \leq 2.7V$	$I_{OH} = -0.1 \text{ mA}$	2.0		V	
		$2.7V \leq V_{CC} \leq 3.6V$	$I_{OH} = -1.0 \text{ mA}$	2.4			
$V_{OL}$	Output LOW Voltage	$2.2V \leq V_{CC} \leq 2.7V$	$I_{OL} = 0.1 \text{ mA}$		0.4	V	
		$2.7V \leq V_{CC} \leq 3.6V$	$I_{OL} = 2.1 \text{ mA}$		0.4		
$V_{IH}$	Input HIGH Voltage	$2.2V \leq V_{CC} \leq 2.7V$		1.8	$V_{CC} + 0.3$	V	
		$2.7V \leq V_{CC} \leq 3.6V$		2.2	$V_{CC} + 0.3$		
$V_{IL}$	Input LOW Voltage	$2.2V \leq V_{CC} \leq 2.7V$		-0.3	0.6	V	
		$2.7V \leq V_{CC} \leq 3.6V$		-0.3	0.8		
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		-1	+1	$\mu\text{A}$	
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output disabled		-1	+1	$\mu\text{A}$	
$I_{CC}$	$V_{CC}$ Operating Supply Current	$f = f_{Max} = 1/t_{RC}$	$V_{CC} = 3.6V$ , $I_{OUT} = 0 \text{ mA}$ , CMOS level		15	30	mA
		$f = 1 \text{ MHz}$			2	4	
$I_{SB1}$	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ , $CE_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ , $V_{IN} \leq 0.2V$ , $f = f_{Max}$ (Address and Data Only), $f = 0$ ( $\overline{OE}$ , $\overline{WE}$ )			2.5	22	$\mu\text{A}$
$I_{SB2}$	Automatic CE Power-down Current— CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ , $CE_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0$ , $V_{CC} = 3.6V$			2.5	22	$\mu\text{A}$

**Capacitance<sup>[8]</sup>**

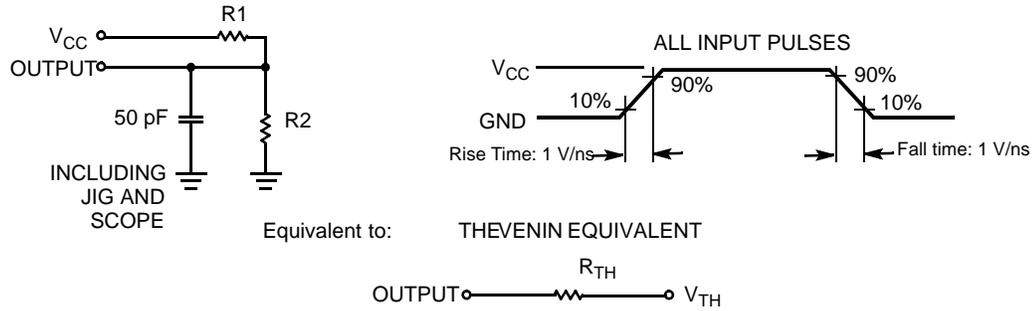
Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{CC} = V_{CC(typ.)}$	8	pF
$C_{OUT}$	Output Capacitance		10	pF

**Notes:**

- $V_{IL(min)}$  = -2.0V for pulse durations less than 20 ns.
- $V_{IH(max)}$  =  $V_{CC} + 0.75V$  for pulse durations less than 20 ns.
- $T_A$  is the "Instant-On" case temperature.
- Full device AC operation assumes a 100  $\mu\text{s}$  ramp time from 0 to  $V_{CC(min)}$  and 100  $\mu\text{s}$  wait time after  $V_{CC}$  stabilization.
- Tested initially and after any design or process changes that may affect these parameters.

**Thermal Resistance<sup>[8]</sup>**

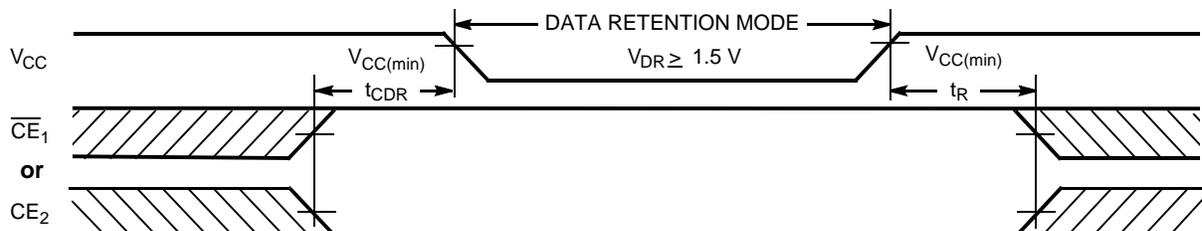
Parameter	Description	Test Conditions	VFBGA	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, 2-layer printed circuit board	55	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		16	°C/W

**AC Test Loads and Waveforms**


Parameters	2.5V	3.0V	Unit
R1	16600	1103	$\Omega$
R2	15400	1554	$\Omega$
$R_{TH}$	8000	645	$\Omega$
$V_{TH}$	1.2	1.75	V

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min.	Typ. <sup>[3]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.5		3.6	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.5V$ $\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			10	$\mu A$
$t_{CDR}^{[8]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[9]}$	Operation Recovery Time		$t_{RC}$			ns

**Data Retention Waveform**

**Note:**

9. Full Device AC operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 100 \mu s$  or stable at  $V_{CC(min.)} \geq 100 \mu s$ .

**Switching Characteristics** Over the Operating Range <sup>[10]</sup>

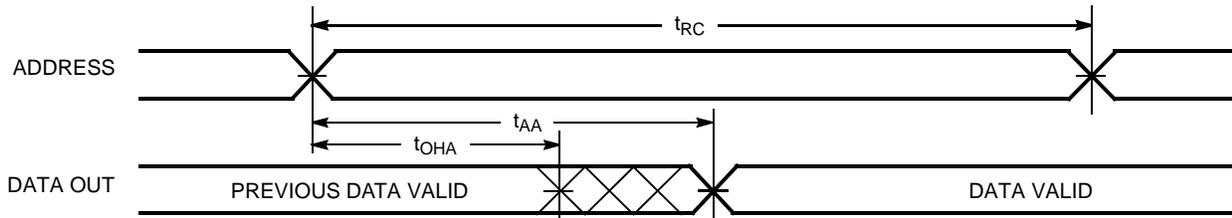
Parameter	Description	55 ns		Unit
		Min.	Max.	
<b>Read Cycle</b>				
$t_{RC}$	Read Cycle Time	55		ns
$t_{AA}$	Address to Data Valid		55	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid		55	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[11]</sup>	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[11, 12]</sup>		20	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z <sup>[11]</sup>	10		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to High Z <sup>[11, 12]</sup>		20	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Power-Up	0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to Power-Down		55	ns
<b>Write Cycle<sup>[13]</sup></b>				
$t_{WC}$	Write Cycle Time	55		ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End	40		ns
$t_{AW}$	Address Set-Up to Write End	40		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	40		ns
$t_{SD}$	Data Set-Up to Write End	25		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[11, 12]</sup>		20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[11]</sup>	10		ns

**Notes:**

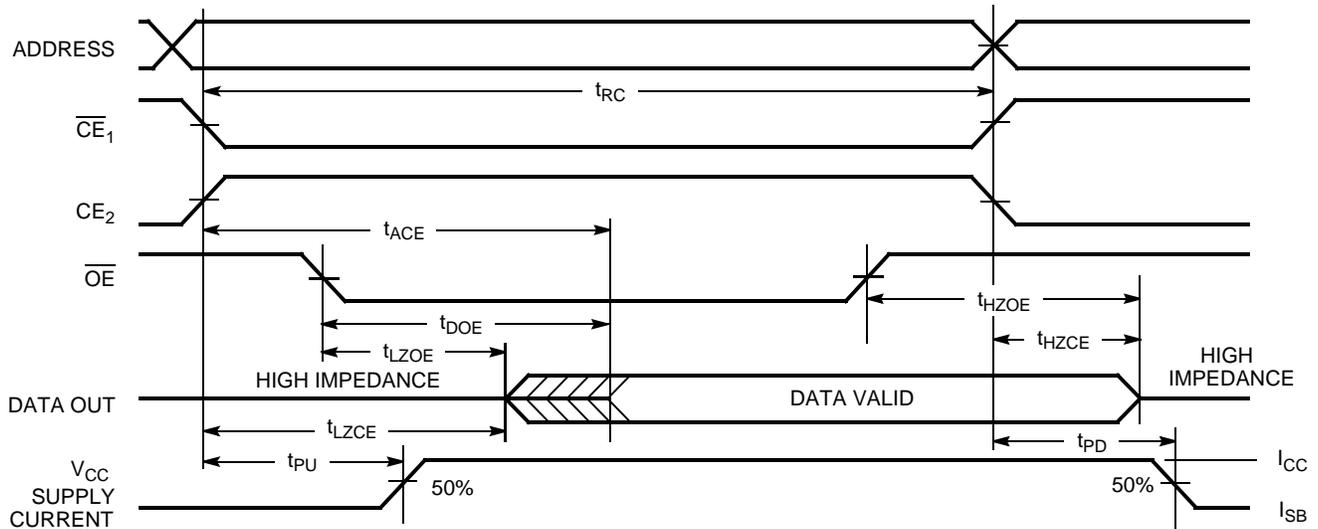
10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3ns or less (1V/ns), timing reference levels of  $V_{CC(typ.)}/2$ , input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.
11. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
12.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
13. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

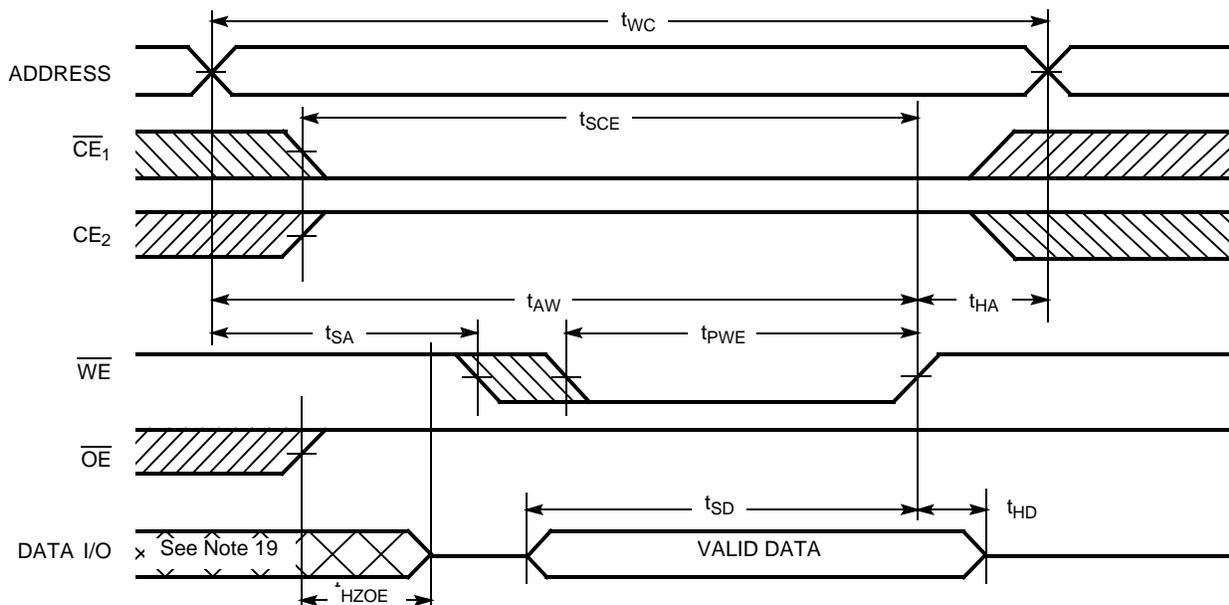
Read Cycle No. 1 (Address Transition Controlled)<sup>[14, 15]</sup>



Read Cycle No. 2 (OE Controlled)<sup>[15, 16]</sup>

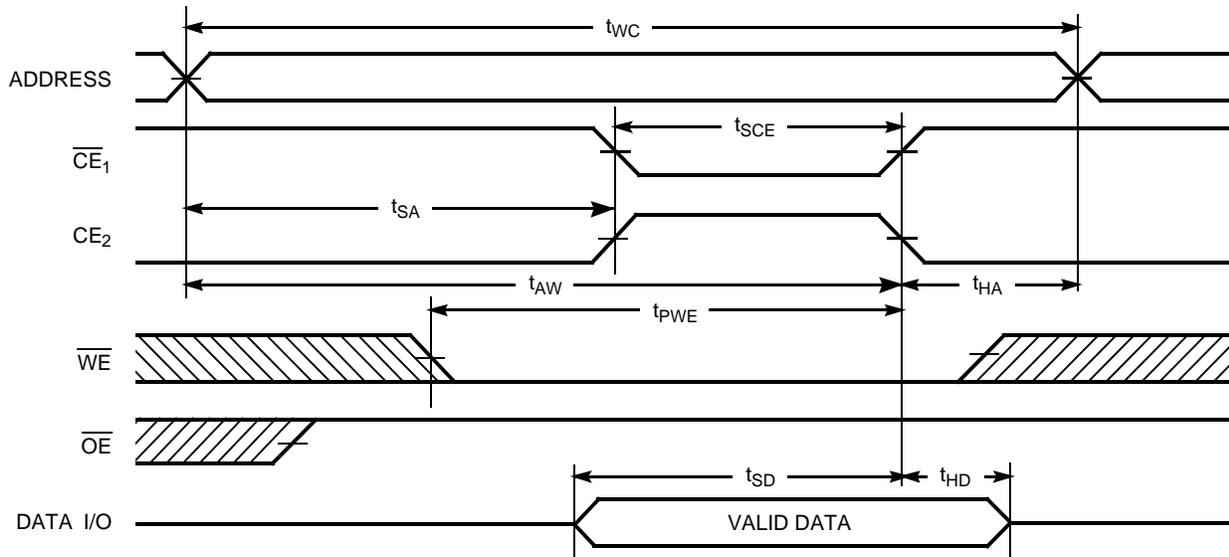
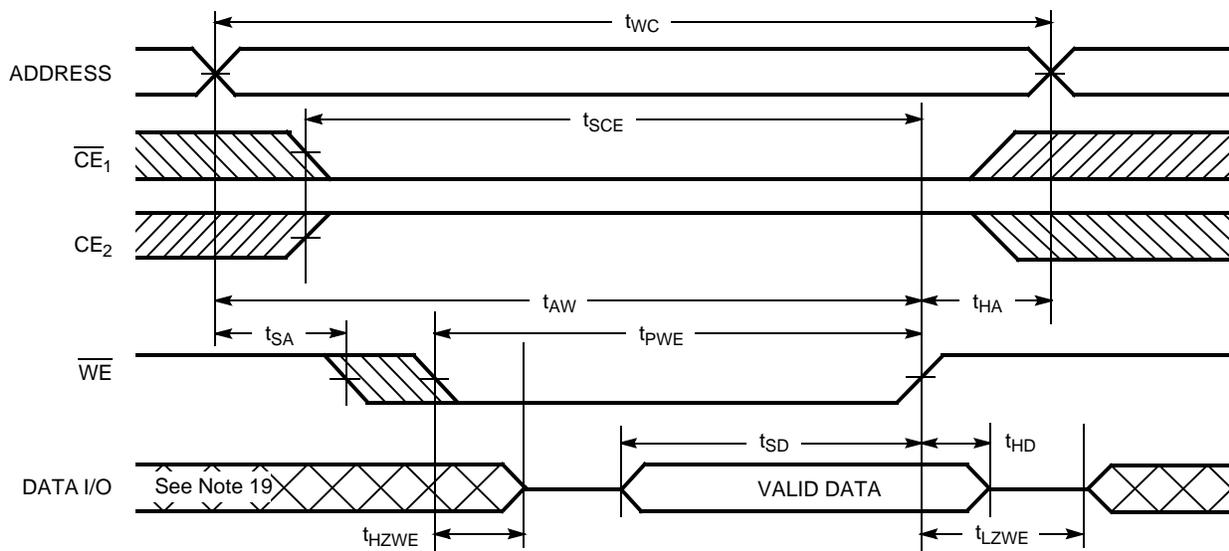


Write Cycle No. 1 (WE Controlled)<sup>[13, 17, 18]</sup>



**Notes:**

- 14. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
- 15.  $\overline{WE}$  is HIGH for read cycle.
- 16. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
- 17. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 18. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  HIGH, the output remains in high-impedance state.
- 19. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled)<sup>[13, 17, 18]</sup>**

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[19]</sup>**

**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
X	L	X	X	High Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	H	L	Data Out (I/O <sub>0</sub> -I/O <sub>7</sub> )	Read	Active ( $I_{CC}$ )
L	H	L	X	Data in (I/O <sub>0</sub> -I/O <sub>7</sub> )	Write	Active ( $I_{CC}$ )
L	H	H	H	High Z	Output Disabled	Active ( $I_{CC}$ )

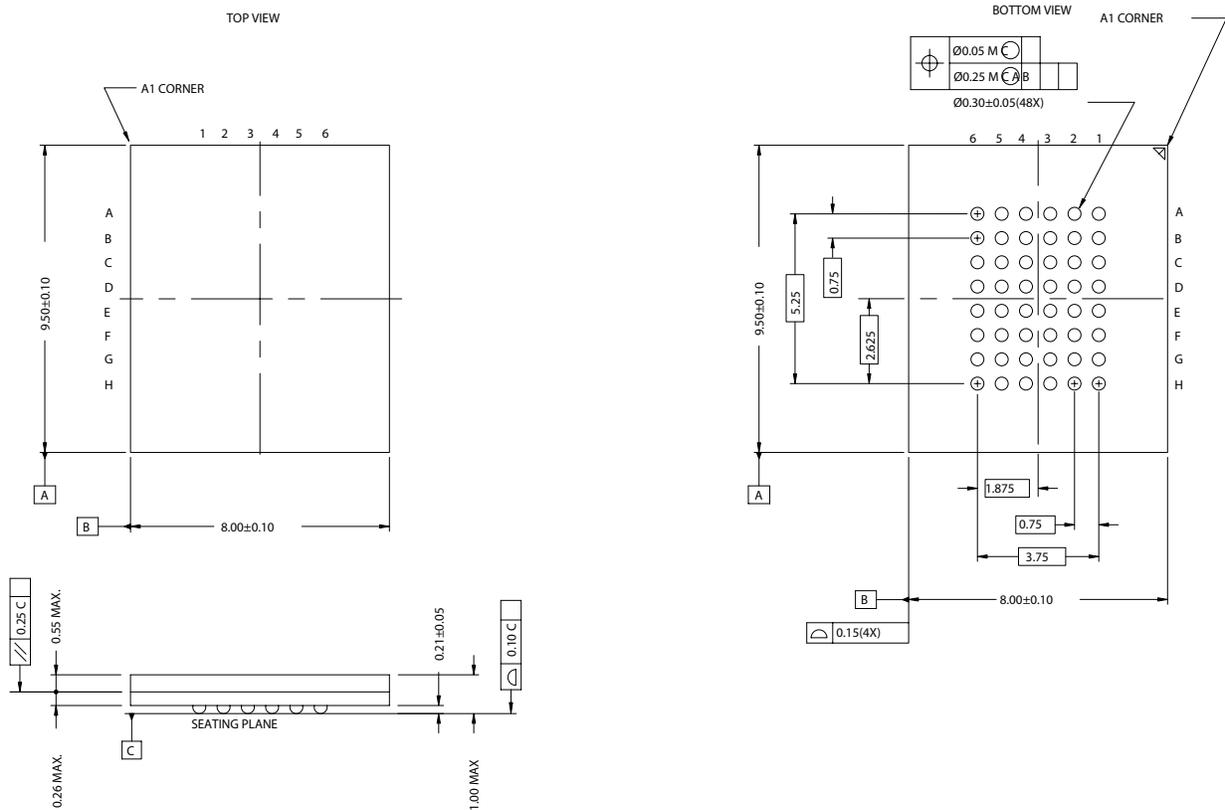
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62168DV30LL-55BVI	51-85178	48-ball Fine Pitch BGA (8 x 9.5 x 1 mm)	Industrial
	CY62168DV30LL-55BVXI		48-ball Fine Pitch BGA (8 x 9.5 x 1 mm) (Pb-free)	

Please contact your local Cypress sales representative for availability of these parts

**Package Diagram**

**48-ball VFBGA (8 x 9.5 x 1 mm) (51-85178)**



51-85178-\*\*

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**Document History Page**

Document Title: CY62168DV30 MoBL <sup>®</sup> , 16-Mbit (2M x 8) MoBL <sup>®</sup> Static RAM				
Document Number: 38-05329				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	118409	09/30/02	GUG	New Data Sheet
*A	123693	02/05/03	DPM	Changed Advance Information to Preliminary Added package diagram
*B	126556	04/24/03	DPM	Minor change: Change sunset owner from DPM to HRT
*C	132869	01/15/04	XRJ	Changed Preliminary to Final
*D	272589	See ECN	PCI	Updated Final data sheet and added Pb-free package.
*E	335864	See ECN	PCI	Removed redundant packages from Ordering Information Table Added Address A <sub>20</sub> to ball G2 in the Pin Configuration
*F	492895	See ECN	VKN	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Removed 70 ns speed bin Removed L power bin from product offering Updated Ordering Information Table