



PERFORM

CY7C1020BN

32K x 16 Static RAM

Features

- High speed
 - $t_{AA} = 12, 15 \text{ ns}$
- CMOS for optimum speed/power
- Low active power
 - 825 mW (max.)
- Low CMOS standby power (L version only)
 - 2.75 mW (max.)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in 44-pin TSOP II and 400-mil SOJ

Functional Description

The CY7C1020BN is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

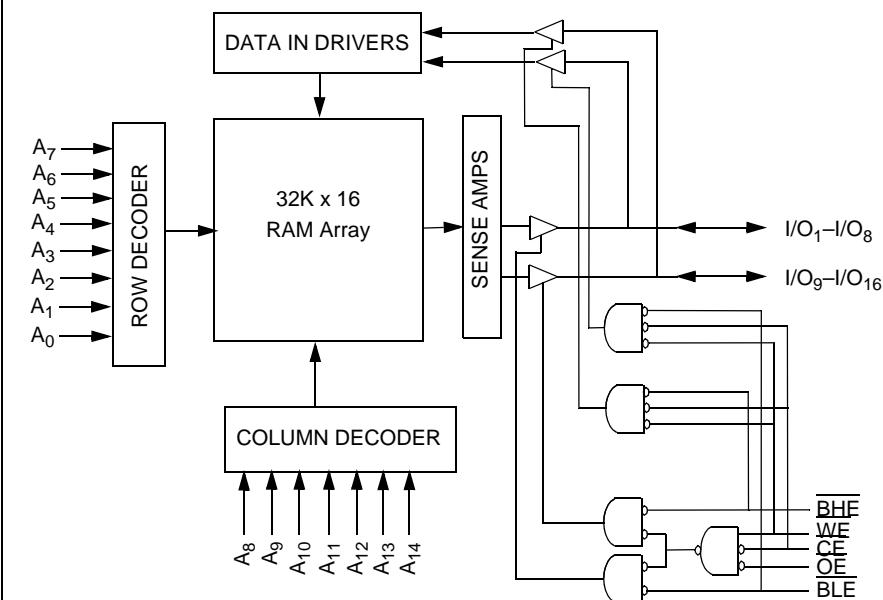
Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₁ through I/O₈) is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₉ through I/O₁₆) is written into the location specified on the address pins (A₀ through A₁₅).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₁ to I/O₈. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₉ to I/O₁₆. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O₁ through I/O₁₆) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1020BN is available in standard 44-pin TSOP Type II and 400-mil-wide SOJ packages.

Logic Block Diagram



Pin Configuration

SOJ / TSOP II

Top View

NC	1	44	A ₅
A ₃	2	43	A ₆
A ₂	3	42	A ₇
A ₁	4	41	OE
A ₀	5	40	BHE
CE	6	39	BLE
I/O ₁	7	38	I/O ₁₆
I/O ₂	8	37	I/O ₁₅
I/O ₃	9	36	I/O ₁₄
I/O ₄	10	35	I/O ₁₃
V _{CC}	11	34	V _{SS}
V _{SS}	12	33	V _{CC}
I/O ₅	13	32	I/O ₁₂
I/O ₆	14	31	I/O ₁₁
I/O ₇	15	30	I/O ₁₀
I/O ₈	16	29	I/O ₉
WE	17	28	NC
A ₁₅	18	27	A ₈
A ₁₄	19	26	A ₉
A ₁₃	20	25	A ₁₀
A ₁₂	21	24	A ₁₁
NC	22	23	NC

Selection Guide

	7C1020BN-12	7C1020BN-15
Maximum Access Time (ns)	12	15
Maximum Operating Current (mA)	140	130
Maximum CMOS Standby Current (mA)	3	3
L	0.5	0.5

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to $+7.0\text{V}$

DC Voltage Applied to Outputs in High Z State^[1] -0.5V to $V_{\text{CC}}+0.5\text{V}$

DC Input Voltage^[1] -0.5V to $V_{\text{CC}}+0.5\text{V}$

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... $>2001\text{V}$
(per MIL-STD-883, Method 3015)

Latch-Up Current $>200\text{ mA}$

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	$0\times\text{C}$ to $+70\times\text{C}$	$5\text{V} \pm 10\%$
Industrial	$-40\times\text{C}$ to $+85\times\text{C}$	$5\text{V} \pm 10\%$

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1020BN-12		7C1020BN-15		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{\text{CC}} = \text{Min.}$, $I_{\text{OH}} = -4.0\text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{\text{CC}} = \text{Min.}$, $I_{\text{OL}} = 8.0\text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	6.0	2.2	6.0	V
V_{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$\text{GND} \leq V_{\text{I}} \leq V_{\text{CC}}$	-1	+1	-1	+1	μA
I_{oz}	Output Leakage Current	$\text{GND} \leq V_{\text{I}} \leq V_{\text{CC}}$, Output Disabled	-1	+1	-1	+1	μA
I_{os}	Output Short Circuit Current ^[3]	$V_{\text{CC}} = \text{Max.}$, $V_{\text{OUT}} = \text{GND}$		-300		-300	mA
I_{cc}	V_{CC} Operating Supply Current	$V_{\text{CC}} = \text{Max.}$, $I_{\text{OUT}} = 0\text{ mA}$, $f = f_{\text{MAX}} = 1/t_{\text{RC}}$		140		130	mA
I_{SB1}	Automatic CE Power-Down Current—TTL Inputs	$\text{Max. } V_{\text{CC}}, \overline{\text{CE}} \geq V_{\text{IH}}$ $V_{\text{IN}} \geq V_{\text{IH}}$ or $V_{\text{IN}} \leq V_{\text{IL}}$, $f = f_{\text{MAX}}$		20		20	mA
I_{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\text{Max. } V_{\text{CC}}, \overline{\text{CE}} \geq V_{\text{CC}} - 0.3\text{V}$, $V_{\text{IN}} \geq V_{\text{CC}} - 0.3\text{V}$, or $V_{\text{IN}} \leq 0.3\text{V}$, $f = 0$	L		3	0.5	mA

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_{\text{A}} = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{\text{CC}} = 5.0\text{V}$	8	pF
C_{OUT}	Output Capacitance		8	pF

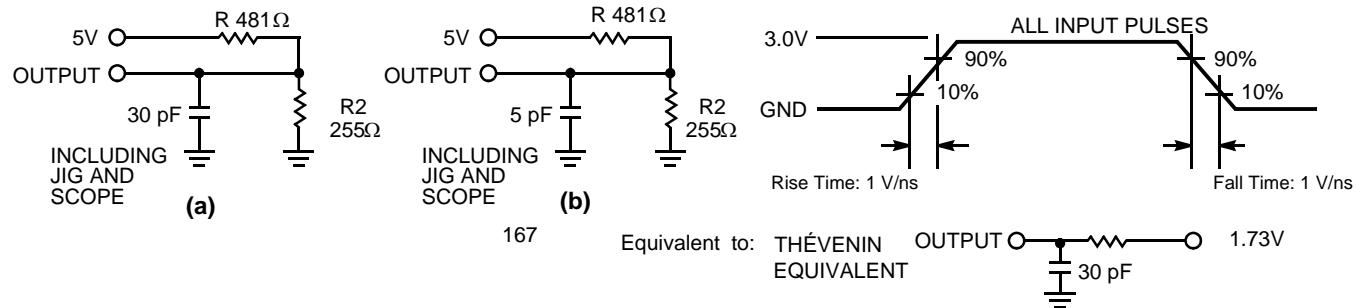
Notes:

1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.

2. T_{A} is the case temperature.

3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Switching Characteristics^[5] Over the Operating Range

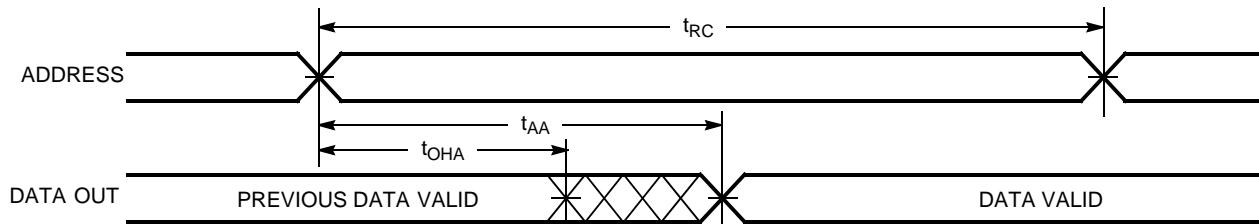
Parameter	Description	7C1020BN-12		7C1020BN-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	12		15		ns
t_{AA}	Address to Data Valid		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		6		7	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[6]	0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		6		7	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[6]	3		3		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		6		7	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		12		15	ns
t_{DBE}	Byte Enable to Data Valid		6		7	ns
t_{LZBE}	Byte Enable to Low Z	0		0		ns
t_{HZBE}	Byte Disable to High Z		6		7	ns
Write Cycle^[8]						
t_{WC}	Write Cycle Time	12		15		ns
t_{SCE}	\overline{CE} LOW to Write End	9		10		ns
t_{AW}	Address Set-Up to Write End	8		10		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	8		10		ns
t_{SD}	Data Set-Up to Write End	6		8		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[6]	3		3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		6		7	ns
t_{BW}	Byte Enable to End of Write	8		9		ns

Notes:

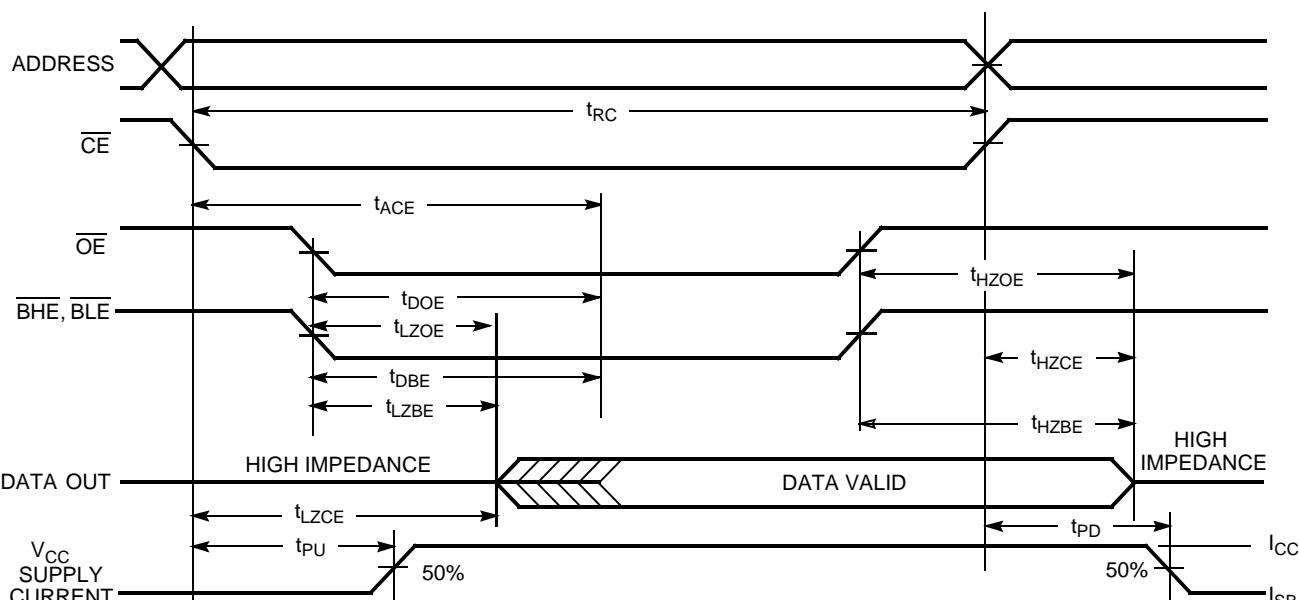
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and $\overline{BHE} / \overline{BLE}$ LOW. \overline{CE} , \overline{WE} and $\overline{BHE} / \overline{BLE}$ must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1^[9, 10]



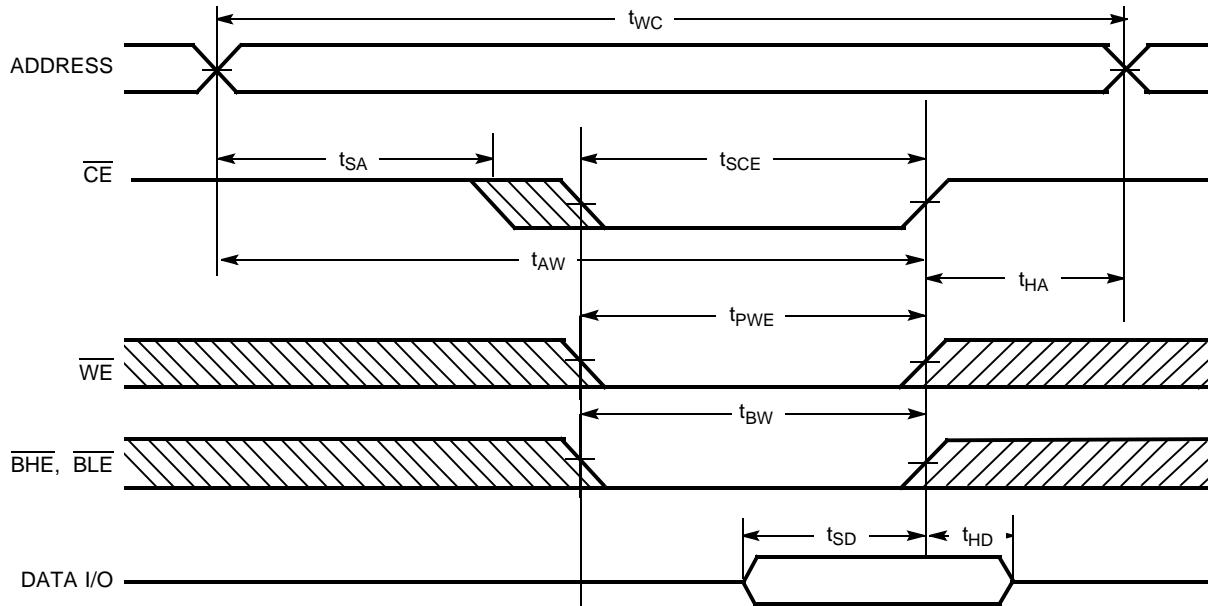
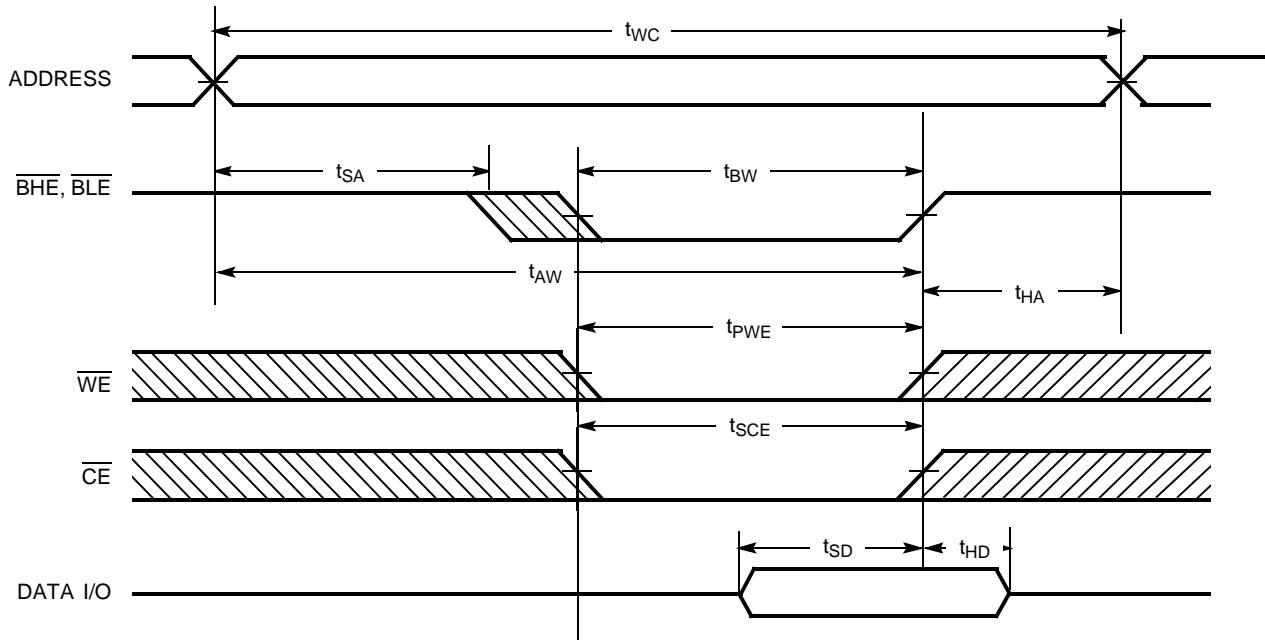
Read Cycle No. 2 (OE Controlled)^[10, 11]



Notes:

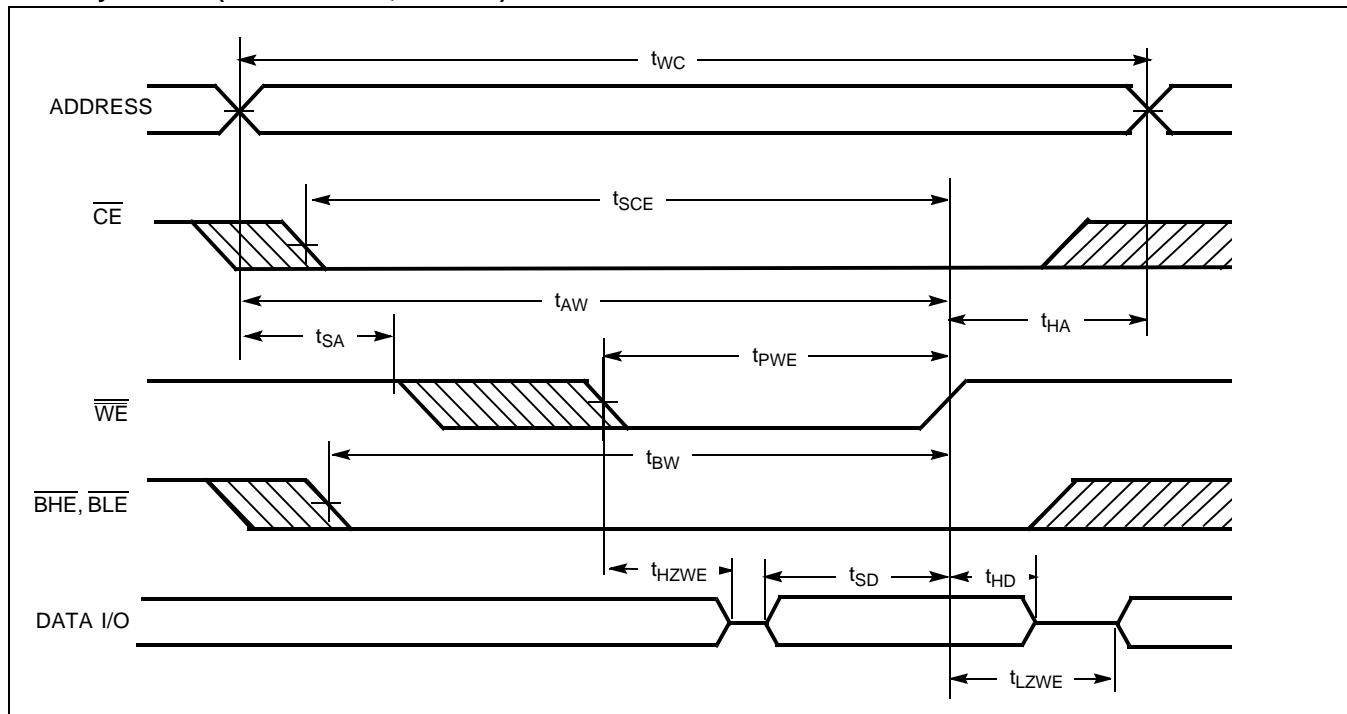
9. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or \overline{BHE} = V_{IL} .
10. WE is HIGH for read cycle.
11. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 (CE Controlled)^[12, 13]

Write Cycle No. 2 (BLE or BHE Controlled)

Notes:

12. Data I/O is high impedance if \overline{OE} or \overline{BHE} and/or $\overline{BLE} = V_{IH}$.
13. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

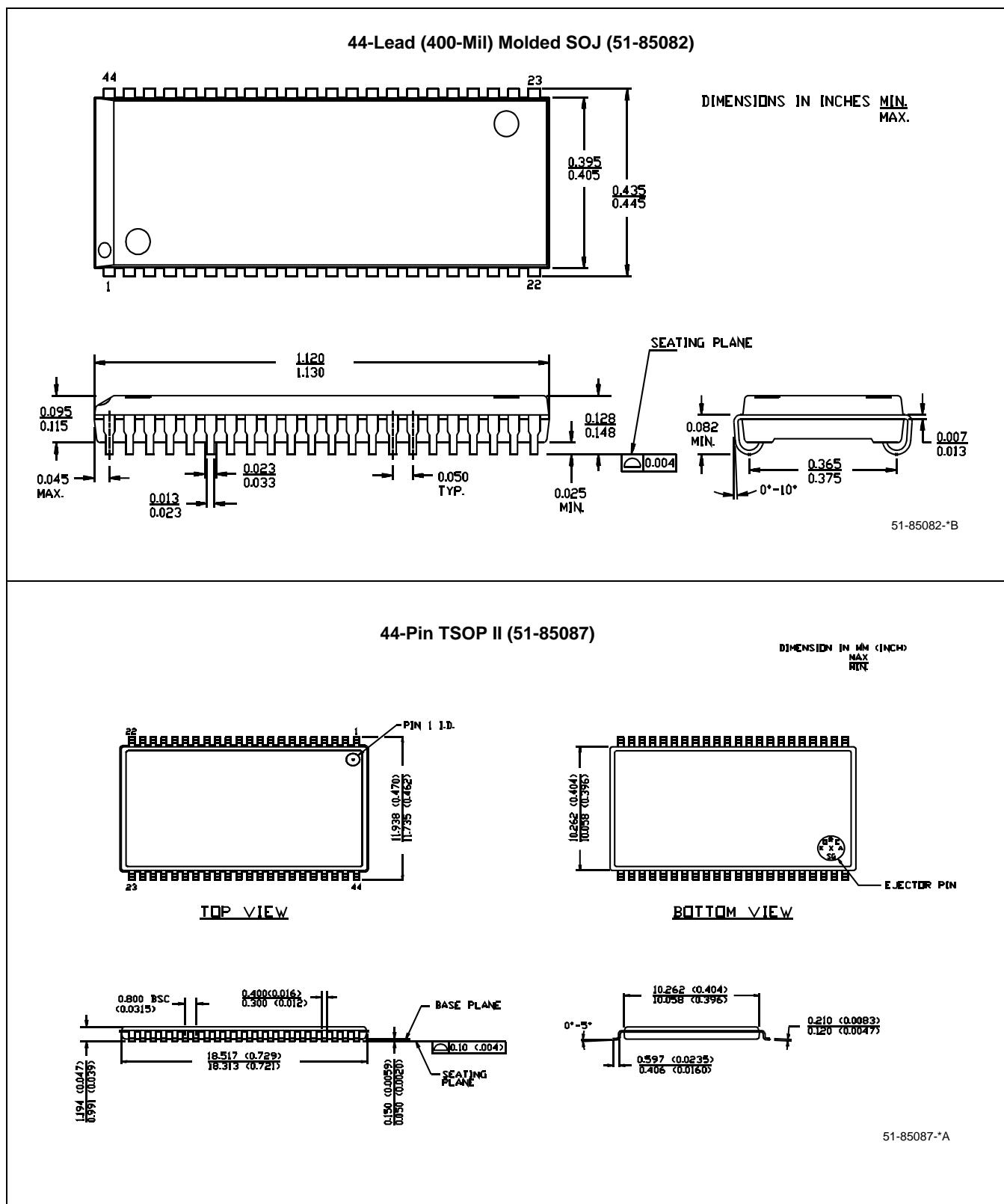
Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)

Truth Table

CE	OE	WE	BLE	BHE	I/O₁–I/O₈	I/O₉–I/O₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1020BN-12VC	51-85082	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020BN-12VXC	51-85082	44-Lead (400-Mil) Molded SOJ (Pb-free)	Commercial
	CY7C1020BN-12ZC	51-85087	44-pin TSOP Type II	Commercial
	CY7C1020BN-12ZXC	51-85087	44-pin TSOP Type II (Pb-free)	Commercial
15	CY7C1020BN-15ZC	51-85087	44-pin TSOP Type II	Commercial
	CY7C1020BN-15ZXC	51-85087	44-pin TSOP Type II (Pb-free)	Commercial

Please contact local sales representative regarding availability of these parts.

Package Diagrams


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Document History Page

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REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	426812	See ECN	NXR	New Data Sheet