

Features

- Temperature ranges
 - Automotive -A: -40°C to 85°C
 - Automotive-E: -40°C to 125°C
- High speed
 - $t_{AA} = 10\text{ ns}$
- Low active power
 - 360 mW (max)
- 2.0 V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features

Functional Description

The CY7C1049CV33 Automotive is a high performance CMOS Static RAM organized as 524,288 words by eight bits. Easy memory expansion is provided by an active LOW Chip Enable (CE), an active LOW Output Enable (OE), and three-state drivers. Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

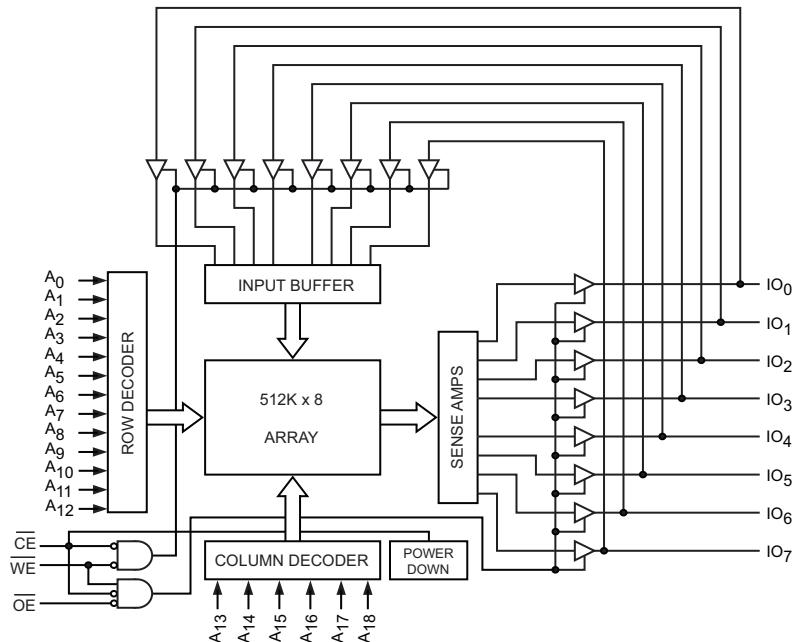
Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1049CV33 Automotive is available in standard 400-mil-wide 36-pin SOJ package and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

Logic Block Diagram



Contents

Selection Guide	3
Pin Configuration	3
Pin Definitions	3
Maximum Ratings	4
Operating Range	4
Electrical Characteristics	4
Capacitance	4
Thermal Resistance	4
AC Switching Characteristics	6
Switching Waveforms	7
Truth Table	8
Ordering Information	9
Ordering Code Definitions	9
Package Diagrams	10
Acronyms	11
Document Conventions	11
Units of Measure	11
Document History Page	12
Sales, Solutions, and Legal Information	13
Worldwide Sales and Design Support	13
Products	13
PSoC Solutions	13

Selection Guide

Description		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Automotive-A	100	95	—	mA
	Automotive-E	—	—	95	mA
Maximum CMOS Standby Current	Automotive-A	10	10	—	mA
	Automotive-E	—	—	15	mA

Pin Configuration

Figure 1. 36-pin SOJ (Top View)

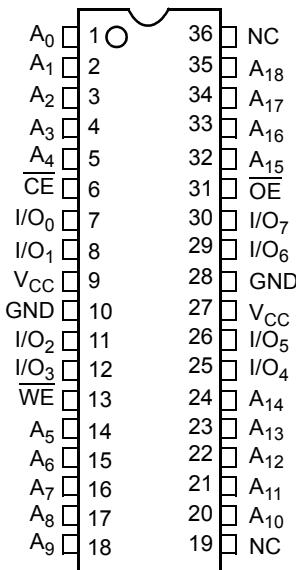
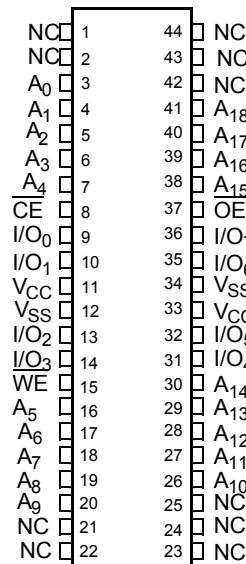


Figure 2. 44-pin TSOP II (Top View)



Pin Definitions

Pin Name	36 SOJ Pin Number	44 TSOP II Pin Number	I/O Type	Description
A ₀ –A ₁₈	1–5, 14–18, 20–24, 32–35	3–7, 16–20, 26–30, 38–41	Input	Address inputs used to select one of the address locations.
I/O ₀ –I/O ₇	7, 8, 11, 12, 25, 26, 29, 30	9, 10, 13, 14, 31, 32, 35, 36	Input/Output	Bidirectional data I/O lines. Used as input or output lines depending on operation
NC ^[1]	19, 36	1, 2, 21, 22, 23, 24, 25, 42, 43, 44	No Connect	No connects. This pin is not connected to the die
WE	13	15	Input/Control	Write Enable input, active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
CE	6	8	Input/Control	Chip Enable input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
OE	31	37	Input/Control	Output Enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins.
V _{SS} , GND	10, 28	12, 34	Ground	Ground for the device. Should be connected to ground of the system.
V _{CC}	9, 27	11, 33	Power Supply	Power supply inputs to the device.

Note

1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with

Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage on V_{CC} to Relative GND^[2] -0.5 V to $+4.6\text{ VDC}$

Voltage Applied to Outputs
in High Z State^[2] -0.5 V to $V_{CC} + 0.5\text{ V}$

Input Voltage^[2] -0.5 V to $V_{CC} + 0.5\text{ V}$

Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Automotive-A	-40°C to $+85^{\circ}\text{C}$	$3.3\text{ V} \pm 0.3\text{ V}$
Automotive-E	-40°C to $+125^{\circ}\text{C}$	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$; $I_{OH} = -4.0\text{ mA}$	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$; $I_{OL} = 8.0\text{ mA}$	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[2]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I_{IX}	Input Load Current	$\text{GND} \leq V_I \leq V_{CC}$	Auto-A	-1	+1	-1	+1	—	μA
			Auto-E	—	—	—	—	-20	
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max}$, $f = f_{\text{MAX}} = 1/t_{\text{RC}}$	Auto-A	—	100	—	95	—	mA
			Auto-E	—	—	—	—	—	
I_{SB1}	Automatic CE Power Down Current —TTL Inputs	Max. V_{CC} , $CE \geq V_{IH}$; $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{\text{MAX}}$	Auto-A	—	40	—	40	—	mA
			Auto-E	—	—	—	—	—	
I_{SB2}	Automatic CE Power Down Current —CMOS Inputs	Max. V_{CC} , $CE \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$, or $V_{IN} \leq 0.3\text{ V}$, $f = 0$	Auto-A	—	10	—	10	—	mA
			Auto-E	—	—	—	—	—	

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter ^[3]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 3.3\text{ V}$	8	pF
C_{OUT}	I/O Capacitance		8	pF

Thermal Resistance

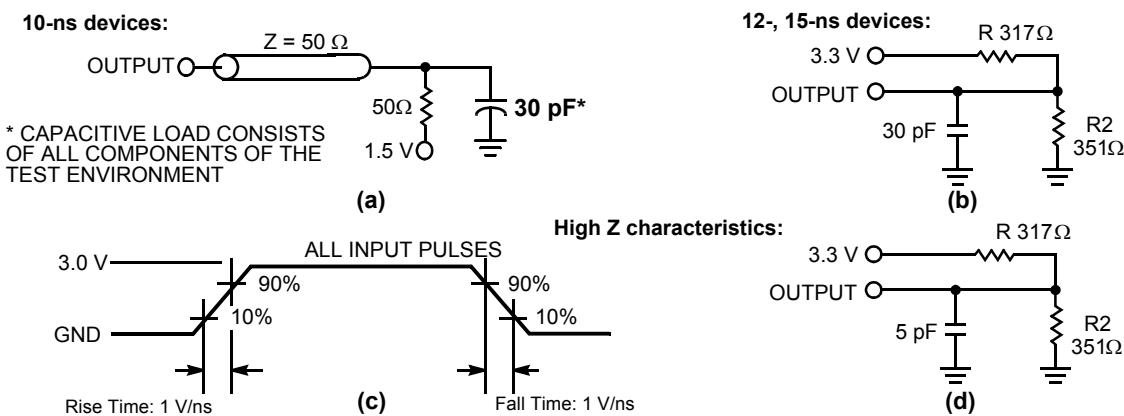
Tested initially and after any design or process changes that may affect these parameters.

Parameter ^[3]	Description	Test Conditions	36-pin SOJ	44-pin TSOP-II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	46.51	41.66	$^{\circ}\text{C/W}$
Θ_{JC}	Thermal Resistance (Junction to Case)		18.8	10.56	$^{\circ}\text{C/W}$

Notes

2. V_{IL} (min) = -2.0 V and V_{IH} (max) = $V_{CC} + 0.5\text{ V}$ for pulse durations of less than 20 ns.

3. Tested initially and after any design or process changes that may affect these parameters.

Figure 3. AC Test Loads and Waveforms [4]

Notes

4. AC characteristics (except High Z) for 10 ns parts are tested using the load conditions shown in [Figure 3 \(a\)](#). All other speeds are tested using the Thevenin load shown in [Figure 3 \(b\)](#). High Z characteristics are tested for all speeds using the test load shown in [Figure 3 \(d\)](#).

AC Switching Characteristics

Over the Operating Range ^[5]

Parameter	Description	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{power} ^[6]	V_{CC} (typical) to the first access	100	—	100	—	100	—	μs
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address to Data Valid	—	10	—	12	—	15	ns
t_{OHA}	Data Hold from Address Change	3	—	3	—	—	3	ns
t_{ACE}	\overline{CE} LOW to Data Valid	—	10	—	12	—	15	ns
t_{DOE}	\overline{OE} LOW to Data Valid	—	5	—	6	—	7	ns
t_{LZOE}	\overline{OE} LOW to Low Z	0	—	0	—	0	—	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[7, 8]	—	5	—	6	—	7	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[8]	3	—	3	—	3	—	ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[7, 8]	—	5	—	6	—	7	ns
t_{PU}	\overline{CE} LOW to Power Up	0	—	0	—	0	—	ns
t_{PD}	\overline{CE} HIGH to Power Down	—	10	—	12	—	15	ns
Write Cycle ^[9, 10]								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{SCE}	\overline{CE} LOW to Write End	7	—	8	—	10	—	ns
t_{AW}	Address Setup to Write End	7	—	8	—	10	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup to Write Start	0	—	0	—	0	—	ns
t_{PWE}	WE Pulse Width	7	—	8	—	10	—	ns
t_{SD}	Data Setup to Write End	5	—	6	—	7	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{LZWE}	WE HIGH to Low Z ^[8]	3	—	3	—	3	—	ns
t_{HZWE}	WE LOW to High Z ^[7, 8]	—	5	—	6	—	7	ns

Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
6. t_{POWER} gives the minimum amount of time that the power supply should be at stable, typical V_{CC} values until the first memory access can be performed.
7. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of Figure 3 on page 5. Transition is measured ± 500 mV from steady-state voltage.
8. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
9. The internal Write time of the memory is defined by the overlap of CE LOW, and WE LOW. CE and WE must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the Write.
10. The minimum Write cycle time for Write Cycle No. 3 (WE controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [11, 12]

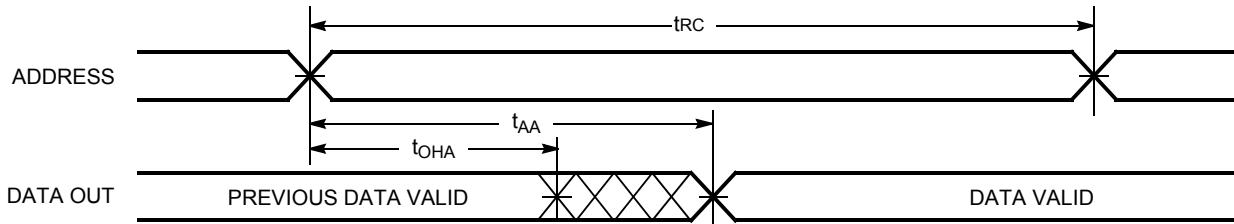


Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [12, 13]

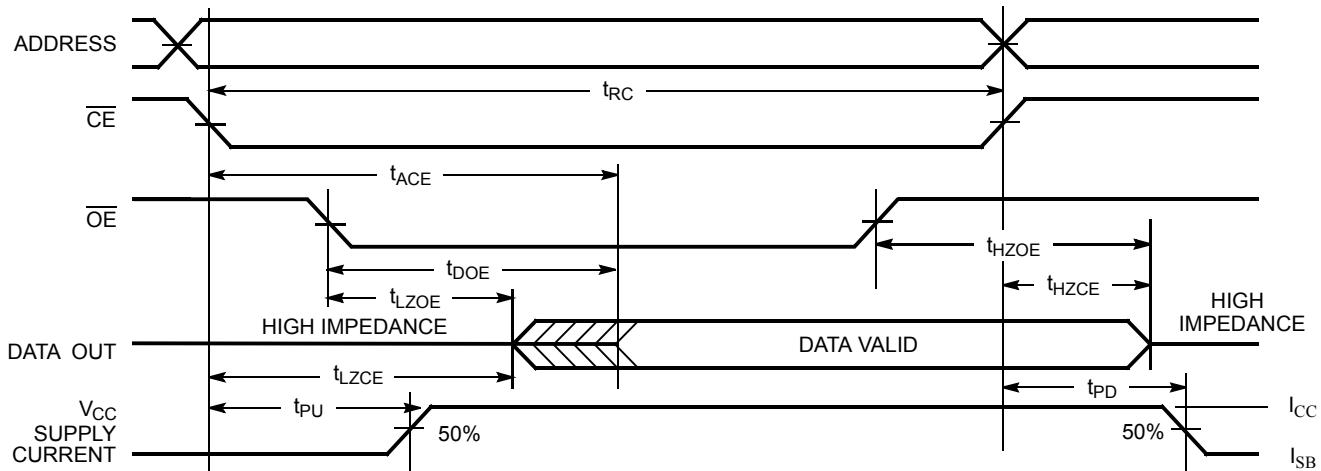
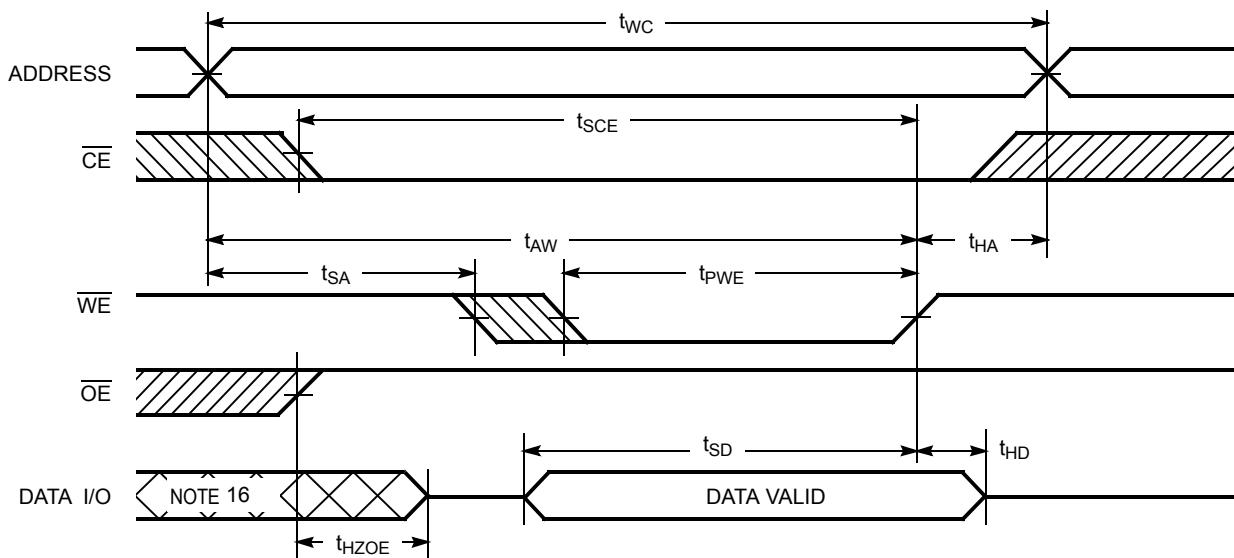


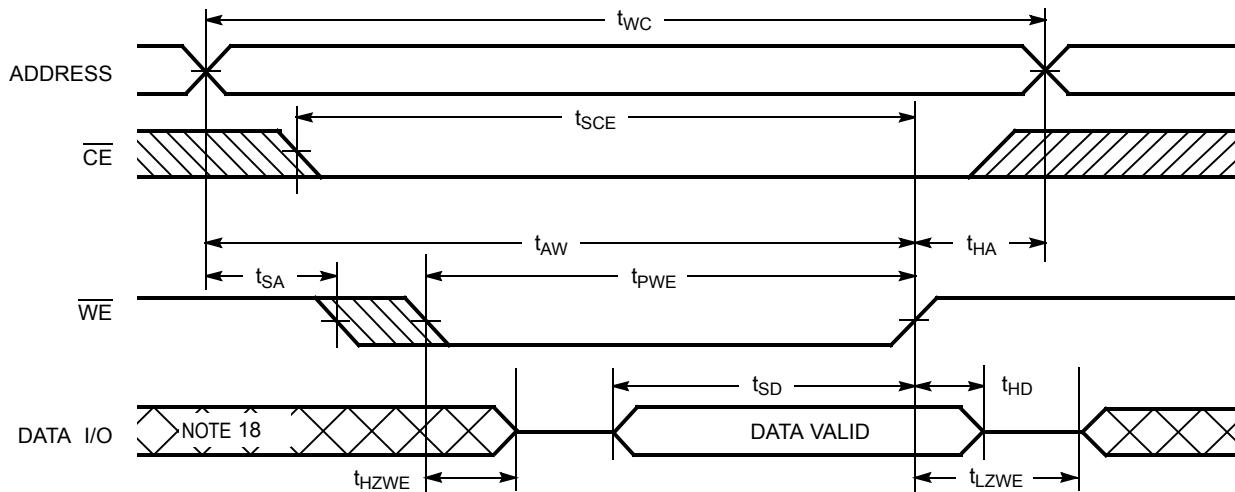
Figure 6. Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} HIGH During Write) [14, 15]



Notes

11. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
12. WE is HIGH for read cycles.
13. Address valid before or similar to \overline{CE} transition LOW.
14. Data I/O is high impedance if $\overline{OE} = V_{IL}$.
15. If \overline{CE} goes HIGH simultaneously with WE HIGH, the output remains in high impedance state.
16. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW) [17]

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	$I/O_0-I/O_7$	Mode	Power
H	X	X	High Z	Power Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

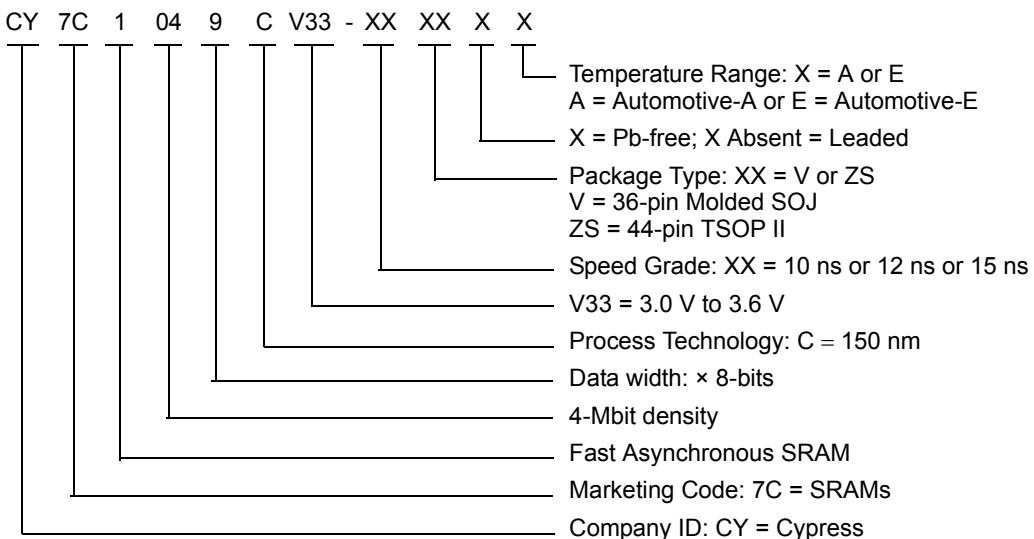
Notes

17. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in high impedance state.
 18. During this period, the I/Os are in output state. Do not apply input signals.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1049CV33-10VXA	51-85090	36-pin (400-Mil) Molded SOJ (Pb-free)	Automotive-A
12	CY7C1049CV33-12ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A
15	CY7C1049CV33-15VXE	51-85090	36-pin (400-Mil) Molded SOJ (Pb-free)	Automotive-E
	CY7C1049CV33-15ZSXE	51-85087	44-pin TSOP II (Pb-free)	Automotive-E

Ordering Code Definitions



Package Diagrams

Figure 8. 36-pin (400-Mil) Molded SOJ, 51-85090

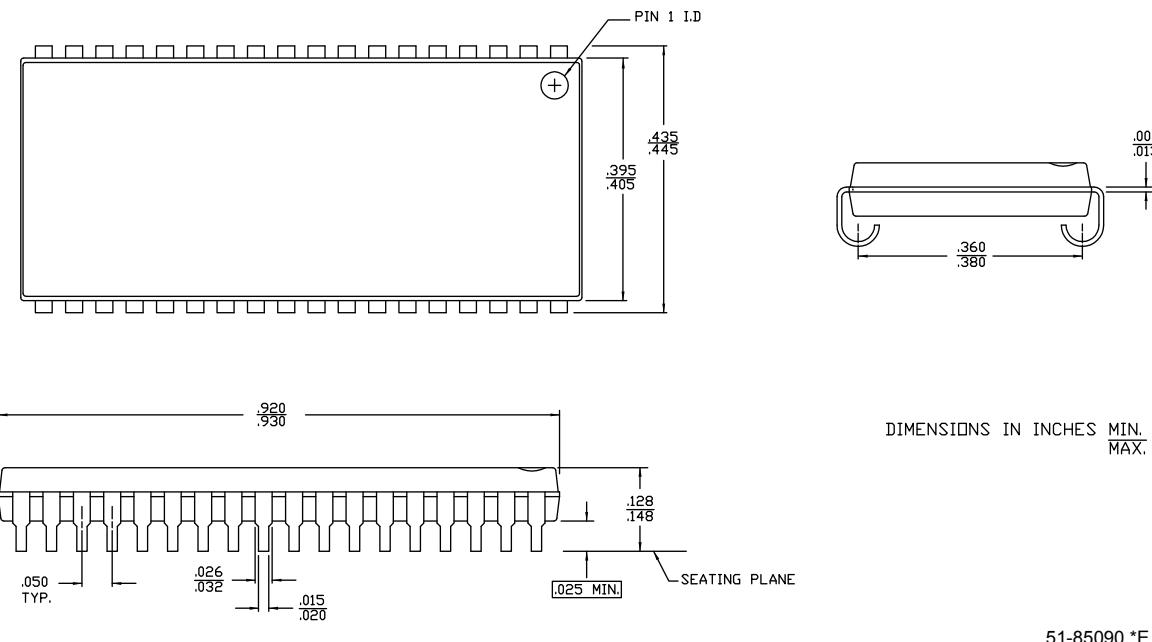
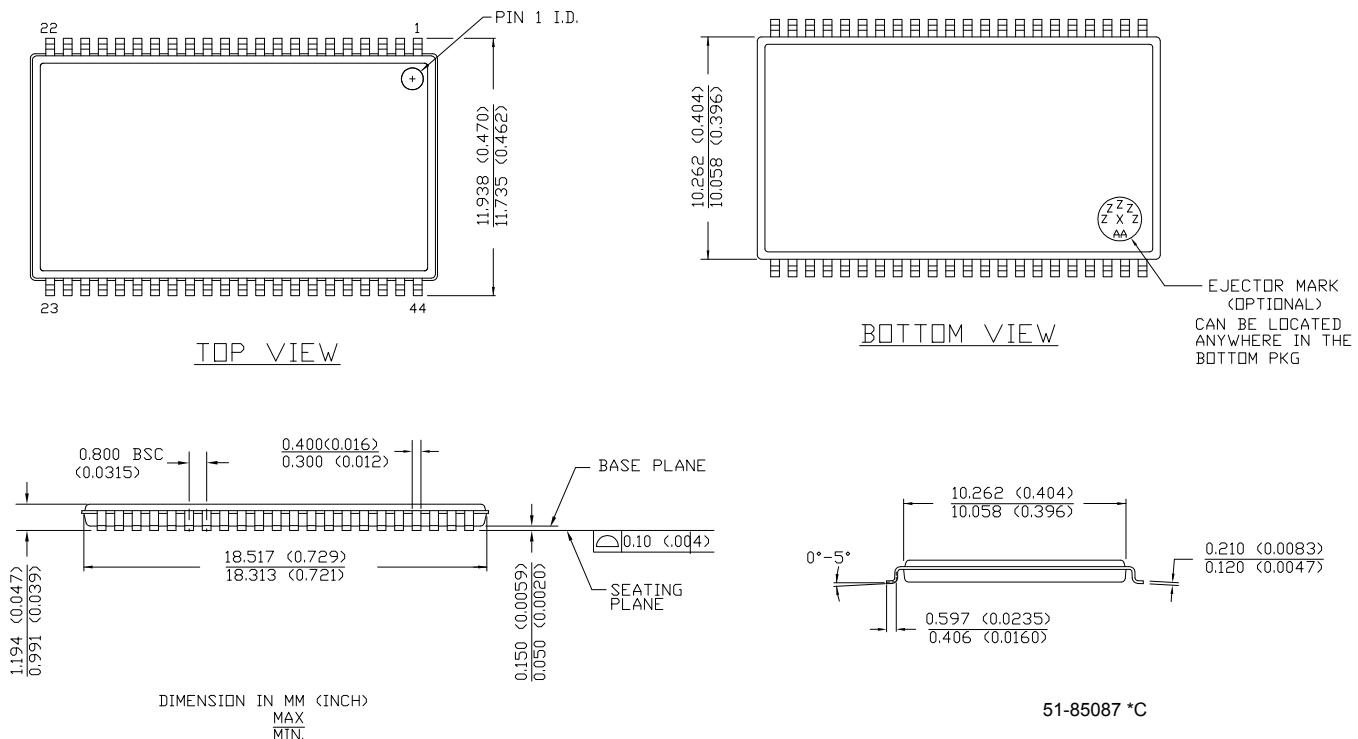


Figure 9. 44-pin TSOP II, 51-85087



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
CE	Chip Enable
OE	Output Enable
RAM	Random Access Memory
I/O	Input/Output
SOJ	small outline J-lead
TTL	transistor-transistor logic
TSOP	thin small outline package
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
Ω	ohms
ns	nano seconds
V	Volts
μs	micro seconds
μA	micro Amperes
mA	milli Amperes
mm	milli meter
ms	milli seconds
MHz	Mega Hertz
pF	pico Farad
%	percent
mW	milli Watts
W	Watts
$^{\circ}C$	degree Celcius

Document History Page

Document Title: CY7C1049CV33 Automotive 4-Mbit (512 K x 8) Static RAM
Document Number: 001-67511

Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	3186792	PRAS	03/03/2011	Separation of the automotive datasheet from CY7C1049CV33 spec no. 38-05006 Rev. *J. Further rev of 38-05006 would include only industrial / commercial parts.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 PSoC 3 PSoC 5

© Cypress Semiconductor Corporation, 2002-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.