CY7C1069G
CY7C1069GE

16-Mbit (2 M words × 8 bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
  - t_{AA} = 10 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby currents
  - I_{CC} = 90 mA typical at 100 MHz
  - I_{SB2} = 20 mA typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Available in Pb-free 54-pin TSOP II, and 48-ball VFBGA packages

Functional Description

The CY7C1069G and CY7C1069GE are dual chip enable high-performance CMOS fast static RAM devices with embedded ECC. The CY7C1069G device is available in standard pin configurations. The CY7C1069GE device includes a single bit error indication pin (ERR) that signals the host processor in the case of an ECC error-detection and correction event.

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{20}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. See Truth Table – CY7C1069G / CY7C1069GE on page 14 for a complete description of Read and Write modes. The input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

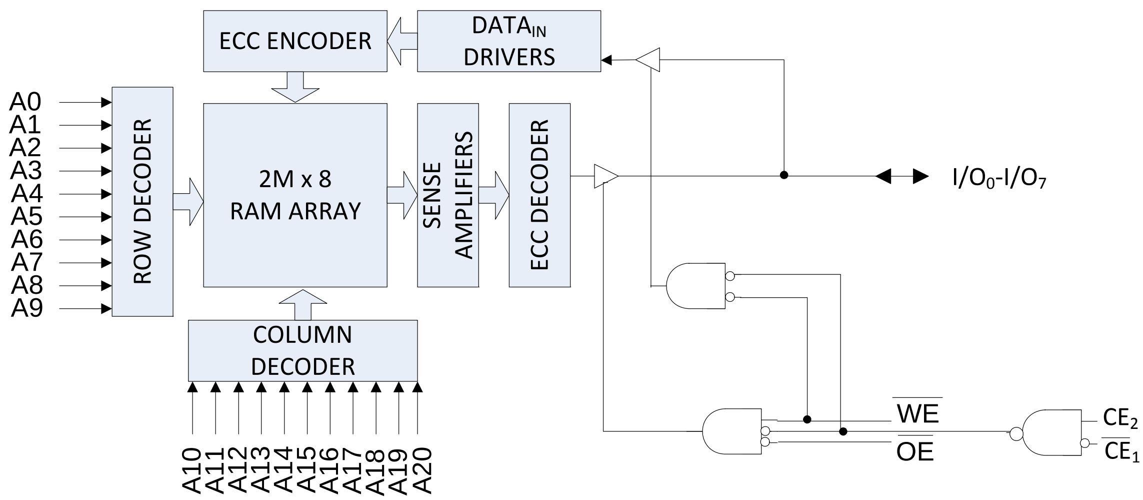
On CY7C1069GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High) [1].

All I/Os (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), and control signals are de-asserted ($\overline{CE}_1$ / CE_2, $\overline{OE}$, $\overline{WE}$). CY7C1069G and CY7C1069GE devices are available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and in a 48-ball VFBGA package.

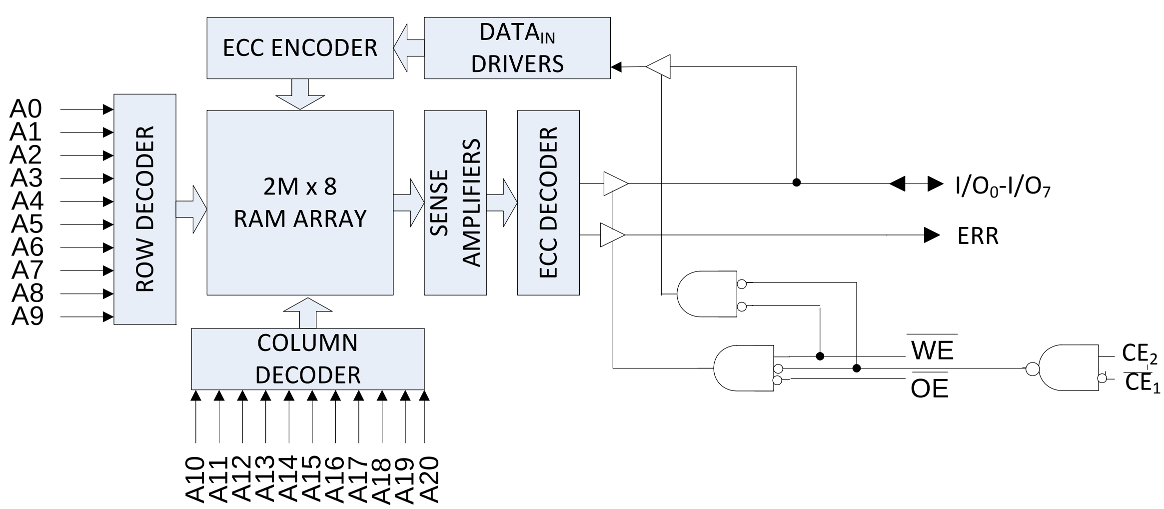
For a complete list of related documentation, here.

Note
1. Automatic write back on error detection feature is not supported in this device.

Logic Block Diagram – CY7C1069G



Logic Block Diagram – CY7C1069GE



Contents

Pin Configurations

Figure 1. 54-pin TSOP II pinout (Top View) – CY7C1069G [2]

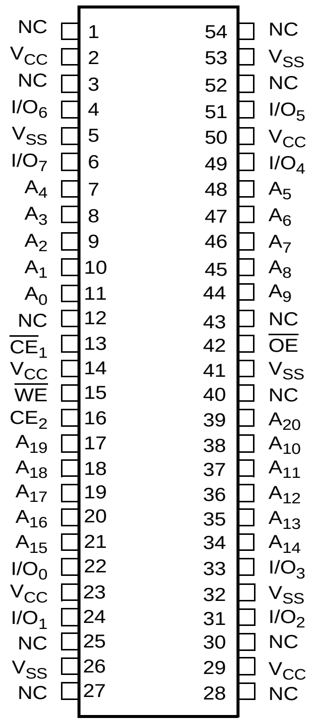
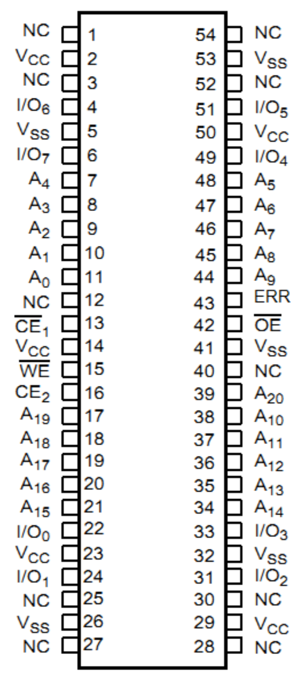


Figure 2. 54-pin TSOP II pinout (Top View) – CY7C1069GE [2, 3]



Note
2. NC pins are not connected on the die.
3. ERR is an Output pin. If not used, this pin should be left floating.

Pin Configurations (continued)

Figure 3. 48-ball VFBGA pinout (Top View) – CY7C1069G [4]

	1	2	3	4	5	6
A	NC	$\overline{OE}$	A_0	A_1	A_2	CE_2
B	NC	NC	A_3	A_4	$\overline{CE}_1$	NC
C	I/O_0	NC	A_5	A_6	NC	I/O_4
D	V_{SS}	I/O_1	A_{17}	A_7	I/O_5	V_{CC}
E	V_{CC}	I/O_2	A_{18}	A_{16}	I/O_6	V_{SS}
F	I/O_3	NC	A_{14}	A_{15}	NC	I/O_7
G	NC	NC	A_{12}	A_{13}	$\overline{WE}$	NC
H	A_{19}	A_8	A_9	A_{10}	A_{11}	A_{20}

Figure 4. 48-ball VFBGA pinout (Top View) – CY7C1069GE [4, 5]

	1	2	3	4	5	6
A	NC	$\overline{OE}$	A_0	A_1	A_2	CE_2
B	NC	NC	A_3	A_4	$\overline{CE}_1$	ERR
C	I/O_0	NC	A_5	A_6	NC	I/O_4
D	V_{SS}	I/O_1	A_{17}	A_7	I/O_5	V_{CC}
E	V_{CC}	I/O_2	A_{18}	A_{16}	I/O_6	V_{SS}
F	I/O_3	NC	A_{14}	A_{15}	NC	I/O_7
G	NC	NC	A_{12}	A_{13}	$\overline{WE}$	NC
H	A_{19}	A_8	A_9	A_{10}	A_{11}	A_{20}

Note

4. NC pins are not connected on the die.
5. ERR is an Output pin. If not used, this pin should be left floating.

Product Portfolio

Product	Features and Options (see the Pin Configurations section)	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation			
					Operating I_{CC}, (mA) $f = f_{max}$		Standby, I_{SB2} (mA)	
					Typ [6]	Max	Typ [6]	Max
CY7C1069G18	Dual-chip enable	Industrial	1.65 V–2.2 V	15	70	80	20	30
CY7C1069G30			2.2 V–3.6 V	10	90	110		
CY7C1069G			4.5 V–5.5 V	10	90	110		
CY7C1069GE18	Dual-chip enable and ERR output		1.65 V–2.2 V	15	70	80		
CY7C1069GE30			2.2 V–3.6 V	10	90	110		
CY7C1069GE			4.5 V–5.5 V	10	90	110		

Notes
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND ....–0.5 V to +6.0 V

DC voltage applied to outputs in High Z State [7] .... –0.5 V to V_{CC} + 0.5 V

DC input voltage [7] .... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) .... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) .... > 2001 V

Latch up current .... > 140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the Operating Range of –40 °C to 85 °C

Parameter	Description		Test Conditions		10 ns / 15 ns			Unit
					Min	Typ [8]	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA		1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.0	–	–	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.2	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1 mA		V_{CC} – 0.4 [9]	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 2 mA		–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V	–		1.4	–	V_{CC} + 0.2	V
		2.2 V to 2.7 V	–		2.0	–	V_{CC} + 0.3	
		2.7 V to 3.6 V	–		2.0	–	V_{CC} + 0.3	
		4.5 V to 5.5 V	–		2.2	–	V_{CC} + 0.5	
V_{IL}	Input LOW voltage [7]	1.65 V to 2.2 V	–		–0.2	–	0.4	V
		2.2 V to 2.7 V	–		–0.3	–	0.6	
		2.7 V to 3.6 V	–		–0.3	–	0.8	
		4.5 V to 5.5 V	–		–0.5	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1.0	–	+1.0	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1.0	–	+1.0	µA
I_{CC}	Operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = 100 MHz	–	90.0	110.0	mA
				f = 66.7 MHz	–	70.0	80.0	
I_{SB1}	Automatic CE power down current – TTL inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{IH} [10], V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	–	40.0	mA
I_{SB2}	Automatic CE power down current – CMOS inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V [10], V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0		–	20.0 [8]	30.0	mA

Notes
7. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 2 ns.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.
9. This parameter is guaranteed by design and is not tested.
10. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

Capacitance

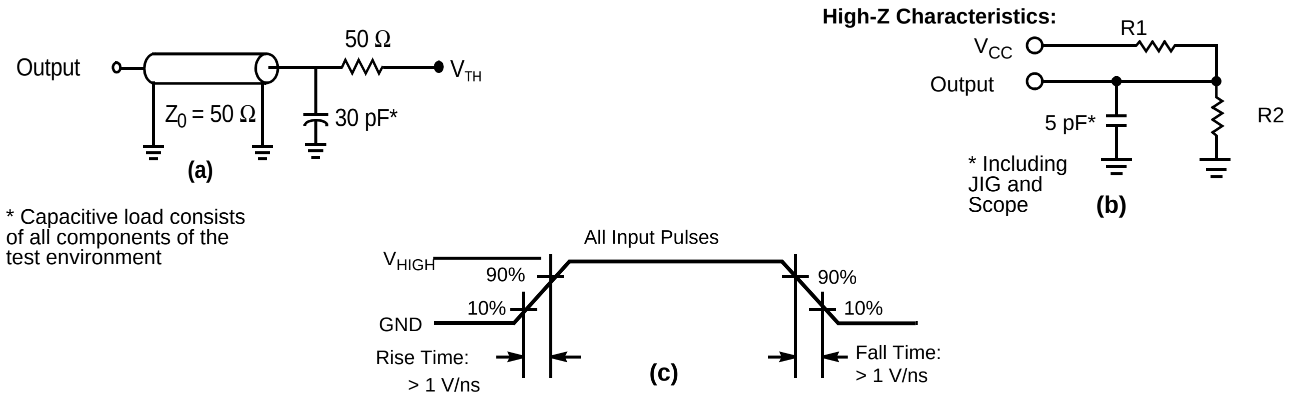
Parameter [11]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	10	pF
C_{OUT}	I/O capacitance		10	10	pF

Thermal Resistance

Parameter [11]	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	93.63	31.50	°C/W
Θ_{JC}	Thermal resistance (junction to case)		21.58	15.75	°C/W

AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms [12]



Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V_{TH}	0.9	1.5	1.5	V
V_{HIGH}	1.8	3	3	V

Notes
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device AC operation assumes a 100-µs ramp time from 0 to V_{CC}(min) and 100-µs wait time after V_{CC} stabilization.

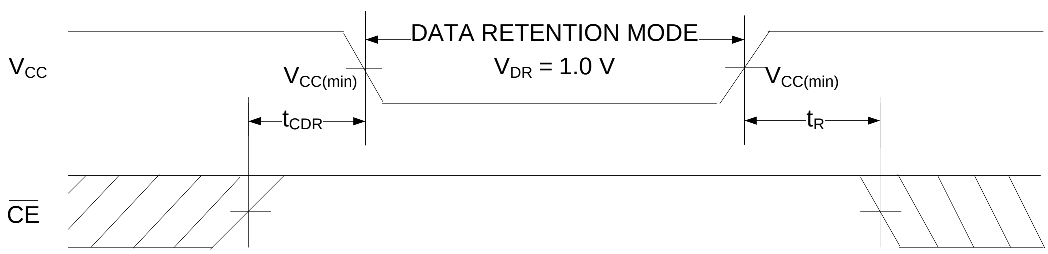
Data Retention Characteristics

Over the Operating Range of –40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	1.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V [13], $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	30.0	mA
t_{CDR}[14]	Chip deselect to data retention time	–	0	–	ns
t_R[14,15]	Operation recovery time	$V_{CC} \geq 2.2$ V	10.0	–	ns
		$V_{CC} < 2.2$ V	15.0	–	ns

Data Retention Waveform

Figure 6. Data Retention Waveform [13]



Notes

13. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
14. This parameter is guaranteed by design and is not tested.
15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

AC Switching Characteristics

Over the Operating Range of –40 °C to 85 °C

Parameter [16]	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{POWER}	V_{CC} stable to first access [17,22]	100.0	–	100.0	–	µs
t_{RC}	Read cycle time	10.0	–	15.0	–	ns
t_{AA}	Address to data / ERR valid	–	10.0	–	15.0	ns
t_{OHA}	Data / ERR hold from address change	3.0	–	3.0	–	ns
t_{ACE}	$\overline{CE}$ LOW to data / ERR valid [18]	–	10.0	–	15.0	ns
t_{DOE}	$\overline{OE}$ LOW to data / ERR valid	–	5.0	–	8.0	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [19, 20, 21]	0	–	1.0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [19, 20, 21]	–	5.0	–	8.0	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [18, 19, 20, 21]	3.0	–	3.0	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [18, 19, 20, 21]	–	5.0	–	8.0	ns
t_{PU}	$\overline{CE}$ LOW to power-up [18, 22]	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down [18, 22]	–	10.0	–	15.0	ns
Write Cycle [23, 24]						
t_{WC}	Write cycle time	10.0	–	15.0	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end [18]	7.0	–	12.0	–	ns
t_{AW}	Address setup to write end	7.0	–	12.0	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7.0	–	12.0	–	ns
t_{SD}	Data setup to write end	5.0	–	8.0	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [19, 20, 21]	3.0	–	3.0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [19, 20, 21]	–	5.0	–	8.0	ns

Notes

16. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$V). Test conditions for the read cycle use output loading shown in part (a) of Figure 5 on page 8, unless specified otherwise.
17. t_{POWER} gives minimum amount of time that the power supply is at stable V_{CC} until first memory access is performed.
18. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
19. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{LZOE}, t_{LZCE}, and t_{LZWE} are specified with a load capacitance of 5 pF as in (b) of Figure 5 on page 8. Transition is measured ±200 mV from steady state voltage.
20. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
21. Tested initially and after any design or process changes that may affect these parameters.
22. These parameters are guaranteed by design and are not tested.
23. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
24. The minimum write pulse width for write cycle No.2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 7. Read Cycle No. 1 of CY7C1069G (Address Transition Controlled) [25, 26]

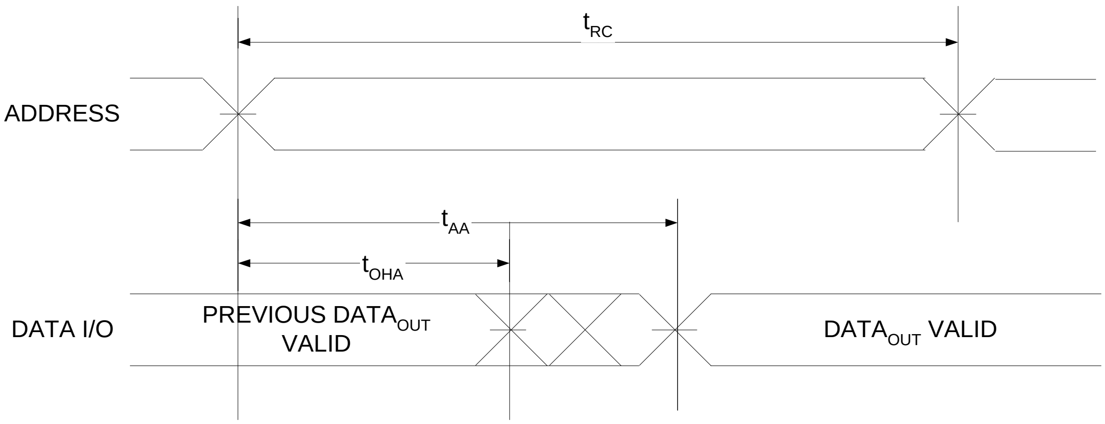
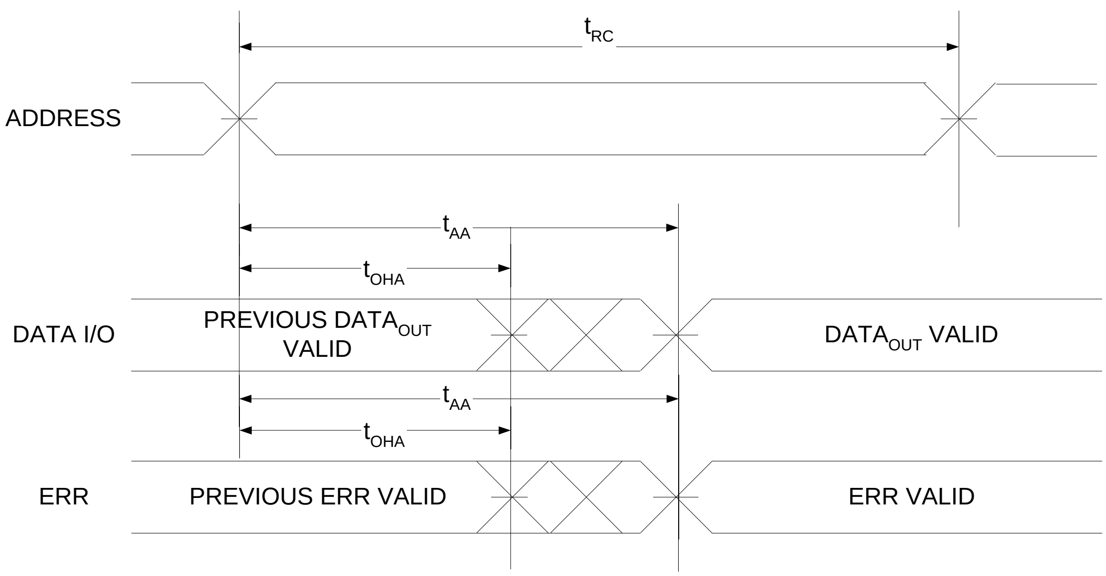


Figure 8. Read Cycle No. 2 of CY7C1069GE (Address Transition Controlled) [25, 26]

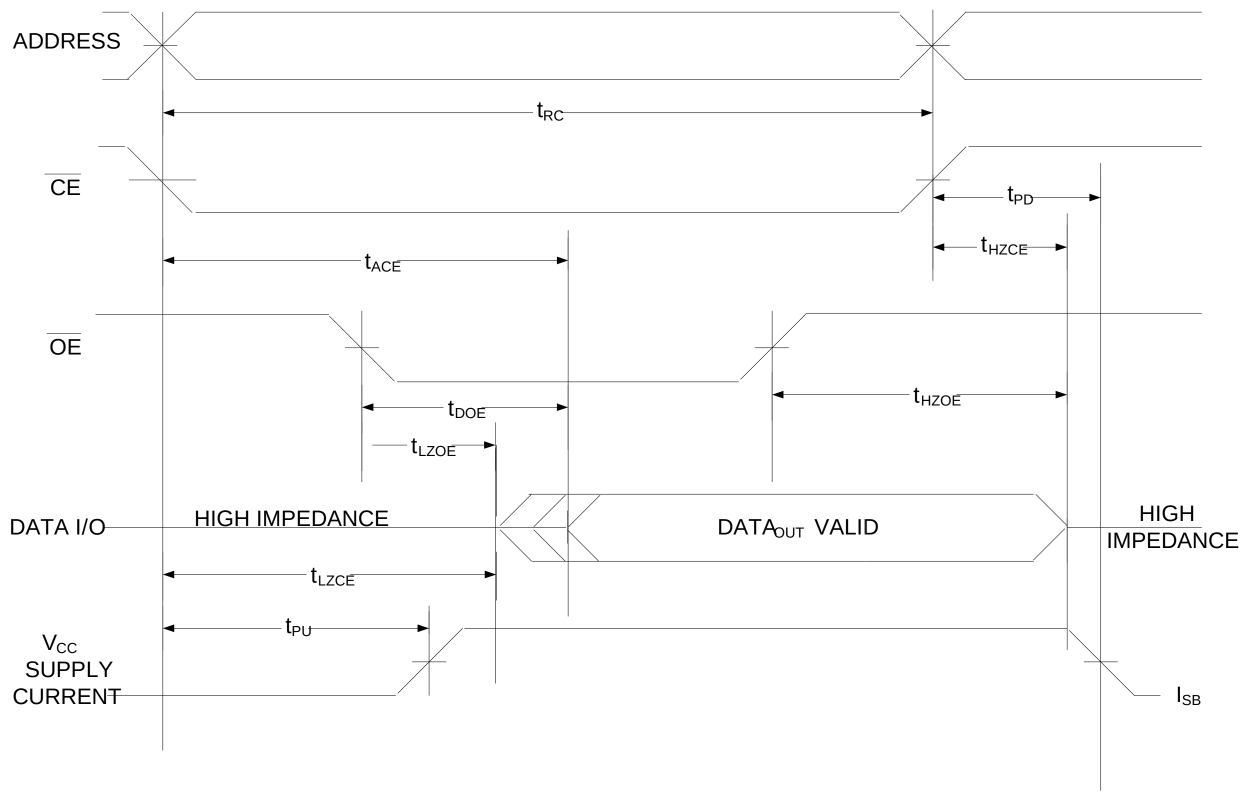


Notes

25. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$.
26. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 9. Read Cycle No. 3 ($\overline{OE}$ Controlled, $\overline{WE}$ HIGH) [27, 28, 29]



Notes

27. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
28. $\overline{WE}$ is HIGH for read cycle.
29. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

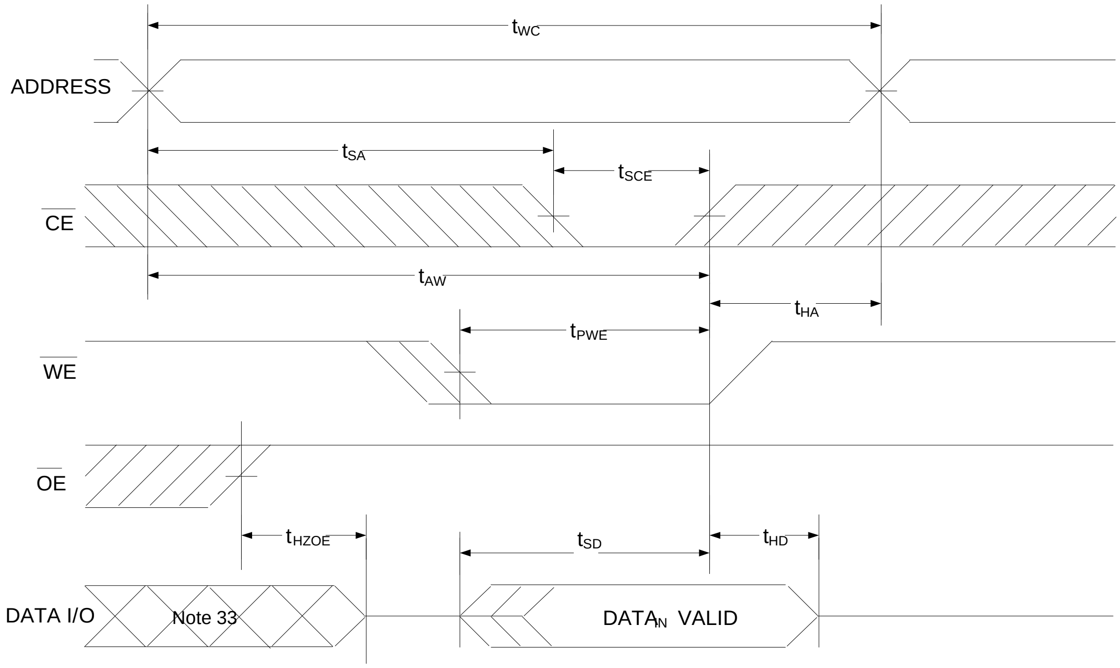


Figure 10. Write Cycle No. 1 (CE Controlled) [30, 31, 32]

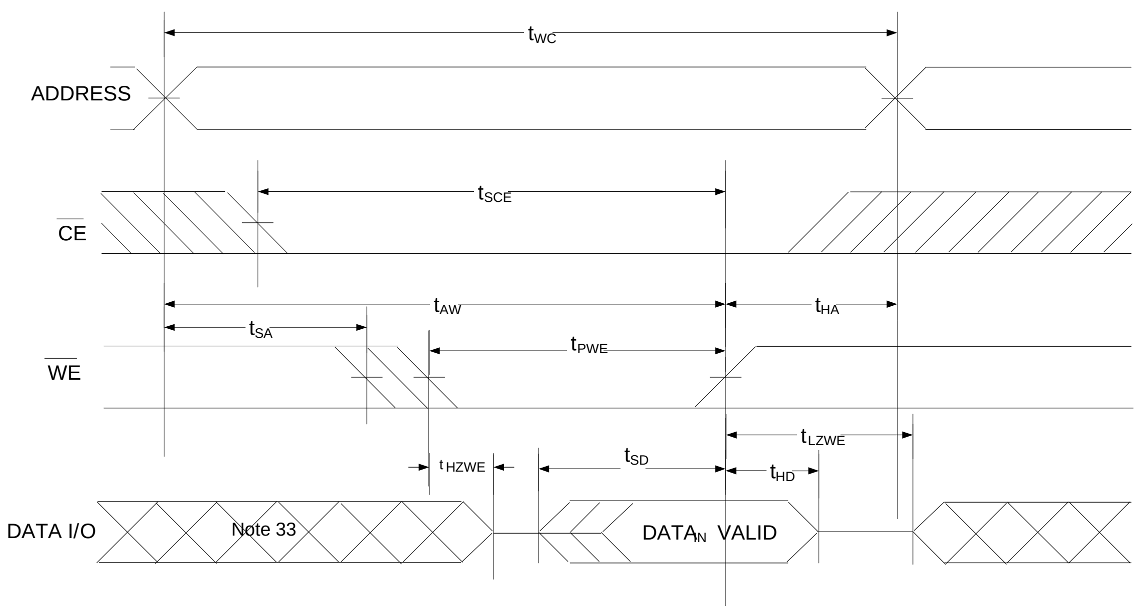


Figure 11. Write Cycle No. 2 (WE Controlled, OE Low) [30, 31, 32, 34]

Notes

30. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
31. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
32. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$.
33. During this time I/O are in output put state. Do not apply input signals.
34. The minimum write cycle width should be sum of t_{HZWE} and t_{SD},

Truth Table – CY7C1069G / CY7C1069GE

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X [35]	X [35]	X [35]	High Z	Power-down	Standby (I_{SB})
X [35]	L	X [35]	X [35]	High Z	Power-down	Standby (I_{SB})
L	H	L	H	Data out	Read all bits	Active (I_{CC})
L	H	X [35]	L	Data in	Write all bits	Active (I_{CC})
L	H	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

ERR Output – CY7C1069GE

Output [36]	Mode
0	Read Operation, no single bit error in the stored data.
1	Read Operation, single bit error detected and corrected.
High Z	Device deselected or Outputs disabled or Write Operation

Note

35. The input voltage levels on these pins should be either at V_{IH} or V_{IL}.
36. ERR is an Output pin.If not used, this pin should be left floating.

Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (All Pb-free)	ERR Pin / Ball	Operating Range
10	2.2 V–3.6 V	CY7C1069G30-10BVXI	51-85150	48-ball VFBGA	No	Industrial
		CY7C1069G30-10ZSXI	51-85160	54-pin TSOP II	No	
		CY7C1069GE30-10ZSXI	51-85160		Yes	
	4.5 V–5.5 V	CY7C1069G-10BVXI	51-85150	48-ball VFBGA	No	
		CY7C1069G-10ZSXI	51-85160	54-pin TSOP II	No	

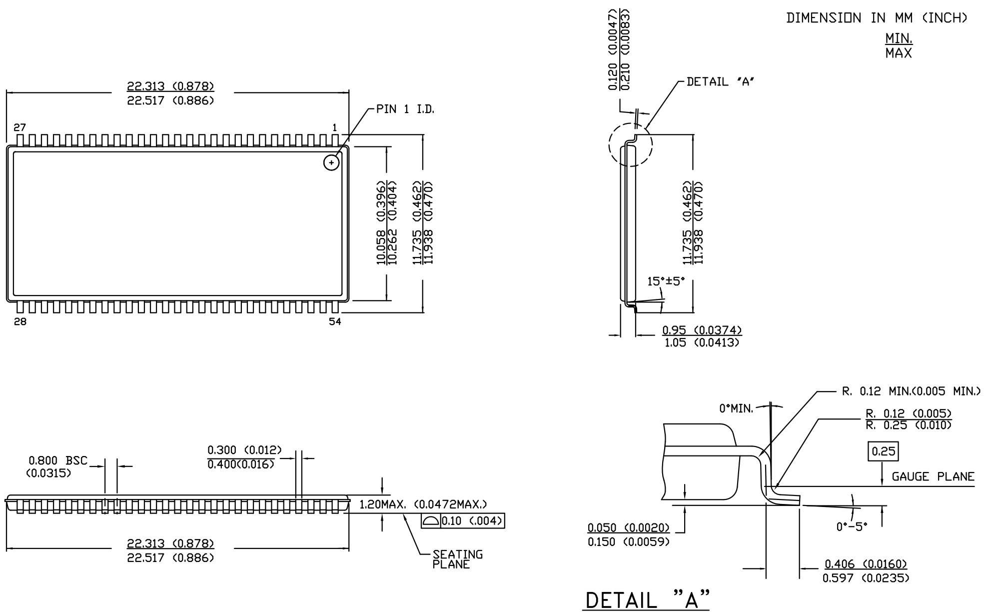
Ordering Code Definitions

CY 7 C 1 06 9 G E XX - XX XX X I

- Temperature Range: I = Industrial
- Pb-free
- Package Type: XX = BV or ZS, BV = 48-ball VFBGA ZS = 54-pin TSOP II
- Speed: XX = 10 ns or 15 ns
- Voltage Range: 18 = 1.65 V–2.2 V; 30 = 2.2 V–3.6 V; no character = 4.5 V–5.5 V
- Single bit error indication
- Process Technology: G = ULL65, 65 nm
- Data width: 9 = × 8-bits
- Density: 06 = 16-Mbit
- Family Code: 1 = Fast Asynchronous SRAM family
- Technology Code: C = CMOS
- Marketing Code: 7 = SRAM
- Company ID: CY = Cypress

Package Diagrams

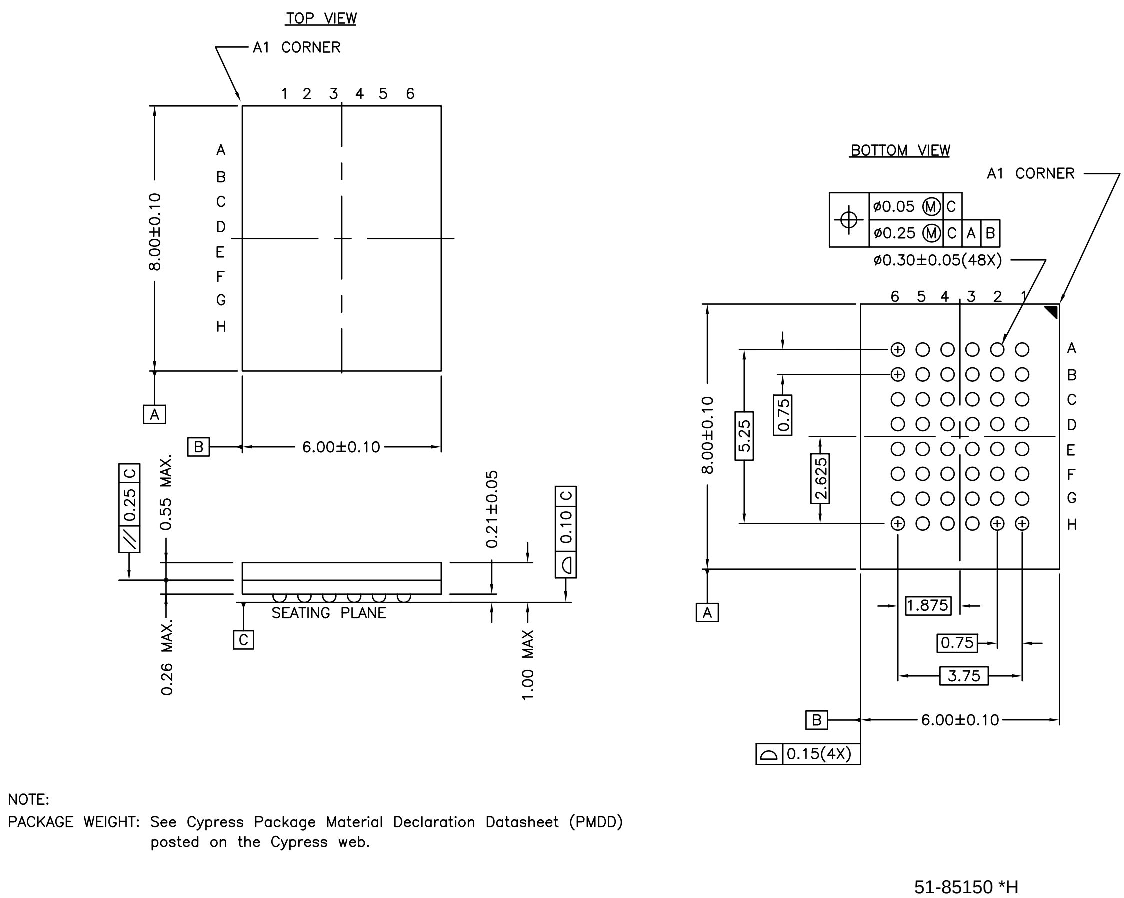
Figure 12. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



51-85160 *E

Package Diagrams (continued)

Figure 13. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1069G/CY7C1069GE, 16-Mbit (2 M words × 8 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81539				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H	4800609	NILE	07/31/2015	Changed status from Preliminary to Final.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support