

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
 - 20 ns
- Low active power
 - 660 mW (commercial)
- Low standby power
 - 110 mW (20 ns)
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- Available in Pb-free 24-pin Molded SOJ, non Pb-free 24-pin (300-Mil) Molded DIP

Functional Description

The CY7C128A is a high-performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (CE), and active LOW Output Enable (OE) and tri-state drivers. The CY7C128A has an automatic power-down feature, reducing the power consumption by 83% when deselected.

Writing to the device is accomplished when the Chip Enable (\overline{CE}) and Write Enable (WE) inputs are both LOW.

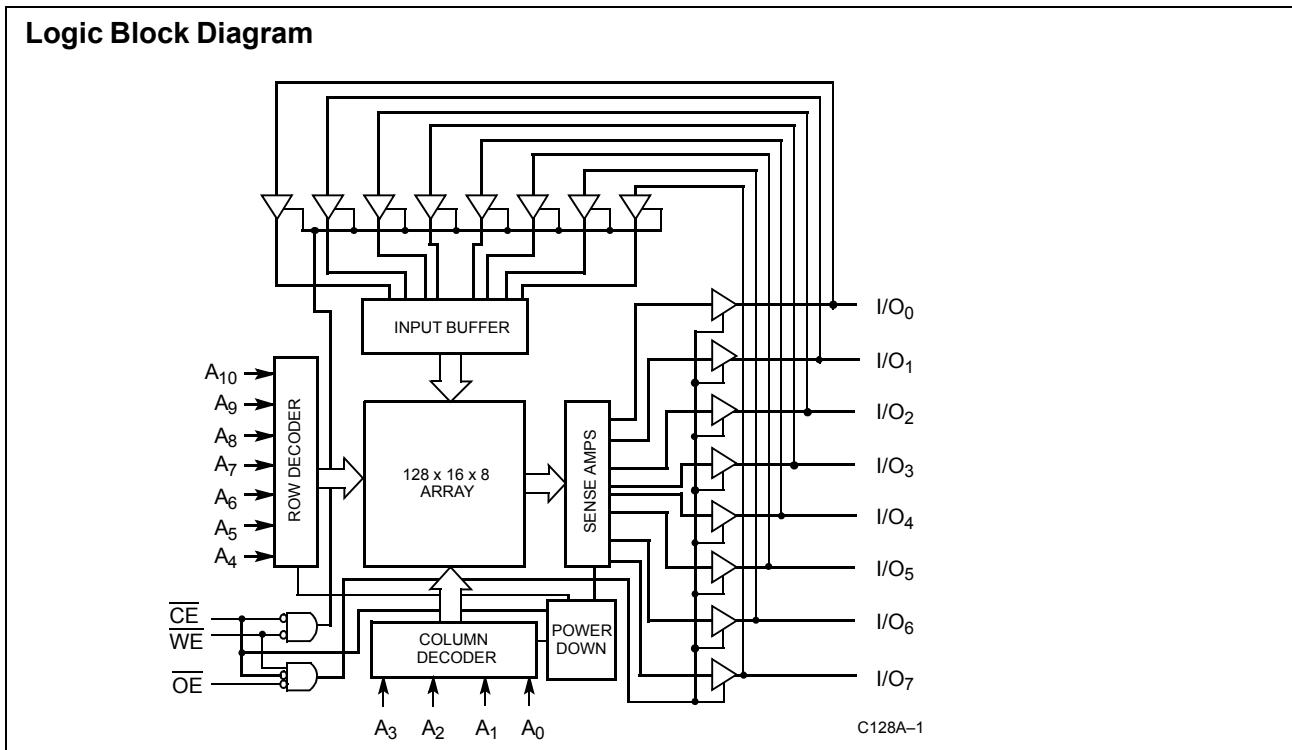
Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{10}).

Reading the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while Write Enable (WE) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight I/O pins.

The I/O pins remain in high-impedance state when Chip Enable (\overline{CE}) or Output Enable (\overline{OE}) is HIGH or Write Enable (WE) is LOW.

The CY7C128A utilizes a die coat to insure alpha immunity.

Logic Block Diagram

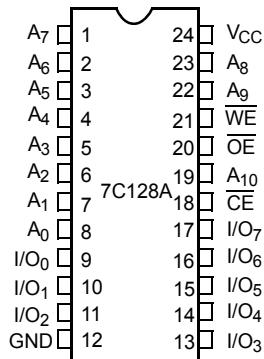


Selection Guide

Description	-20	-45
Maximum Access Time (ns)	20	45
Maximum Operating Current (mA)	120	120
Maximum CMOS Standby Current (mA)	20	20

Pin Configuration

Figure 1. 24-Pin DIP/SOJ (Top View)



Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with

Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage to Ground Potential

(Pin 28 to Pin 14) -0.5V to $+7.0\text{V}$

DC Voltage Applied to Outputs
in High Z State -0.5V to $+7.0\text{V}$

DC Input Voltage -3.0V to $+7.0\text{V}$

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage $>2001\text{V}$
(per MIL-STD-883, Method 3015)

Latch-Up Current $>200\text{ mA}$

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Electrical Characteristics

Over the Operating Range^[2]

Parameter	Description	Test Conditions	-20		-45		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $I_{OH} = -4.0\text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $I_{OL} = 8.0\text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage ^[3]		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Leakage Current	$\text{GND} \leq V_I \leq V_{CC}$	-10	+10	-10	+10	μA
I_{OZ}	Output Leakage Current	$\text{GND} \leq V_I \leq V_{CC}$ Output Disabled	-10	+10	-10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}$, $I_{OUT} = 0\text{ mA}$		120		120	mA
I_{SB1}	Automatic \overline{CE} Power-Down Current	$\text{Max. } V_{CC}, \overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%		40		20	mA
I_{SB2}	Automatic \overline{CE} Power-Down Current	$\text{Max. } V_{CC}, \overline{CE}_1 \geq V_{CC} - 0.3\text{V}$, $V_{IN} \geq V_{CC} - 0.3\text{V}$ or $V_{IN} \leq 0.3\text{V}$		20		20	mA

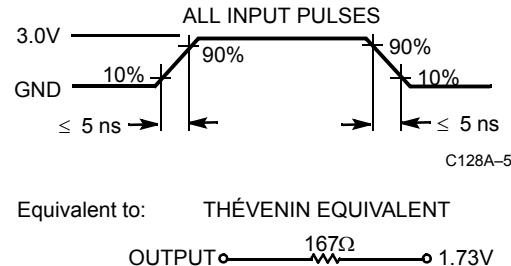
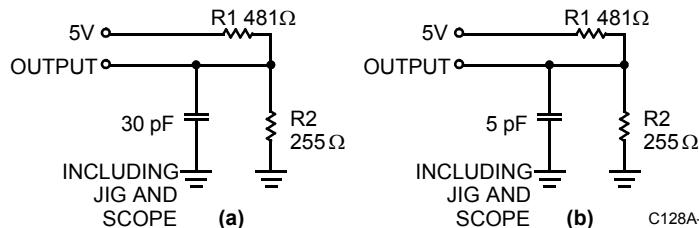
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} (min.) = -3.0V for pulse durations less than 30 ns.

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C, f = 1 \text{ MHz}, V_{CC} = 5.0V$	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range^[2, 5]

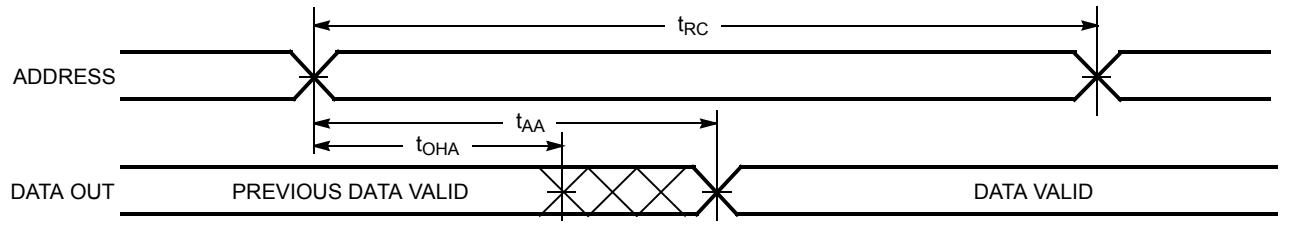
Parameter	Description	-20		-45		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	20		45		ns
t_{AA}	Address to Data Valid		20		45	ns
t_{OHA}	Data Hold from Address Change	5		5		ns
t_{ACE}	CE LOW to Data Valid		20		45	ns
t_{DOE}	OE LOW to Data Valid		10		20	ns
t_{LZOE}	OE LOW to Low Z	3		3		ns
t_{HZOE}	OE HIGH to High Z ^[6]		8		15	ns
t_{LZCE}	CE LOW to Low Z ^[7]	5		5		ns
t_{HZCE}	CE HIGH to High Z ^[6, 7]		8		15	ns
t_{PU}	CE LOW to Power-Up	0		0		ns
t_{PD}	CE HIGH to Power-Down		20		25	ns
WRITE CYCLE^[8]						
t_{WC}	Write Cycle Time	20		40		ns
t_{SCE}	CE LOW to Write End	15		30		ns
t_{AW}	Address Set-Up to Write End	15		30		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	WE Pulse Width	15		20		ns
t_{SD}	Data Set-Up to Write End	10		15		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	WE LOW to High Z ^[6]		7		15	ns
t_{LZWE}	WE HIGH to Low Z	5		5		ns

Notes:

- Tested initially and after any design or process changes that may affect these parameters
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{LZWE} are specified with $C_L = 5 \text{ pF}$ as in part (b) of AC Test Loads. Transition is measured $\pm 500 \text{ mV}$ from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

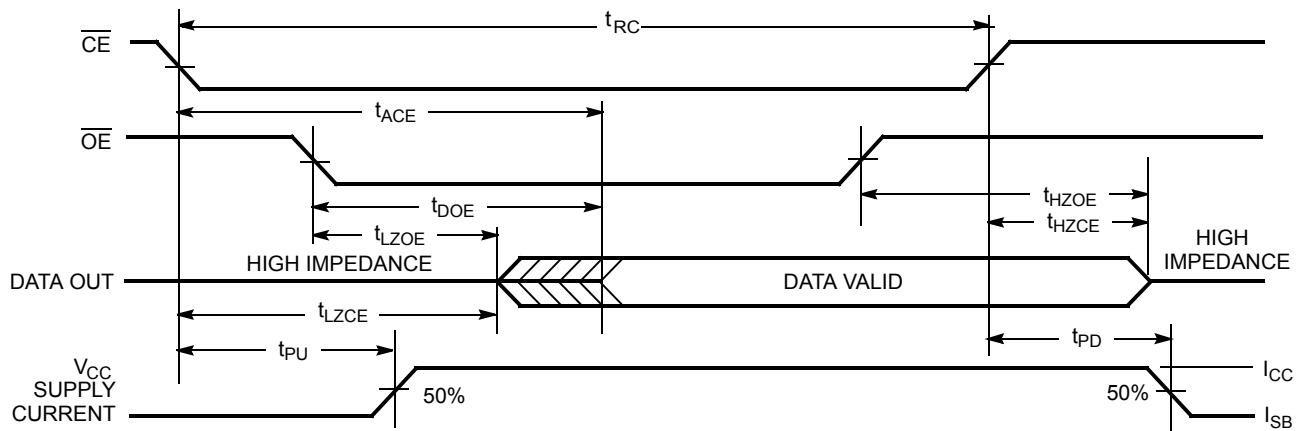
Switching Waveforms

Read Cycle No. 1^[9, 10]



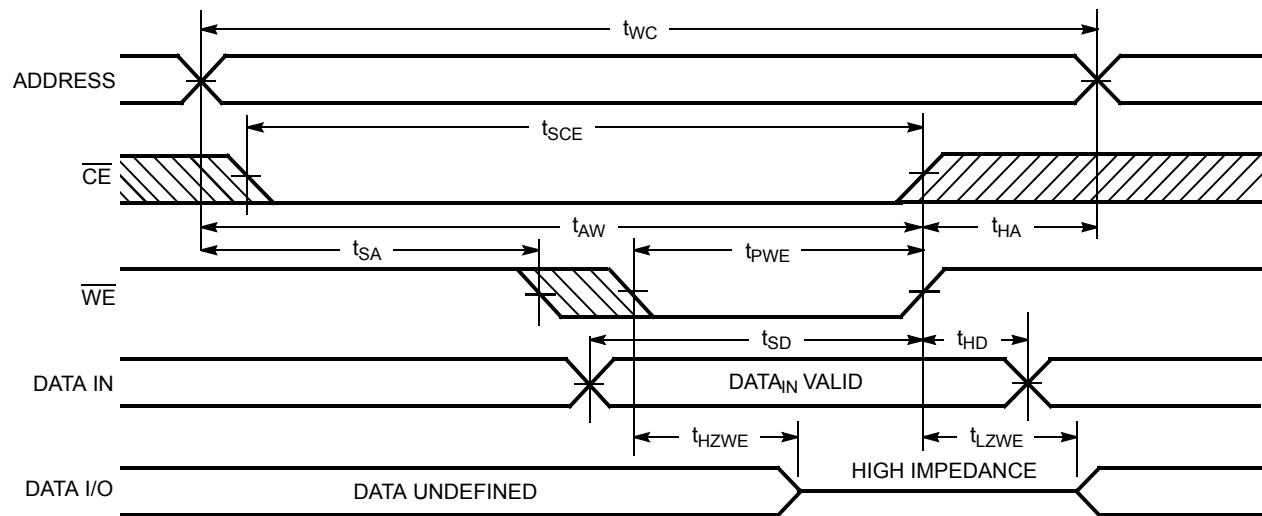
C128A-6

Read Cycle No. 2^[9, 11]



C128A-7

Write Cycle No. 1 (WE Controlled)^[8]



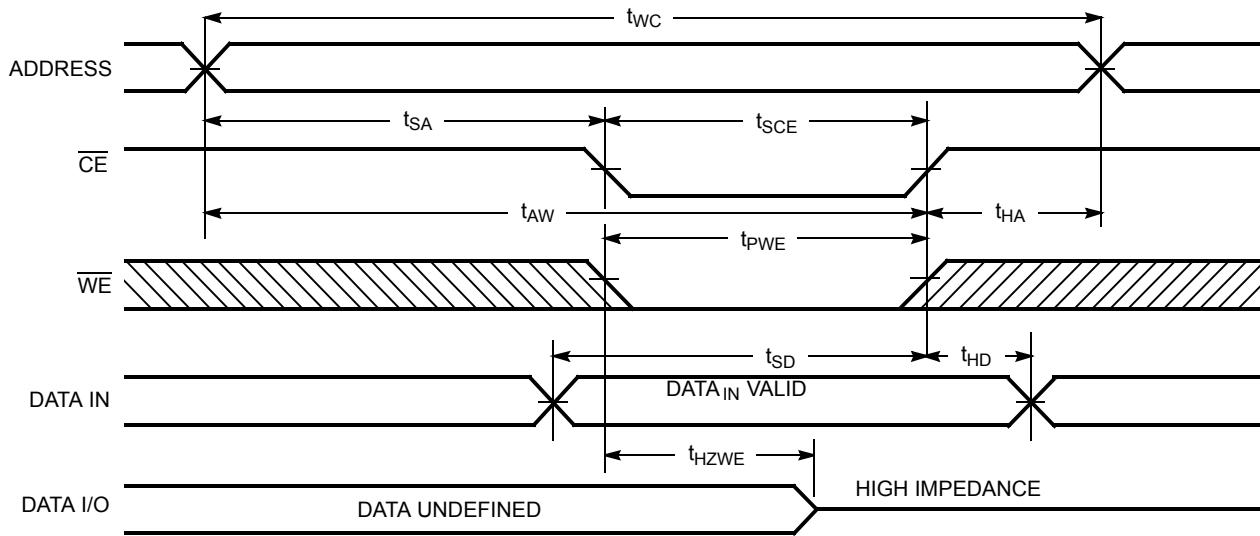
C128A-8

Notes:

9. WE is HIGH for read cycle.
10. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
11. Address valid prior to or coincident with CE transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 (CE Controlled)^[8, 12, 13]

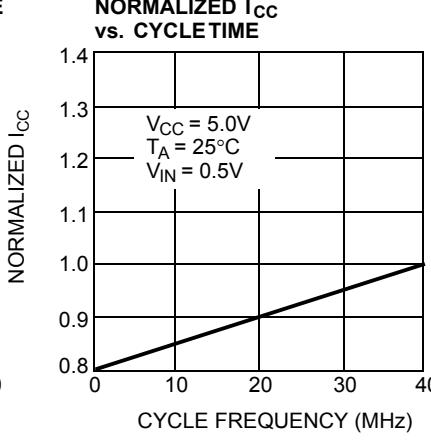
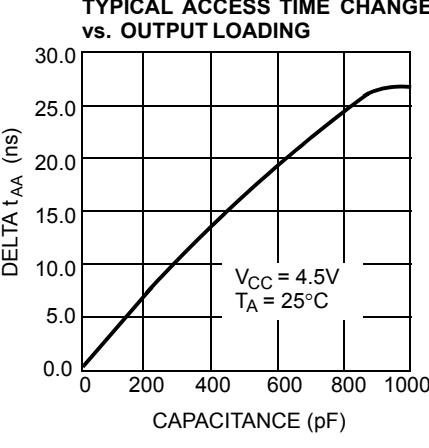
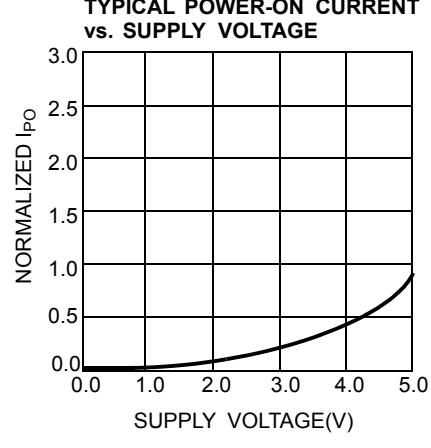
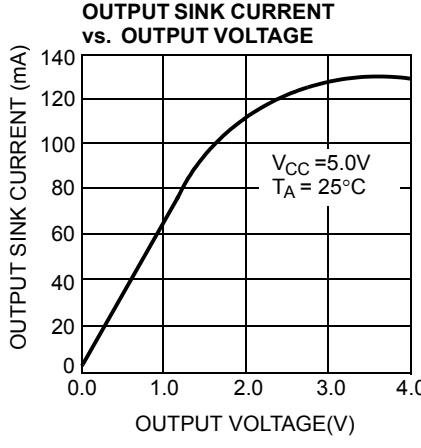
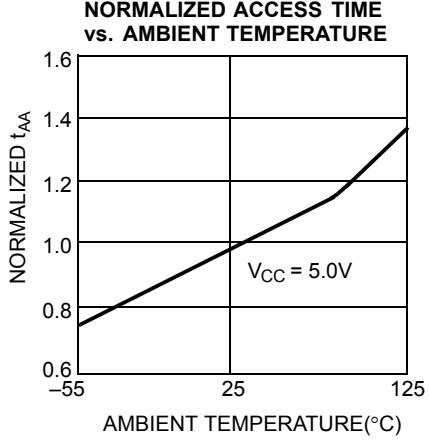
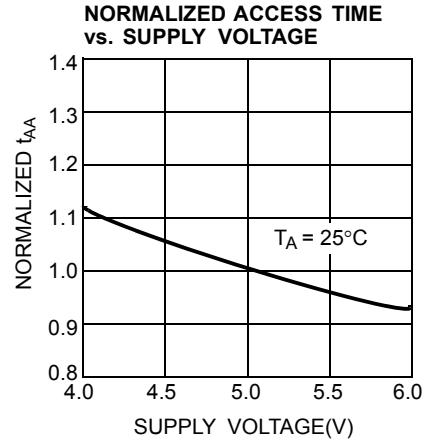
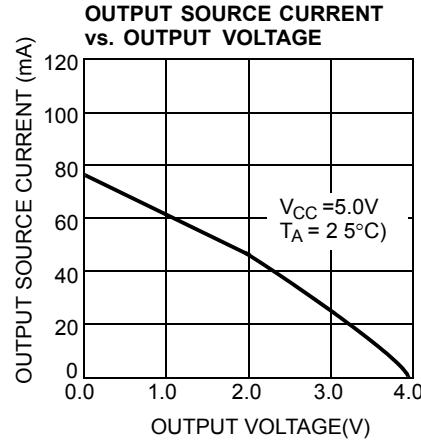
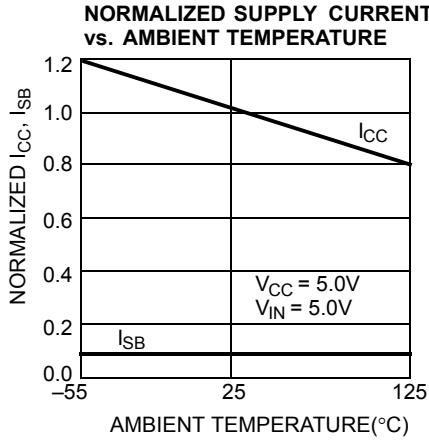
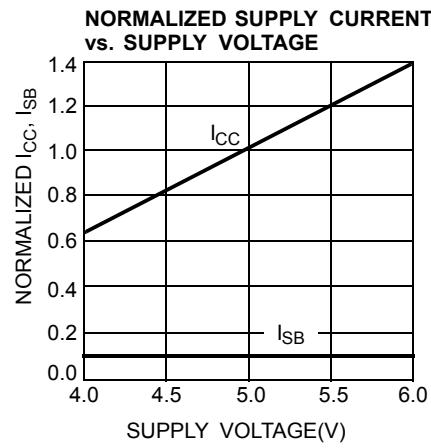


C128A-9

Notes:

12. Data I/O pins enter high-impedance state, as shown, when \overline{OE} is held LOW during write.
13. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
20	CY7C128A-20VXC	51-85030	24-pin Molded SOJ (Pb-free)	Commercial
45	CY7C128A-45PC	51-85013	24-pin (300-Mil) Molded DIP	Commercial

Please contact local sales representative regarding availability of these parts

Package Diagrams

Figure 2. 24-pin (300-Mil) Molded DIP (51-85013)

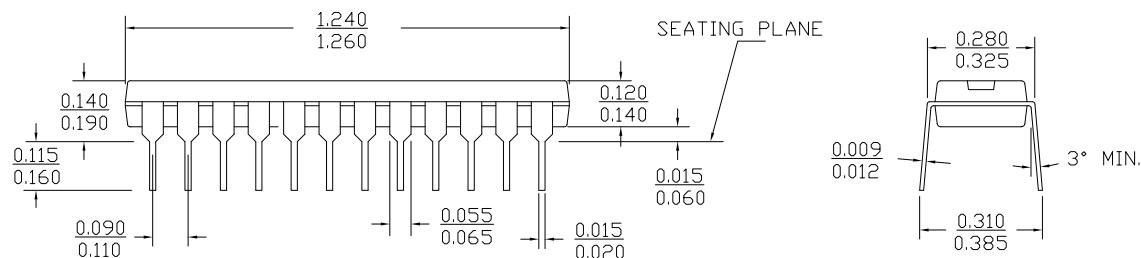
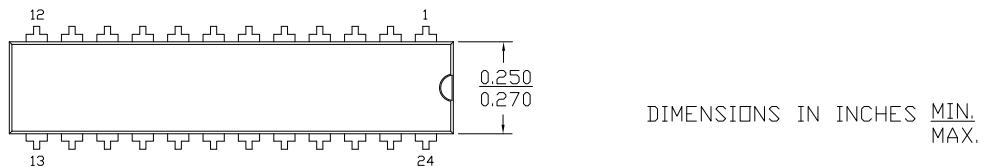
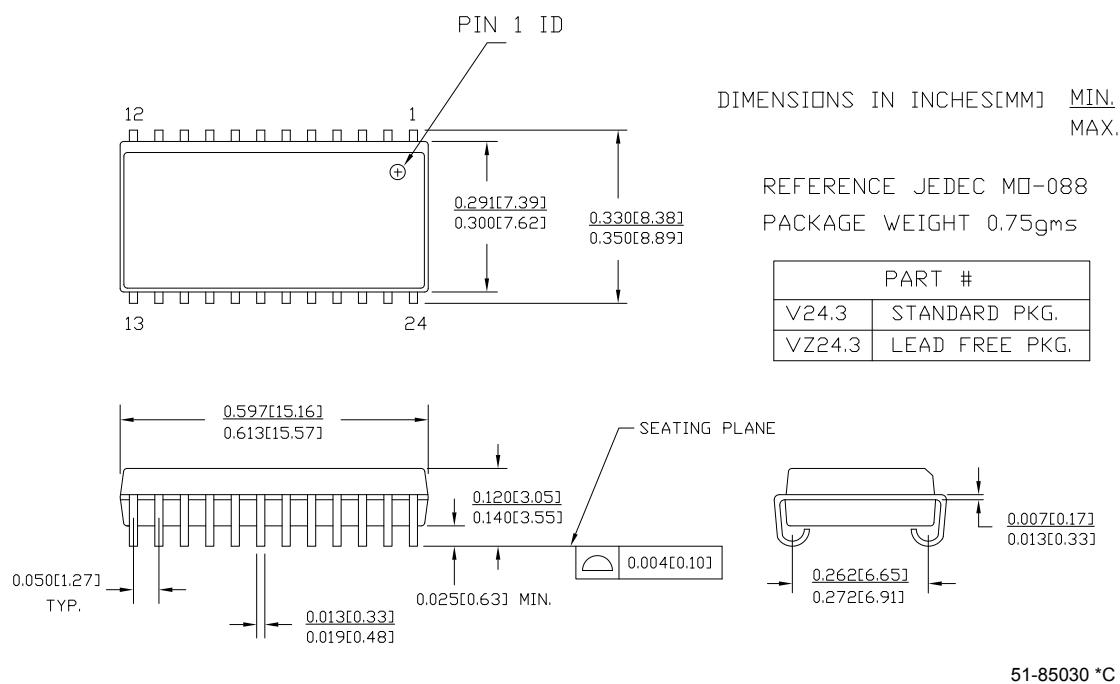


Figure 3. 24-pin (300-Mil) SOJ (51-85030)



51-85030 *C

Document History Page

Document Title: CY7C128A 2K x 8 Static RAM
Document Number: 38-05028

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106814	09/10/01	SZV	Change from Spec number: 38-00094 to 38-05028
*A	493543	See ECN	NXR	Removed 25 ns speed bin Removed Military Operating Range Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated ordering Information Table
*B	2892244	03/19/2010	VKN	Removed 15ns and 35ns speed bin Updated Ordering Information table Updated Package Diagrams (Figure 2 and Figure 3) Added Sales, Solutions, and Legal Information

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