ADVANCE

CYWB02XX Family

West Bridge® Astoria

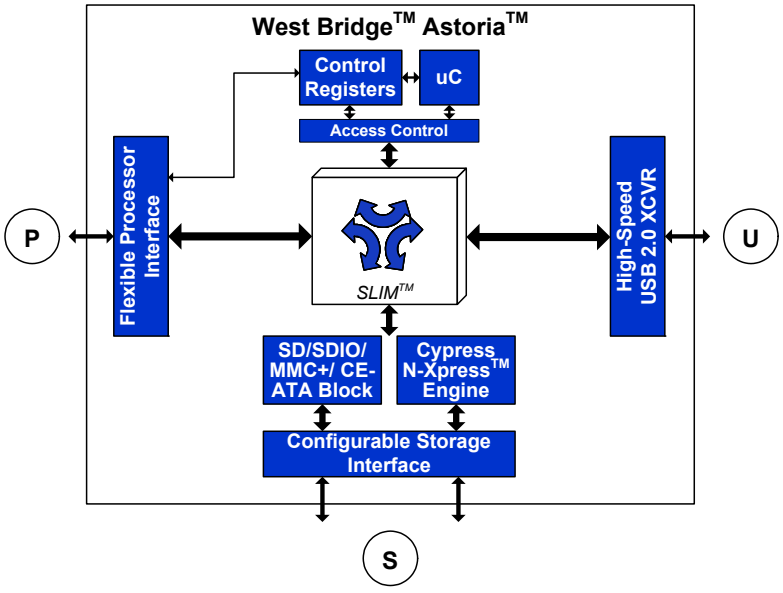
Features

- N-Xpress NAND Controller Technology
  - Interleave up to 16 NANDs with 8 Chip Enables (CE#) for ×8 or ×16 flash devices.
  - 4-bit Error Correction Coding
  - Bad Block Management
  - Static Wear Leveling
- Multimedia Device Support
  - Up to two SD/SDIO/MMC/MMC+/CE-ATA devices
- Simultaneous Link to Independent Multimedia (SLIM®) Architecture, enabling simultaneous and independent Data Paths between the Processor and USB, and between the USB and Mass Storage.
- Fully Backward Compatible (including pin to pin) to Antioch (CYWB0124AB)
- High Speed USB at 480 Mbps
  - USB 2.0 compliant
  - Integrated USB 2.0 transceiver, smart Serial Interface Engine
  - 16 programmable endpoints
- Flexible Processor Interface, which supports:
  - Multiplexing and non-multiplexing address and data interface
  - SRAM interface
  - Pseudo CRAM interface (Antioch Interface)
  - Pseudo NAND Flash interface
  - SPI (slave mode) interface
  - DMA slave support
- Ultra Low Power, 1.8 V Core Operation
- Low Power Modes
- Small Footprint, 6 × 6 mm VFBGA, and WLCSP
- Supports I^2C Boot and Processor Boot
- Selectable Clock Input Frequencies
  - 19.2 MHz, 24 MHz, 26 MHz, and 48 MHz

Applications

- Cellular Phones
- Portable Media Players
- Personal Digital Assistants
- Portable Navigation Devices
- Digital Cameras
- POS Terminals
- Portable Video Recorders

Logic Block Diagram



Functional Overview

The SLIM Architecture

The SLIM architecture enables three different interfaces (P-port, S-port, and U-port) to connect to each other independently.

With this architecture, a device using Astoria is connected to a PC through a USB, without disturbing any of the device functions. The device can still access mass storage when the PC is synchronizing with the main processor.

The SLIM architecture enables new usage models, in which a PC accesses a mass storage device independent of the main processor, or enumerates access to both the mass storage and the main processor at the same time.

In a handset using SLIM architecture, the user can do the following:

- Use the phone as a thumb drive.
- Download media files to the phone with all the functionalities still available on the phone.
- Use the same phone as a modem to connect the PC to the internet.

8051 Microprocessor

The 8051 microprocessor embedded in Astoria does basic transaction management for all transactions between the P-Port, S-Port, and the U-Port. The 8051 does not reside in the data path; it manages the path. The data path is optimized for performance. The 8051 executes firmware that supports NAND, SD, SDIO, MMC+, and CE-ATA devices at the S-Port. For the NAND device, the 8051 firmware follows the Smart Media algorithm to support the following:

- Physical to Logical Management
- ECC Correction support
- Wear Leveling
- NAND Flash bad blocks handling

Configuration and Status Registers

The West Bridge Astoria device includes configuration and status registers that are accessible as memory-mapped registers through the processor interface. The configuration registers enable the system to specify some behaviors of Astoria. For example, it can mask certain status registers from raising an interrupt. The status registers convey the status of Astoria, such as the addresses of buffers for read operations.

Processor Interface (P-Port)

Communication with the external processor is realized through a dedicated processor interface. This interface is configured to support different interface standards. This interface supports multiplexing and non-multiplexing address or data bus in both synchronous and asynchronous pseudo CRAM-mapped, and non-multiplexing address or data asynchronous SRAM-mapped memory accesses. The interface may be configured to pseudo NAND interface to support the processor's NAND interface. In addition, this interface may be configured to support the slave SPI interface. This ensures straightforward electrical communication with the processor, which may have other devices connected on a shared memory bus. Asynchronous accesses can reach a bandwidth of up to 66.7 MBps. Synchronous accesses are performed at 33 MHz across 16 bits for up to 66.7 MBps bandwidth.

The memory address is decoded to access any of the multiple endpoint buffers inside Astoria. These endpoints serve as buffers for data between each pair of ports; for example, between the processor port and the USB port. The processor writes and reads into these buffers through the memory interface.

Access to these buffers is controlled by using a DMA protocol or using an interrupt to the main processor. These two modes are configured by the external processor.

As a DMA slave, Astoria generates a DMA request signal to notify the main processor that a specific buffer is ready to be read from or written to. The external processor monitors this signal and polls Astoria for the specific buffers ready for a read or write operation. It then performs the appropriate read or write operations on the buffer through the processor interface. As a result, the external processor only deals with the buffers to access a multitude of storage devices connected to Astoria.

In the Interrupt mode, Astoria communicates important buffer status changes to the external processor using an interrupt signal. The external processor then polls Astoria for the specific buffers ready for read or write, and it performs the appropriate read or write operations through the processor interface.

USB Interface (U-Port)

In accordance with the USB 2.0 specification, Astoria can operate in both full speed and high speed USB modes. The USB interface consists of the USB transceiver. The USB interface can access and be accessed by both the P-Port and the S-Port.

The Astoria USB interface supports programmable CONTROL/BULK/INTERRUPT/ISOCHRONOUS endpoints.

Mass Storage Support (S-Port)

The S-Port may be configured in three different modes, which simultaneously support the following:

- An SD/SDIO/MMC+/CE-ATA port and a ×8 NAND port
- Two SD/SDIO/MMC+/CE-ATA ports
- Up to eight Chip Enable (CE#) for ×8 or ×16 NAND flash access ports

These configurations are controlled by the 8051 firmware. The 16-bit NAND interface is used only when there is no other mass storage device connected to the S-Port.

N-Xpress NAND Controller (S-Port)

Astoria, as part of its mass storage management functions, can fully manage the SLC and MLC NAND flash devices. The embedded 8051 manages the actual reading and writing of the NAND, along with its required protocols. It performs standard NAND management functions, such as ECC and wear leveling. The Astoria supports single bit ECC for the SLC and 4-bit ECC for MLC NAND flash. SLC NAND flash devices are supported by CYWB0244ABS. CYWB0244ABM supports both SLC and MLC NAND flash devices.

SD/SDIO/MMC+/CE-ATA Port (S-Port)

When Astoria is configured through firmware to support SD/SDIO/MMC+/CE-ATA, this interface supports the following:

- The Multimedia Card System Specification, MMCA Technical Committee, Version 4.1.
- SD Memory Card Specification - Part 1, Physical Layer Specification, SD Group, Version 1.10, October 15, 2004.
- SD Memory Card Specification - Part 1, Physical Layer Specification, SD Group, Version 2.0, May 9, 2006.
- SD Specifications - Part E1 SDIO specification, Version 1.10, August 18, 2004.
- CE-ATA Specification - CE-ATA Digital Protocol, CE-ATA Committee, Version 1.1, September, 2005.

WestBridge Astoria provides support for 1-bit and 4-bit SD and SDIO cards; 1-bit, 4-bit, and 8-bit MMC; MMC+ cards, and CE-ATA drive. For the SD, SDIO, MMC/MMC Plus, and CE-ATA, this block supports one card for one physical bus interface.

Astoria supports SD commands including the multisector program command, which is handled by API.

Table 1. Astoria Pin Assignments

	Pin Name												Pin Description	Power Domain
	Ball #	PCRAM Non Multiplexing	I/O	Addr/Data bus Multiplexing (ADM)	I/O	SRAM	I/O	PNAND	I/O	SPI	I/O			
P Port	J2	CLK (pull low in Asyn mode)	I	CLK (pull low in Async mode)	I	Ext pull low	I	Ext pull low	I	SCK	I		Clock	PVDDQ VGND
	G1	CE#	I	CE#	I	CE#	I	CE#	I	SS#	I		CE# or SPI Slave Select	
	H3	A7	I	Ext pull up	I	A7	I	A7 => 1:SBD A7 => 0: LBD	I	Ext pull up	I		Addr. Bus 7	
	H2	A6	I	SDA	I/O	A6	I	SDA	I/O	SDA	I/O		A6 or I2C data	
	H1	A5	I	SCL	I/O	A5	I	SCL	I/O	SCL	I/O		A5 or I2C clock	
	J3	A4	I	Ext pull up	I	A4	I	WP#	I	Ext pull up	I		A4 or PNAND WP	
	J1	A3	I	A3 = 0 (Ext pull low)	I	A3	I	A3 = 0 (Ext pull low)	I	A3 = 1 (Ext pull up)	I		A3	
	K3	A2	I	A2 = 1 (Ext pull up)	I	A2	I	A2 = 0 (Ext pull low)	I	A2 = 0 (Ext pull low)	I		A2	
	K2	A1	I	Ext pull up	I	A1	I	RB#	O	Ext pull up	I		A1 or PNAND R/B#	
	K1	A0	I	Ext pull up	I	A0	I	CLE	I	Ext pull up	I		A0 or PNAND CLE	
	G2	DQ[15]	I/O	AD[15]	I/O	DQ[15]	I/O	I/O[15]	I/O	Ext pull up	I		D15, AD15, or IO15	
	G3	DQ[14]	I/O	AD[14]	I/O	DQ[14]	I/O	I/O[14]	I/O	Ext pull up	I		D14, AD14, or IO14	
	F1	DQ[13]	I/O	AD[13]	I/O	DQ[13]	I/O	I/O[13]	I/O	Ext pull up	I		D13, AD13, or IO13	
	F2	DQ[12]	I/O	AD[12]	I/O	DQ[12]	I/O	I/O[12]	I/O	Ext pull up	I		D12, AD12, or IO12	
	F3	DQ[11]	I/O	AD[11]	I/O	DQ[11]	I/O	I/O[11]	I/O	Ext pull up	I		D11, AD11, or IO11	
	E1	DQ[10]	I/O	AD[10]	I/O	DQ[10]	I/O	I/O[10]	I/O	Ext pull up	I		D10, AD10, or IO10	
	E2	DQ[9]	I/O	AD[9]	I/O	DQ[9]	I/O	I/O[9]	I/O	Ext pull up	I		D9, AD9, or IO9	
	E3	DQ[8]	I/O	AD[8]	I/O	DQ[8]	I/O	I/O[8]	I/O	Ext pull up	I		D8, AD8, or IO8	
	D1	DQ[7]	I/O	AD[7]	I/O	DQ[7]	I/O	I/O[7]	I/O	Ext pull up	I		D7, AD7, or IO7	
	D2	DQ[6]	I/O	AD[6]	I/O	DQ[6]	I/O	I/O[6]	I/O	Ext pull up	I		D6, AD6, or IO6	
	D3	DQ[5]	I/O	AD[5]	I/O	DQ[5]	I/O	I/O[5]	I/O	Ext pull up	I		D5, AD5, or IO5	
	C1	DQ[4]	I/O	AD[4]	I/O	DQ[4]	I/O	I/O[4]	I/O	Ext pull up	I		D4, AD4, or IO4	
	C2	DQ[3]	I/O	AD[3]	I/O	DQ[3]	I/O	I/O[3]	I/O	Ext pull up	I		D3, AD3, or IO3	
	C3	DQ[2]	I/O	AD[2]	I/O	DQ[2]	I/O	I/O[2]	I/O	Ext pull up	I		D2, AD2, or IO2	
	B1	DQ[1]	I/O	AD[1]	I/O	DQ[1]	I/O	I/O[1]	I/O	SDO	O		SPI SDO, AD1or D1	
	B2	DQ[0]	I/O	AD[0]	I/O	DQ[0]	I/O	I/O[0]	I/O	SDI	I		SPI SDI, AD0, or D0	
	A1	ADV#	I	ADV#	I		I	ALE	I	Ext pull up	I		Address Valid	
	B3	OE#	I	OE#	I	OE#	I	RE#	I	Ext pull up	I		Output Enable	
	A2	WE#	I	WE#	I	WE#	I	WE#	I	Ext pull up	I		WE#	
DRQ & Int	A3	INT#	O	INT#	O	INT#	O	INT#	O	SINT#	O		INT Request	GVDDQ VGND
	A4	DRQ#	O	DRQ#	O	DRQ#	O	DRQ#	O	N/C	O		DMA Request	
	B4	DACK#	I	DACK#	I	DACK#	I	DACK#	I	Ext pull up	I		DMA Acknowledgement	
U-Port	A5	D+									I/O/Z		USB D+	UVDDQ UVSSQ
	A6	D-									I/O/Z		USB D-	
	A7	SWD+									I/O/Z		USB Switch DP	
	C6	SWD-									I/O/Z		USB Switch DM	

Table 1. Astoria Pin Assignments *(continued)*

	Pin Name													Pin Description	Power Domain
	Ball #	PCRAM Non Multiplexing	I/O	Addr/Data bus Multiplexing (ADM)	I/O	SRAM	I/O	PNAND	I/O	SPI			I/O		
		SDIO & NAND Configuration	I/O	NAND only Configuration	I/O	Double SDIO Configuration	I/O	NAND & GPIO Configuration	I/O	SDIO & GPIO Configuration	I/O	GPIO only Configuration	I/O		
S-Port	G9	SD_D[7]	I/O	NAND_IO[15] or PD[7] (GPIO)	I/O	SD_D[7:0]	I/O	NAND_IO[15] or PD[7] (GPIO)	I/O	SD_D[7:0]	I/O	PD[7:0] (GPIO)	I/O	SD Data or NAND I/O or GPIO	SSVD-DQ VGND
	G10	SD_D[6]	I/O	NAND_IO[14] or PD[6] (GPIO)	I/O	SD_D[6]	I/O	NAND_IO[14] or PD[6] (GPIO)	I/O	SD_D[6]	I/O	PD[6] (GPIO)	I/O	SD Data or NAND I/O or GPIO	
	F9	SD_D[5]	I/O	NAND_IO[13] or PD[5] (GPIO)	I/O	SD_D[5]	I/O	NAND_IO[13] or PD[5] (GPIO)	I/O	SD_D[5]	I/O	PD[5] (GPIO)	I/O	SD Data or NAND I/O or GPIO	
	F10	SD_D[4]	I/O	NAND_IO[12] or PD[4] (GPIO)	I/O	SD_D[4]	I/O	NAND_IO[12] or PD[4] (GPIO)	I/O	SD_D[4]	I/O	PD[4] (GPIO)	I/O	SD Data or NAND I/O or GPIO	
	E9	SD_D[3]	I/O	NAND_IO[11] or PD[3] (GPIO)	I/O	SD_D[3]	I/O	NAND_IO[11] or PD[3] (GPIO)	I/O	SD_D[3]	I/O	PD[3] (GPIO)	I/O	SD Data or NAND I/O or GPIO	
	E10	SD_D[2]	I/O	NAND_IO[10] or PD[2] (GPIO)	I/O	SD_D[2]	I/O	NAND_IO[10] or PD[2] (GPIO)	I/O	SD_D[2]	I/O	PD[2] (GPIO)	I/O	SD Data or NAND I/O or GPIO	
	D9	SD_D[1]	I/O	NAND_IO[9] or PD[1] (GPIO)	I/O	SD_D[1]	I/O	NAND_IO[9] or PD[1] (GPIO)	I/O	SD_D[1]	I/O	PD[1] (GPIO)	I/O	SD Data or NAND I/O or GPIO	
	D10	SD_D[0]	I/O	NAND_IO[8] or PD[0] (GPIO)	I/O	SD_D[0]	I/O	NAND_IO[8] or PD[0] (GPIO)	I/O	SD_D[0]	I/O	PD[0] (GPIO)	I/O	SD Data or NAND I/O or GPIO	
	F8	SD_CLK	O	NAND_CE8# or NAND_R/B4#	O I	SD_CLK	O	PC-7 (GPIO) or NAND_CE8# or NAND_R/B4#	I/O O I	SD_CLK		PC-7 (GPIO)	I/O	SD Clock, NAND CE8# or R/B4#	
	G8	SD_CMD	I/O	NAND_CE7# or NAND_R/B3#	O I	SD_CMD	I/O	PC-3 (GPIO) or NAND_CE7# or NAND_R/B3#	I/O O I	SD_CMD	I/O	PC-3 (GPIO)	I/O	SD CMD, NAND CE7# or R/B3#	
	H8	SD_POW	O	NAND_CE6#	O	SD_POW		PC-6 (GPIO) or NAND_CE6#	I/O O	SD_POW		PC-6 (GPIO)	I/O	SD POW or NAND CE6#	
	H10	SD_WP	I	NAND_CE5#	O	SD_WP	I	PC-5 (GPIO) or NAND_CE5#	I/O	SD_WP	I	N/C	I	SD WP, GPIO, or NAND CE5#	
	K7	NAND_IO[7]	I/O	NAND_IO[7]	I/O	SD2_D[7]	I/O	NAND_IO[7]	O	PB[7] (GPIO)	I/O	PB[7] (GPIO)	I/O	NAND Lower I/O bus	SNVD-DQ VGND
	K8	NAND_IO[6]	I/O	NAND_IO[6]	I/O	SD2_D[6]	I/O	NAND_IO[6]	O	PB[6] (GPIO)	I/O	PB[6] (GPIO)	I/O	NAND Lower I/O bus	
	J8	NAND_IO[5]	I/O	NAND_IO[5]	I/O	SD2_D[5]	I/O	NAND_IO[5]	O	PB[5] (GPIO)	I/O	PB[5] (GPIO)	I/O	NAND Lower I/O bus	
	K9	NAND_IO[4]	I/O	NAND_IO[4]	I/O	SD2_D[4]	I/O	NAND_IO[4]	O	PB[4] (GPIO)	I/O	PB[4] (GPIO)	I/O	NAND Lower I/O bus	
	J9	NAND_IO[3]	I/O	NAND_IO[3]	I/O	SD2_D[3]	I/O	NAND_IO[3]	O	PB[3] (GPIO)	I/O	PB[3] (GPIO)	I/O	NAND Lower I/O bus	
	H9	NAND_IO[2]	I/O	NAND_IO[2]	I/O	SD2_D[2]	I/O	NAND_IO[2]	O	PB[2] (GPIO)	I/O	PB[2] (GPIO)	I/O	NAND Lower I/O bus	
	K10	NAND_IO[1]	I/O	NAND_IO[1]	I/O	SD2_D[1]	I/O	NAND_IO[1]	O	PB[1] (GPIO)	I/O	PB[1] (GPIO)	I/O	NAND Lower I/O bus	
	J10	NAND_IO[0]	I/O	NAND_IO[0]	I/O	SD2_D[0]	I/O	NAND_IO[0]	O	PB[0] (GPIO)	I/O	PB[0] (GPIO)	I/O	NAND Lower I/O bus	
	K6	NAND_CLE	O	NAND_CLE	O	SD2_CLK	O	NAND_CLE	O	PA-6 (GPIO)	I/O	PA-6 (GPIO)	I/O	CMD Latch Enable	
	J6	NAND_ALE	O	NAND_ALE	O	SD2_CMD	I/O	NAND_ALE	O	PA-7 (GPIO)	I/O	PA-7 (GPIO)	I/O	Address Latch Enable	
	J5	NAND_CE#	O	NAND_CE#	O	SD2_POW	O	NAND_CE#	O	PC-0 (GPIO)	I/O	PC-0 (GPIO)	I/O	Chip Enable	
	K4	NAND_RE#	O	NAND_RE#	O	N/C	O	NAND_RE#	O	N/C	O	N/C	O	Read Enable	
	H6	NAND_WE#	O	NAND_WE#	O	N/C	O	NAND_WE#	O	N/C	O	N/C	O	Write Enable	
	J7	NAND_WP#	O	NAND_WP#	O	PA-5 (GPIO)	I/O	NAND_WP#	I	PA-5 (GPIO)	I/O	PA-5 (GPIO)	I/O	Write Protect	
	J4	NAND_R/B#	I	NAND_R/B#	I	N/C	I	NAND_R/B#	I	N/C	I	N/C	I	Ready/Busy	
	K5	NAND_CE2#	O	NAND_CE2#	O	SD2_WP	O	NAND_CE2#	O	PC-2 (GPIO)	I/O	PC-2 (GPIO)	I/O	Chip Enable 2	

Table 1. Astoria Pin Assignments *(continued)*

	Pin Name														Pin Description	Power Domain
	Ball #	PCRAM Non Multiplexing	I/O	Addr/Data bus Multiplexing (ADM)	I/O	SRAM	I/O	PNAND	I/O	SPI				I/O		
Other	B10	RESETOUT or NAND_R/B2#	O I	NAND_R/B2#	I	RESETOUT	O	RESETOUT or NAND_R/B2#	0 I	RESETOUT	O	RESETOUT		O	RESETOUT or NAND R/B2#	GVDDQ VGND
	C9	PC-5 (GPIO[1]) or NAND_CE3#	I/O O	NAND_CE3#	O	PC-5 (GPIO[1]) or SD2_CD	I/O I	PC-5 (GPIO[1]) or NAND_CE3#	I/O O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])		I/O	GPIO, SD2 CD, or NAND CE3#	
	D8	PC-4 (GPIO[0]) or SD_CD or NAND_CE4#	I/O I O	NAND_CE4#	O	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0]) or NAND_CE4#	I/O O	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0])		I/O	GPIO, SD1 CD, or NAND CE4#	
Conf	C10	RESET#												I	RESET	
	C7	WAKEUP												I	Wake Up Signal	
	C5	XTALSLC[1]												I	Clock Select 1	GVDDQ VGND
	C4	XTALSLC[0]													Clock Select 0	
	E8	TEST[2]												I	Test Cfg 2	
	C8	TEST[1]													Test Cfg 1	
	D7	TEST[0]													Test Cfg 0	
Clock	A8	XTALIN												I	Crystal/Clock IN	XVDDQ VGND
	B8	XTALOUT												O	Crystal Out	
Power	D4 H4	PVDDQ												Power	Processor I/F VDD	
	H5	SNVDDQ												Power	NAND VDD	
	B5	UVDDQ												Power	USB VDD	
	H7	SSVDDQ												Power	SDIO VDD	
	D6	GVDDQ												Power	Misc I/O VDD	
	B9	AVDDQ												Power	Analog VDD	
	B7	XVDDQ												Power	Crystal VDD	
	D5, G4, G5, G6, G7, F7	VDD												Power	Core VDD	
	A10	VDD33												Power	Independent 3.3V	
	B6	UVSSQ												Power	USB GND	
	A9	AVSSQ												Power	Analog GND	
	E4, E5, E6, E7, F4, F5, F6	VGND												Power	Core GND	

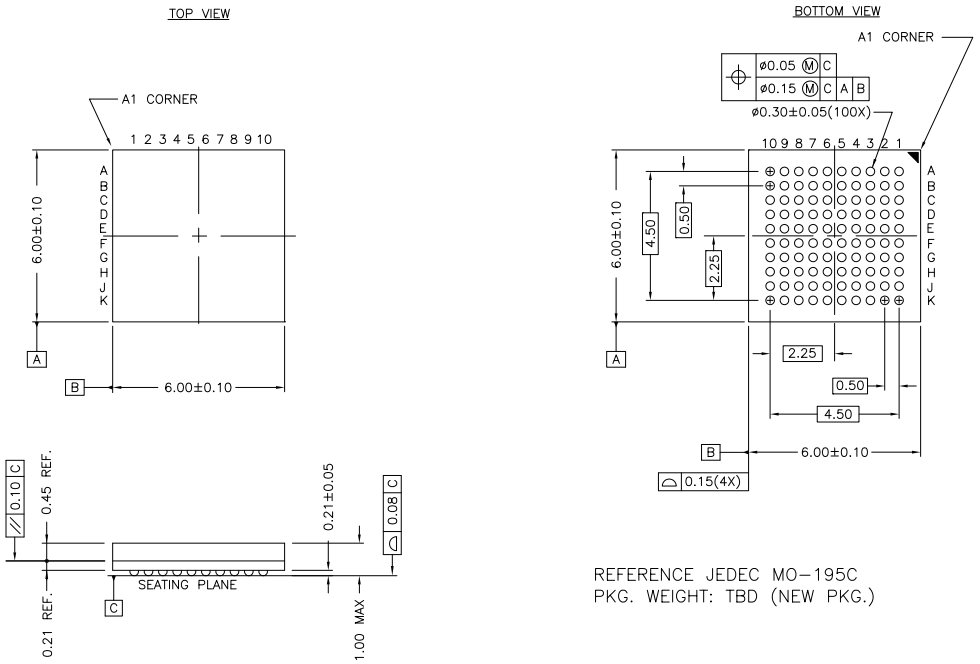
Ordering Information

Astoria provides many options with multiple ordering part numbers as shown in the following table:

Ordering Code	Package Type	Optional Features				Clock Input Frequencies (MHz)
		FlexBoot	USB Switch	Turbo MTP	SLC NAND Flash	
CYWB0224ABS-BVXI	100 VFBGA – Pb-free				√	19.2, 24, 26, 48
CYWB0225ABS-BVXI	100 VFBGA – Pb-free			√	√	19.2, 24, 26, 48
CYWB0226ABS-BVXI	100 VFBGA – Pb-free		√		√	19.2, 24, 26, 48
CYWB0227ABS-BVXI	100 VFBGA – Pb-free		√	√	√	19.2, 24, 26, 48
CYWB0228ABS-BVXI	100 VFBGA – Pb-free	√			√	19.2, 24, 26, 48
CYWB0229ABS-BVXI	100 VFBGA – Pb-free	√		√	√	19.2, 24, 26, 48
CYWB0230ABS-BVXI	100 VFBGA – Pb-free	√	√		√	19.2, 24, 26, 48
CYWB0231ABS-BVXI	100 VFBGA – Pb-free	√	√	√	√	19.2, 24, 26, 48
CYWB0224ABSX-FDXI	WLCSP – Pb-free Contact Sales for more info				√	19.2, 26
CYWB0225ABSX-FDXI	WLCSP – Pb-free Contact Sales for more info			√	√	19.2, 26
CYWB0226ABSX-FDXI	WLCSP – Pb-free Contact Sales for more info		√		√	19.2, 26
CYWB0227ABSX-FDXI	WLCSP – Pb-free Contact Sales for more info		√	√	√	19.2, 26
CYWB0228ABSX-FDXI	WLCSP – Pb-free Contact Sales for more info	√			√	19.2, 26
CYWB0229ABSX-FDXI	WLCSP – Pb-free Contact Sales for more info	√		√	√	19.2, 26
CYWB0230ABSX-FDXI	WLCSP – Pb-free Contact Sales for more info	√	√		√	19.2, 26
CYWB0231ABSX-FDXI	WLCSP – Pb-free Contact Sales for more info	√	√	√	√	19.2, 26
CYWB0220ABSX2-FDXI	WLCSP – Pb-free Contact Sales for more info		√		√ **(SD only)**	26

Package Diagram

Figure 1. 100 VFBGA (6 × 6 × 1.0 mm) BZ100A



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Document History Page

Document Title: CYWB02XX Family West Bridge® Astoria Document Number: 001-11710				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	567055	See ECN	VSO	New data sheet
*A	1830226	See ECN	VSO/AESA	In the Feature list, adding the bullets of “N-Xpress Controller Technology” and “Multimedia Device Support” In the Feature list, removed the bullet of “Mass Storage device support” Update the bullet of Application Update Logic Block Diagram. Updated the section of “NAND Port” to N-Xpress NAND Controller” Updated the pin Assignment Table Fix the typo of VGAN in pin Assignment Table
*B	2764148	09/15/09	OGC/AESA	Added mention of WLCSP package Adding new BGA pin list extracted from 001-13805 data sheet. Changed part number in title to CYWB02XX
*C	2767923	09/23/09	OGC/AESA	Post to External Web
*D	3126447	01/03/2010	ESH	Updated Package Diagram. Updated in new template.

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