

Precision CMOS Analog Switches

DESCRIPTION

The DG417, DG418, DG419 monolithic CMOS analog switches were designed to provide high performance switching of analog signals. Combining low power, low leakages, high speed, low on-resistance and small physical size, the DG417 series is ideally suited for portable and battery powered industrial and military applications requiring high performance and efficient use of board space.

To achieve high-voltage ratings and superior switching performance, the DG417 series is built on Vishay Siliconix's high voltage silicon gate (HVSG) process. Break-before-make is guaranteed for the DG419, which is an SPDT configuration. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

The DG417 and DG418 respond to opposite control logic levels as shown in the Truth Table.

FEATURES

- ± 15 V analog signal range
- On-resistance - $R_{DS(on)}$: 20 Ω
- Fast switching action - t_{ON} : 100 ns
- Ultra low power requirements - P_D : 35 nW
- TTL and CMOS compatible
- MiniDIP and SOIC packaging
- 44 V supply max. rating
- 44 V supply max. rating
- Compliant to RoHS directive 2002/95/EC



Available
RoHS*
COMPLIANT

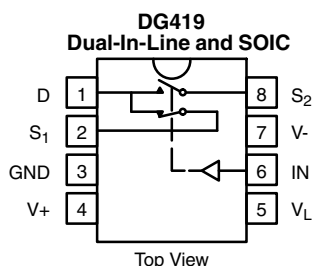
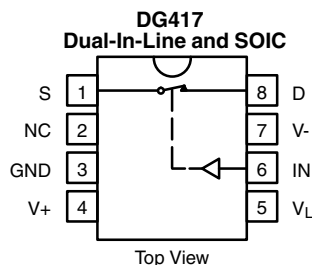
BENEFITS

- Wide dynamic range
- Low signal errors and distortion
- Break-before-make switching action
- Simple interfacing
- Reduced board space
- Improved reliability

APPLICATIONS

- Precision test equipment
- Precision instrumentation
- Battery powered systems
- Sample-and-hold circuits
- Military radios
- Guidance and control systems
- Hard disk drives

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	DG417	DG418
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

TRUTH TABLE DG419

Logic	SW ₁	SW ₂
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

* Pb containing terminations are not RoHS compliant, exemptions may apply

ORDERING INFORMATION		
Temp. Range	Package	Part Number
DG417, DG418		
- 40 °C to 85 °C	8-Pin Plastic MiniDIP	DG417DJ DG417DJ-E3
		DG418DJ DG418DJ-E3
	8-Pin Narrow SOIC	DG417DY DG417DY-E3 DG417DY-T1 DG417DY-T1-E3
		DG418DY DG418DY-E3 DG418DY-T1 DG418DY-T1-E3
DG419		
- 40 °C to 85 °C	8-Pin Plastic MiniDIP	DG419DJ DG419DJ-E3
	8-Pin Narrow SOIC	DG419DY DG419DY-E3 DG419DY-T1 DG419DY-T1-E3

ABSOLUTE MAXIMUM RATINGS			
Parameter (Voltages referenced to V-)		Limit	Unit
V+		44	V
GND		25	
V _L		(GND - 0.3) to (V+) + 0.3	
Digital Inputs ^a , V _S , V _D		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Current , (Any Terminal) Continuous		30	mA
Current, S or D (Pulsed at 1 ms, 10 % Duty Cycle)		100	
Storage Temperature	(AK Suffix)	- 65 to 150	°C
	(DJ, DY Suffix)	- 65 to 125	
Power Dissipation (Package) ^b	8-Pin Plastic MiniDIP ^c	400	mW
	8-Pin Narrow SOIC ^d	400	
	8-Pin CerDIP ^e	600	

Notes:

- Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC board.
- Derate 6 mW/°C above 75 °C.
- Derate 6.5 mW/°C above 75 °C.
- Derate 12 mW/°C above 75 °C.

SPECIFICATIONS ^a										
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 15 V, V ₋ = - 15 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f		Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
						Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Dynamic Characteristics										
Source Off Capacitance	C _{S(off)}	f = 1 MHz, V _S = 0 V		Room	8					pF
Drain Off Capacitance	C _{D(off)}			DG417 DG418	Room	8				
Channel On Capacitance	C _{D(on)}	f = 1 MHz, V _S = 0 V	DG417 DG418	Room	30					
			DG419	Room	35					
Power Supplies										
Positive Supply Current	I ₊	V ₊ = 16.5 V, V ₋ = - 16.5 V V _{IN} = 0 or 5 V		Room Full	0.001		1 5		1 5	μA
Negative Supply Current	I ₋			Room Full	- 0.001	- 1 - 5		- 1 - 5		
Logic Supply Current	I _L			Room Full	0.001		1 5		1 5	
Ground Current	I _{GND}			Room Full	- 0.0001	- 1 - 5		- 1 - 5		

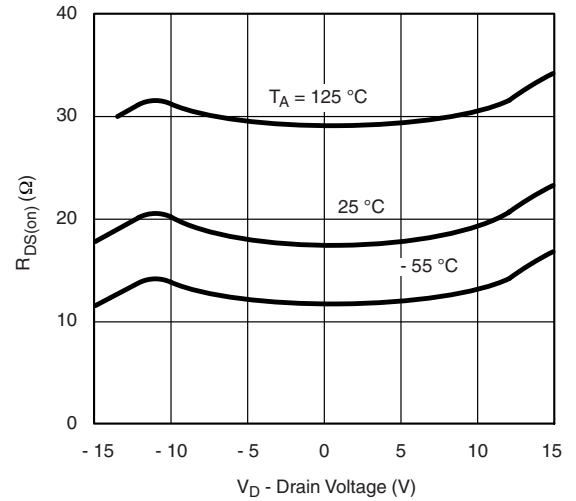
SPECIFICATIONS ^a for Unipolar Supplies									
Parameter	Symbol	Test Conditions Unless Otherwise Specified V ₊ = 12 V, V ₋ = 0 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f	Temp. ^b	Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit
					Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	R _{DS(on)}	I _S = - 10 mA, V _D = 3.8 V V ₊ = 10.8 V	Room	40					Ω
Dynamic Characteristics									
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF, V _S = 8 V See Switching Time Test Circuit	Room	110					ns
Turn-Off Time	t _{OFF}		Room	40					
Break-Before-Make Time Delay	t _D	DG419 Only R _L = 300 Ω, C _L = 35 pF	Room	60					
Charge Injection	Q	C _L = 10 nF, V _{gen} = 0 V, R _{gen} = 0 Ω	Room	5					pC
Power Supplies									
Positive Supply Current	I ₊	V ₊ = 13.2 V, V _L = 5.25 V V _{IN} = 0 or 5 V	Room	0.001					μA
Negative Supply Current	I ₋		Room	- 0.001					
Logic Supply Current	I _L		Room	0.001					
Ground Current	I _{GND}		Room	- 0.001					

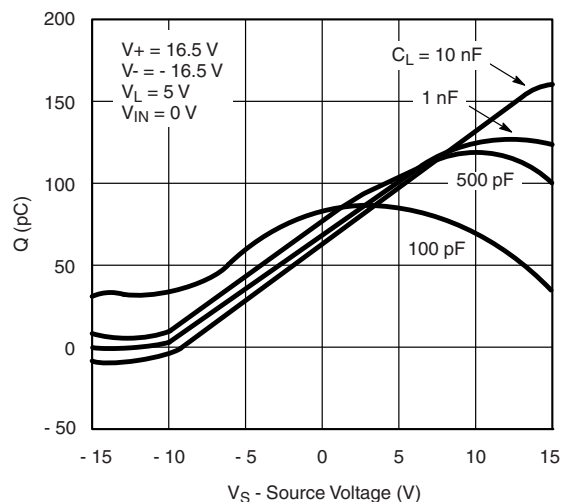
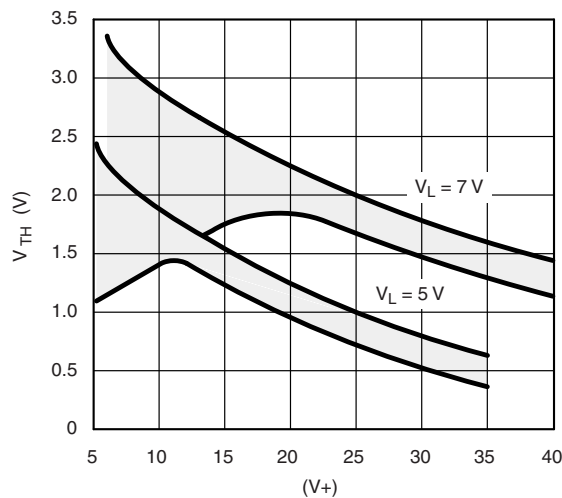
Notes:

- Refer to Process Option Flowchart.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

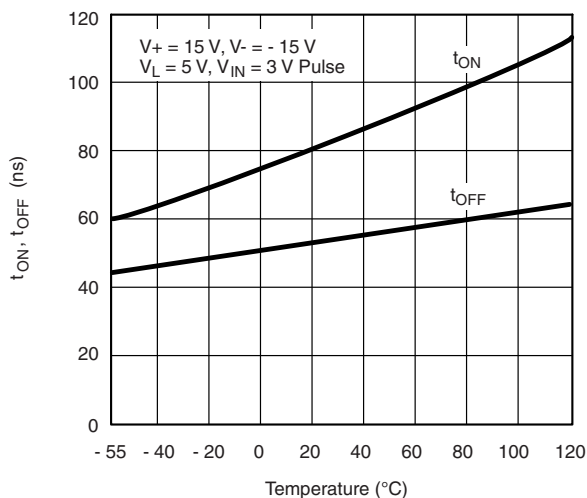
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

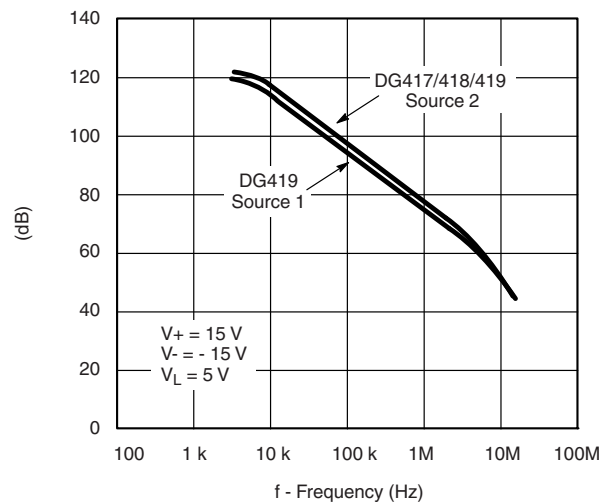
 $R_{DS(on)}$ vs. V_D and Supply Voltage

 $R_{DS(on)}$ vs. Temperature

Leakage Currents vs. Analog Voltage

Drain Charge Injection

Input Switching Threshold vs. Supply Voltages

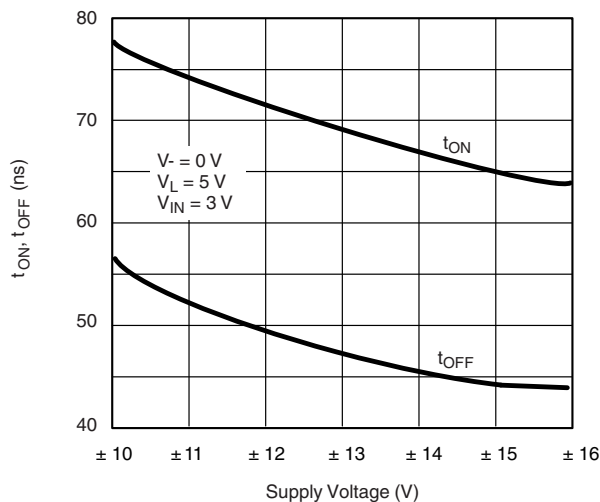
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



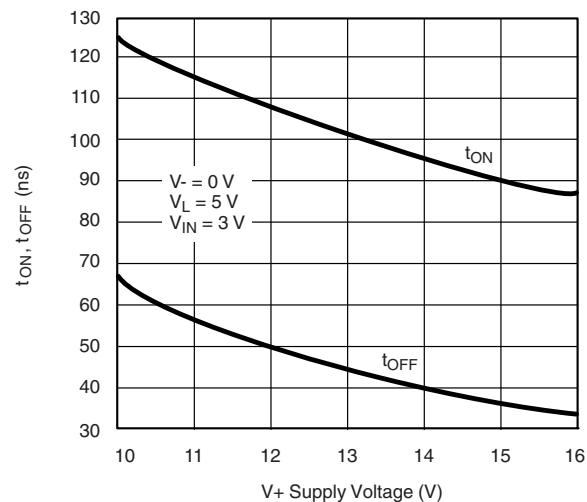
Switching Time vs. Temperature



Crosstalk and Off Isolation vs. Frequency



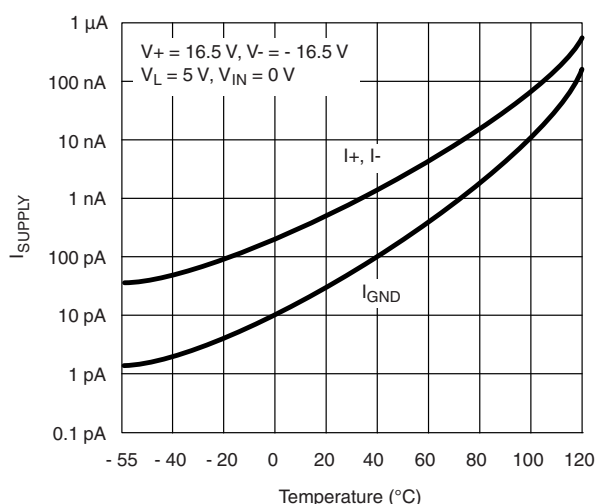
Switching Time vs. Supply Voltages



Switching Time vs. V_+



Power Supply Currents vs. Switching Frequency



Supply Current vs. Temperature

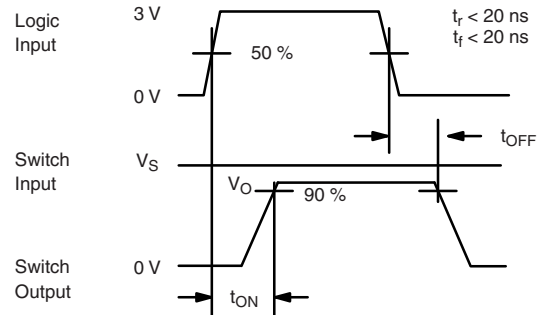
TEST CIRCUITS

V_O is the steady state output with the switch on.



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 2. Switching Time (DG417, DG418)



C_L (includes fixture and stray capacitance)



Figure 3. Break-Before-Make (DG419)



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



Figure 4. Transition Time (DG419)

TEST CIRCUITS

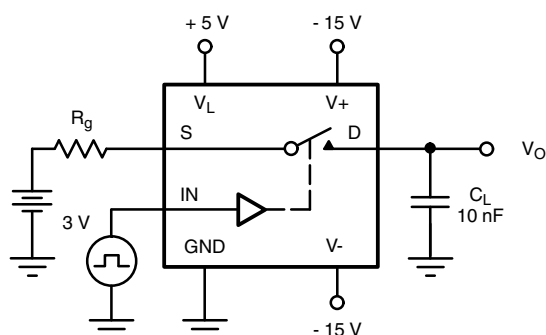


Figure 5. Charge Injection

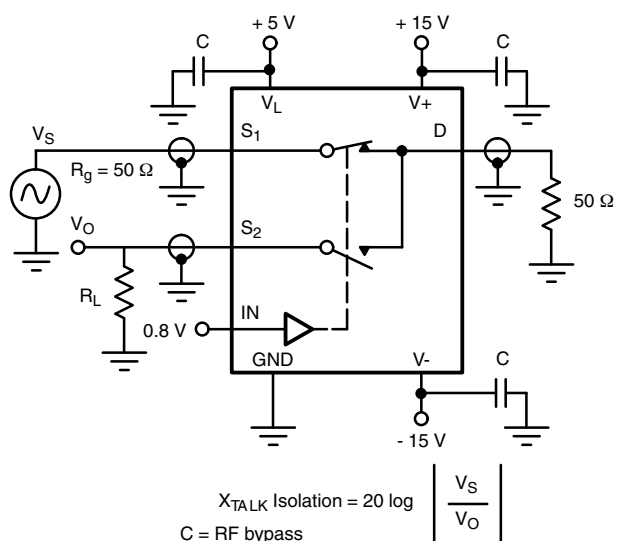
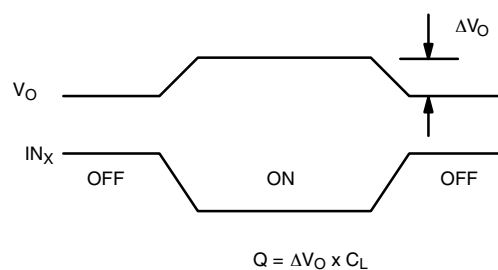


Figure 6. Crosstalk (DG419)

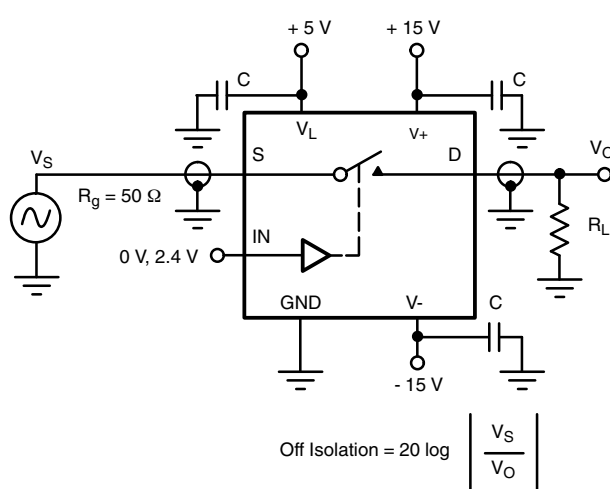


Figure 7. Off Isolation

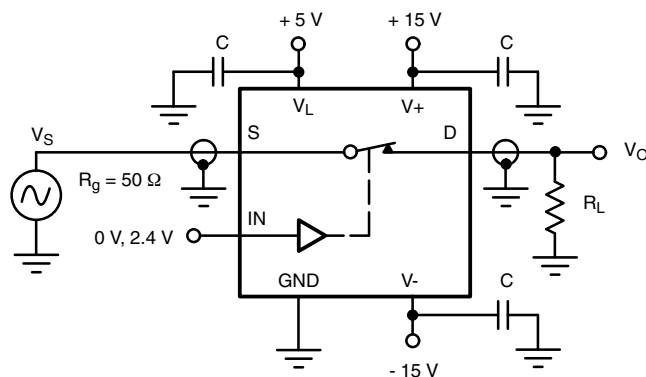


Figure 8. Insertion Loss

TEST CIRCUITS

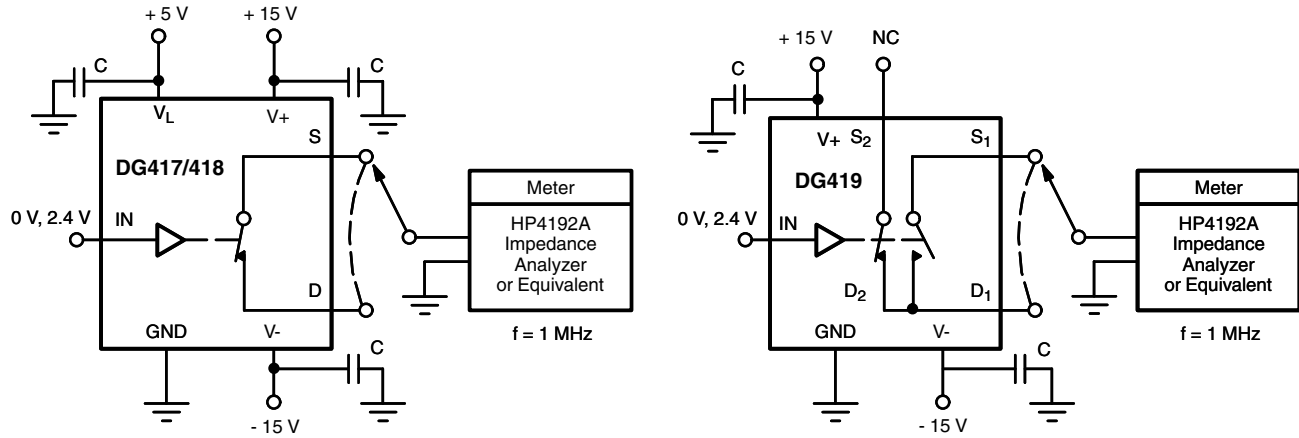


Figure 9. Source/Drain Capacitances

APPLICATIONS

Switched Signal Powers Analog Switch

The analog switch in Figure 10 derives power from its input signal, provided the input signal amplitude exceeds 4 V and its frequency exceeds 1 kHz.

This circuit is useful when signals have to be routed to either of two remote loads. Only three conductors are required: one for the signal to be switched, one for the control signal and a common return.

A positive input pulse turns on the clamping diode D_1 and charges C_1 . The charge stored on C_1 is used to power the chip; operation is satisfactory because the switch requires less than $1 \mu\text{A}$ of stand-by supply current. Loading of the signal source is imperceptible. The DG419's on-resistance is a low 100Ω for a 5 V input signal.

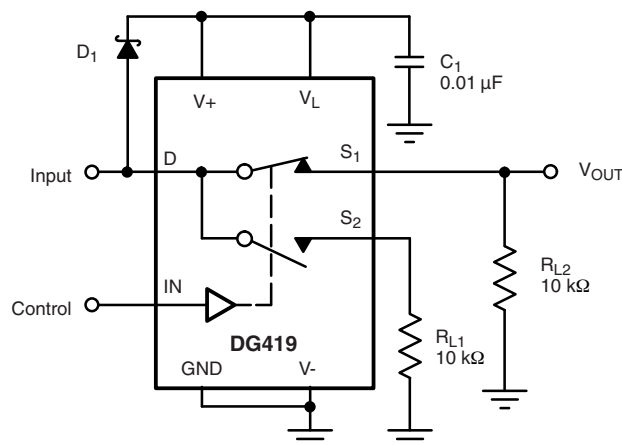


Figure 10. Switched Signal Powers Remote SPDT Analog Switch

APPLICATIONS

Micropower UPS Transfer Switch

When V_{CC} drops to 3.3 V, the DG417 changes states, closing SW_1 and connecting the backup cell, as shown in Figure 10. D_1 prevents current from leaking back towards the rest of the circuit. Current consumption by the CMOS analog switch is around 100 pA; this ensures that most of the power available is applied to the memory, where it is really needed. In the stand-by mode, hundreds of A are sufficient to retain memory data.

When the 5 V supply comes back up, the resistor divider senses the presence of at least 3.5 V, and causes a new change of state in the analog switch, restoring normal operation.

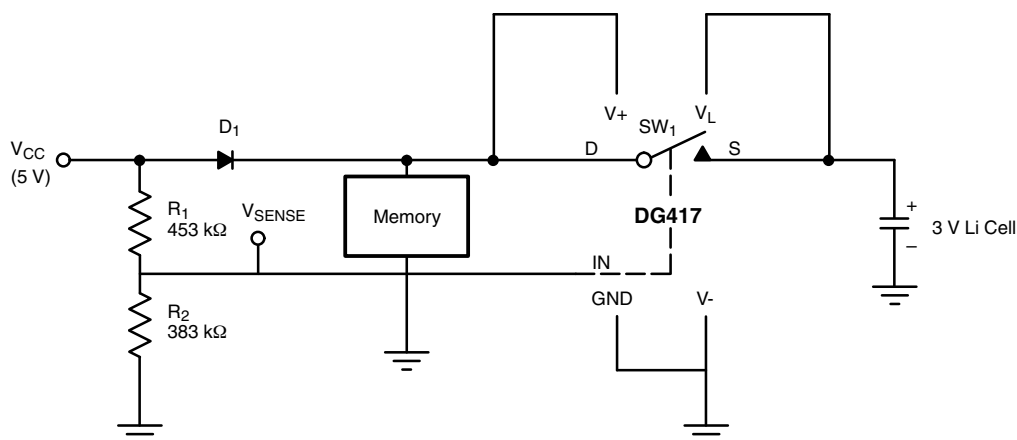


Figure 11. Micropower UPS Circuit

Programmable Gain Amplifier

The DG419, as shown in figure 11, allows accurate gain selection in a small package. Switching into virtual ground reduces distortion caused by $R_{DS(on)}$ variation as a function of analog signal amplitude.

GaAs FET Driver

The DG419, as shown in figure 12 may be used as a GaAs FET driver. It translates a TTL control signal into - 8 V, 0 V level outputs to drive the gate.

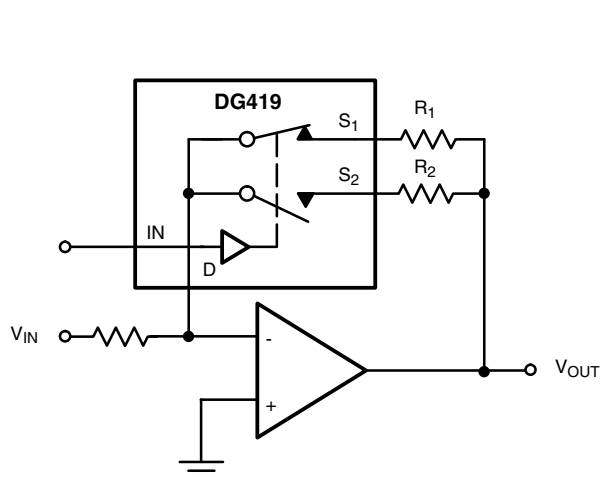


Figure 12. Programmable Gain Amplifier

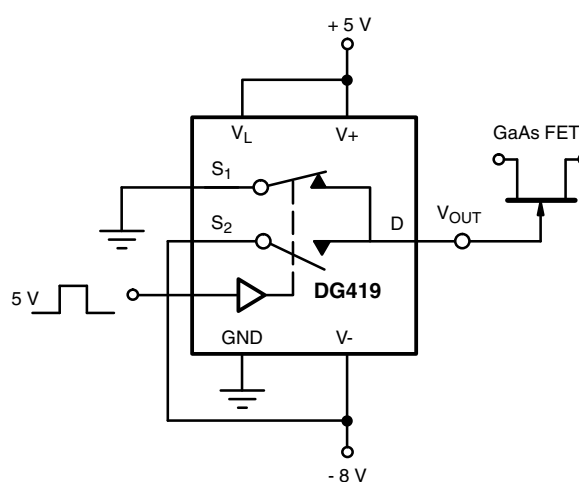


Figure 13. GaAs FET Driver

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SOIC (NARROW): 8-LEAD

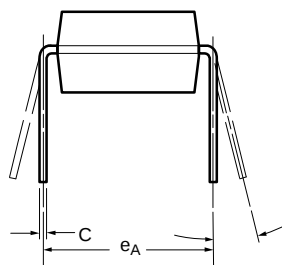
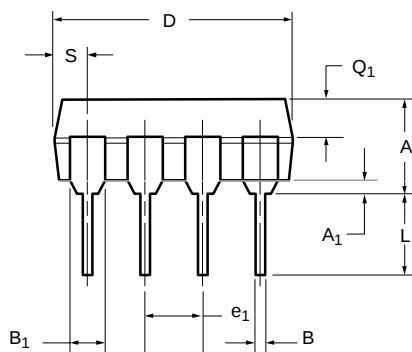
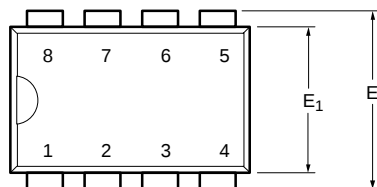
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				



PDIP: 8-LEAD



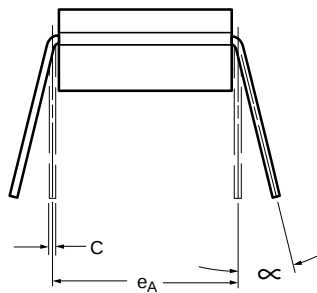
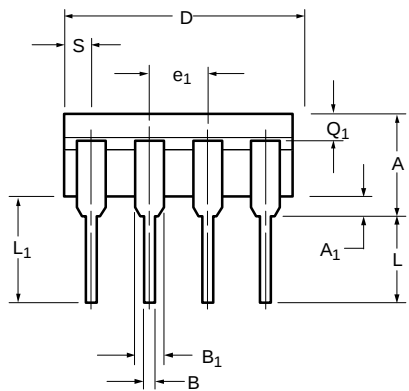
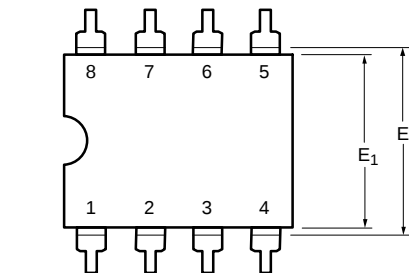
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A₁	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B₁	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	9.02	10.92	0.355	0.430
E	7.62	8.26	0.300	0.325
E₁	5.59	7.11	0.220	0.280
e₁	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q₁	1.27	2.03	0.050	0.080
S	0.76	1.65	0.030	0.065

ECN: S-03946—Rev. E, 09-Jul-01
DWG: 5478

NOTE: End leads may be half leads.



CERDIP: 8-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A ₁	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B ₁	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	9.40	10.16	0.370	0.400
E	7.62	8.26	0.300	0.325
E ₁	6.60	7.62	0.260	0.300
e ₁	2.54 BSC		0.100 BSC	
e _A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L ₁	3.18	5.08	0.150	0.200
Q ₁	1.27	2.16	0.050	0.085
S	0.64	1.52	0.025	0.060
α	0°	15°	0°	15°

ECN: S-03946—Rev. C, 09-Jul-01
DWG: 5348

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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