



Precision Monolithic Low-Voltage CMOS Analog Switches

FEATURES

- 2.7- thru 12-V Single Supply or ± 3 - thru ± 6 -Dual Supply
- On-Resistance— r_{ON} : 14 Ω
- Fast Switching— t_{ON} : 28 ns
— t_{OFF} : 13 ns
- TTL, CMOS Compatible
- Low Leakage: <100 pA

BENEFITS

- Widest Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

APPLICATIONS

- Precision Automatic Test Equipment
- Precision Data Acquisition
- Communication Systems
- Battery Powered Systems
- Computer Peripherals
- SDSL, DSLAM
- Audio and Video Signal Routing

DESCRIPTION

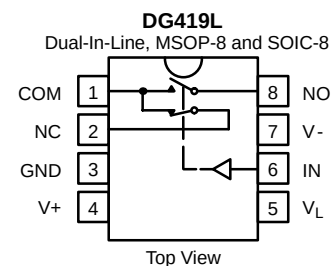
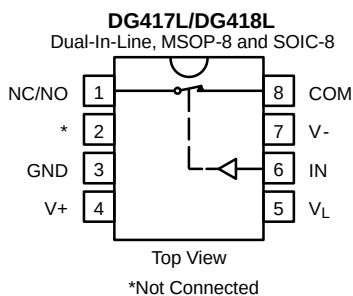
The DG417L/418L/419L are low voltage pin-for-pin compatible companion devices to the industry standard DG417/418/419 with improved performance

Using BiCMOS wafer fabrication technology allows the DG417L/418L/419L to operate on single and dual supplies. Single supply voltage ranges from 3 to 12 V while dual supply operation is recommended with ± 3 to ± 6 V.

Combining high speed (t_{ON} : 28 ns), flat r_{ON} over the analog signal range (6 Ω), minimal insertion loss (up to 100 MHz), and excellent crosstalk and off-isolation performance (-70 dB at 1 MHz), the DG417L/418L/419L are ideally suited for audio and video signal switching.

The DG417L and DG418L respond to opposite control logic as shown in the Truth Table. The DG419L has an SPDT configuration.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	DG417L	DG418L
0	ON	OFF
1	OFF	ON

TRUTH TABLE—DG419L

Logic	SW ₁	SW ₂
0	ON	OFF
1	OFF	ON

ORDERING INFORMATIONDG417L/418L

Temp Range	Package	Part Number
-40 to 85°C	8-Pin Narrow SOIC	DG417LDY
		DG418LDY
	8-Pin MSOP	DG417LDQ
		DG418LDQ
-55 to 125°C	8-Pin CerDIP	DG417LAK/883
		DG417LAK
		DG418LAK/883
		DG418LAK

ORDERING INFORMATIONDG419L

Temp Range	Package	Part Number
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	8-Pin MSOP	DG419LDQ
-55 to 125°C	8-Pin CerDIP	DG419LAK/883
		DG419LAK

ABSOLUTE MAXIMUM RATINGS

V+ to V-	-0.3 TO 13 V
GND to V-	7 V
V _L	(GND -0.3 V) to (V+) +0.3 V
I _N , COM, NC, NO ^a	-0.3 to (V+ +0.3 V) or 30 mA, whichever occurs first
Continuous Current (Any Terminal)	30 mA
Peak Current, S or D (Pulsed 1 ms, 10% Duty Cycle)	100 mA
Storage Temperature (AK, DQ, DY Suffix)	-65 to 150°C

Power Dissipation (Package)^b

8-Pin MSOP ^c	320 mW
8-Pin SOIC ^c	400 mW
8-Pin CerDIP ^d	600 mW

Notes:

- Signals on NC, NO, COM, or IN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 25°C
- Derate 12 mW/°C above 75°C

SPECIFICATIONS (SINGLE SUPPLY 12 V)									
Parameter	Symbol	Test Conditions Unless Specified V+ = 12 V, V- = 0 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f	Temp ^b	Typ ^c	A Suffix Limits -55 to 125°C		D Suffix Limits -40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		0	12	0	12	V
On-Resistance	r _{ON}	V+ = 10.8 V, V- = 0 V I _{NO} , I _{NC} = 5 mA, V _{COM} = 2/9 V	Room Full	13		20 32		20 23.5	Ω
Switch Off Leakage Current	I _{NO(off)} , I _{NC(off)}	V _{COM} = 1/11 V V _{NO} , V _{NC} = 11/1 V	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	I _{COM(off)}		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current	I _{COM(on)}	V _{NO} , V _{NC} = V _{COM} = 11/1 V	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Input Current	I _{INL} or I _{INH}		Full	0.01	-1.5	1.5	-1	1	μA
Dynamic Characteristics									
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF V _{NO} , V _{NC} = 5 V See Figure 2	Room Full	28		43 50		43 46	ns
Turn-Off Time	t _{OFF}		Room Full	13		31 35		31 32	
Break-Before-Make Time Delay	t _D	DG419L Only, V _{NC} , V _{NO} = 5 V R _L = 300 Ω, C _L = 35 pF	Room	13					
Charge Injection ^e	Q _{INJ}	V _g = 0 V, R _g = 0 Ω, C _L = 1 nF	Room	1					pC
Off Isolation ^e	OIRR	R _L = 50 Ω, C _L = 5 pF f = 1 MHz	Room	-71					dB
Channel-to-Channel Crosstalk ^e	X _{TALK}		Room	-71					
Source Off Capacitance ^e	C _{NO(off)} , C _{NC(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room	5					pF
Channel On Capacitance ^e	C _{ON}		Room	15					
Power Supplies									
Positive Supply Current	I+	V _{IN} = 0 or V _L	Room Full	0.02		1 7.5		1 5	μA
Negative Supply Current	I-		Room Full	-0.002	-1 -7.5		-1 -5		
Logic Supply Current	I _L		Room Full	0.002		1 7.5		1 5	
Ground Current	I _{GND}		Room Full	-0.002	-1 -7.5		-1 -5		



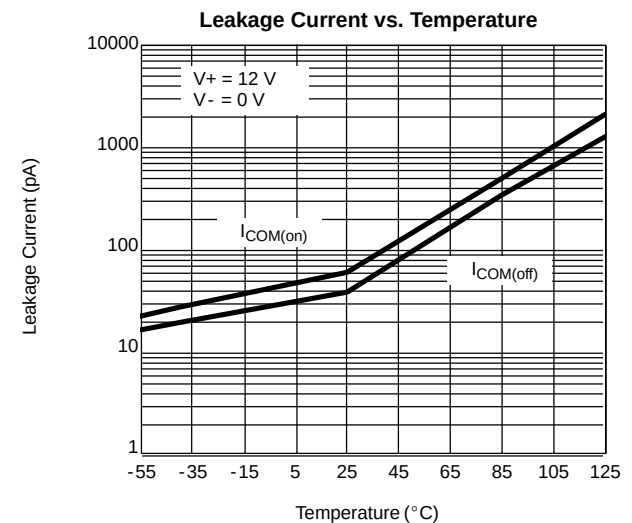
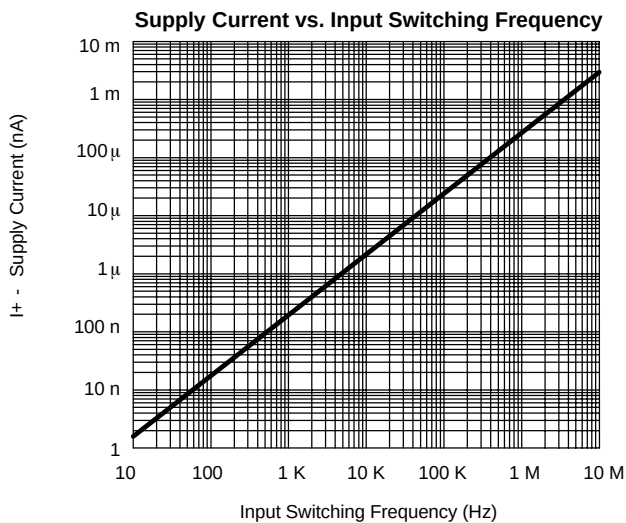
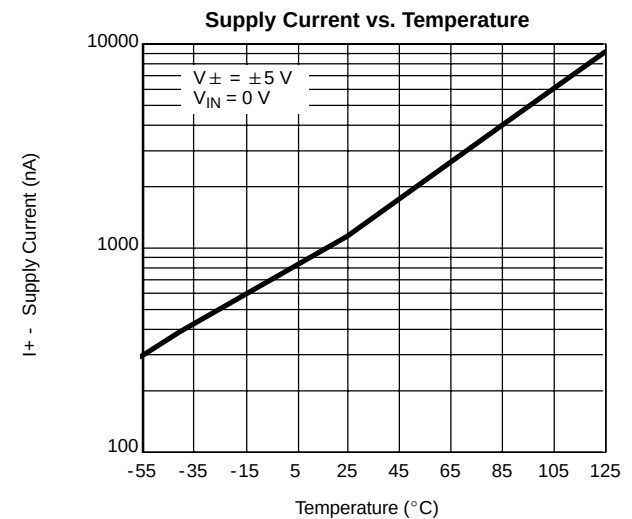
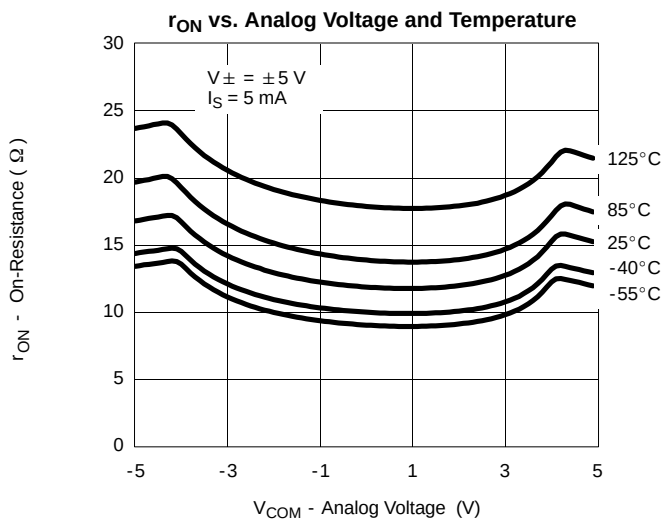
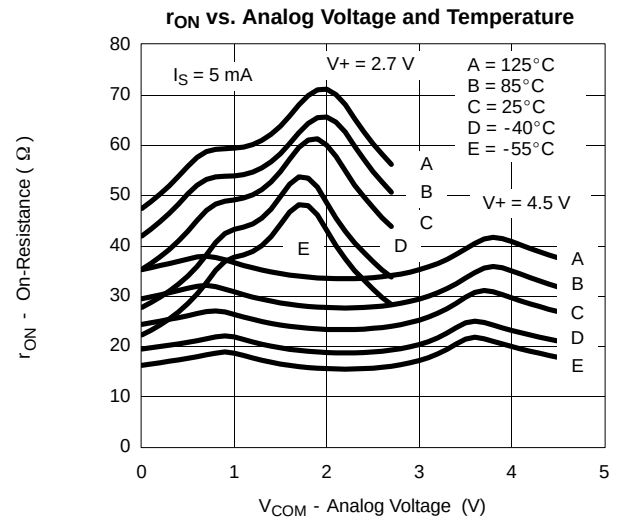
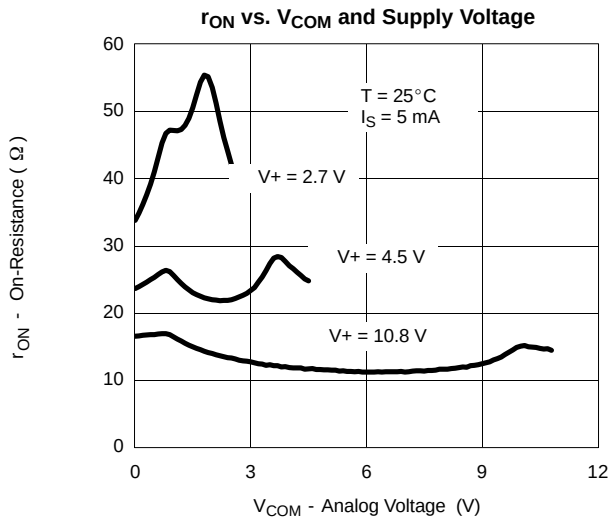
SPECIFICATIONS (DUAL SUPPLY ± 5 V)									
Parameter	Symbol	Test Conditions Unless Specified V+ = 5 V, V- = -5 V VL = 5 V, VIN = 2.4 V, 0.8 V ^f	Temp ^b	Typ ^c	A Suffix Limits -55 to 125° C		D Suffix Limits -40 to 85° C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	VANALOG		Full		-5	5	-5	5	V
On-Resistance	rON	V+ = 5 V, V- = -5 V INO, INC = 5 mA, VCOM = ± 3.5 V	Room Full	14		18.5 30		18.5 21	Ω
Switch Off Leakage Current ^a	I _{NO(off)} , I _{NC(off)}	V+ = 5.5 V, V- = -5.5 V VCOM = ± 4.5 V, VNO, VNC = ∓ 4.5 V	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	ICOM(off)		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current ^a	ICOM(on)	V+ = 5.5 V, V- = -5.5 V VNO, VNC = VCOM = ± 4.5 V	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Input Current ^a	IINL or IINH		Full	0.05	-1.5	1.5	-1	1	μA
Dynamic Characteristics									
Turn-On Time ^e	tON	RL = 300 Ω, CL = 35 pF VNO, VNC = ± 3.5 V See Figure 2	Room Full	30		41 50		41 44	ns
Turn-Off Time ^e	tOFF		Room Full	16		32 36		32 33	
Break-Before-Make Time Delay ^e	td	DG419L Only, VNO, VNC = 3.5 V RL = 300 Ω, CL = 35 pF	Room	10					
Transition Time	tTRANS	RL = 300 Ω, CL = 35 pF V _{S1} = ± 3.5 V, V _{S2} = ∓ 3.5 V	Room	33		47		47	
Charge Injection ^e	QINJ	Vg = 0 V, Rg = 0 Ω, CL = 1 nF	Room	3					pC
Off Isolation ^e	OIRR	RL = 50 Ω, CL = 5 pF f = 1 MHz	Room	-71					dB
Channel-to-Channel Crosstalk ^e	XTALK		Room	-76					
Source Off Capacitance ^e	C _{NO(off)} C _{NC(off)}	f = 1 MHz	Room	5.2					pF
Channel On Capacitance ^e	CON		Room	15					
Power Supplies									
Positive Supply Current ^e	I+	VIN = 0 or VL	Room Full	0.03		1 7.5		1 5	μA
Negative Supply Current ^e	I-		Room Full	-0.002	-1 -7.5		-1 -5		
Logic Supply Current ^e	IL		Room Full	0.002		1 7.5		1 5	
Ground Current ^e	IGND		Room Full	-0.002	-1 -7.5		-1 -5		

SPECIFICATIONS (SINGLE SUPPLY 5 V)									
Parameter	Symbol	Test Conditions Unless Specified V+ = 5 V, V- = 0 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f	Temp ^b	Typ ^c	A Suffix Limits -55 to 125°C		D Suffix Limits -40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full			5		5	V
On-Resistance ^e	r _{ON}	V+ = 4.5 V, I _{NO} , I _{NC} = 5 mA V _{COM} = 1 V, 3.5 V	Room Full	26		36.5 50		36.5 40.5	Ω

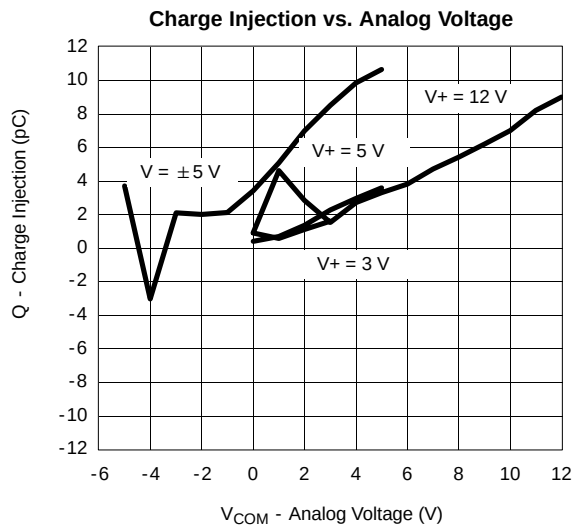
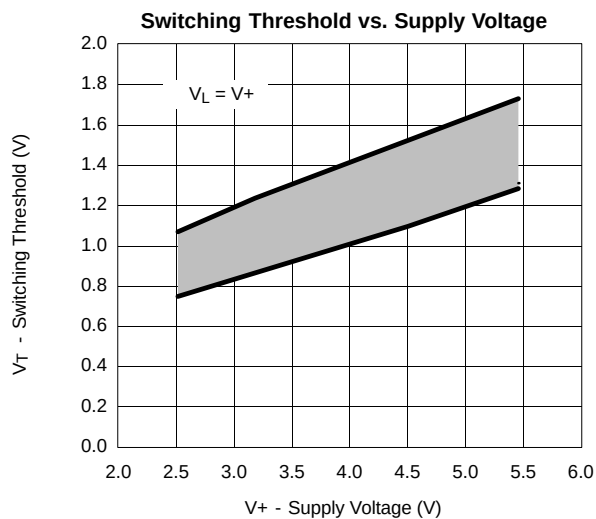
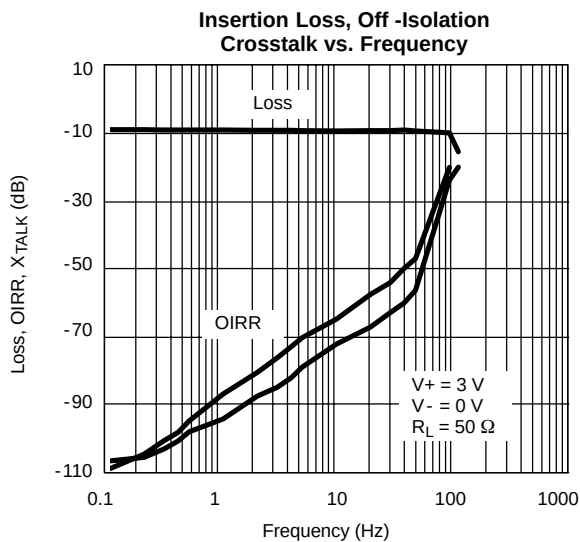
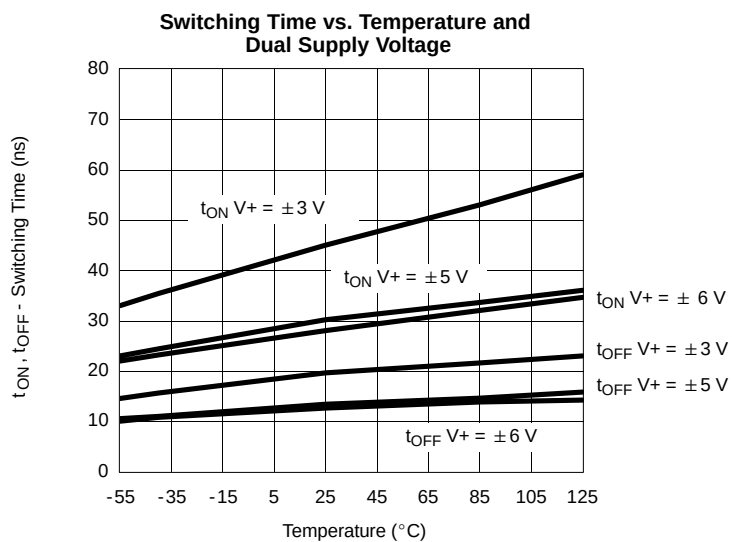
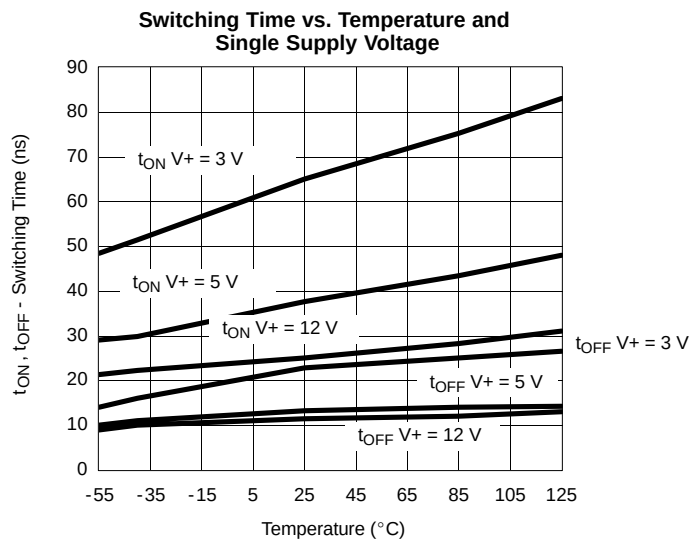
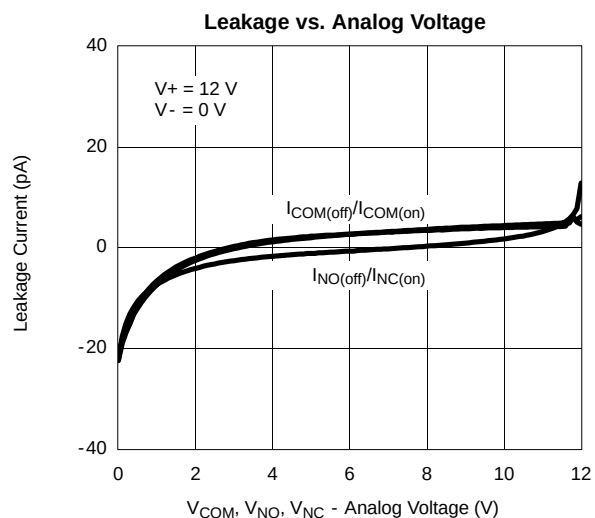
SPECIFICATIONS (SINGLE SUPPLY 5 V)									
Parameter	Symbol	Test Conditions Unless Specified V ₊ = 5 V, V ₋ = 0 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^f	Temp ^b	Typ ^c	A Suffix Limits -55 to 125°C		D Suffix Limits -40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Dynamic Characteristics									
Turn-On Time ^e	t _{ON}	R _L = 300 Ω, C _L = 35 pF V _{NO} , V _{NC} = 3.5 V, See Figure 2	Room Full	37		49 60		49 54	ns
Turn-Off Time ^e	t _{OFF}		Room Full	16		31 35		31 32	
Break-Before-Make Time Delay ^e	t _D	DG419L Only, V _{NO} , V _{NC} = 3.5 V R _L = 300 Ω, C _L = 35 pF	Room	19					pC
Charge Injection ^e	Q _{INJ}	V _g = 0 V, R _g = 0 Ω, C _L = 1 nF	Room	0.4					
Power Supplies									
Positive Supply Current ^e	I ₊	V _{IN} = 0 or V _L	Room Full	0.02		1 7.5		1 5	μA
Negative Supply Current ^e	I ₋		Room Full	-0.002	-1 -7.5		-1 -5		
Logic Supply Current ^e	I _L		Room Full	0.002		1 7.5		1 5	
Ground Current ^e	I _{GND}		Room Full	-0.002	-1 -7.5		-1 -5		
SPECIFICATIONS (SINGLE SUPPLY 3 V)									
Parameter	Symbol	Test Conditions Unless Specified V ₊ = 3 V, V ₋ = 0 V V _L = 3 V, V _{IN} = 2.0 V, 0.4 V ^f	Temp ^b	Typ ^c	A Suffix Limits -55 to 125°C		D SuffixLimits -40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		0	3	0	3	V
On-Resistance	r _{ON}	V ₊ = 2.7 V, V ₋ = 0 V I _{NO} , I _{NC} = 5 mA, V _{COM} = 0.5, 2.2 V	Room Full	47		70 80		70 75	Ω
Switch Off Leakage Current ^a	I _{NO(off)} , I _{NC(off)}	V ₊ = 3.3 V, V ₋ = 0 V V _{COM} = 1, 2 V, V _{NO} , V _{NC} = 2, 1 V	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	I _{COM(off)}		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current ^a	I _{COM(on)}	V ₊ = 3.3 V, V ₋ = 0 V V _{NO} , V _{NC} = V _{COM} = 1, 2 V	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Input Current ^a	I _{INL} or I _{INH}		Full	0.005	-1.5	1.5	-1	1	μA
Dynamic Characteristics									
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF V _{NO} , V _{NC} = 1.5 V See Figure 2	Room Full	65		75 95		75 85	ns
Turn-Off Time	t _{OFF}		Room Full	26		41 45		41 43	
Break-Before-Make Time Delay	t _D	DG419L Only, V _{NO} , V _{NC} = 1.5 V R _L = 300 Ω, C _L = 35 pF	Room	33					
Charge Injection ^e	Q _{INJ}	V _g = 0 V, R _g = 0 Ω, C _L = 1 nF	Room	1					pC
Off Isolation ^e	OIRR	R _L = 50 Ω, C _L = 5 pF f = 1 MHz	Room	-71					dB
Channel-to-Channel Crosstalk ^e	X _{TALK}		Room	-77					
Source Off Capacitance ^e	C _{NO(off)} , C _{NC(off)}	f = 1 MHz	Room	5.6					pF
Channel On Capacitance ^e	C _{D(on)}		Room	16					

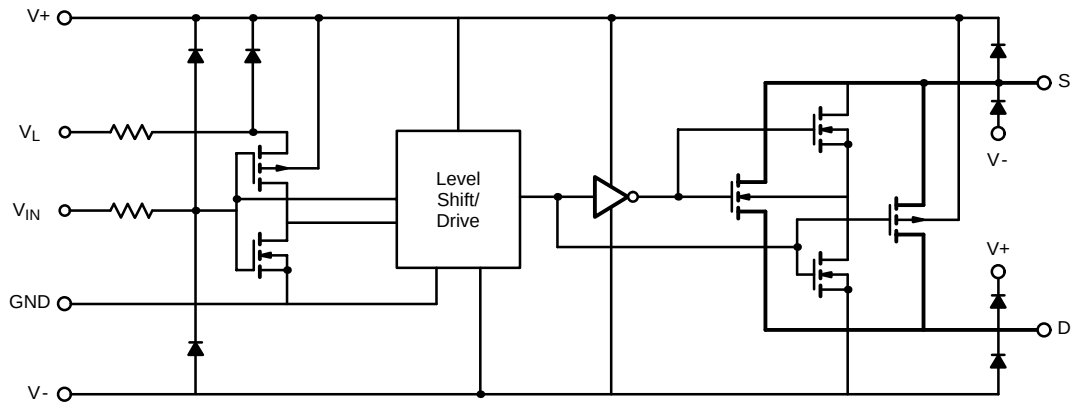
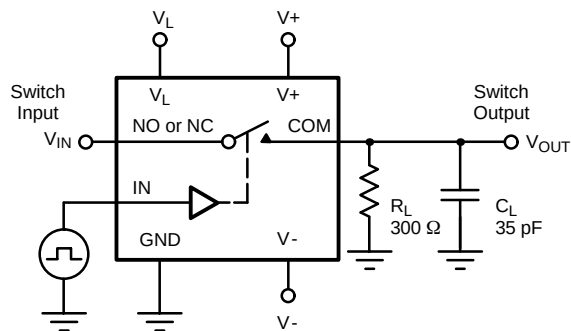
Notes:

- Leakage parameters are guaranteed by worst case test condition and not subject to production test.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

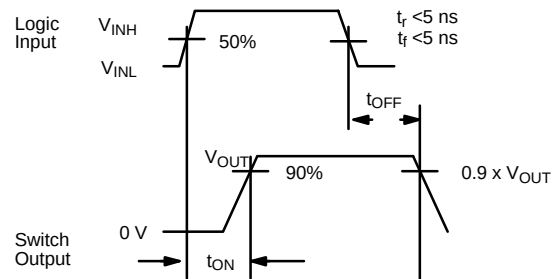
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

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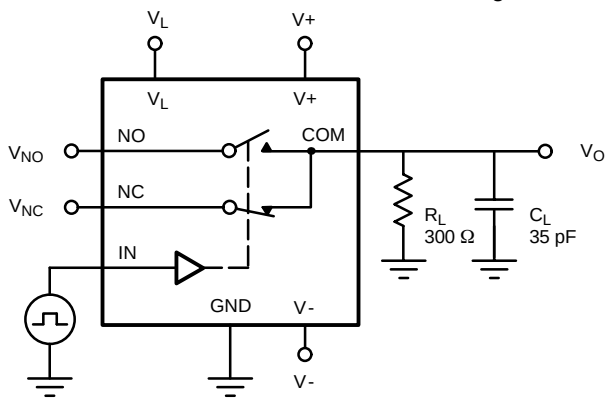
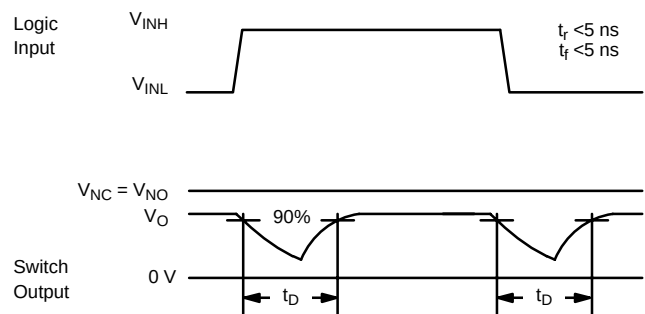


SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

Figure 1.
TEST CIRCUITS

 C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{IN} \frac{R_L}{R_L + r_{ON}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time

 C_L (includes fixture and stray capacitance)

Figure 3. Break-Before-Make (DG419L)

TEST CIRCUITS

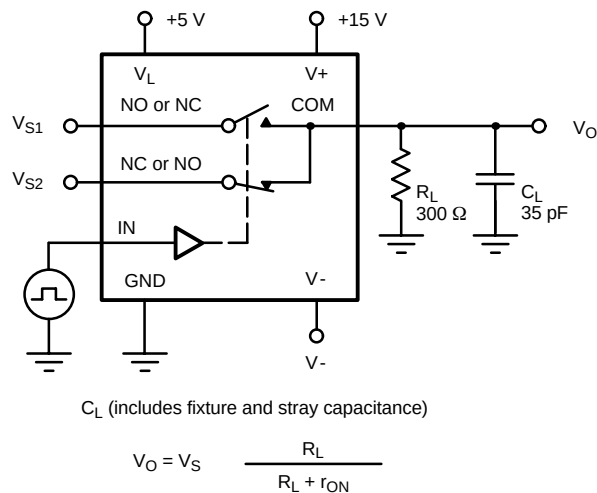
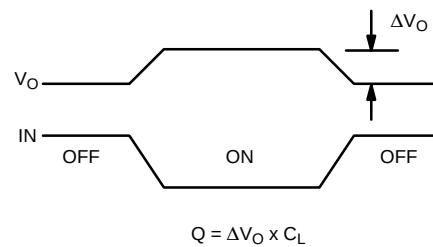
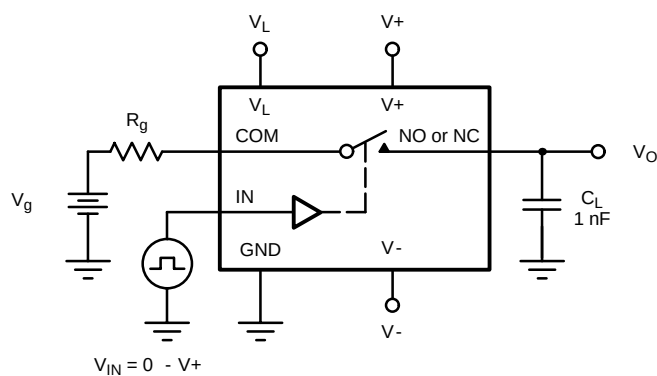
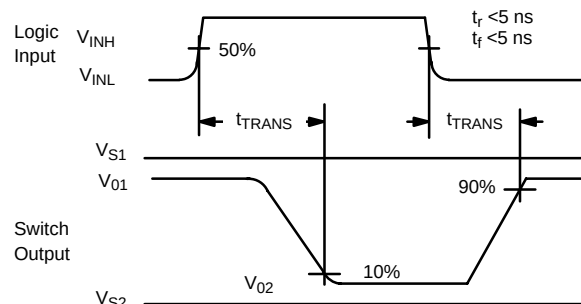


Figure 4. Transition Time (DG419L)



IN dependent on switch configuration Input polarity determined by sense of switch.

Figure 5. Charge Injection

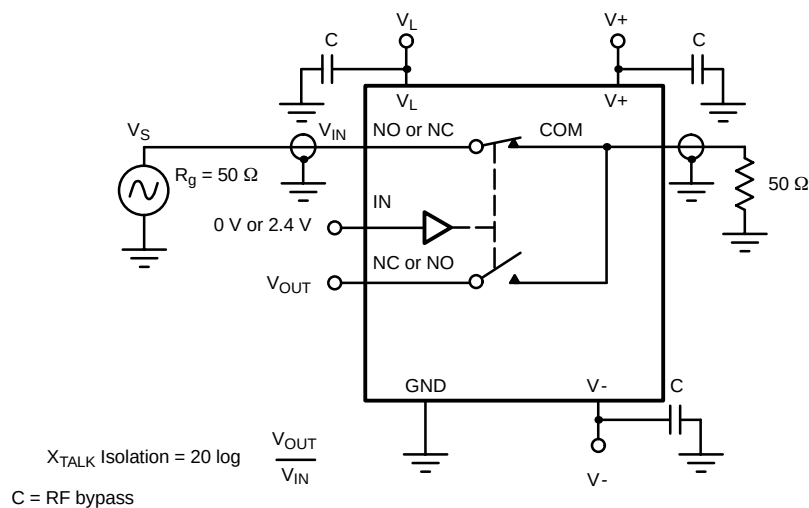


Figure 6. Crosstalk (DG419L)

TEST CIRCUITS

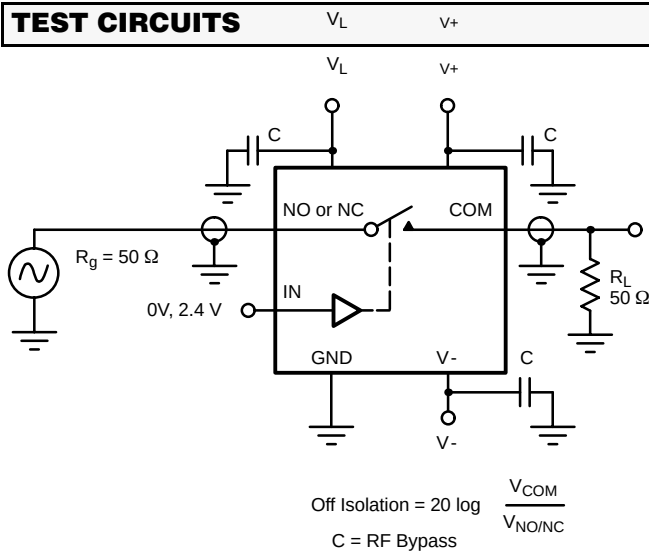


Figure 7. Off Isolation

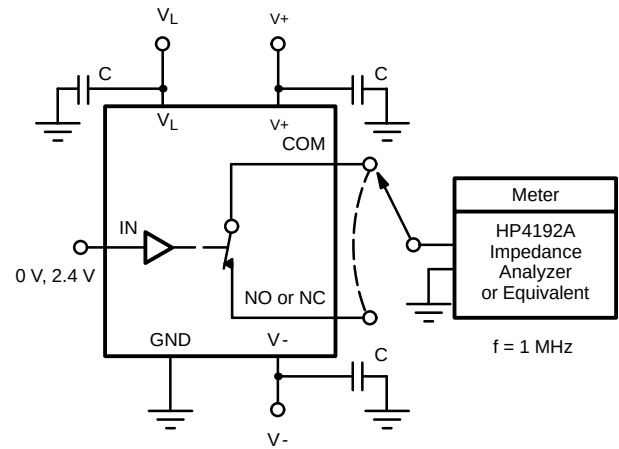


Figure 8. Source/Drain Capacitances