Low Power, High Voltage SPST Analog Switches

DESCRIPTION

The DG467 and DG468 are dual supply single-pole/single-throw (SPST) switches. On resistance is 10 Ω max. and flatness is 2 Ω max. over the specified analog signal range. These analog switches were designed to provide high speed, low error switching of precision analog signals. The primary application areas are in the routing and switching in telecommunications and test equipment. Combining low power, low leakages, low on-resistance and small physical size, the DG467/468 are also ideally suited for portable and battery powered industrial and military equipment.

The DG467 has one normally closed switch, while the DG468 switch is normally open. They operate either from a single + 7 V to 36 V supply or from dual ± 4.5 V to ± 20 V supplies. They are offered in the very popular, small TSOP6 package.

FEATURES

- ± 15 V Analog Signal Range
- On-Resistance - $R_{DS(on)}$: 10 Ω max.
- Fast Switching Action - T_{ON}: 100 ns
- V_L Logic Supply Not Required
- TTL CMOS Input Compatible
- Rail To Rail Signal Handling
- Dual Or Single Supply Operation
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

BENEFITS

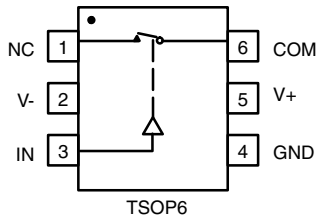
- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Befor-Make Switching Action
- Simple Interfacing
- Reduced Board Space
- Improved Reliability

APPLICATIONS

- Precision Test Equipment
- Precision Instrumentaion
- Communications Systems
- PBX, PABX Systems
- Audio Equipment
- Redundant Systems
- PC Multimedia Boards
- Hard Disc Drivers

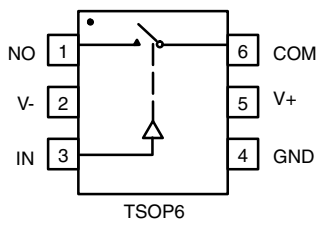
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG467



TSOP6

DG468



TSOP6

TRUTH TABLE

Logic	DG467	DG468
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Device Marking:
DG467DV = G7xxx
DG468DV = G8xxx

ORDERING INFORMATION

Temp Range	Package	Part Number
DG467/DG468		
- 40 °C to 85 °C	6-Pin TSOP	DG467DV-T1-E3
		DG468DV-T1-E3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter Referenced To V-		Symbol	Limit	Unit
V+			44	V
GND			25	
Digital Inputs[a], $V_{NO/NC}$, V_{COM}			(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Current, (Any Terminal) Continuous			30	mA
Current (NO or NC or COM) Pulsed at 1 ms, 10 % duty cycle			100	
Storage Temperature			- 65 to 150	°C
Power Dissipation (Package)[b]	6-Pin TSOP[c]		570	mW

Notes:
a. Signals on NO, NC, COM, or IN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 7 mW/°C above 70 °C.

For technical questions, contact: analogswitchtechsuoort@vishay.com
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SPECIFICATIONS[a] (V ± = ± 15 V)							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 15 V, V- = - 15 V V_{IN} = 2.4 V, 0.8 V[f]	**Temp.**[b]	**D Suffix** - 40 °C to 85 °C **Min.**[d]	**Typ.**[c]	**Max.**[d]	**Unit**
Analog Switch							
Analog Signal Range[eron]	V_{ANALOG}		Full	- 15		15	V
Drain-Source On-Resistance	R_{ON}	$I_{NO/NC}$ = 10 mA, V_{COM} = 10 V V+ = 13.5 V, V- = - 13.5 V	Room Full		7	9 10	Ω
On-Resistance Flatness	R_{ON} Flatness	$I_{NO/NC}$ = 10 mA, V_{COM} = ± 5 V, 0 V V+ = 13.5 V, V- = - 13.5 V	Room Full		0.7	1 2	Ω
Switch Off Leakage Current	$I_{NO/NC(off)}$	V+ = 16.5, V- = - 16.5 V V_{COM} = ± 15.5 V $V_{NO/NC}$ = -/+ 15.5 V	Room Full	- 1 - 10	- 0.1	1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10	- 0.1	1 10	
Channel On Leakage Current	$I_{COM(on)}$	V+ = 16.5 V, V- = - 16.5 V_{COM} = $V_{NO/NC}$ = ± 15.5 V	Room Full	- 1 - 10	- 0.1	1 10	
Digital Control							
Input, High Voltage	V_{INH}		Full	2.4			V
Input, Low Voltage	V_{INL}		Full			0.8	
Input Capacitance[e]	C_{IN}		Room		5		pF
Input Current	I_{IN}	V_{IN} = 0 or 5 V		- 1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF $V_{NO/NC}$ = ± 10 V	Room Full		100	140 160	ns
Turn-Off Time	t_{OFF}		Room Full		50	80 100	
Charge Injection[e]	Q	C_L = 1 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		21		pC
Off-Isolation[e]	OIRR	C_L= 5 pF, R_L = 50 Ω, f = 1 MHz	Room		- 61		dB
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room		30		pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room		15		
Channel On Capacitance[e]	$C_{D(on)}$	f = 1 MHz	Room		76		
Power Supplies							
Positive Supply Current	I+	V+ = 16.5 V, V- = - 16.5 V V_{IN} = 0 or 5 V	Room Full		5	15 20	µA
Negative Supply Current	I-		Room Full	- 1 - 10	- 0.02		

SPECIFICATIONS[a] (V+ = 12 V)							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 12 V, V- = 0 V V_{IN} = 2.4 V, 0.8 V[f]	**Temp.**[b]	**D Suffix** - 40 °C to 85 °C **Min.**[d]	**Typ.**[c]	**Max.**[d]	**Unit**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	0		12	V
Drain-Source On-Resistance	R_{ON}	$I_{NO/NC}$ = –10 mA, V_{COM} = 8 V V+ = 10.8 V	Room Full		12	16 20	Ω
On-Resistance Flatness	R_{ON} Flatness	$I_{NO/NC}$ = 10 mA, V_{COM} = 2, 6, 8 V V+ = 10.8 V	Room Full		1.5	3 4	Ω
Dynamic Characteristics							
Turn-On Time	t_{ON}	$V_{NO, NC}$ = ± 10 V, R_L = 300 Ω, C_L = 35 pF	Room Full		130	160 200	nS
Turn-Off Time	t_{OFF}		Room Full		50	80 100	
Charge Injection[e]	Q	C_L = 1 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		8		pC
Power Supplies							
Positive Supply Current	I+	V+ = 13.2 V, V_{IN} = 0 V, 5 V	Room Full		3	7 10	µA

Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For technical questions, contact: analogswitchtechsuoort@vishay.com

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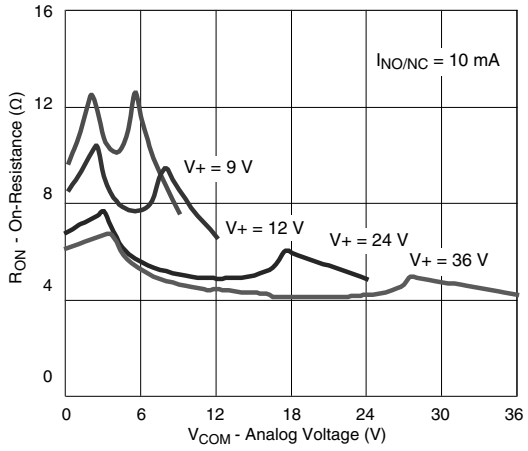
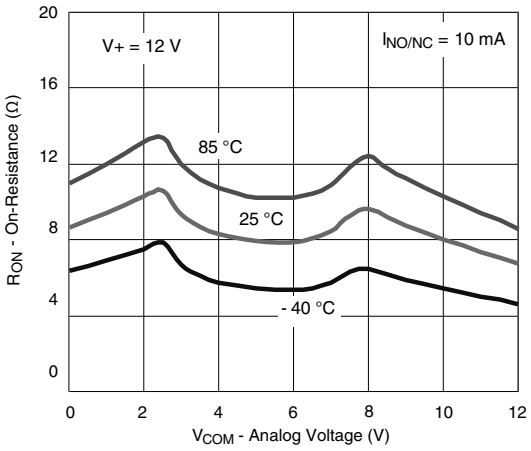
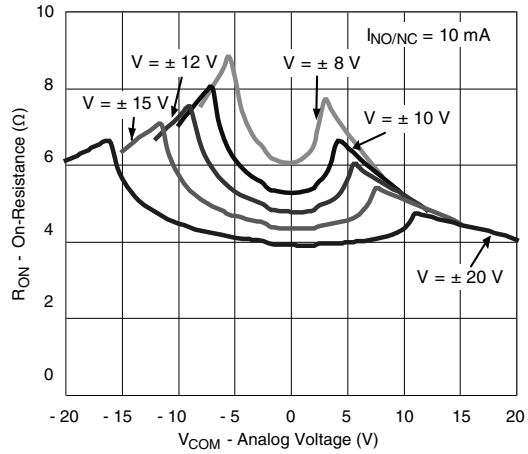
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



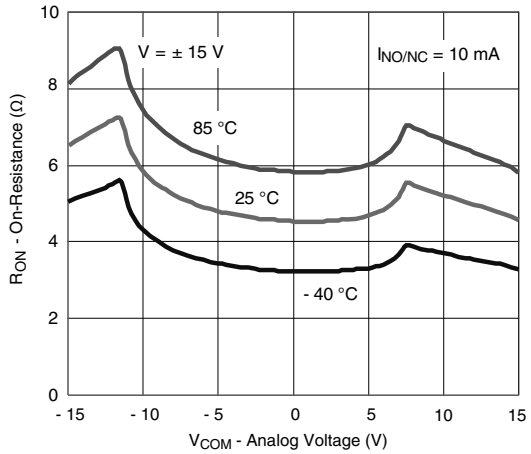
R_{ON} vs. V_{COM} and Single Supply Voltage



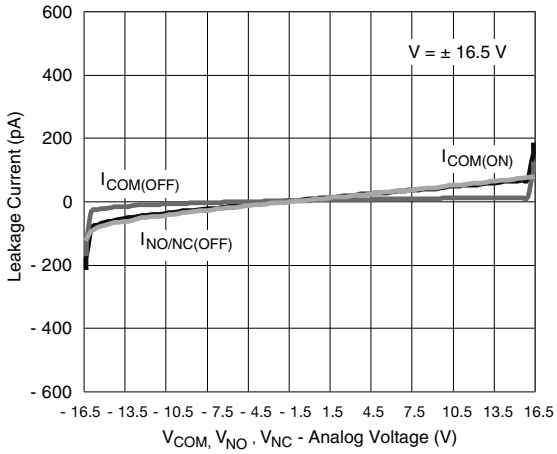
R_{ON} vs. Analog Voltage and Temperature



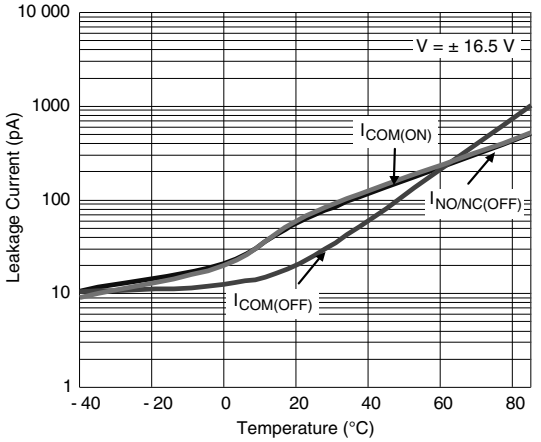
R_{ON} vs. V_{COM} and Dual Supply Voltage



R_{ON} vs. Analog Voltage and Temperature

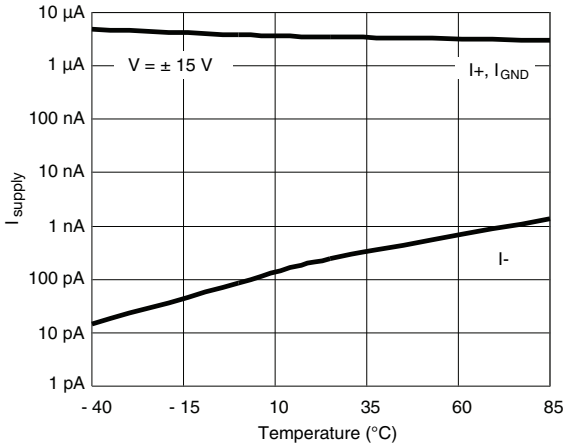


Leakage vs. Analog Voltage

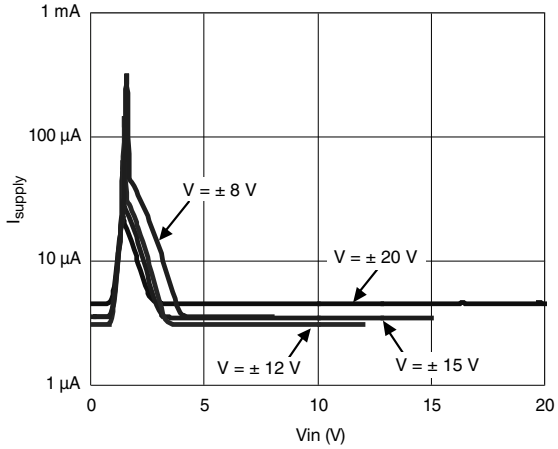


Leakage Current vs. Temperature

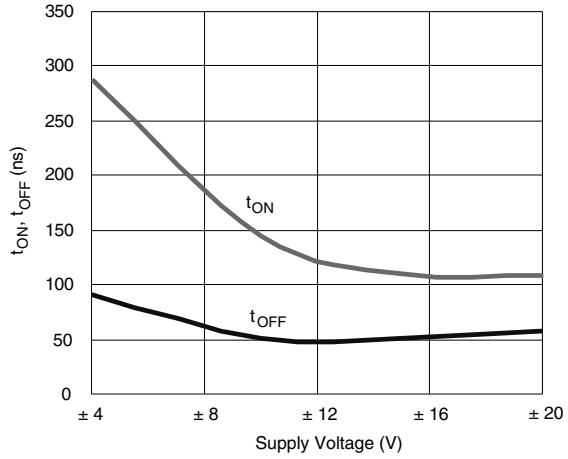
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



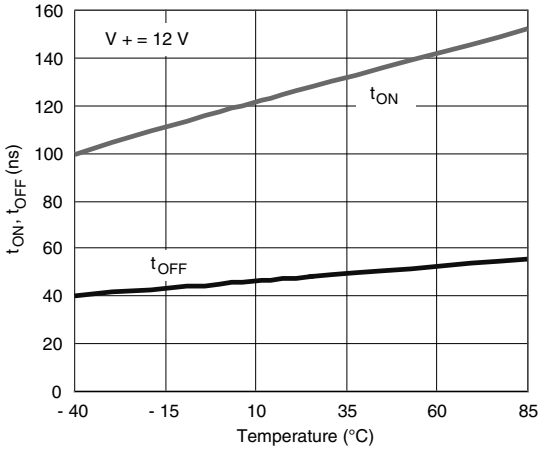
Supply Current vs. Temperature



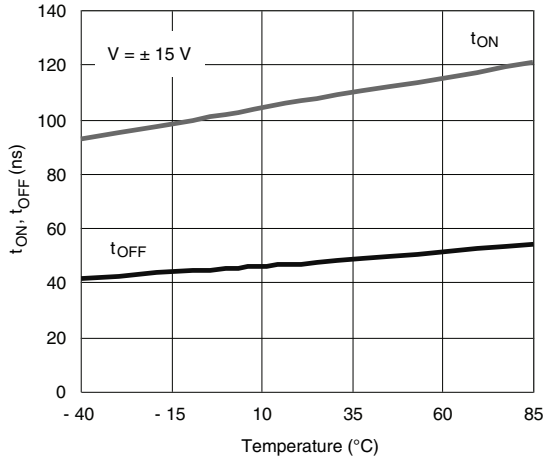
Supply Current vs. V_{IN}



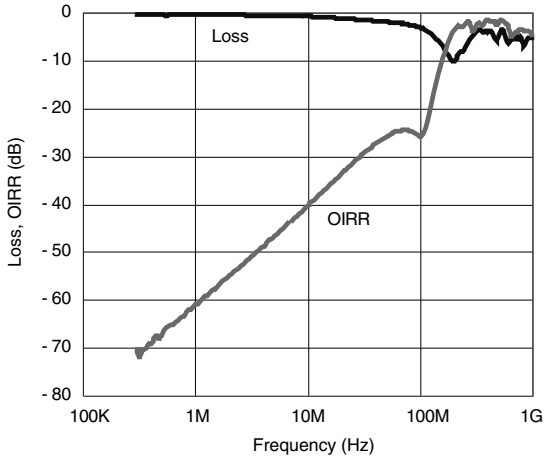
Switching Time vs. Supply Voltages



Switching Time vs. Temperature



Switching Time vs. Temperature



Off Isolation and Insertion Loss vs. Frequency

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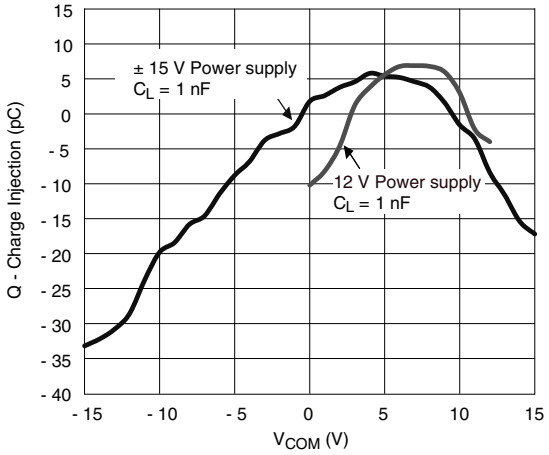
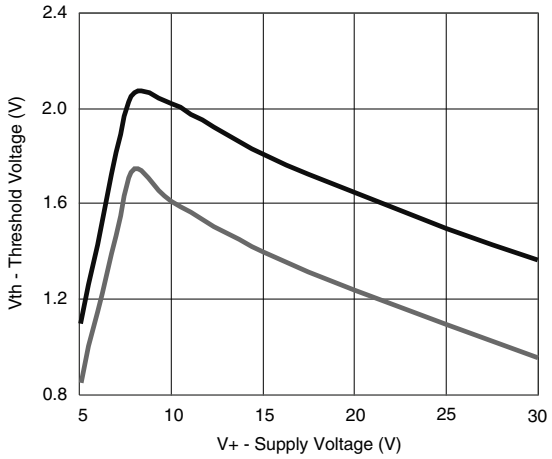
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



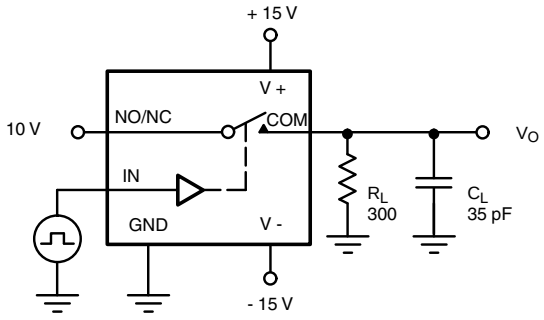
Charge Injection vs. Analog Voltage



Input Switching Threshold vs. Supply Voltage

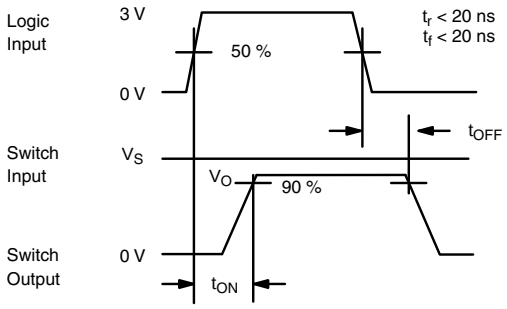
TEST CIRCUITS

V_O is the steady state output with the switch on.



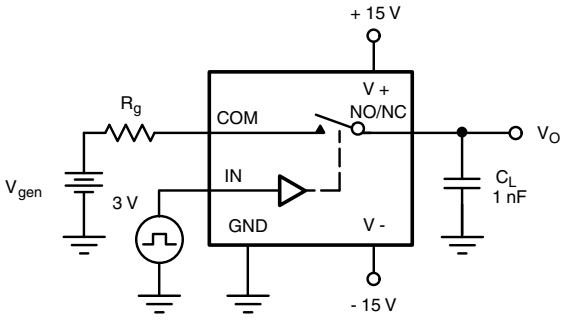
C_L (includes fixture and stray capacitance)

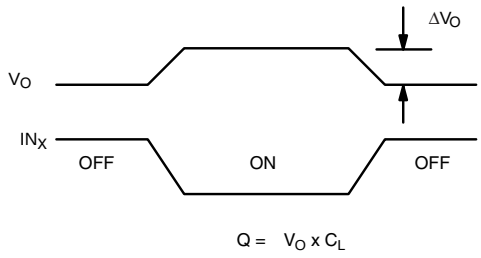
$$V_O = V_S \frac{R_L}{R_L + r_{ON}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 1. Switching Time





$$Q = V_O \times C_L$$

Figure 2. Charge Injection

TEST CIRCUITS

V_O is the steady state output with the switch on.

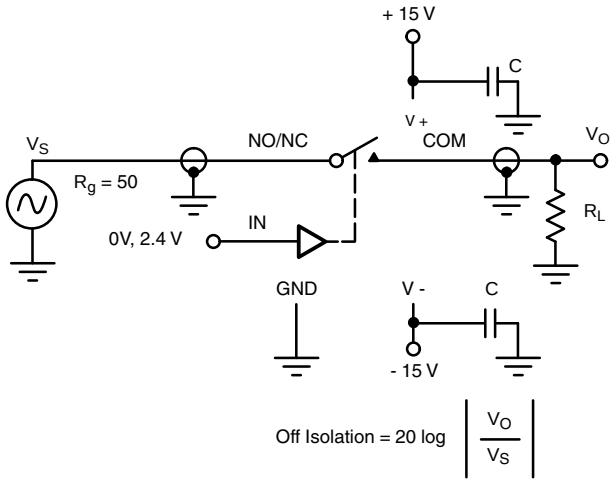


Figure 3. Off Isolation

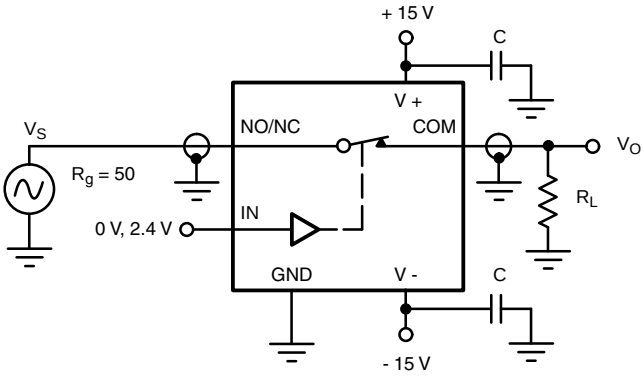


Figure 4. Insertion Loss

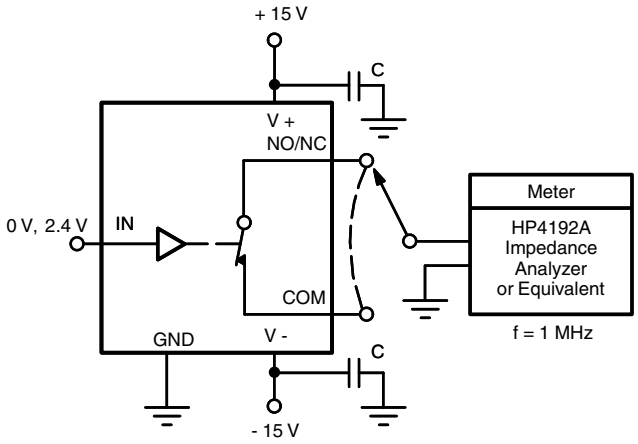
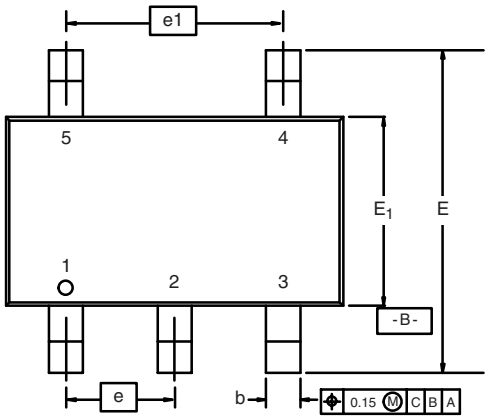


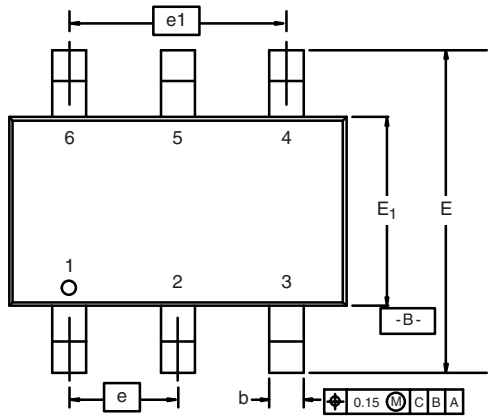
Figure 5. Source/Drain Capacitances

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?74413.

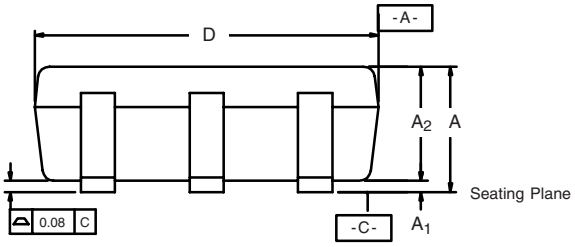
TSOP: 5/6–LEAD
JEDEC Part Number: MO-193C

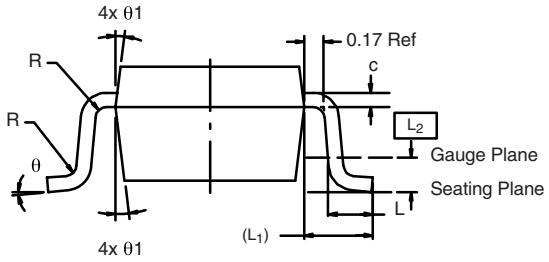


5-LEAD TSOP



6-LEAD TSOP





Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A_1	0.01	-	0.10	0.0004	-	0.004
A_2	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e_1	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L_1	0.60 Ref			0.024 Ref		
L_2	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ_1	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540						

Mounting LITTLE FOOT® TSOP-6 Power MOSFETs

Surface mounted power MOSFET packaging has been based on integrated circuit and small signal packages. Those packages have been modified to provide the improvements in heat transfer required by power MOSFETs. Leadframe materials and design, molding compounds, and die attach materials have been changed. What has remained the same is the footprint of the packages.

The basis of the pad design for surface mounted power MOSFET is the basic footprint for the package. For the TSOP-6 package outline drawing see http://www.vishay.com/doc?71200 and see http://www.vishay.com/doc?72610 for the minimum pad footprint. In converting the footprint to the pad set for a power MOSFET, you must remember that not only do you want to make electrical connection to the package, but you must made thermal connection and provide a means to draw heat from the package, and move it away from the package.

In the case of the TSOP-6 package, the electrical connections are very simple. Pins 1, 2, 5, and 6 are the drain of the MOSFET and are connected together. For a small signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

Figure 1 shows the copper spreading recommended footprint for the TSOP-6 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlays the basic pattern on pins 1,2,5, and 6. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. Notice that the planar copper is shaped like a “T” to move heat away from the drain leads in all directions. This pattern uses all the available area underneath the body for this purpose.

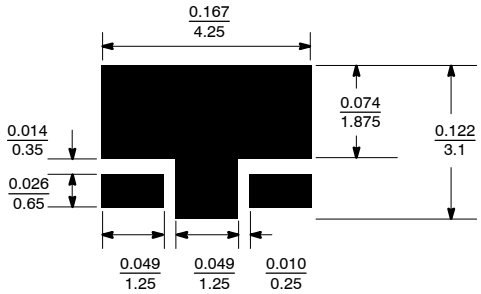


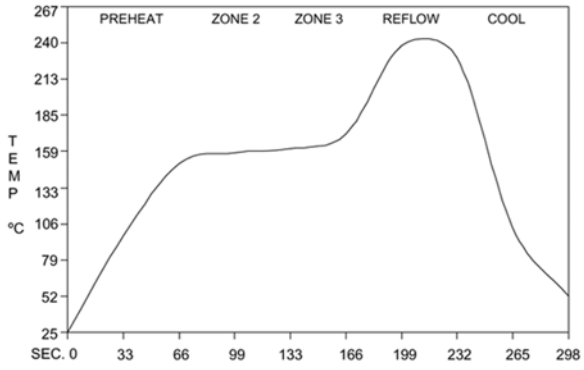
FIGURE 1. Recommended Copper Spreading Footprint

Since surface mounted packages are small, and reflow soldering is the most common form of soldering for surface mount components, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

REFLOW SOLDERING

Vishay Siliconix surface-mount packages meet solder reflow reliability requirements. Devices are subjected to solder reflow as a test preconditioning and are then reliability-tested using temperature cycle, bias humidity, HAST, or pressure pot. The solder reflow temperature profile used, and the temperatures and time duration, are shown in Figures 2 and 3.



Ramp-Up Rate	+6°C/Second Maximum
Temperature @ 155 ± 15°C	120 Seconds Maximum
Temperature Above 180°C	70 – 180 Seconds
Maximum Temperature	240 +5/–0°C
Time at Maximum Temperature	20 – 40 Seconds
Ramp-Down Rate	+6°C/Second Maximum

FIGURE 2. Solder Reflow Temperature Profile

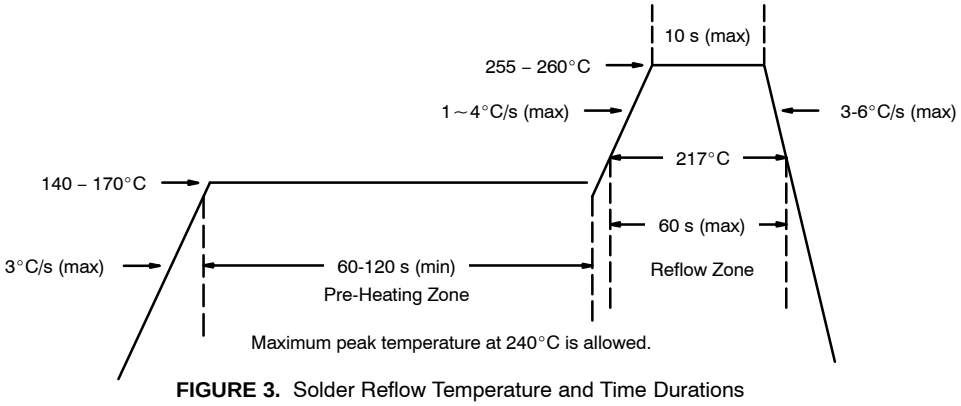


FIGURE 3. Solder Reflow Temperature and Time Durations

THERMAL PERFORMANCE

A basic measure of a device's thermal performance is the junction-to-case thermal resistance, $R\theta_{jc}$, or the junction-to-foot thermal resistance, $R\theta_{jf}$. This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only, in other words, independent of the properties of the object to which the device is mounted. Table 1 shows the thermal performance of the TSOP-6.

TABLE 1.

Equivalent Steady State Performance—TSOP-6	
Thermal Resistance $R\theta_{jf}$	30°C/W

SYSTEM AND ELECTRICAL IMPACT OF TSOP-6

In any design, one must take into account the change in MOSFET $r_{DS(on)}$ with temperature (Figure 4).

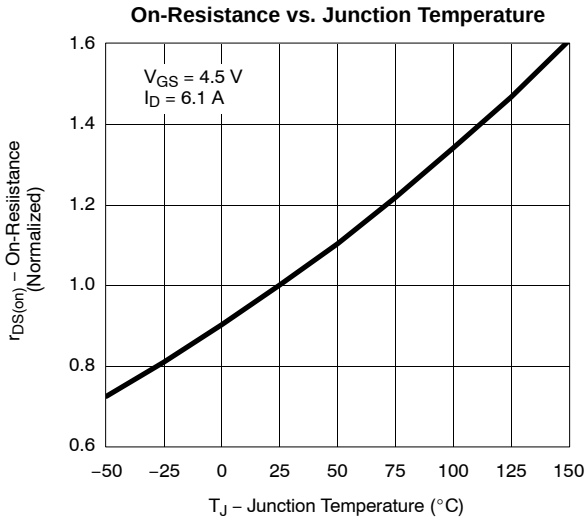
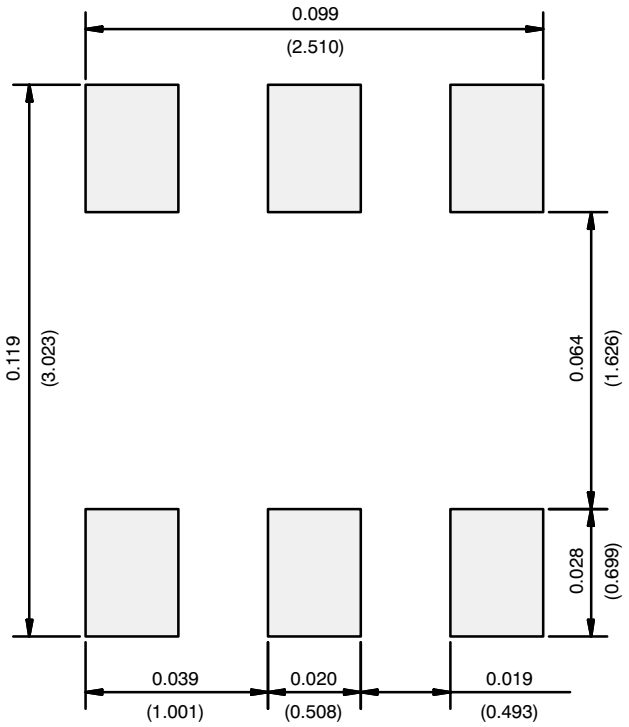


FIGURE 4. Si3434DV

RECOMMENDED MINIMUM PADS FOR TSOP-6



Recommended Minimum Pads
Dimensions in Inches/(mm)

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