Latchable Single 8-Ch/Differential 4-Ch Analog Multiplexers

DESCRIPTION

The DG528 is an 8-channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). DG529, a 4-channel dual analog multiplexer, is designed to connect one of four differential inputs to a common differential output as determined by its 2-bit binary address (A_0, A_1) logic.

These analog multiplexers have on-chip address and control latches to simplify design in microprocessor based applications. Break-before-make switching action protects against momentary shorting of the input signals. The DG528/529 are built on the improved PLUS-40 CMOS process. A buried layer prevents latchup.

The on chip TTL-compatible address latches simplify digital interface design and reduce board space in data acquisition systems, process controls, avionics, and ATE.

FEATURES

- Low $R_{DS(on)}$: 270 Ω
- 44 V Power Supply Rating
- On-Board Address Latches
- Break-Before-Make
- Low Leakage - $I_{D(on)}$: 30 pA

BENEFITS

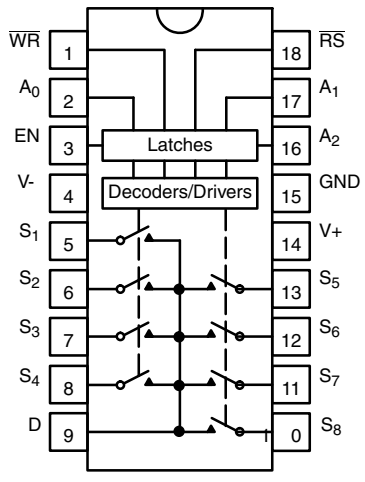
- Improved System Accuracy
- Microporcessor Bus Compatible
- Easily Interfaced
- Reduced Crosstalk

APPLICATIONS

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics and Military Systems
- Medical Instrumentation

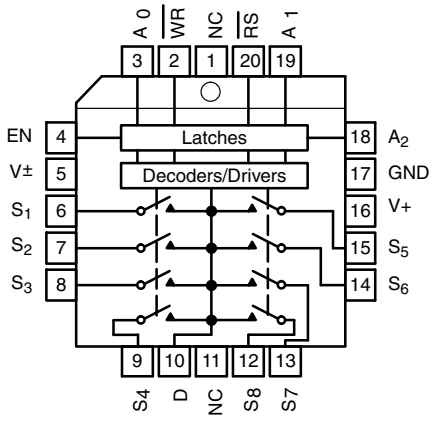
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG528
Dual-In-Line



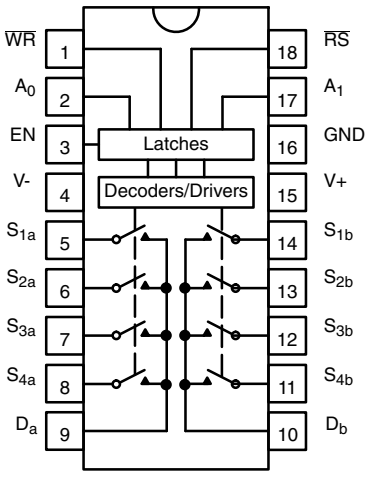
Top View

DG528
PLCC



Top View

DG529
Dual-In-Line



Top View

TRUTH TABLES AND ORDERING INFORMATION

TRUTH TABLE - DG528

8-Channel Single-Ended Multiplexer						
A_2	A_1	A_0	EN	WR	RS	On Switch
Latching						
X	X	X	X	↑	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	None (latches cleared)
Transparent Operation						
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

TRUTH TABLE - DG529

Differential 4-Channel Multiplexer				
A_0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching				
X	X	↑	1	Maintains previous switch condition
Reset				
X	X	X	0	None (latches cleared)
Transparent Operation				
X	0	0	1	None
0	1	0	1	1
1	1	0	1	2
0	1	0	1	3
1	1	0	1	4

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

ORDERING INFORMATION - DG528

Temp Range	Package	Part Number
0 °C to 70 °C	18-pin Plastic DIP	DG528CJ
	20-pin PLCC	DG528DN
- 25 °C to 85 °C	18-pin Cer DIP	DG528BK
- 55 °C to 125 °C		DG528AK
		DG528AK/883
		5962-8768901VA

ORDERING INFORMATION - DG529

Temp Range	Package	Part Number
0 °C to 70 °C	18-pin Plastic DIP	DG529CJ
- 25 °C to 85 °C	18-pin Cer DIP	DG529BK
- 55 °C to 125 °C		DG529AK/883

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Limit	Unit
Voltages Referenced to V-	V+		44	V
	GND		25	
Digital Inputs[a], V_S, V_D			(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Current (Any Terminal Except S or D)			30	mA
Continuous Current, S or D			20	
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max)			40	
Storage Temperature	(AK, BK Suffix)		- 65 to 150	°C
	(CJ, DN Suffix)		- 65 to 125	
Power Dissipation (Package)[b]	18-pin Plastic DIP[c]		470	mW
	18-pin CerDIP[d]		900	
	20-pin PLCC[e]		800	

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6.3 mW/°C above 75 °C.
d. Derate 12 mW/°C above 75 °C.
e. Derate 10 mW/°C above 75 °C.

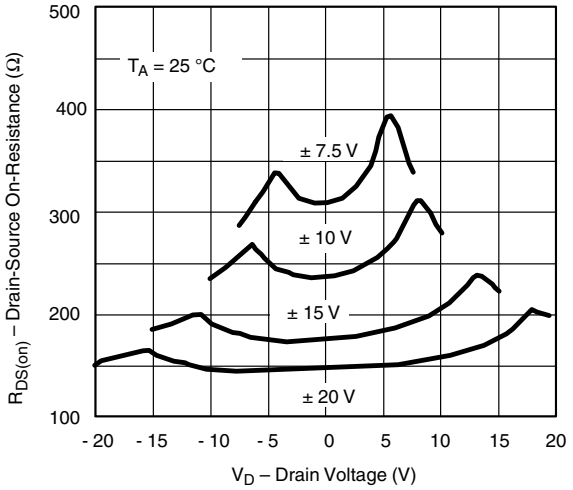
SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V, $\overline{WR}$ = 0, $\overline{RS}$ = 2.4 V, V_{IN} = 2.4 V, 0.8 µF[f]		Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C Min.[d]	A Suffix - 55 °C to 125 °C Max.[d]	B, C, D Suffix - 40 °C to 85 °C Min.[d]	B, C, D Suffix - 40 °C to 85 °C Max.[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_D = ± 10 V, I_S = - 200 µA		Room Full	270		400 500		450 550	Ω
Greatest Change in $R_{DS(on)}$ Between Channels[f]	$\Delta R_{DS(on)}$	- 10 V < V_S < 10 V		Room	6					%
Source Off Leakage Current	$I_{S(off)}$	V_{EN} = 0 V, V_D = ± 10 V V_S = ± 10 V		Room Full	± 005	- 1 - 50	1 50	- 5 - 50	5 50	nA
Drain Off Leakage Current	$I_{D(off)}$	V_{EN} = 0 V, V_D = ± 10 V V_S = ± 10 V	DG528	Room Full	± 0.015	- 10 - 200	10 200	- 20 - 200	20 200	
			DG529	Room Full	± 0.008	- 10 - 100	10 100	- 20 - 100	20 100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ± 10 V V_{EN} = 2.4 V	DG528	Room Full	± 0.03	- 10 - 200	10 200	- 20 - 200	20 200	
			DG529	Room Full	± 0.015	- 10 - 100	10 100	- 20 - 100	20 100	
Digital Control										
Logic Input Current	I_{AH}	V_A = 2.4 V		Room Hot	- 0.002	- 10 - 30		- 10 - 30		µA
Input Voltage High		V_A = 15 V		Room Hot	0.006		10 30		10 30	
Logic Input Current Input Voltage Low	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V $\overline{RS}$ = 0 V, $\overline{WR}$ = 0 V		Room Hot	- 0.002	- 10 - 30		- 10 - 30		
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 5		Room	0.6		1			µs
Break-Before-Make Interval	t_{OPEN}	See Figure 4		Room	0.2					
EN and $\overline{WR}$ Turn-On Time	$t_{ON(EN,WR)}$	See Figure 6 and 7		Room	1		1.5			
EN and $\overline{WR}$ Turn-Off Time	$t_{OFF(EN,RS)}$	See Figure 6 and 8		Room	0.4		1			
Charge Injection	Q	V_S = 0 V, R_y = 0 Ω, C_L = 10 µF		Room	4					pC
Off Isolation	OIRR	V_{EN} = 0 V, R_L = 1 kΩ, C_L = 15 pF V_S = 7 V_{RMS}, f = 500 kHz		Room	68					dB
Logic Imput Capacitance	C_{in}	f = 1 MHz		Room	2.5					pF
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_D = 0 V, f = 140 kHz		Room	5					
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V, V_D = 0 V f = 140 kHz	DG528	Room	25					
			DG529	Room	12					
Minimum Input Timing Requirements										
Write Pulse Width	t_W			Full		300		300		ns
A_X, EN Data Set Up time	t_S			Full		180		180		
A_X, EN Data Hold Time	t_H			Full		30		30		
Reset Pulse Width	t_{RS}	V_S = 5 V, See Figure 3		Full		500		500		
Power Supplies										
Positive Supply Current	I+	V_{EN} = V_A = 0 V		Room			2.5		2.5	mA
Negative Supply Current	I-			Room		- 1.5		- 1.5		

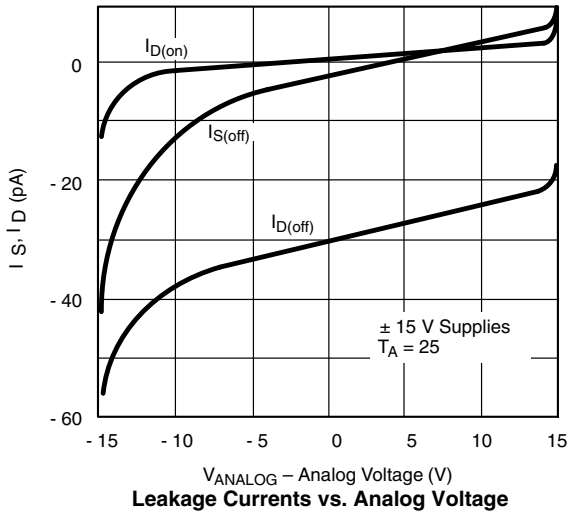
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

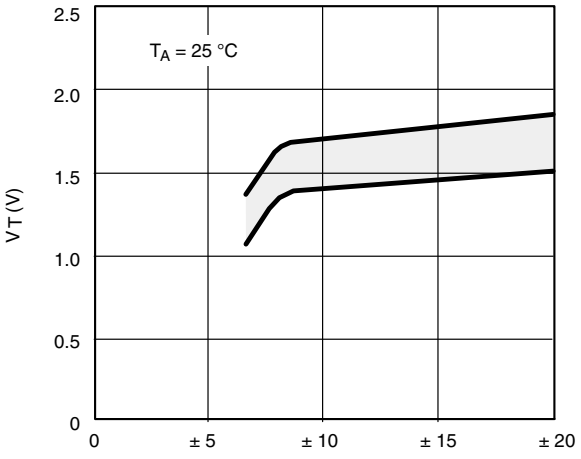
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless noted)



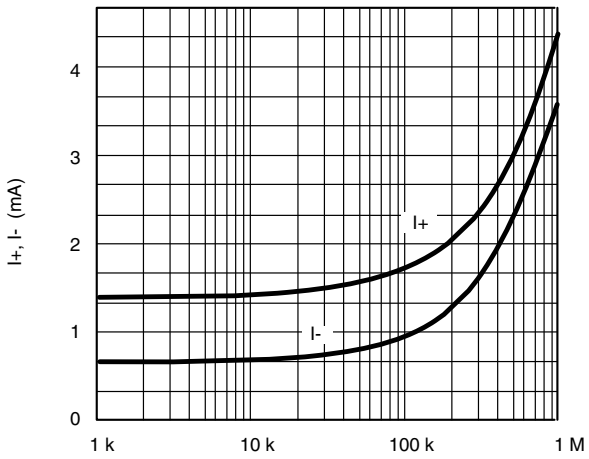
$R_{DS(on)}$ vs. V_D and Power Supply



Leakage Currents vs. Analog Voltage



Input Switching Threshold vs. V+ and V- Supply Voltages



Supply Currents vs. Toggle Frequency

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

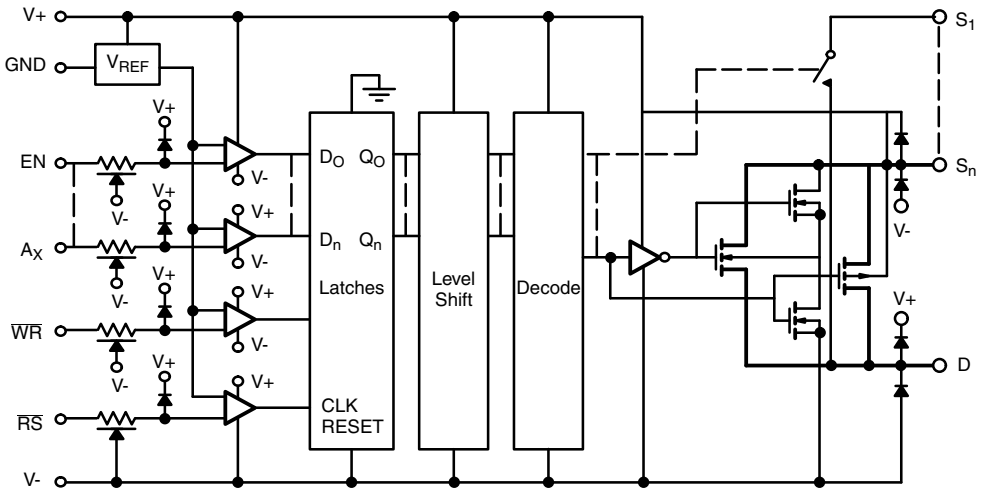


Figure 1.

DETAILED DESCRIPTION

The internal structure of the DG528/DG529 includes a 5-V logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel n- and p-channel MOSFETs (see Figure 1).

The logic interface circuit compares the TTL input signal against a TTL threshold reference voltage. The output of the comparator feeds the data input of a D type latch. The level sensitive D latch continuously places the D_X input signal on the Q_X output when the $\overline{WR}$ input is low, resulting in transparent latch operation. As soon as $\overline{WR}$ returns high, the latches hold the data last present on the D_X input, subject to the minimum input timing requirements.

Following the latches the Q_X signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting insures full on/off switch operation for any analog signal present between the V+ and V- supply rails.

The EN pin is used to enable the address latches during the $\overline{WR}$ pulse. It can be hard-wired to the logic supply or to V+ if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The $\overline{RS}$ pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The $\overline{WR}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Truth Tables).

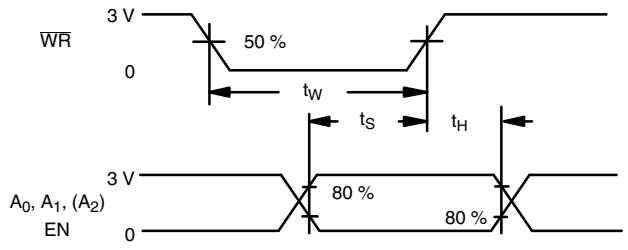


Figure 2.

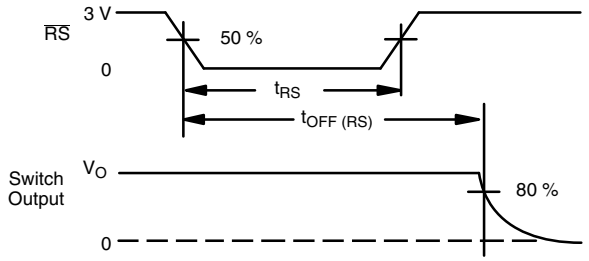


Figure 3.

TEST CIRCUITS

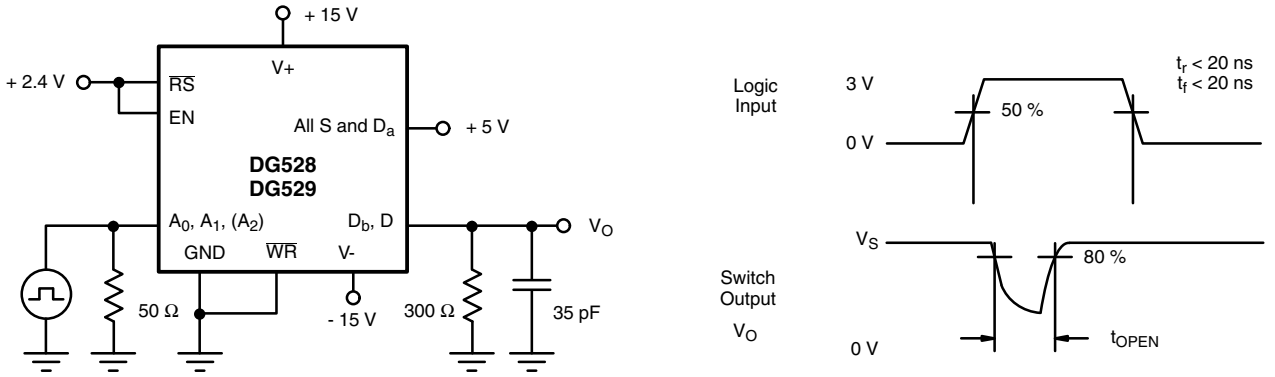


Figure 4. Break-Before-Make

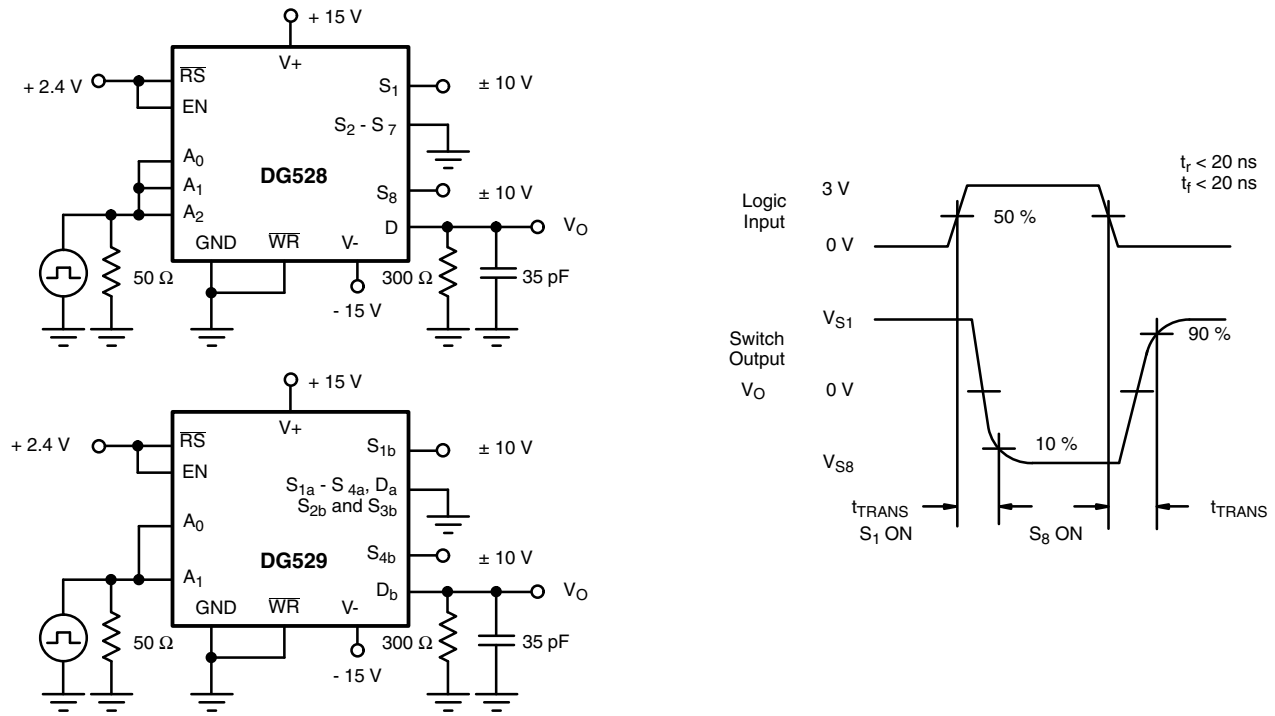
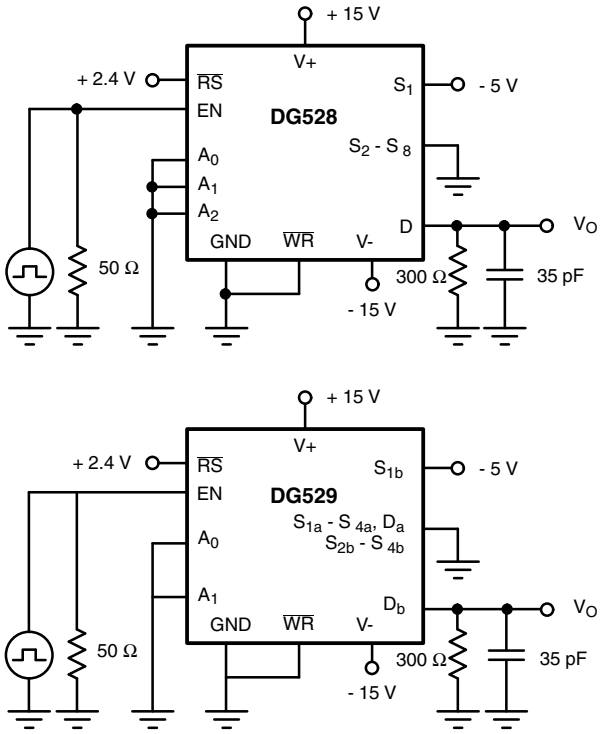


Figure 5. Transition Time

TEST CIRCUITS



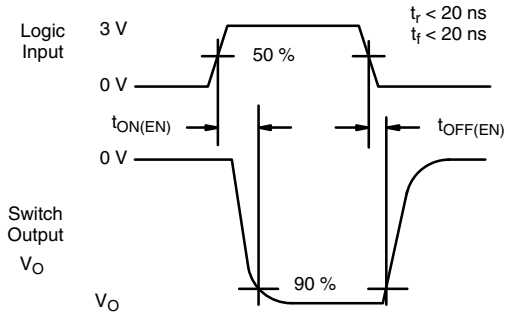
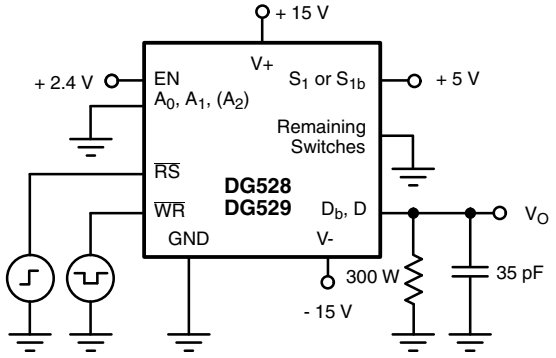


Figure 6. Enable $t_{ON/tOFF}$ Time



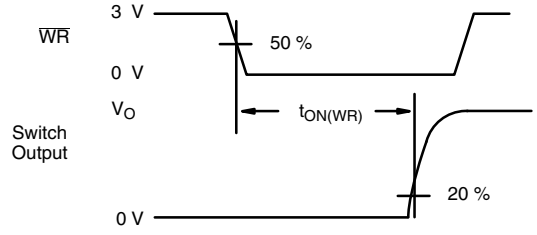


Figure 7. Write Turn-On Time $t_{ON(WR)}$

TEST CIRCUITS

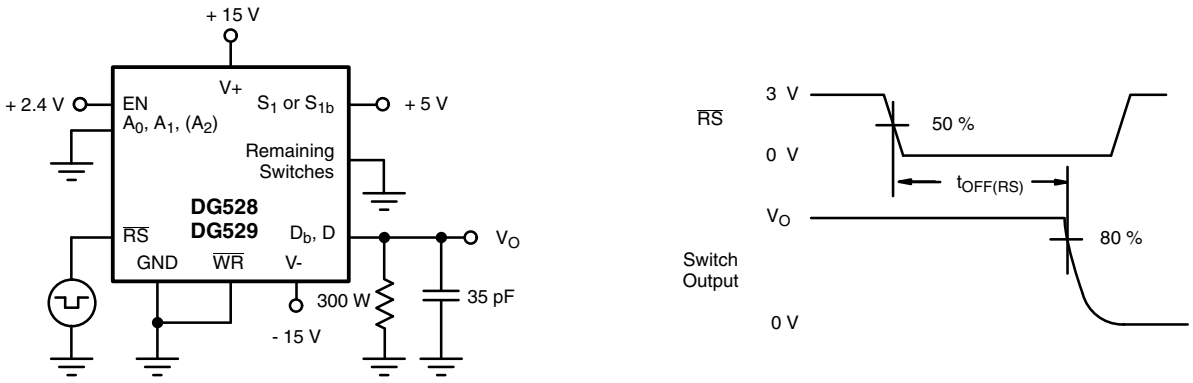


Figure 8. Reset Turn-Off Time $t_{OFF(RS)}$

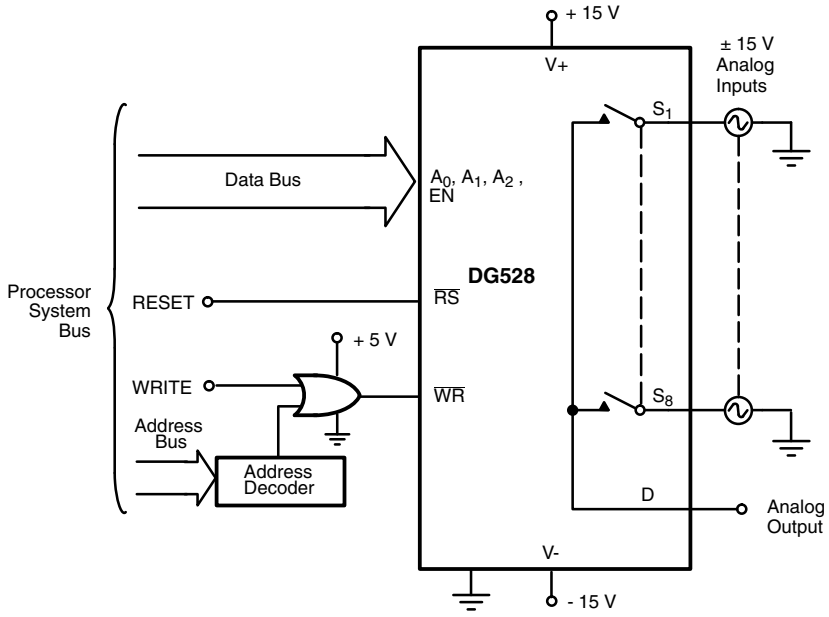


Figure 9. Bus Interface

APPLICATION HINTS[a]			
V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
20	- 20	2.4/0.8	± 20
15[b]	- 15	2.4/0.8	± 15
8[c]	- 8 (min)	2.4/0.8	± 8

Notes:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Electrical Parameter Chart based on V+ = 15 V, V- = - 15 V, V_R = GND.
c. Operation below ± 8 V is not recommended.

The DG528/DG529 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers write-only memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 on) until the microprocessor determines it is necessary to turn different switches on or turn all switches off (see Figure 9).

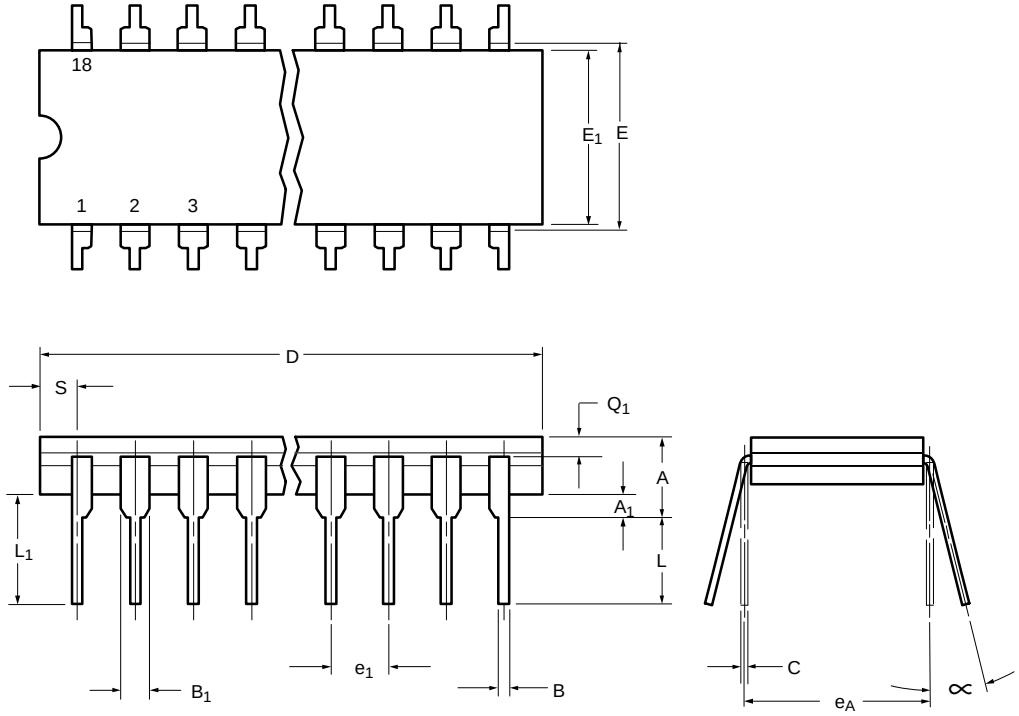
The input latches become transparent when $\overline{WR}$ is held low; therefore, these multiplexers operate by direct command of the coded switch state on A_2, A_1, A_0. In this mode the DG528 is identical to the popular DG508A. The same is true of the DG529 versus the popular DG509A.

During system power-up, $\overline{RS}$ would be low, maintaining all eight switches in the off state. After $\overline{RS}$ returned high the DG528 maintains all switches in the off state. When the system program performs a write operation to the address assigned to the DG528, the address decoder provides a $\overline{CS}$ active low signal which is gated with the WRITE ($\overline{WR}$) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the $\overline{WR}$ signal returns to the high state, (positive edge) the input latches of the DG528 save the data from the DATA BUS. The coded information in the A_0, A_1, A_2 and EN latches is decoded and the appropriate switch is turned on.

The EN latch allows all switches to be turned off under program control. This becomes useful when two or more DG528s are cascaded to build 16-line and larger multiplexers.

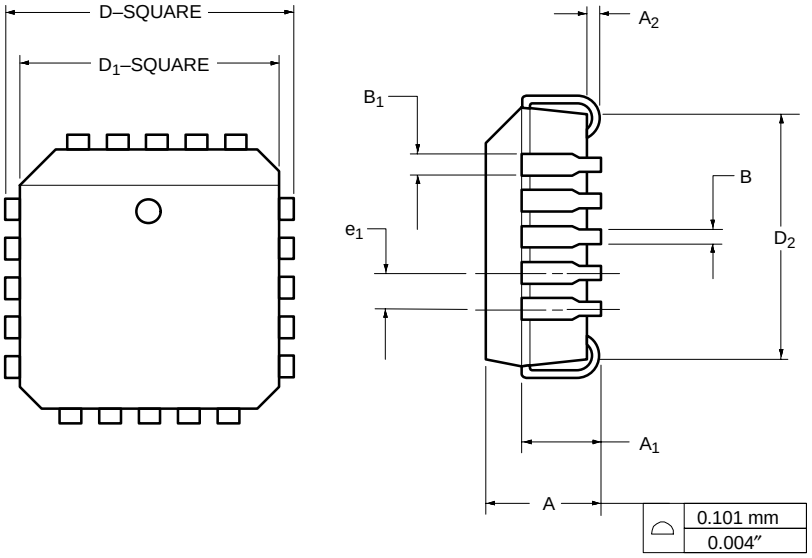
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70068.

CERDIP: 18-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A_1	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B_1	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	22.35	22.86	0.880	0.900
E	7.62	8.26	0.300	0.325
E_1	6.60	7.62	0.260	0.300
e_1	2.54 BSC		0.100 BSC	
e_A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L_1	3.81	5.08	0.150	0.200
Q_1	1.27	2.16	0.050	0.085
S	0.76	1.52	0.030	0.060
∝	0°	15°	0°	15°
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5313				

PLCC: 20-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.20	4.57	0.165	0.180
A_1	2.29	3.04	0.090	0.120
A_2	0.51	–	0.020	–
B	0.331	0.553	0.013	0.021
B_1	0.661	0.812	0.026	0.032
D	9.78	10.03	0.385	0.395
D_1	8.890	9.042	0.350	0.356
D_2	7.37	8.38	0.290	0.330
e_1	1.27 BSC		0.050 BSC	

ECN: S-03946—Rev. C, 09-Jul-01
DWG: 5306

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