DS26522DK
Dual T1/E1/J1 Transceiver Demo Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS26522DK is an easy-to-use demo kit for the DS26522 T1/E1/J1 dual transceiver. The DS26522DK is a stand-alone system. The board comes complete with a transceiver, transformer, termination resistors, configuration switches, network connectors, microprocessor, and RS-232 connector. The on-board processor and Dallas' ChipView software give point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status, as well as multiple clock and signal routing configurations.

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DEMO KIT CONTENTS

DS26522DK PCB

CD_ROM Including:

- ChipView Software
- DS26522 Definition files
- DS26522 Initialization files
- DS26522DK Data Sheet
- DS26522 Data Sheet

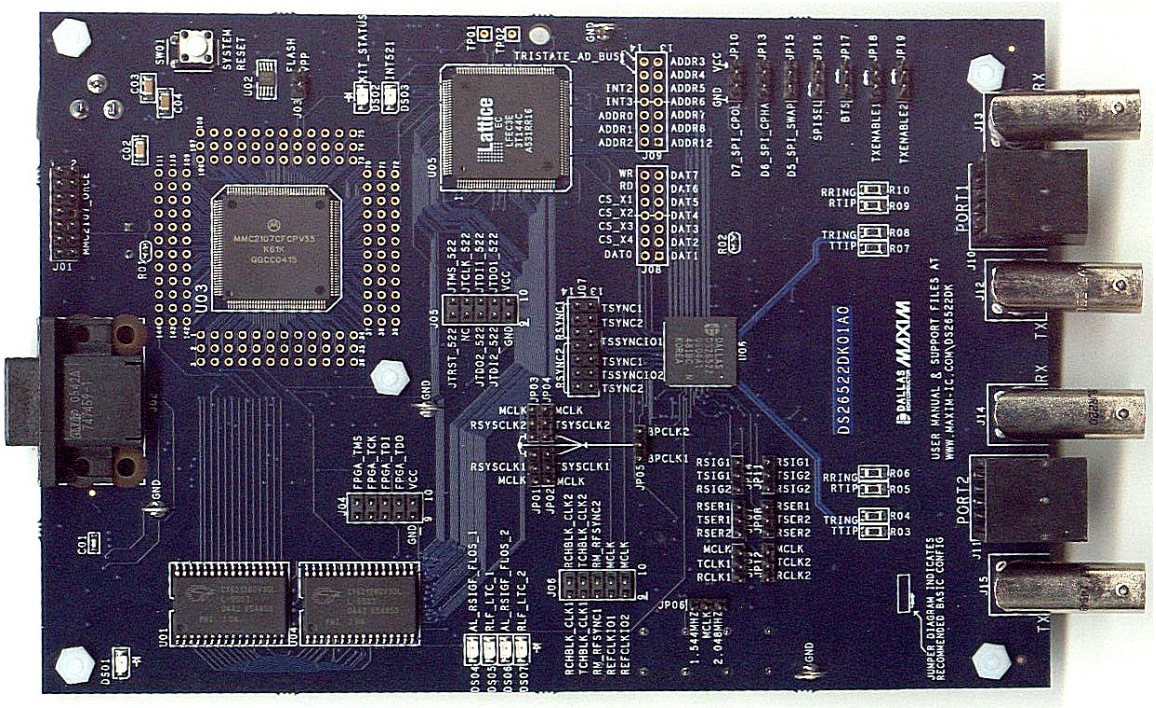
DS26522 Errata Sheet (if applicable)

FEATURES

- **Demonstrates Key Functions of DS26522 T1/E1/J1 Dual Transceiver**
- **Includes Transceiver, Transformers, and Termination Passives**
- **BNC Connections for 75Ω E1**
- **RJ48 Connector for 120Ω E1 and 100Ω T1**
- **On-Board Processor and ChipView Software Provide Point-and-Click Access to the DS26522 Register Set**
- **Accessible Address/Data Bus with Tri-State Control to Allow Interface for External Processor**
- **All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink**
- **LEDs for Loss-of-Signal and Interrupt Status**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

ORDERING INFORMATION

PART	DESCRIPTION
DS26522DK	Demo kit for DS26522



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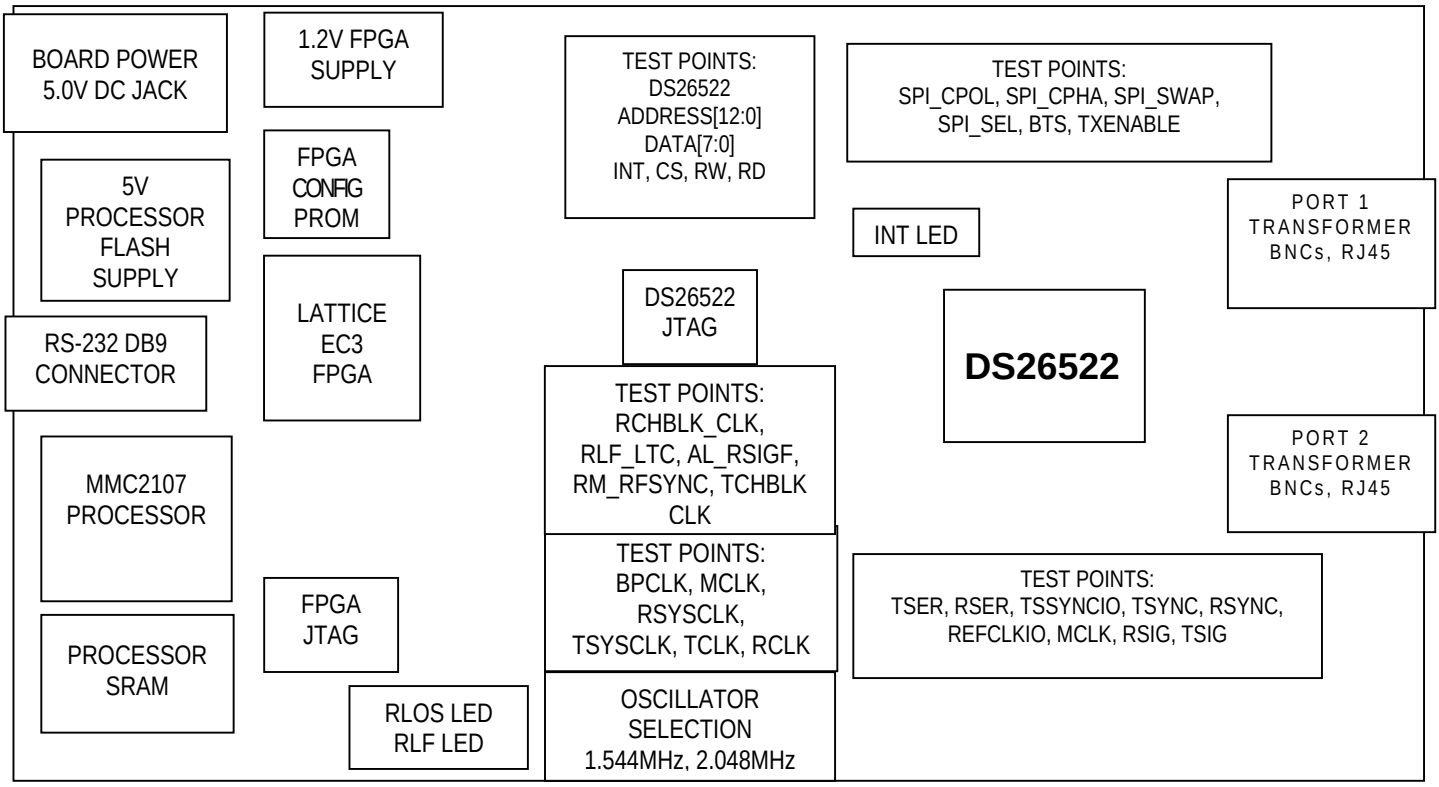
1. BOARD FLOORPLAN



2. PCB ERRATA

DS26522DK01A0
4/17/2006:
A 100pF capacitor has been added between processor reset and VCC. This was added to eliminate crosstalk issues present in the OnCE programming pod.

3. BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/DS26522DK QuickView page.

3.1 Hardware Configuration

- Supply 5.0V to the wall jack receptacle on the bottom of the PCB.
- Install the following jumpers (see Table 5-1):
  - JP06: MCLK driven by 1.544MHz for T1. (Set E1 for 2.048MHz.)
  - JP01, JP03: RSYSCLK driven by MCLK.
  - JP02, JP04: TSYSCLK driven by MCLK.
  - JP09, JP12: TCLK driven by MCLK.
  - JP16 SPI_SEL to GND. JP17 BTS to VCC. JP18, JP19 TXENABLE to VCC.
- From the **Programs** menu, launch the host application named *ChipView.exe*. Run the ChipView application. If the default installation options were used, click the **Start** button on the Windows toolbar and select **Programs** → **ChipView** → **ChipView**.

3.1.1 General

Upon power-up, the RLF and AL_LOS LEDs (red) will be lit, but the INT LED (red) will not be lit. The board draws approximately 200mA at power-up.

3.2 Quick Setup (Register View)

1) The PC loads ChipView, offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select REGISTER VIEW.
2) The program will request a definition file. Navigate to the .def files in the T1 or E1 folder, then select the file named *DS26522_GLB_T1_DEV1.def* (T1 mode) or *DS26522_GLB_E1_DEV1.def* (E1 mode).
   Note: Through the *Links* section, this will also load the LIU def file and framer def file.
3) Repeat Step 2 for *DS26522_GLB_T1_DEV2.def* (or *DS26522_GLB_E1_DEV2.def)*.
4) The **Register View Screen** will appear, showing the register names, acronyms, and values for the DS26522.
5) Predefined register settings for several functions are available as initialization files.
   - .ini files are loaded by selecting the menu **File→Reg Ini File→Load Ini File**.
   - Load the .ini file *Load_T1_LBO0_0_133_impMatchOn_DEV1.ini* (T1 mode) or *Load_E1_75_impMatchOn_DEV1.ini* (E1 mode).
   - Load the .ini file *Load_T1_LBO0_0_133_impMatchOn_DEV2.ini* (T1 mode) or *Load_E1_75_impMatchOn_DEV2.ini* (E1 mode).
6) After loading the .ini file, the following may be observed:
   - The DS26522 begins transmitting AIS with impedance match.
   - The AL_LOS LEDs extinguishes upon external loopback.

3.2.1 Miscellaneous

The DS26522 uses three register definition files. All three files are loaded when the *DS26522_GLOBAL*.def* file is loaded. Individual files are selected from the **Def File Selection** menu in ChipView.

4. ADDRESS MAP

The on-board microcontroller is configured to start the user address space at 0x81000000. All offsets given in Table 4-1 are relative to the beginning of the user address space.

Table 4-1. Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Board identification and FPGA test registers
0X2000 to 0X3FFF	DS26522	DS26522 framer, LIU, and BERT registers on CS1
0X4000 to 0X5FFF	DS26522	DS26522 framer, LIU and BERT registers on CS2

5. TEST POINTS AND CONNECTORS

The DS26522DK has several connectors, test points, oscillators, and jumpers. Table 5-1 provides a description of these signals, given in order of appearance on the PCB from left to right, then top to bottom (with the board held so that the RS-232 connector is on the top edge).

Table 5-1. Main Board PCB Configuration

SILKSCREEN REFERENCE	FUNCTION	DEFAULT SETTING	SCHEMATIC PAGE	DESCRIPTION
JB01 (PCB bottom side)	Power supply	5.0V	3	System V_{DD}. Always connected to power supply.
DS01	LED	On (green)	3	Power OK LED.
J02	RS-232 Connector	Connected to host PC	6	Used for communication with host PC. Basic setting is 57.6K baud, 8 bits, no stop bit, 1 parity bit (57.6, 8, N, 1).
J01	OnCE BDM Connector	—	6	OnCE debug connector for MMC2107 processor.
SW01	System Reset	—	4	System reset. Connects to all device reset pins.
J03	Flash VPP Jumper	Not Installed	6	Provides flash programming voltage (5V) to processor.
J04	Lattice FPGA	—	9	JTAG connector for Lattice EC3 FPGA.
DS04, DS06	LED	—	11	DS26522 LEDs. Analog loss or receive signaling freeze or framer LOS.
DS05, DS07	LED	—	11	DS26522 LEDs. Receive loss of frame or loss of transmit clock.
J05	DS26522 Test points	—	10	DS26522 JTAG chains.
J06	DS26522 Test points	—	14	DS26522 test points for RCHBLK, TCHBLK, RMSYNC, REFCLKIO.
JP01, JP03	RSYSCLK Selection	Jumpered Pins 1+2	14	RSYSCLK selection: MCLK (default), BPCLK.
JP02, JP04	TSYSCLK Selection	Jumpered Pins 1+2	14	TSYSCLK selection: MCLK (default), BPCLK.
JP05	BPCLK MUX	Jumpered Pins 1 + 2	14	BPCLK mux, driven to pin 3 of JP01, JP02, JP03, JP04.
J07	DS26522 Test points	—	14	DS26522 test points for RSYNC, TSYNC, and TSSYNCIO.
YB01, YB02 (PCB bottom side)	Oscillators	—	14	Oscillators for 2.048MHz and 1.544MHz.
J08, J09	Test points	—	8	Test points for DS26522 address/data bus and control lines.

SILKSCREEN REFERENCE	FUNCTION	DEFAULT SETTING	SCHEMATIC PAGE	DESCRIPTION
J09.12 + J09.14	Bus Tri-state	Not Jumpered	8	Install jumper to tri-state the FPGA pins that connect to the DS26522.
JP06	MCLK Selection	Jumpered Pins 2+3	14	MCLK Selection: 1.544MHz, 2.048MHz (default).
JP09, JP12	TCLK Selection	Jumpered Pins 1+2	14	TCLK Selection: MCLK (default), RCLK.
JP07, JP08	TSER Selection	Not Jumpered	14	TSERx Selection: RSER2, RSER1.
JP14, JP11	TSIG Selection	Not Jumpered	14	TSIGx Selection: RSIG2, RSIG1.
JP10	SPI_CPOL Bias	Not Jumpered	10	SPI_CPOL Selection: pulldown, pullup.
JP13	SPI_CPHA Bias	Not Jumpered	10	SPI_CPHA Selection: pulldown, pullup
JP15	SPI_SWAP Bias	Not Jumpered	10	SPI_SWAP Selection: pulldown, pullup
JP16	SPI_SEL Bias	Jumpered Pins 1+2	10	SPI_SEL Selection: pulldown (default), pullup.
JP17	BTS Bias	Jumpered Pins 2+3	10	BTS Selection: pulldown, pullup (default).
JP18, JP19	TXENABLE Bias	Jumpered Pins 2+3	10	TXENABLE Selection: pulldown, pullup (default).
J15 + J14	Network BNC	—	12	Port 2 BNC for 75Ω network connection and RJ48 network connection.
J11	Network RJ48			
J12 + J13	Network BNC	—	13	Port 1 BNC for 75Ω network connection and RJ48 network connection.
J10	Network RJ48			

6. ADDITIONAL INFORMATION/RESOURCES

6.1 DS26522 Information

For more information about the DS26522, refer to the DS26522 data sheet at www.maxim-ic.com/DS26522.

6.2 DS26522DK Information

For more information about the DS26522DK including software downloads, refer to the DS26522DK Quick View page at www.maxim-ic.com/DS26522DK.

6.3 Technical Support

For additional technical support, e-mail your questions to telecom.support@dalsemi.com.

7. COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C01, CB08, CB11-CB13, CB16, CB18, CB21, CB31, CB34-CB36, CB38-CB40	15	0.1µF ±10%, 16V ceramic capacitors (0603)	Phycomp	06032R104K7B20D
C02	1	1µF ±10%, 16V ceramic capacitor (1206)	Panasonic	ECJ-3YB1C105K
C03, C04, CB01, CB02	4	10F ±20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
CB03, CB05	2	68µF ±20%, 16V tantalum capacitors (D case)	Panasonic	ECS-T1CD686R
CB04	1	470µF ±20%, 6.3V tantalum capacitor (D case)	Digi-Key	399-3002-1-ND
CB06, CB09, CB15, CB17, CB19, CB25, CB27, CB29, CB32, CB41, CB42	11	10µF ±20% 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
CB07, CB24, CB26, CB28, CB43, CB44	6	0.1µF ±20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
CB10, CB14, CB20, CB22, CB23, CB30, CB33, CB37	8	4.7µF, 6.3V multilayer ceramic capacitors (0603)	Digi-Key	ECJ-1VB0J475M
CB45, CB46	2	560pF ±5%, 50V ceramic capacitors (1206)	Digi-Key	478-1489-2-ND
DB01	1	1A, 40V Schottky diode	Internatioanl Rectifier	10BQ040
DS01	1	Green LED (SMD)	Panasonic	LN1351C
DS02	1	Green LED (SMD)	Panasonic	LN1351C
DS03–DS07	5	Red LEDs (SMD)	Panasonic	LN1251C
GND_TP02, GND_TP19–GND_TP22, GND_TP24	6	Standard ground clip	Keystone Electronics	4954
H01, H02, H04, H07, h08, H09	6	Kit, 4-40 hardware, 0.50 nylon standoff and nylon hex-nut	—	4-40KIT4
J01	1	100-mil 2-7 position jumper	Lab Stock	—
J02	1	DB9 right-angle connector (long case)	AMP	747459-1
J03	1	100-mil 2-position jumper	Lab Stock	—
J04, J05, J06	3	10-pin terminal strip headers (dual row, vertical)	Samtec	TSW-105-07-T-D
J07	1	14-pin header (dual row, vertical)	Samtec	HDR-TSW-107-14-T-D
J08, J09	2	14-pin headers (dual row, vertical) **NON POPULATED**	Samtec	NOPOP-HDR-TSW-107-14-T-D

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
J10, J11	2	8-pin single-port connectors (RJ48)	Molex	15-43-8588
J12–J15	4	5-pin right-angle BNC connectors	Trompetor	UCBJR220
JB01	1	2.1mm/5.5mm closed frame power jack, high current (right angle PCB, 24VDC at 5A) Also requires 5V AC-DC adapter. Input: 100–240VAC, 50–60Hz, 0.6A. Output: DC 5V, 2.6A. PN DMS050260-P5P-SZ. Model 3Z-161WP05	CUI Inc.	PJ-002AH
JP01–JP09, JP10–JP19	19	3 position jumpers (100 mils)	Lab Stock	—
R01, R02, RB28, RB41, RB42, RB43, RB48–RB52	11	1.0kΩ ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ102V
R03–R09, R10, RB09	9	0Ω ±5%,1/8W resistors (1206)	Panasonic	ERJ-8GEYJ0R00V
RB01–RB06, RB11–RB17, RB20, RB21, RB23, RB30	17	10kΩ ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
RB07	1	1.0MΩ ±5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ105V
RB08, RB24, RB32–RB35	6	330Ω ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V
RB10, RB19, RB25, RB26, RB31, RB38, RB39, RB40	8	10kΩ ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
RB18	1	1.0kΩ ±5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ102V
RB22	1	330Ω ±5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ331V
RB27	1	0.0Ω ±5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEY0R00V
RB29	1	10kΩ ±1%, 1/10W resistor (0805)	Panasonic	ERJ-6ENF1002V
RB36, RB37	2	30Ω ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ300V
RB44–RB47	4	61.9Ω ±1%, 1/10W resistors (0805)	Panasonic	ERJ-6ENF61R9V
RB53, RB54	2	51.1Ω ±1%, 1/10W resistors (0805)	Panasonic	ERJ-6ENF51R1V
RPB01–RPB07	7	30Ω ±5% 4-pack resistors (0402)	Panasonic	EXB-N8V300JX
SW01	1	4-pin single-pole switch	Panasonic	EVQPAE04M
TB01, TB02	2	16-pin SMT transformers	Pulse Engineering	TX1099
TP01, TP02	2	1 plated hole test points **DO NOT STUFF**	Lab Stock	—
U01, U04	2	Cypress SRAM	Lab Stock	—
U02	1	3V to 5V Regulating charge pump	Maxim	MAX1686HEUA
U03	1	Processor	Freescale Semiconductor	MMC2107

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
U05	1	1.2V FPGA (144-pin, 20mm x 20mm TQFP)	Lattice	LFEC3E-3T144C
U06	1	Dual T1/E1/J1 transceiver (144-pin, 12mm x 12mm CSBGA)	Dallas Semiconductor	DS26522
UB01	1	Dual RS-232 transceivers with 3.3V/5V internal capacitors	Maxim	MAX3233E
UB02	1	Linear regulator (1.5W, 3.3V or adjustable, 1A, 16-pin TSSOP-EP)	Maxim	MAX1793EUE-33
UB03	1	Microprocessor voltage monitor (2.93V reset, 4-pin SOT143)	Maxim	MAX811SEUS-T
UB04	1	2Mb High-speed serial flash memory (2.7V to 3.6V, 8-pin SO)	Atmel	AT25F2048N-10SU-2.7
UB05	1	300mA LDO regulator with $\overline{\text{RESET}}$ (1.20V output, 6-pin thin SOT23-6)	Maxim	MAX1963EZT120-T
UB06, UB07	2	High-speed buffers	Fairchild	NC7SZ86
XB01	1	8.0MHz low-profile crystal	ECL	EC1-8.000M
YB01	1	3.3V 1.544MHz crystal clock oscillator	SaRonix	NTH 039A3-1.5440
YB02	1	3.3V 2.048MHz crystal clock oscillator	SaRonix	NTH 039A3-2.0480

8. SCHEMATICS

The DS26522DK schematics are featured in the following 14 pages.

Maxim/Dallas Semiconductor cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim/Dallas Semiconductor product. No circuit patent licenses are implied. Maxim/Dallas Semiconductor reserves the right to change the circuitry and specifications without notice at any time.

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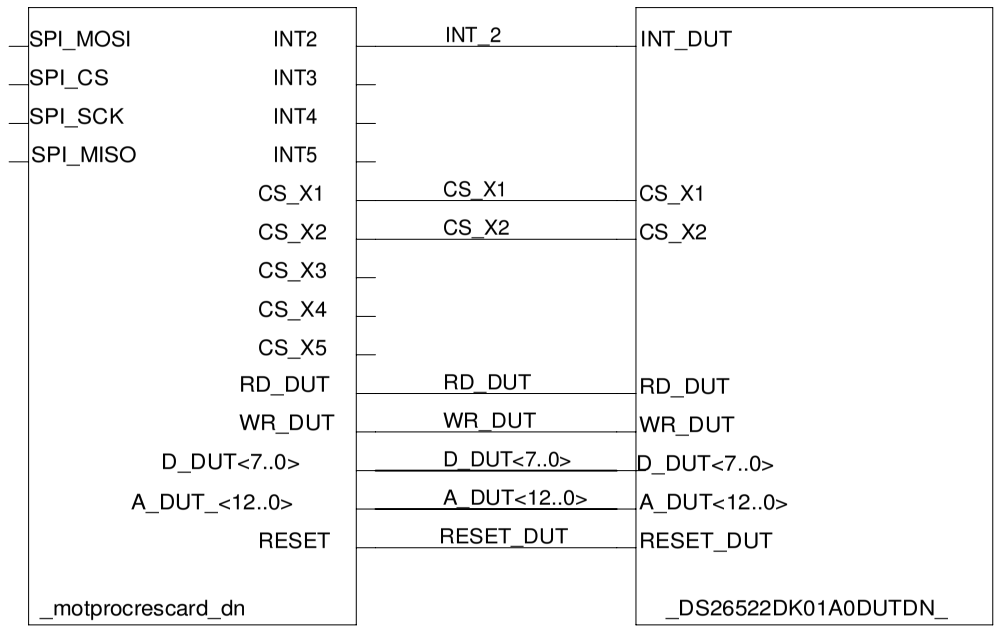
MICROPROCESSOR HIERARCHY BLOCK
PAGES 04-09

DS26522 HIERARCHY BLOCK
PAGES 10-14 I9



CONTENTS

PAGE 01: DS26522 DESIGN KIT TOP LEVEL HIERARCHY BLOCKS
PAGE 02: DECOUPLING / MOUNTING HOLES

HIERARCHY BLOCKS:

PAGES 03-03: POWER SUPPLY
PAGES 04-09: MICROPROCESSOR AND INTERFACE
PAGES 10-14: DS26522 DEVICE, LINE BUILDOUT AND TESTPOINTS

NOTES: EACH HIERARCHY BLOCK IS INDEPENDENT OF THE NEXT.
ONLY SIGNALS WITH IMPORT/OUTPORT CONNECTORS HAVE CONNECTION OUTSIDE THE HIERARCHY BLOCK. THESE SIGNALS APPEAR AS PINS ON THE HIERARCHY BLOCK CONNECTOR

TITLE: DS26522DK01A0 DS26522DK TOP LEVEL	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 1/14(TOTAL)

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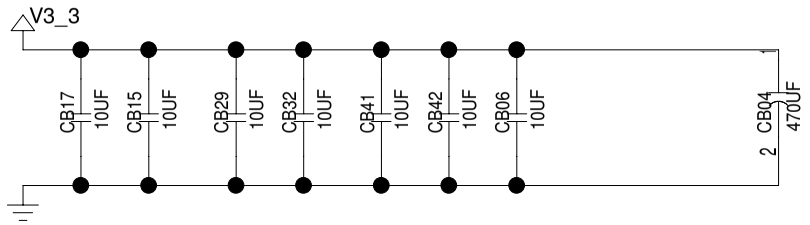
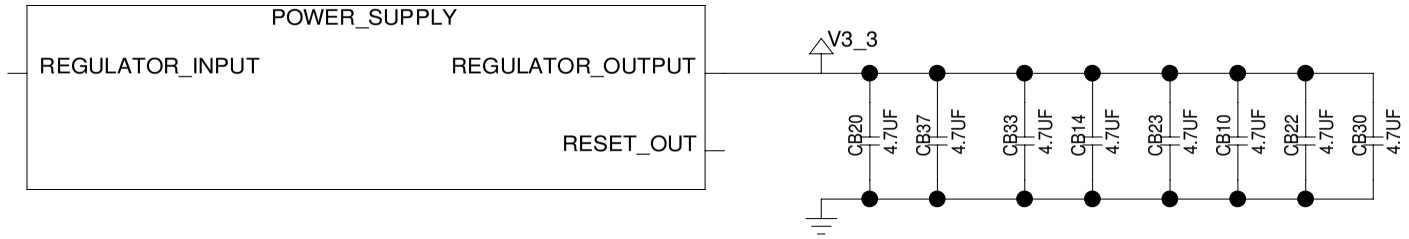
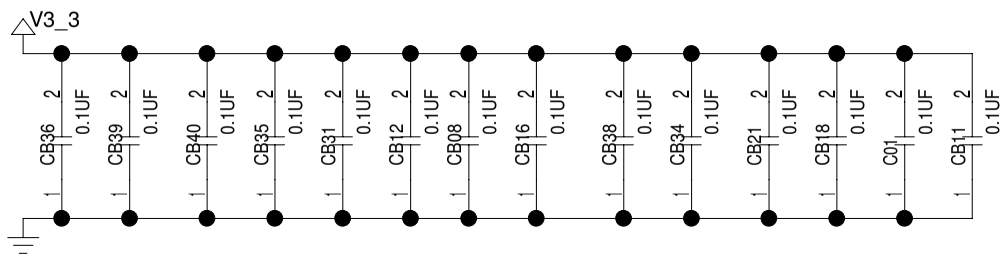


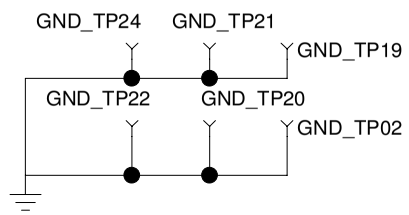
H09 H04 H07 H01 H02 H08

POWER SUPPLY HIERARCHY BLOCK

PAGES 03-03







TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 2/14(TOTAL)

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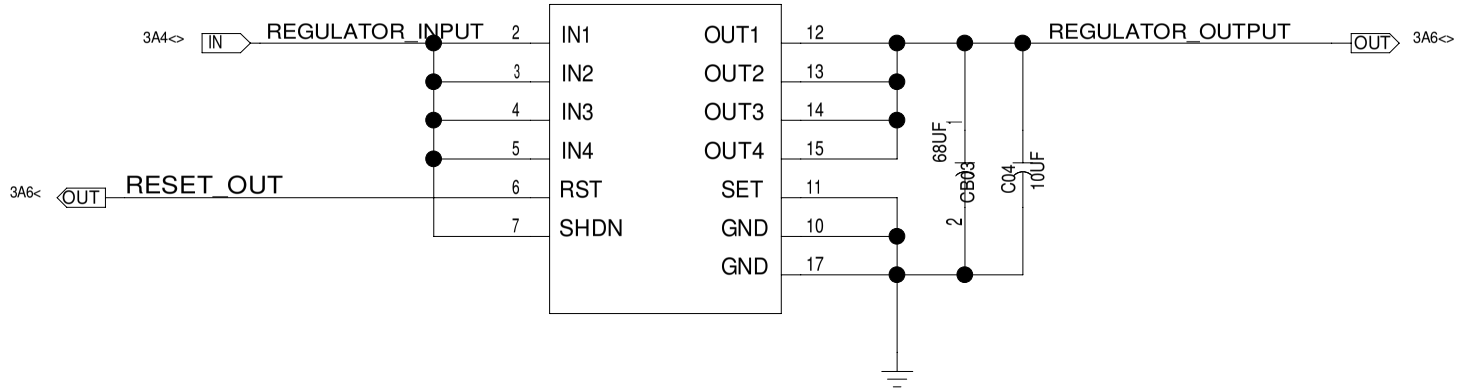
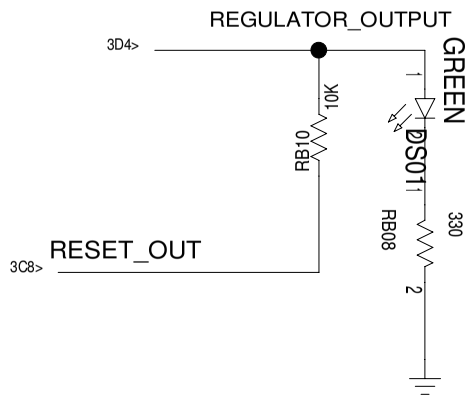
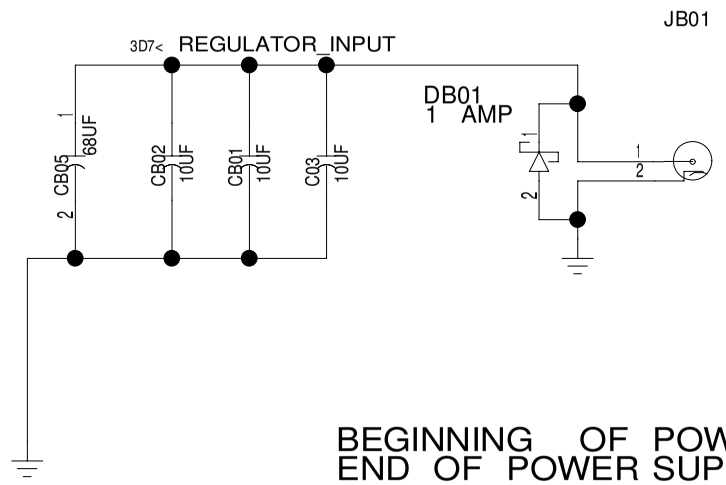
3.3V 1% REGULATOR

3.3V

UB02
MAX1793_U







5V DC POWER SUPPLY
REVERSE BIAS PROTECTION

BEGINNING OF POWER SUPPLY HIERARCHY BLOCK
END OF POWER SUPPLY HIERARCHY BLOCK

TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 1/1(BLOCK) 3/14(TOTAL)

BLOCK NAME: power_supply_1amp_dn. PARENT BLOCK: _ds26522topdn_\

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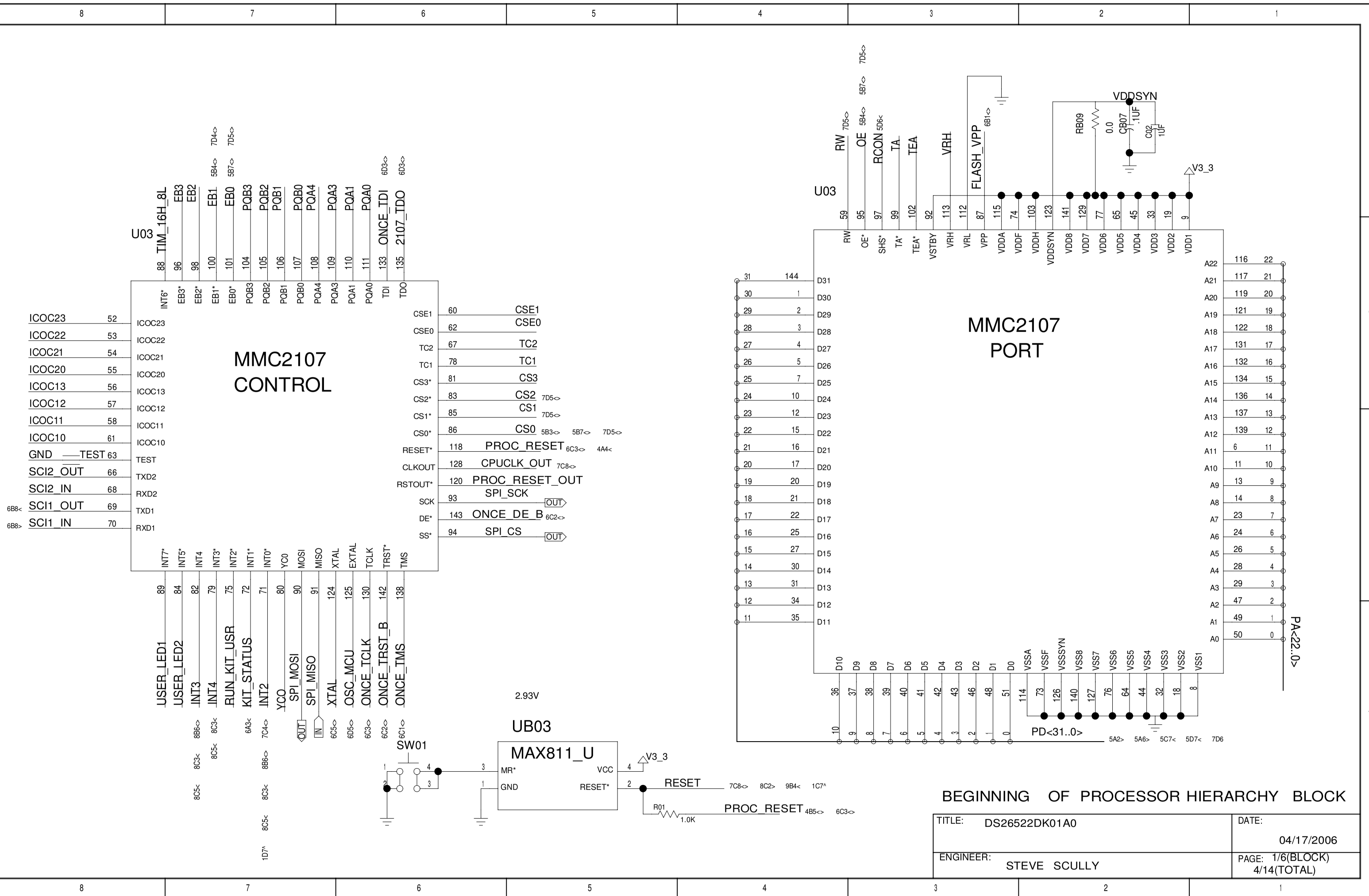


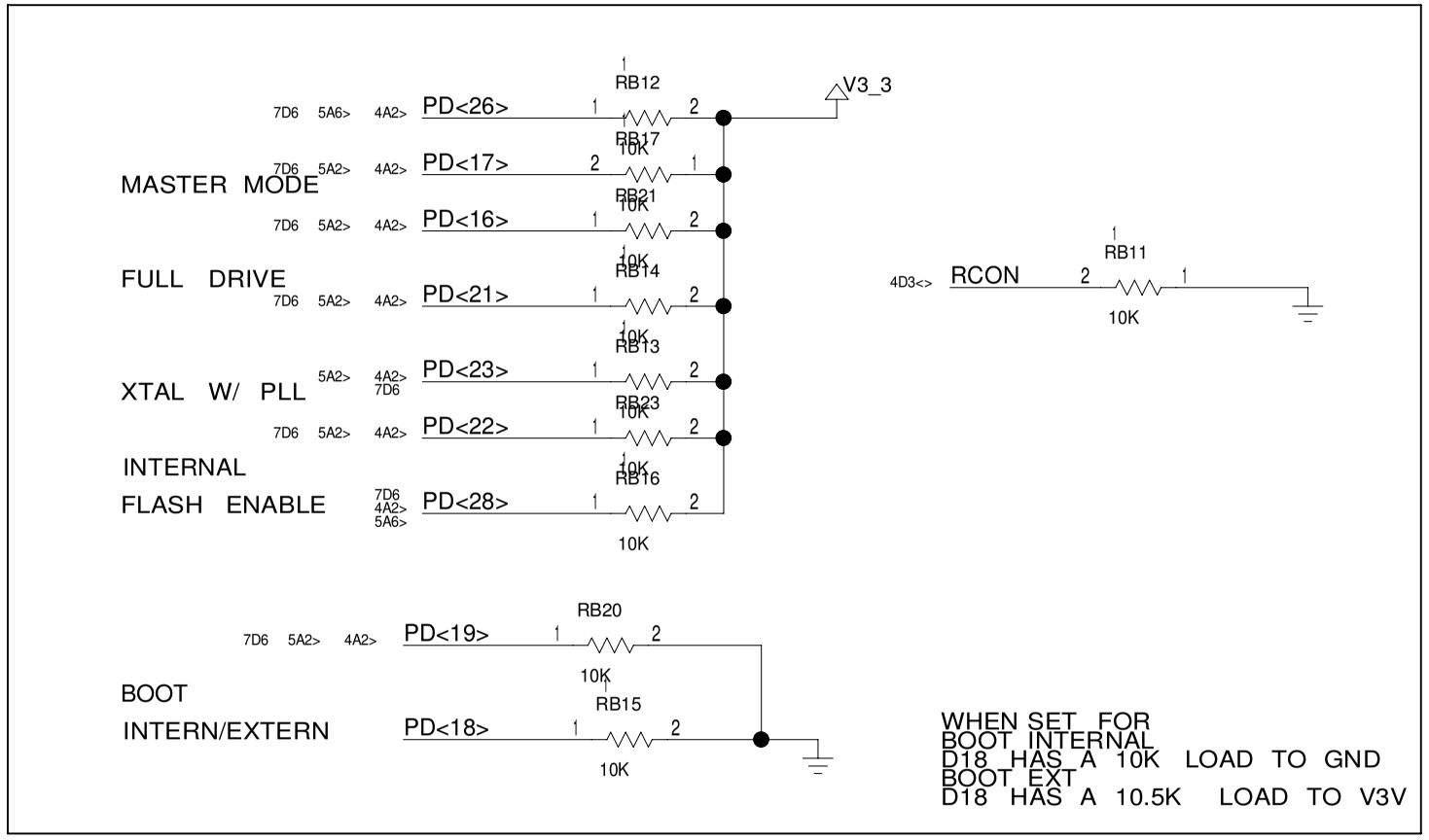
BEGINNING OF PROCESSOR HIERARCHY BLOCK

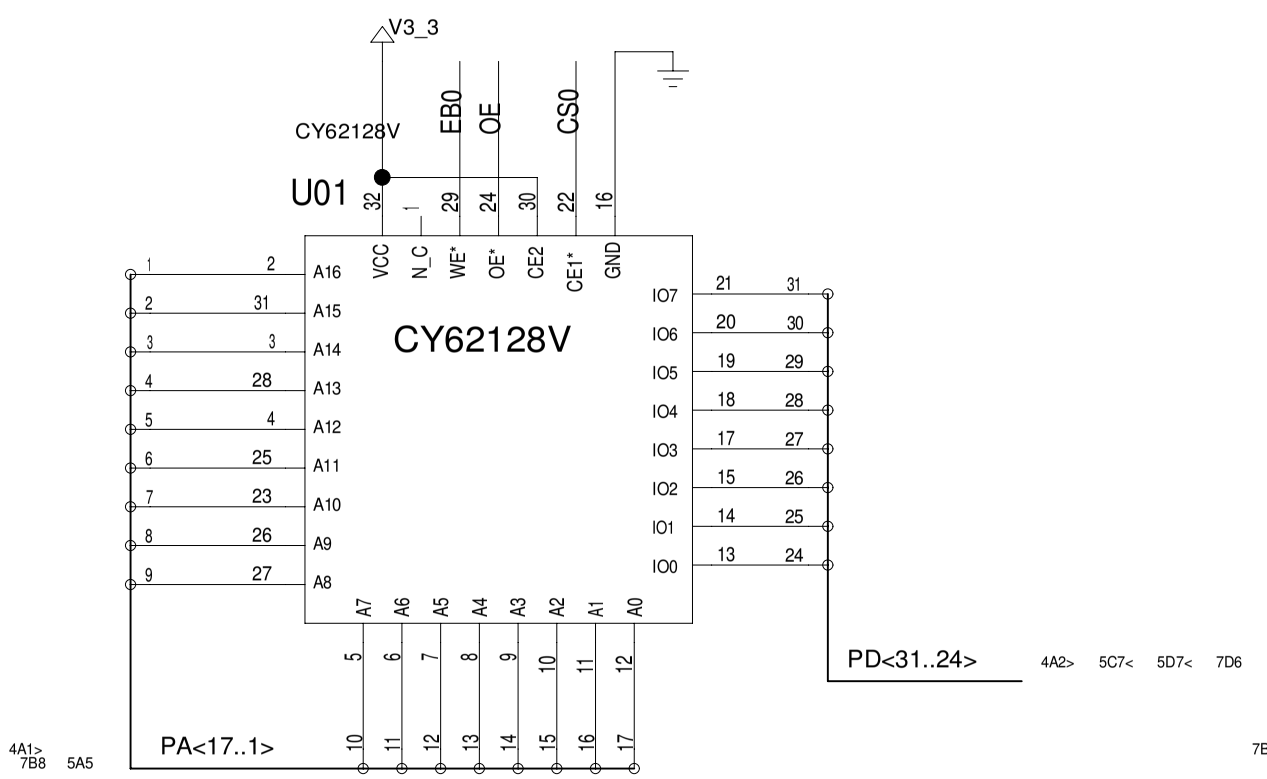
TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 1/6(BLOCK) 4/14(TOTAL)

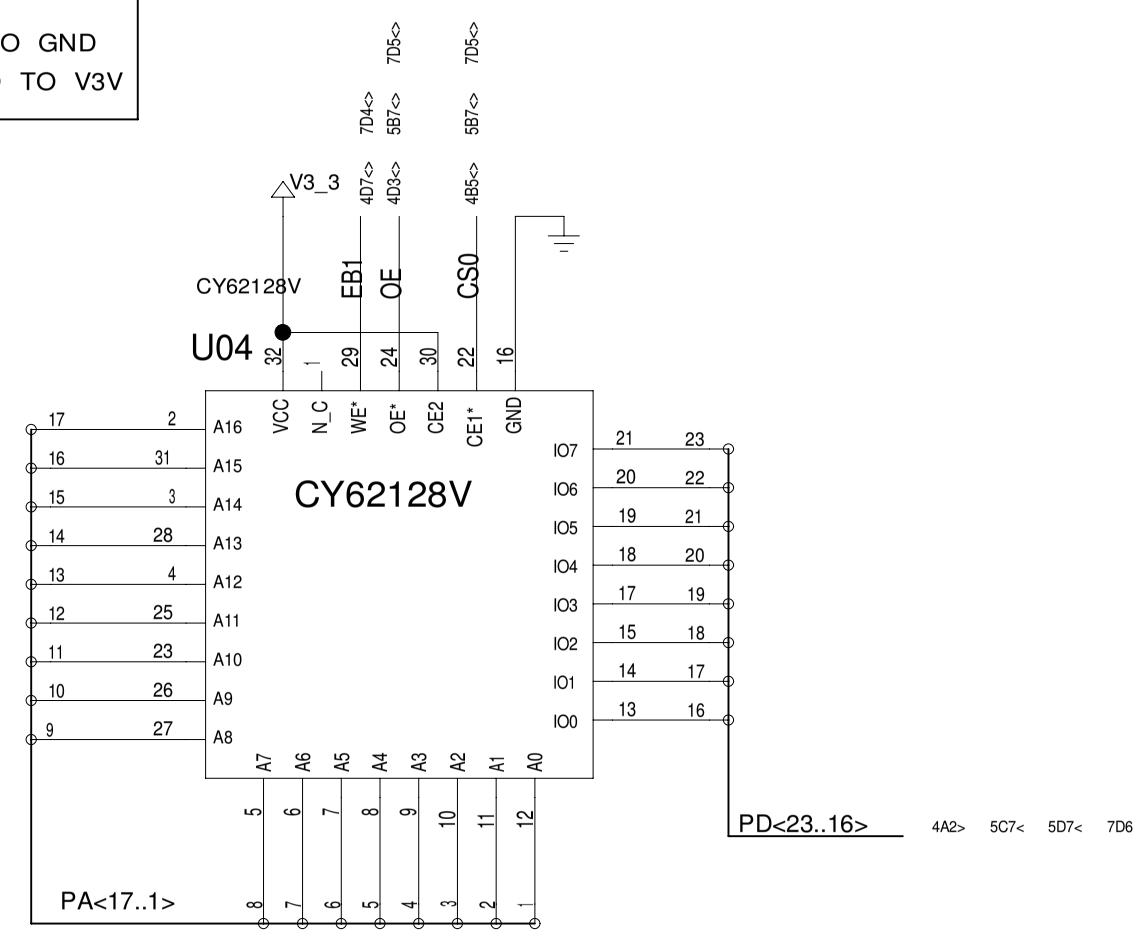
BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _ds26522topdn_\

PRINTED Fri Aug 04 13:58:16 2006

RESET CONFIGURATION







TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 2/6(BLOCK) 5/14(TOTAL)

XB01

8.0MHZ

OSC_MCU 4A6<>

RB07 1.0M

PLACE PADS FOR CAP
BUT DO NOT POPULATE

XTAL 4A7<>

V3_3

RB01 10K

RB05 10K

J01

CON14P

CON14P

4D6<> ONCE_TDI 1 2

4D6<> 2107_TDO 3 4

4A6<> ONCE_TCLK 5 6

7 8 ALIGN KEY

4A4< 4B5<> V3_3 PROC_RESET 9 10 ONCE_TMS 4A6<>

11 4B5<> 12 ONCE_DE_B

13 4A6<> 14 ONCE_TRST_B

RB06 10K

NOTE: A 100PF CAPACITOR
HAS BEEN ADDED BETWEEN PROC_RESET AND VCC
THIS ADDITION IS NOT SHOWN IN THE SCHEMATIC
(SEE ERRATA SECTION OF DESIGN KIT USER MANUAL)

V3_3

UB01

MAX3233E

4B8<> SCI1_OUT	4 T1IN	R2IN 20	
	1 R2OUT	T2OUT 19	
	2 INVALID*	GND 18	
	3 T2IN	V- 17	
	5 FORCEON	C2- 16	
4B8<> SCI1_IN	6 R1OUT	C2+ 15	
6A8<> PRT1_OUT	7 T1OUT	C1- 14	
6A8<> PRT1_IN	8 R1IN	C1+ 13	
	9 VCC	V+2 12	
	10 FORCEOFF*	V+1 11	

CB13 0.1UF

MAX1686_U

U02

V3_3 IN SHDN V3/5* OUT CXN CXP GND PGND

J03

RB18 1.0K

FLASH_VPP 4D3<

CB09 10UF

V3_3

RB02 10K

RB03 10K

RB04 10K

J02

PRT1_OUT 6B8> 2 B

PRT1_IN 6B8< 3 C

4 D

5 E

A 1

F 6

G 7

H 8

J 9

CONN_DB9P

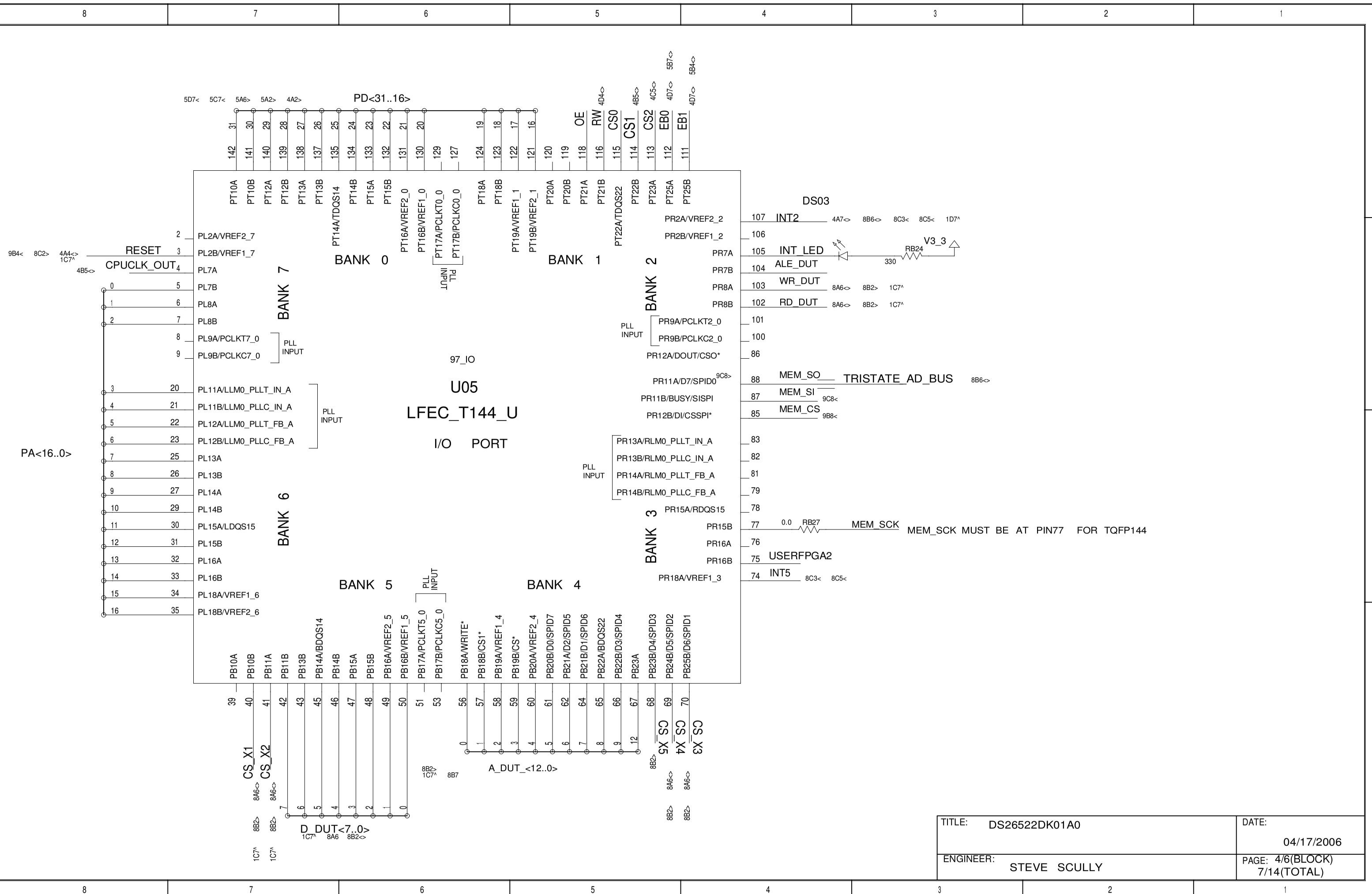
DS02

4A7<> KIT_STATUS RB22 330 GREEN

TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 3/6(BLOCK) 6/14(TOTAL)

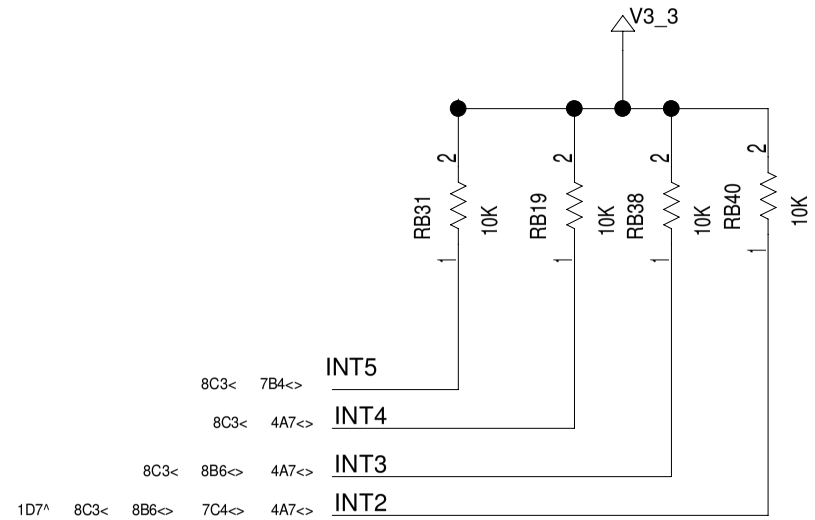
BLOCK_NAME: motprocrescard_dn. PARENT_BLOCK: \ ds26522topdn \

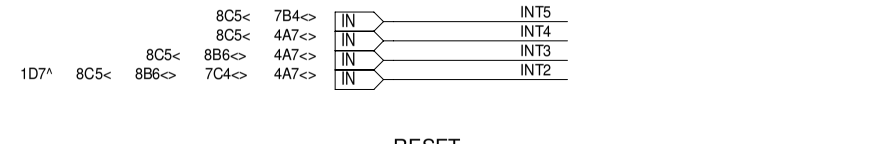
CR-7 : @_ZTOP_LIB_DS26522TOPDN_\(SCH_1):PAGE1_I6@_ZTOP_LIB_MOTPROCRESCARD_DN\(SCH_1):PAGE4

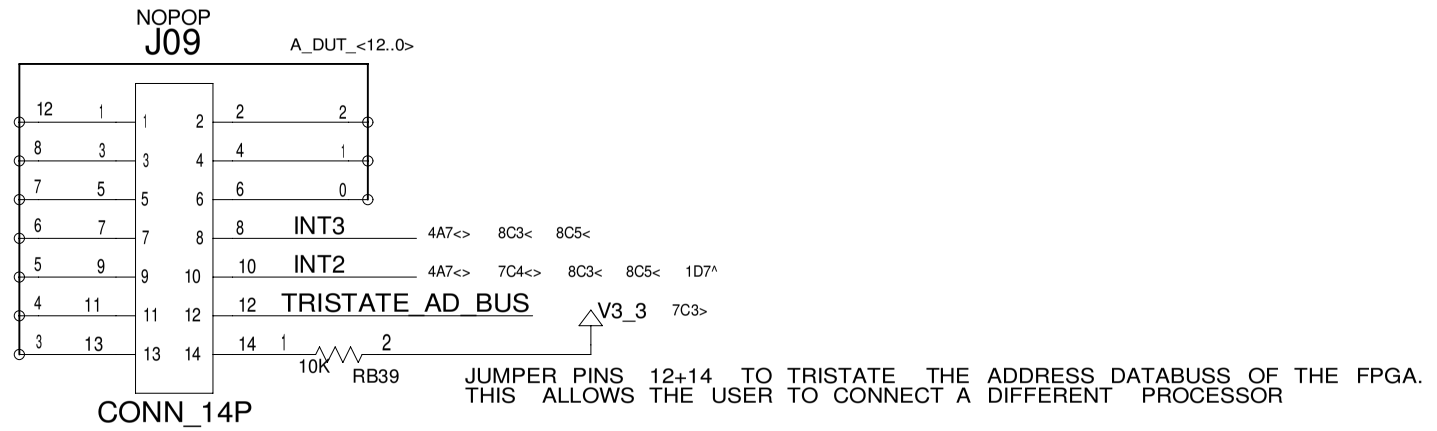


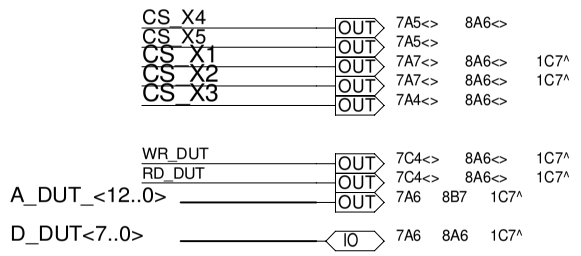
TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 4/6(BLOCK) 7/14(TOTAL)

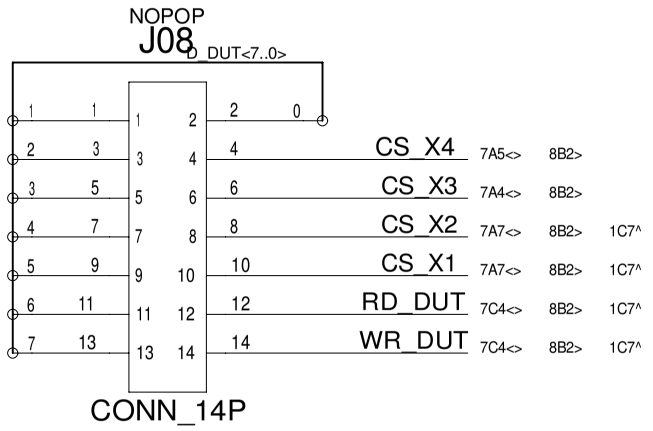
BLOCK NAME: motprocrescard_dn. PARENT BLOCK: \ ds26522topdn \







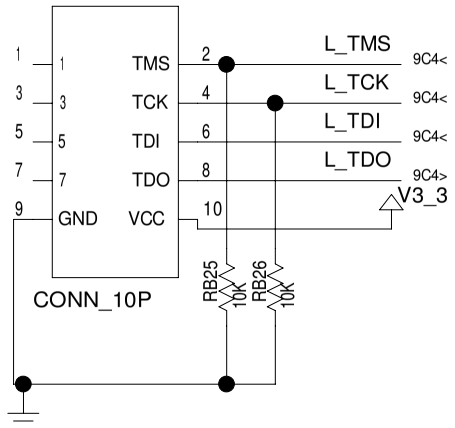




TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 5/6(BLOCK) 8/14(TOTAL)

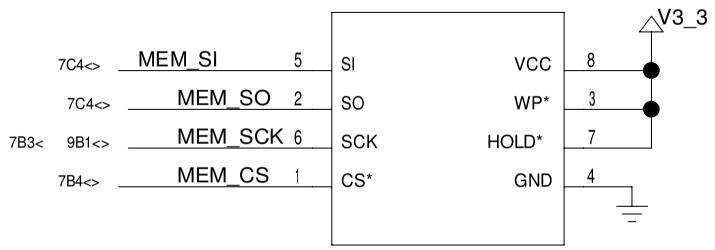
BLOCK_NAME: motprocrescard_dn PARENT_BLOCK: \ ds26522topdn \

I24
J04

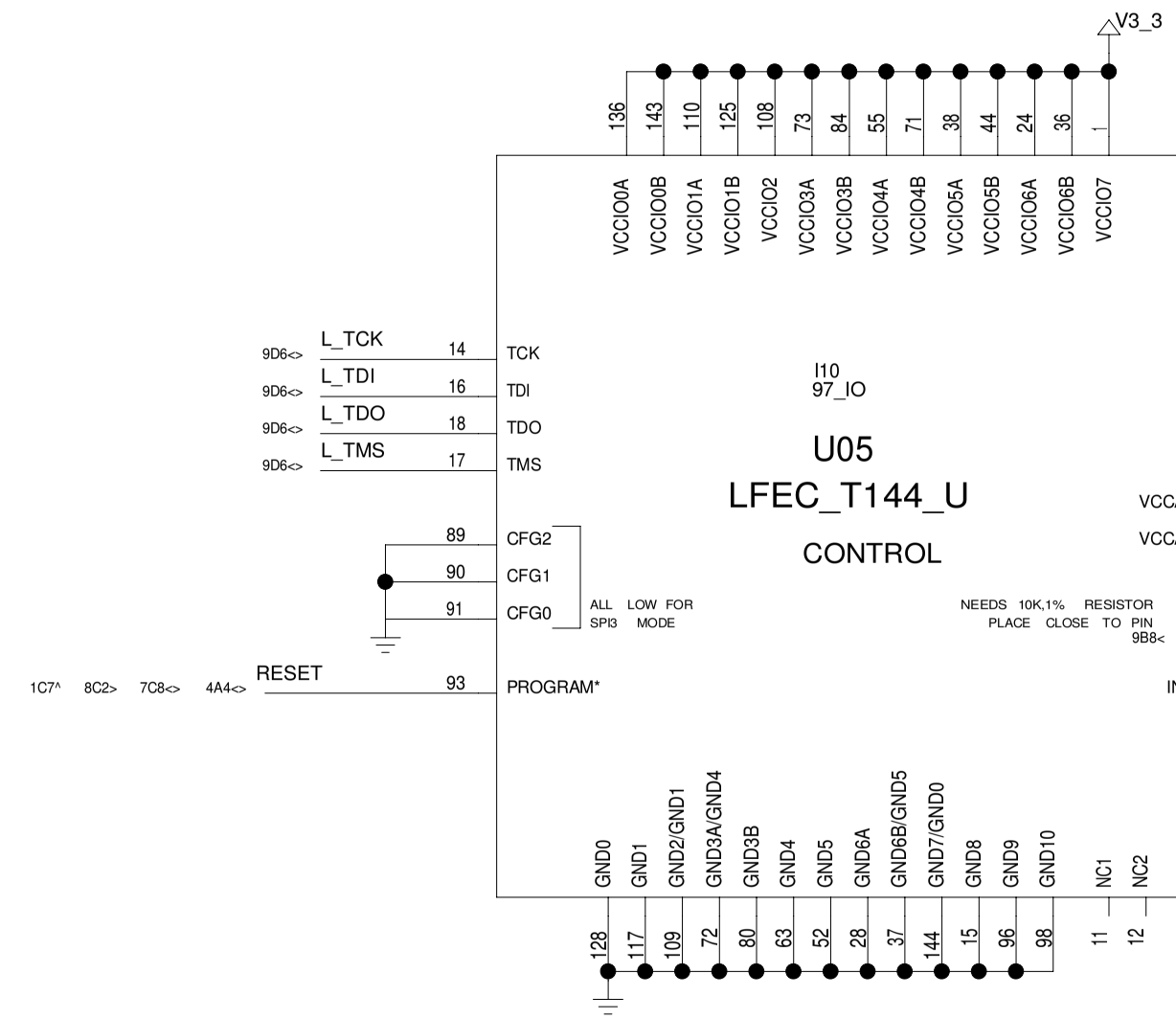


I26
2.7V

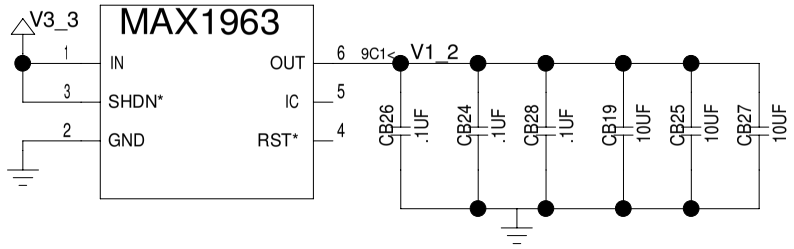
UB04



AT25160A_U



I28
UB05
MAX1963



END OF PROCESSOR HIERARCHY BLOCK

TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 6/6(BLOCK) 9/14(TOTAL)

BLOCK NAME: motprocrescard_dn PARENT BLOCK: \ ds26522topdn \

CS_X2 IN 10B8< 1C6^
CS_X1 IN 10B8< 1C6^
RD_DUT IN 10B8< 1C6^
WR_DUT IN 10B8< 1C6^
INT_DUT NI 10C8> 1D6^
RESET_DUT IN 10B8< 1C6^
A_DUT<12..0> NI 10B4 1C6^
D_DUT<7..0> IO 10C3 1C6^

V3_3

H5 K9 D5 D4 D3 D2 D1 C9 C8 D11 D12 C10 A6 B6 C11 C12 G4 H4 J4 G3 G10 J9 J10 H10
ACVDD1_1 ACVDD2_2 ARVDD1_1 ARVDD1_2 ARVDD1_3 ARVDD1_4 ARVDD1_5 ARVDD2_1 ARVDD2_2 ARVDD2_3 ARVDD2_4 ATVDD2_5 ATVDD1_1 ATVDD1_2 ATVDD2_1 ATVDD2_2 DVDD1_1 DVDD1_2 DVDD1_3 DVDD1_4 DVDD2_1 DVDD2_2 DVDD2_3 DVDD2_4

14D5> MCLK_TAP7 M9 MCLK
1D6^ 10D7< INT_DUT K4 INT
10A8<> JTRST_DUT L6 JTRST
10A7<> JTMS_DUT M5 JTMS
10A8<> JTDO_2_DUT M8 JTDO2
10A7<> JTDO_1_DUT M7 JTDO1
10A8<> JTDI_2_DUT L7 JTDI2
10A7<> JTDI_1_DUT L5 JTDI1
10A7< 10A7<> JTCLK_DUT M6 JTCLK
1C6^ 10D7< RD_DUT H3 RDB_DBS
1C6^ 10D7< WR_DUT J3 WRB_RWB
1C6^ 10D7< CS_X2 M4 CSB2
1C6^ 10D7< CS_X1 L4 CSB1
10B2< SCANMO_DUT C6 SCAN_MODE
10A2< SCANEN_DUT D6 SCAN_EN
10B2< SPISEL_DUT D7 SPI_SEL
10B2< BTS_DUT E5 BTS
1C6^ 10D7< RESET_DUT K3 RESETB

I219
BGA
DS26522
U06

D0 M3 0
D1 L3 1
D2 M2 2
D3 M1 D3 I238 3
D4 L2 D4 I237 4
D5 L1 D5_SPI_SWAP I236 5
D6 K2 10C2< D6_SPI_CPHA I235 6
D7 K1 D7_SPI_CPOL I234 7
D_DUT<7..0>

A12 E1 12
A8 E2 8
A7 F1 7
A6 F2 6
A5 G1 5
A4 G2 4
A3 H1 3
A2 H2 2
A1 J1 1
A0 J2 0
1C6^ 10D7<
A_DUT<12..0>

DVSS2_8 DVSS2_7 DVSS2_6 DVSS2_5 DVSS2_4 DVSS2_3 DVSS2_2 DVSS2_1 DVSS1_4 DVSS1_3 DVSS1_2 DVSS1_1 ATVSS2_2 ATVSS2_1 ATVSS1_2 ATVSS1_1 ARVSS2_5 ARVSS2_4 ARVSS2_3 ARVSS2_2 ARVSS2_1 ARVSS1_5 ARVSS1_4 ARVSS1_3 ARVSS1_2 ARVSS1_1 ACVSS2_2 ACVSS2_1 ACVSS1_2 ACVSS1_1
E9 H9 G9 E8 D8 E10 F9 F10 E3 F4 E4 F3 A10 B10 A3 B3 D9 D10 A7 C7 B7 C1 C4 C3 C2 C5 K10 K11 F5 G5

I231
J05
10C8< JTRST_DUT 1 — 1 TMS — 2 JTMS_DUT 10C8<
3 — 3 TCK — 4 JTCLK_DUT 10A7< 10C8<
10C8> JTDO_2_DUT 5 — 5 TDI — 6 JTDI_1_DUT 10C8<
10C8< JTDI_2_DUT 7 — 7 TDO — 8 JTDO_1_DUT 10C8>
9 GND VCC 10 V3_3
CONN_10P
RB28 1.0K JTCLK_DUT 10A7<> 10C8<

V3_3
I520
10C4<> D5_SPI_SWAP RB48 1.0K 2 JP15
I521
10D7<> 1C6^ 10C4<> D6_SPI_CPHA RB43 1.0K 2 JP13
I515
10C4<> D7_SPI_CPOL RB41 1.0K 2 JP10
I525
10B8< SPISEL_DUT (LOW FOR PARALLEL PORT) RB49 1.0K 2 JP16
I527
10B8< BTS_DUT (HIGH FOR MOTO MODE) RB50 1.0K 2 JP17
10B8< SCANMO_DUT (LOW FOR NORMAL OPERATION) R02 1.0K
10B8< SCANEN_DUT (LOW FOR NORMAL OPERATION) RB42 1.0K
I535
11C7< TXENABLE_1 RB51 1.0K 2 JP18
(HIGH FOR NORMAL OPERATION)
I538
11A7< TXENABLE_2 RB52 1.0K 2 JP19

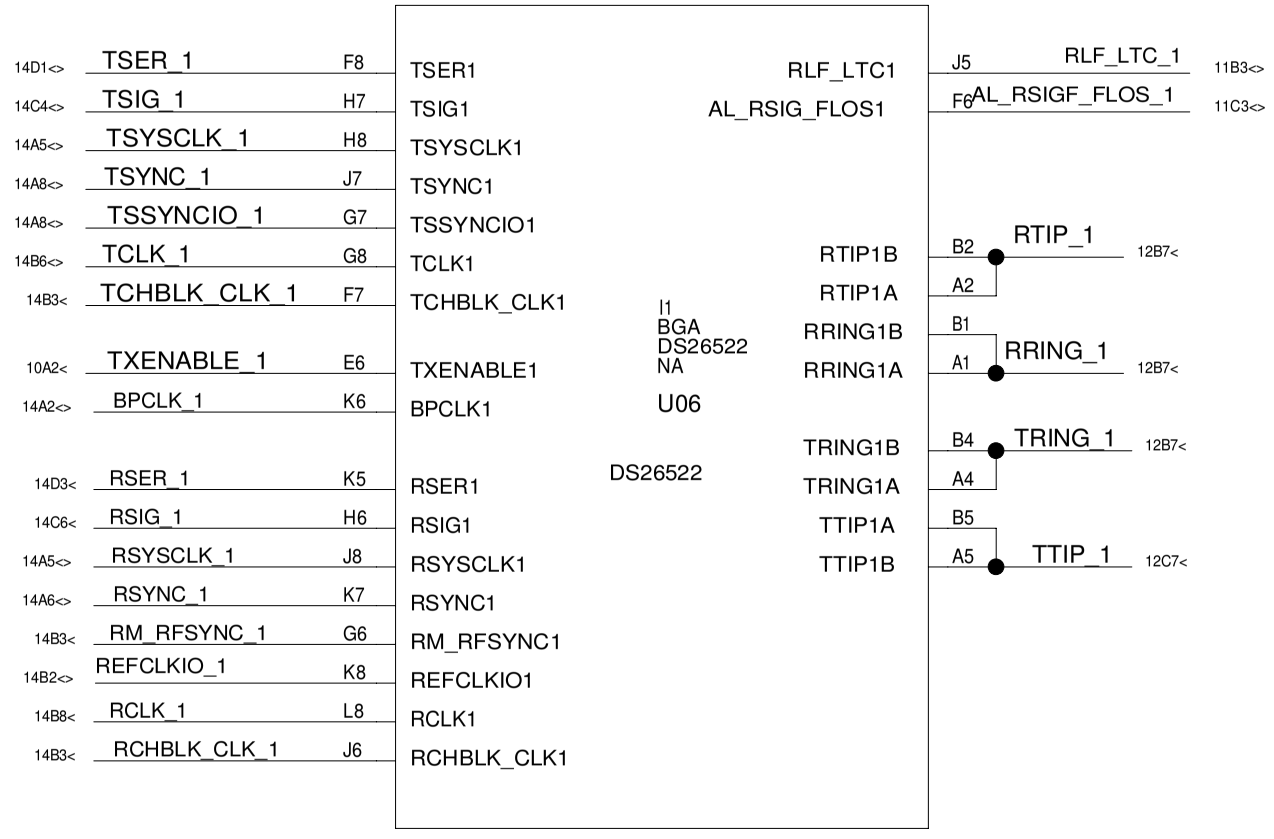
INT_LED AND TESTPOINTS FOR ADDR/DATA/CTRL
TESTPOINTS FOR ADDR/DATA/CTRL
ARE IN THE MICRO PROCESSOR BLOCK

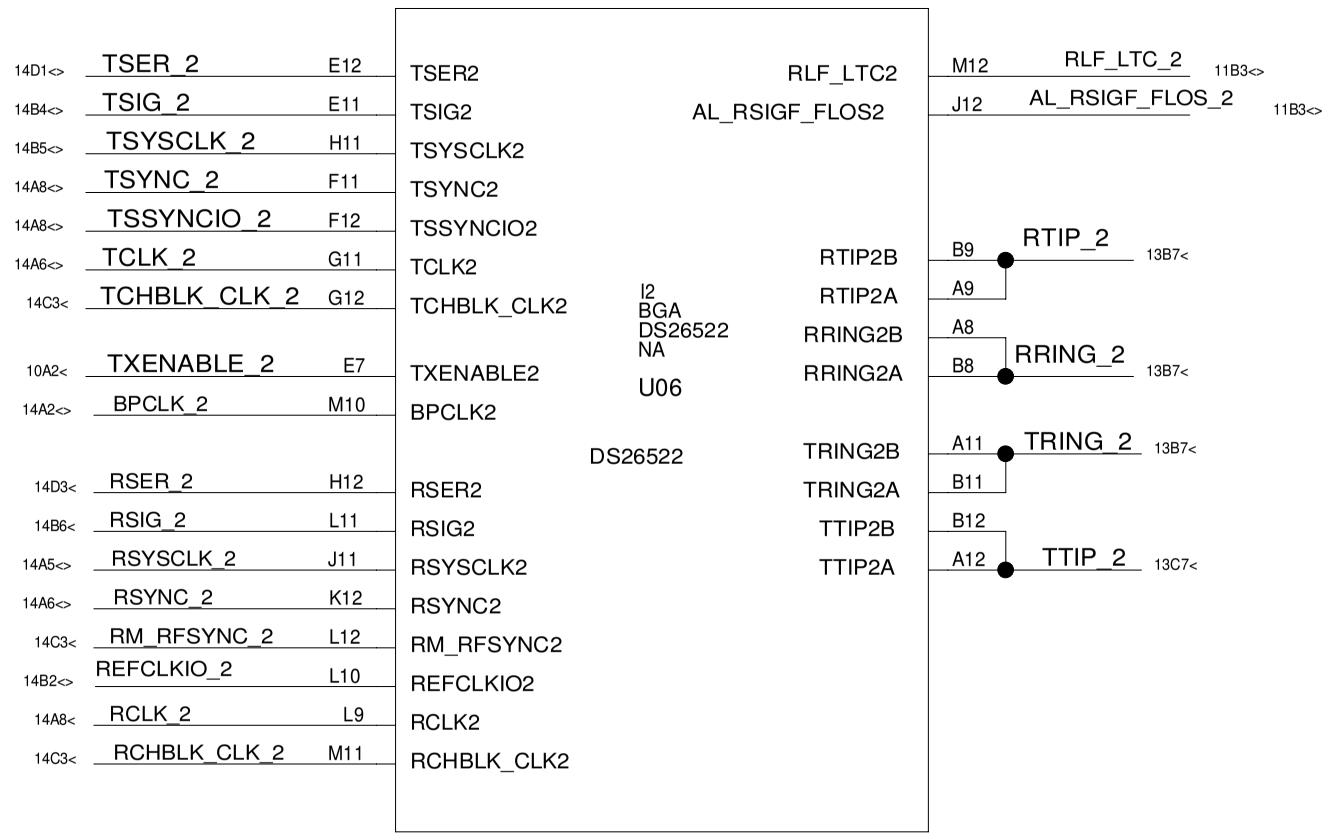
BEGINNING OF DS26522DK HIERARCHY BLOCK

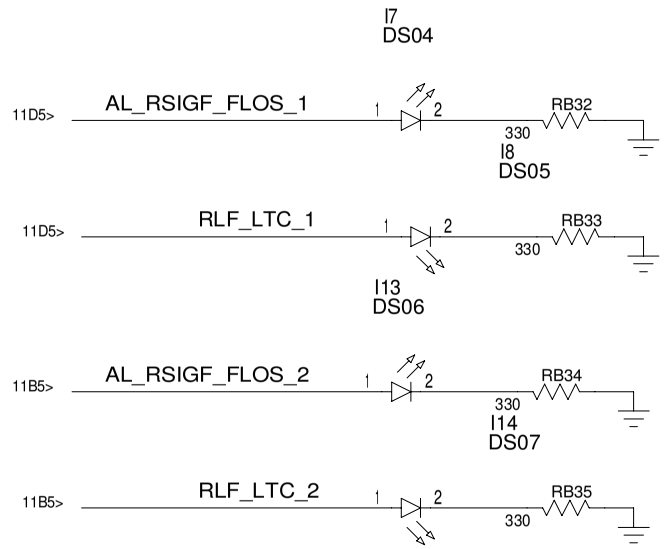
TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 1/5(BLOCK) 10/14(TOTAL)

BLOCK NAME: ds26522dk01a0dutdn . PARENT BLOCK: \ ds26522topdn \

CR-11 : @_ZTOP_LIB_DS26522TOPDN_\(SCH_1):PAGE1_I9@_ZTOP_LIB_DS26522DK01A0DUTDN_\(SCH_1):PAGE2



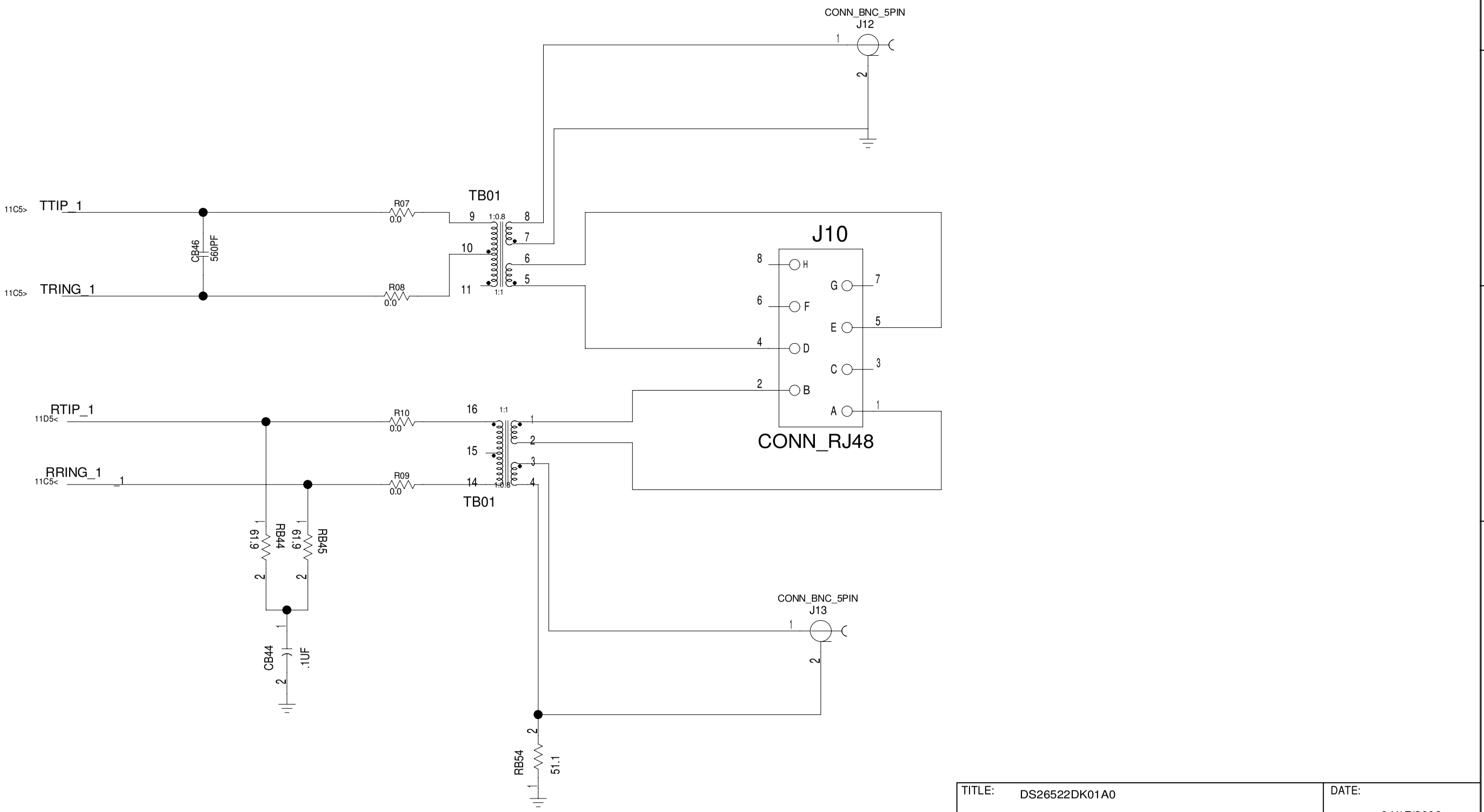




TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 2/5(BLOCK) 11/14(TOTAL)

BLOCK NAME: ds26522dk01a0dutdn . PARENT BLOCK: \ ds26522topdn \

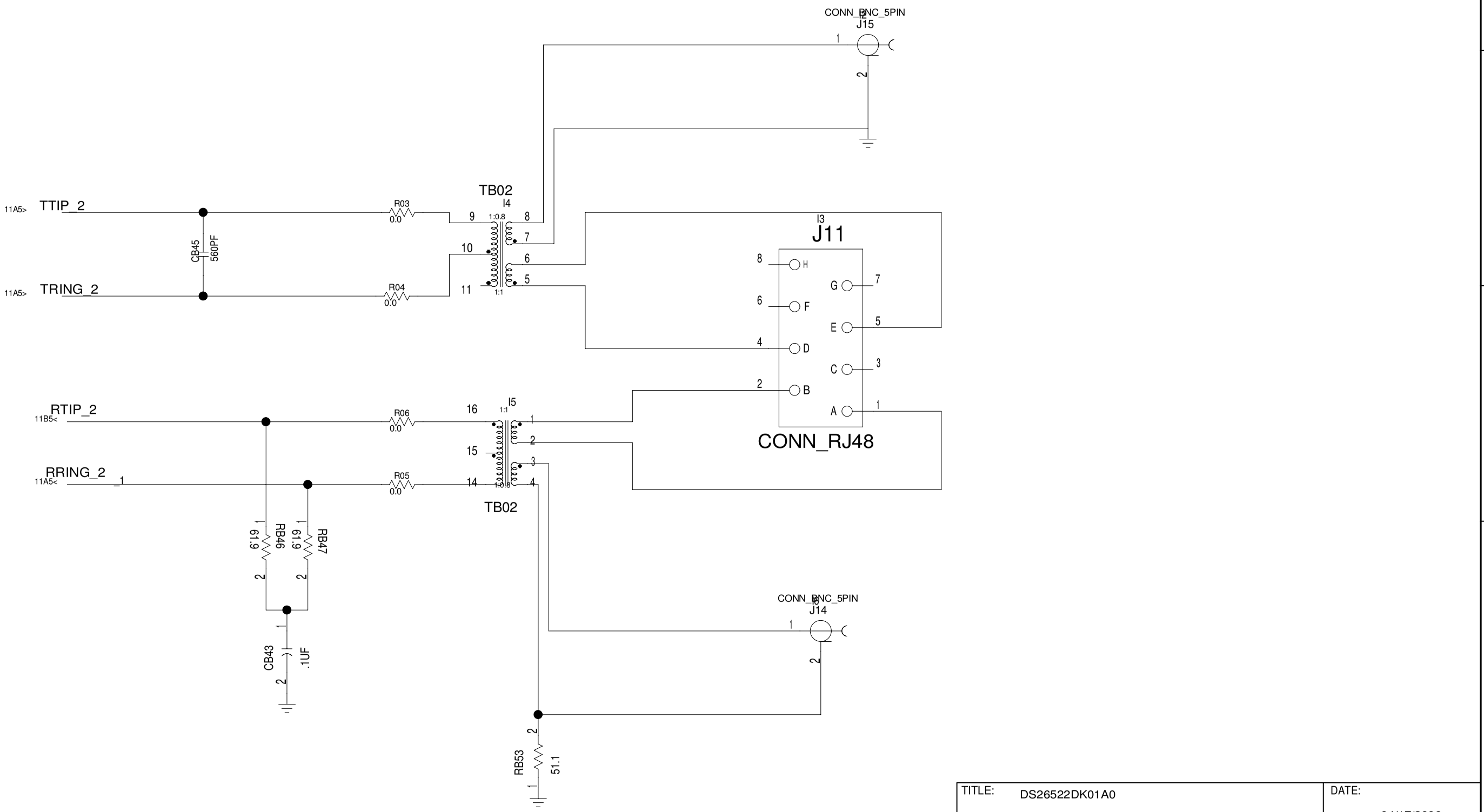
CR-12 : @_ZTOP_LIB_DS26522TOPDN_\(SCH_1):PAGE1_19@_ZTOP_LIB_DS26522DK01A0DUTDN_\(SCH_1):PAGE3



TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 3/5(BLOCK) 12/14(TOTAL)

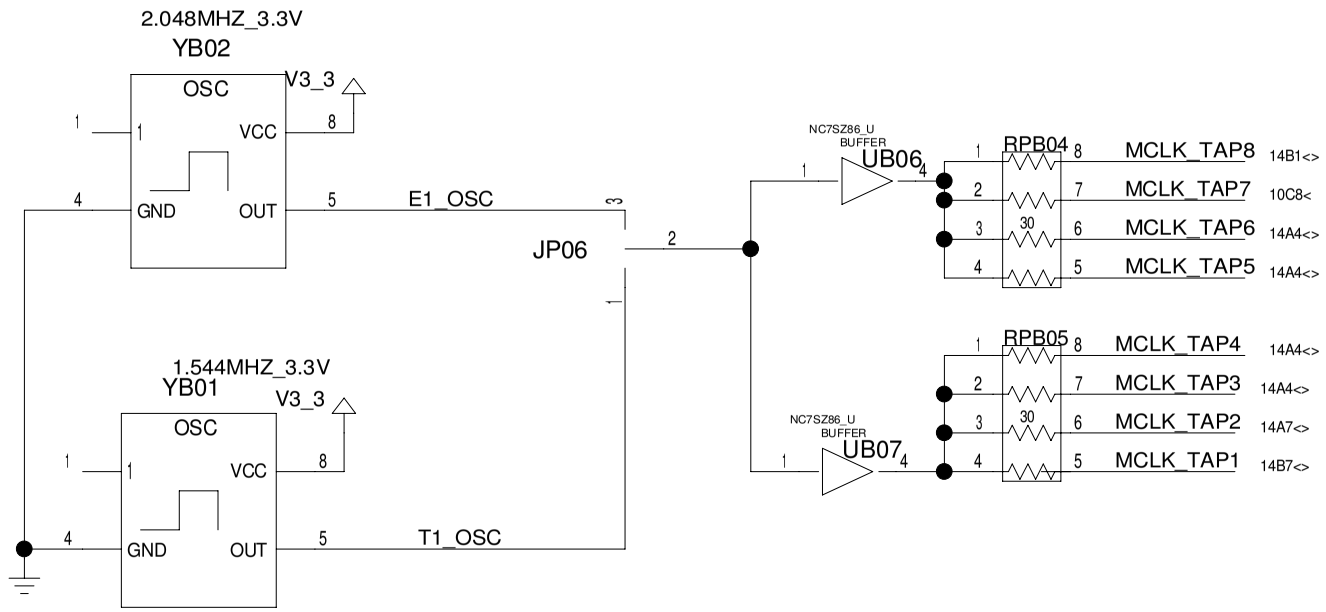
BLOCK NAME: ds26522dk01a0dutdn . PARENT BLOCK: \ ds26522topdn \

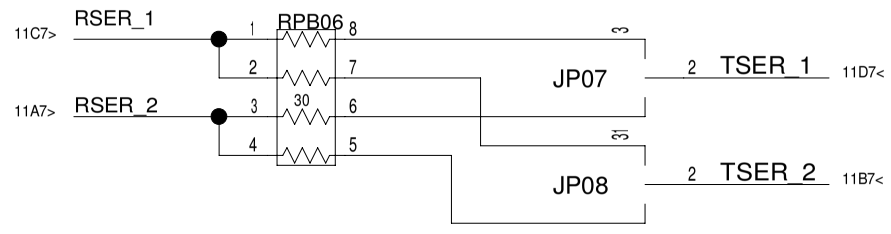
CR-13 : @_ZTOP_LIB_DS26522TOPDN_\(SCH_1):PAGE1_I9@_ZTOP_LIB_DS26522DK01A0DUTDN_\(SCH_1):PAGE4

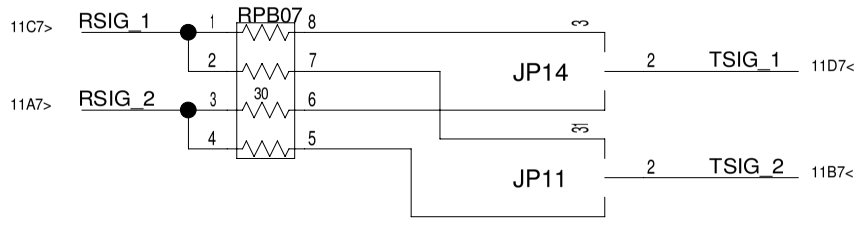


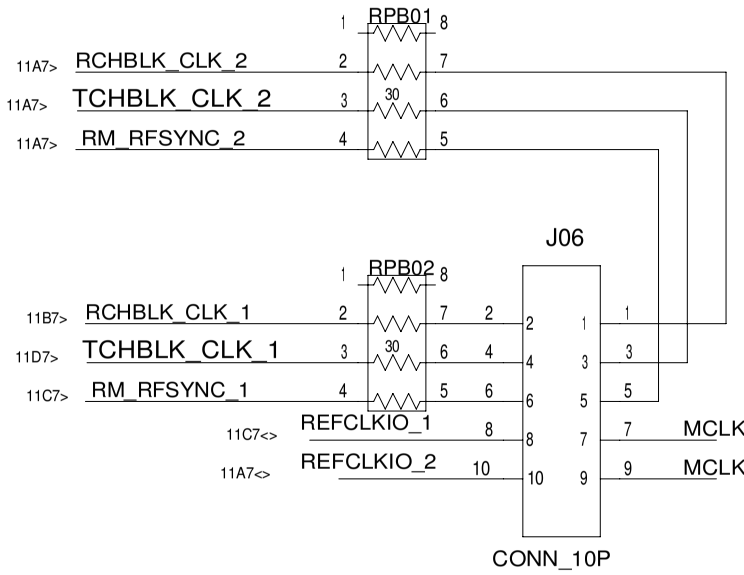
TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 2/4(BLOCK) 11/34(TOTAL)

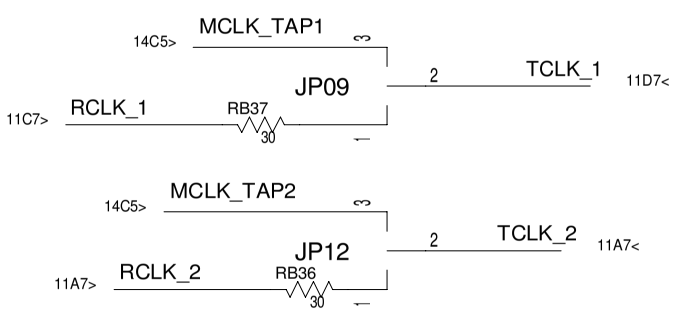
BLOCK NAME: ds26522dk01a0dutdn , PARENT BLOCK: \ ds26522topdn \

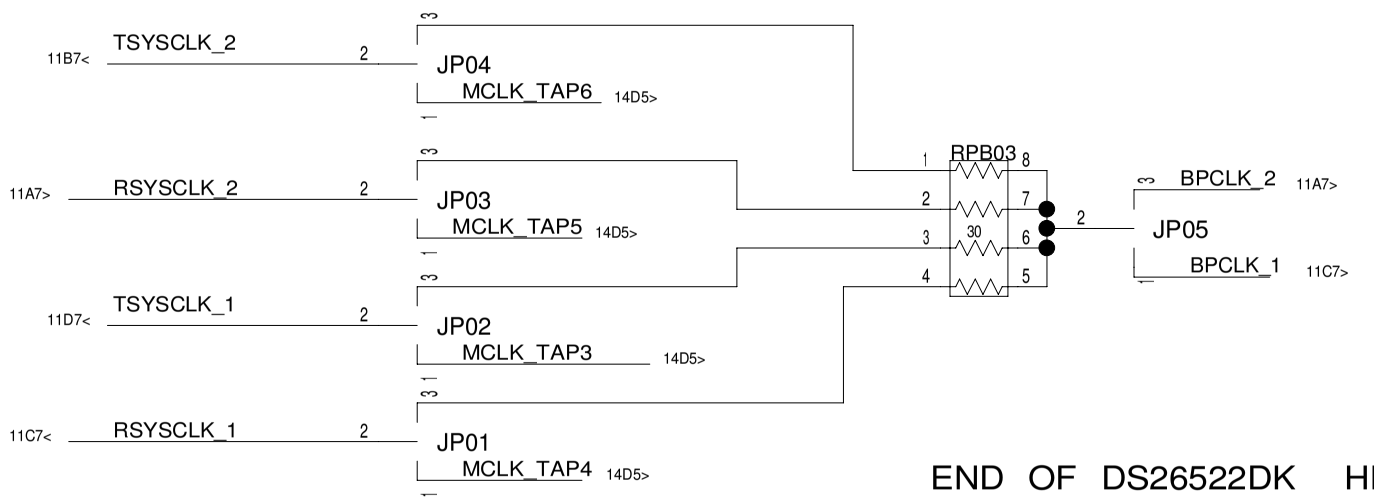


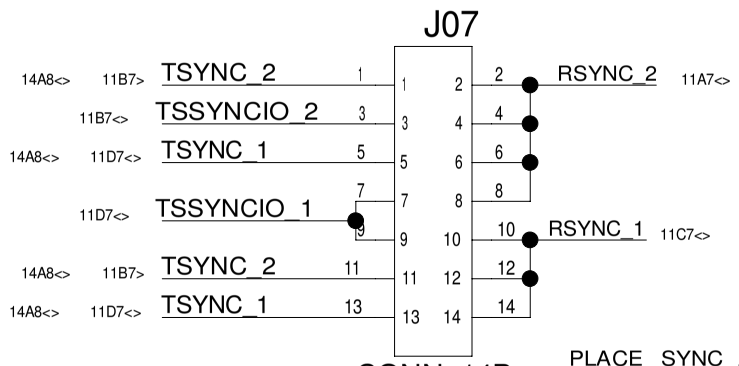












PLACE SYNC AND SYNCIO PINS CLOSE TO DUT (NO TERMINATION RESISTORS)

END OF DS26522DK HIERARCHY BLOCK

TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 5/5(BLOCK) 14/14(TOTAL)

BLOCK NAME: ds26522dk01a0dutdn . PARENT BLOCK: \ ds26522topdn \

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

DS26522DK