

54LS74,DM54LS74A,DM74LS74A

*54LS74 DM54LS74A DM74LS74A Dual Positive-Edge-Triggered D Flip-Flops with
Preset, Clear and Complementary Outputs*



Literature Number: SNOS313A

54LS74/DM54LS74A/DM74LS74A Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

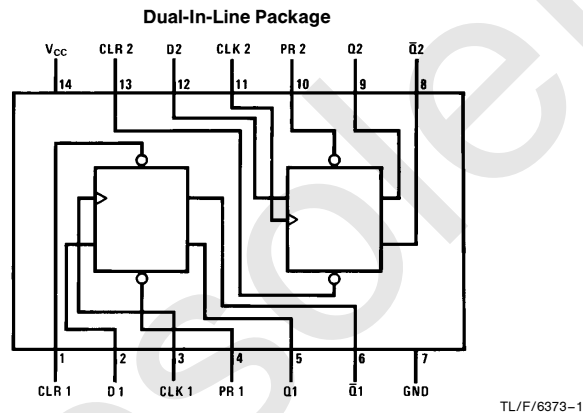
This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not

violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate military/aerospace device (54LS74) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



Order Number 54LS74DMQB, 54LS74FMQB, 54LS74LMQB,
DM54LS74AJ, DM54LS74AW, DM74LS74AM or DM74LS74AN
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	$\bar{Q}_0$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going Transition

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

Q₀ = The output logic level of Q before the indicated input conditions were established.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		DM54LS74A			DM74LS74A			Units
			Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage		2			2			V
V _{IL}	Low Level Input Voltage				0.7			0.8	V
I _{OH}	High Level Output Current				−0.4			−0.4	mA
I _{OL}	Low Level Output Current				4			8	mA
f _{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
f _{CLK}	Clock Frequency (Note 3)		0		20	0		20	MHz
t _w	Pulse Width (Note 2)	Clock High	18			18			ns
		Preset Low	15			15			
		Clear Low	15			15			
t _w	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	20			20			
		Clear Low	20			20			
t _{SU}	Setup Time (Notes 1 and 2)		20 ↑			20 ↑			ns
t _{SU}	Setup Time (Notes 1 and 3)		25 ↑			25 ↑			ns
t _H	Hold Time (Note 1 and 4)		0 ↑			0 ↑			ns
T _A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C, and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C, and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	DM54 2.5 DM74 2.7	3.4 3.4		V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	DM54 DM74	0.25 0.35	0.4 0.5	V
		$I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$	DM74	0.25	0.4	
I_I	Input Current @Max Input Voltage	$V_{CC} = \text{Max}$ $V_I = 7V$	Data Clock Preset Clear		0.1 0.1 0.2 0.2	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.7V$	Data Clock Clear Preset		20 20 40 40	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4V$	Data Clock Preset Clear		-0.4 -0.4 -0.8 -0.8	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	DM54 DM74	-20 -20	-100 -100	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 3)		4	8	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

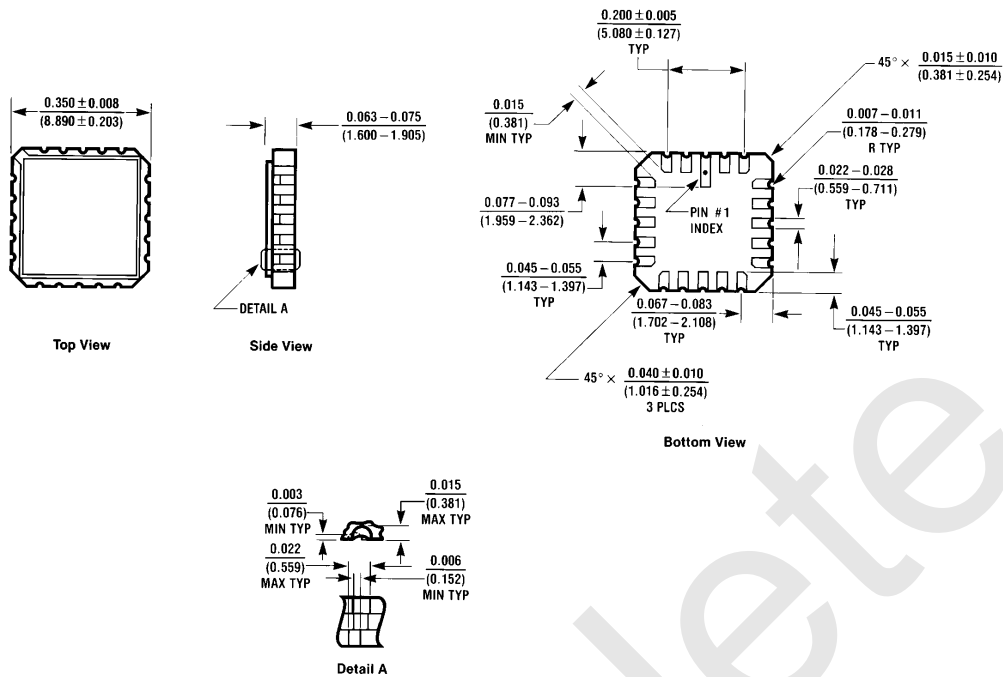
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where $V_O = 2.25V$ and $2.125V$ for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with CLOCK grounded after setting the Q and $\bar{Q}$ outputs high in turn.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

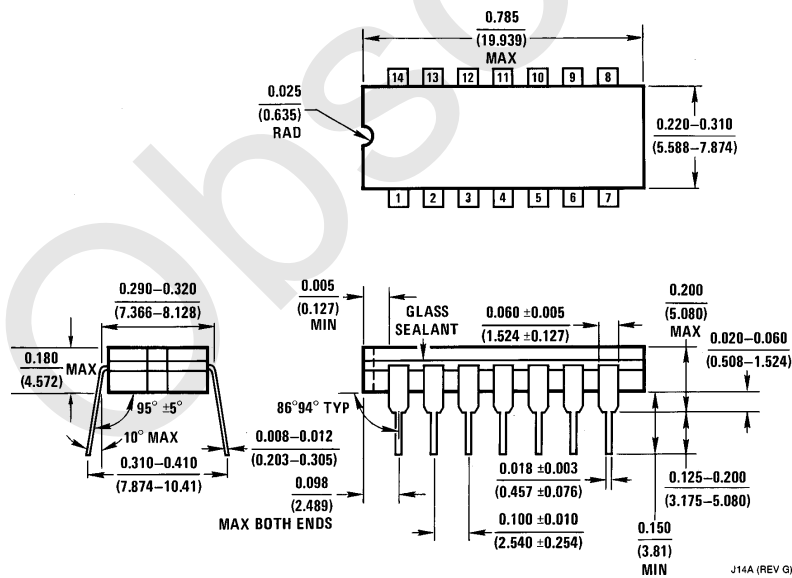
Symbol	Parameter	From (Input) To (Output)	$R_L = 2\text{ k}\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		30		35	ns

Physical Dimensions inches (millimeters)



Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS74LMQB
NS Package Number E20A

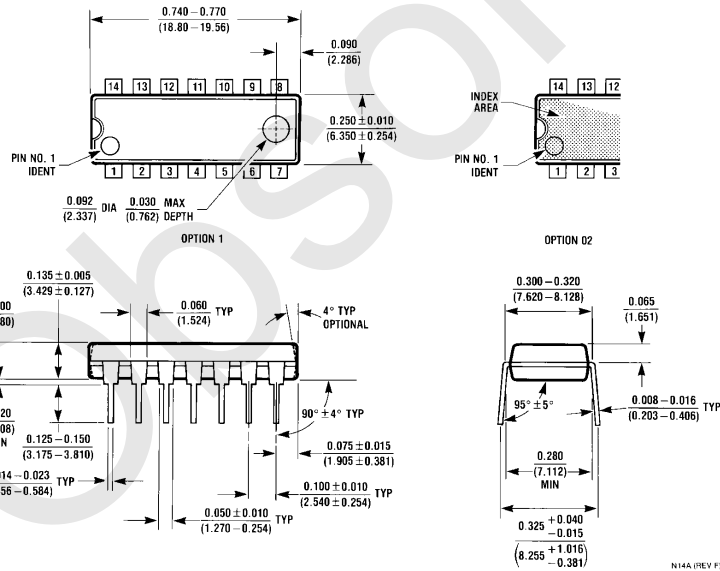
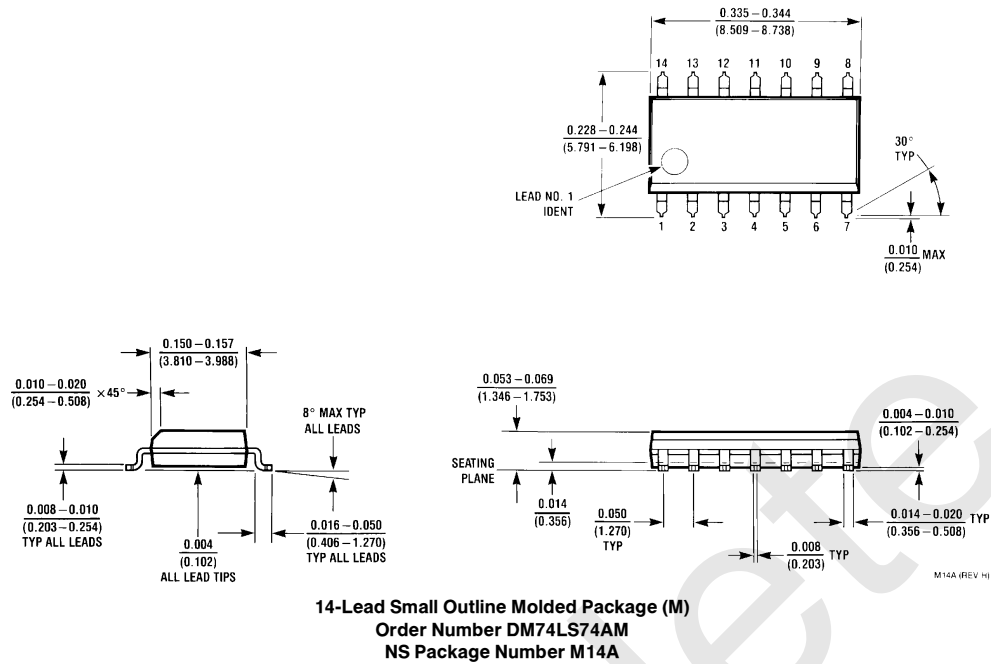
E20A (REV D)



14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS74DMQB or DM54LS74AJ
NS Package Number J14A

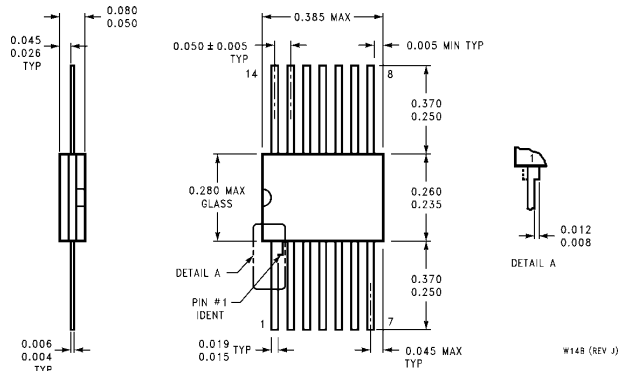
J14A (REV G)

Physical Dimensions inches (millimeters) (Continued)



54LS74/DM54LS74A/DM74LS74A Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS74FMB or DM54LS74AW
NS Package Number W14B

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