

October 1988 Revised March 2000

DM74LS377

Octal D-Type Flip-Flop with Common Enable and Clock

General Description

The DM74LS377 is an 8-bit register built using advanced low power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common input enable. The device is packaged in the space-saving (0.3 inch row spacing) 20-pin package.

Features

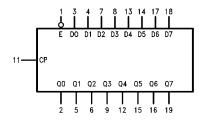
- 8-bit high speed parallel registers
- Positive edge-triggered D-type flip-flops
- Fully buffered common clock and enable inputs

Ordering Code:

Order Number Package Number Package Description		
DM74LS377WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS377N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

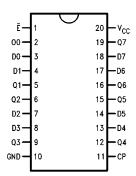
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



V_{CC} = Pin 20 GND = Pin 10

Connection Diagram



Pin Descriptions

Pin Names	Description		
Ē	Enable Input (Active LOW)		
D0-D7	Data Inputs		
CP	Clock Pulse Input (Active Rising Edge)		
Q0-Q7	Flip-Flop Outputs		

Truth Table

Ī	Inputs			Output
	Ē	СР	D _n	Q_n
ĺ	Н	X	X	No Change
	L	~	Н	Н
	L	~	L	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

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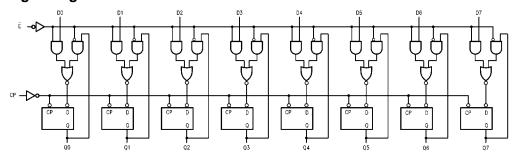
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Functional Description

The DM74LS377 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable input (\overline{E}) are common to all flip-flops.

When \overline{E} is LOW, new data is entered into the register on the next LOW-to-HIGH transition of CP. When \overline{E} is HIGH, the register will retain the present data independent of the CP.

Logic Diagram



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Absolute Maximum Ratings(Note 1)

Supply Voltage 7V Input Voltage 7V Operating Free Air Temperature Range 0° C to $+70^{\circ}$ C Storage Temperature Range -65° C to $+150^{\circ}$ C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	
V _{CC}	Supply Voltage	4.75	5	5.25	V	
V _{IH}	HIGH Level Input Voltage	2			V	
V _{IL}	LOW Level Input Voltage			0.8	V	
I _{OH}	HIGH Level Output Current			-0.4	mA	
I _{OL}	LOW Level Output Current			8	mA	
T _A	Free Air Operating Temperature	0		70	°C	
t _S (H)	Setup Time HIGH or LOW	10			ns	
t _S (L)	D _n to CP	10				
t _H (H)	Hold Time HIGH or LOW	5.0			ns	
t _H (L)	D _n to CP	5.0				
t _S (H)	Setup Time HIGH or LOW	10				
t _S (L)	E to CP	20			ns	
t _H (H)	Hold Time HIGH or LOW	5.0				
t _H (L)	E to CP	5.0			ns	
t _W (H)	CP Pulse Width HIGH or LOW	20			20	
t _W (L)		20			ns	

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$			-1.5	V
V _{OH}	HIGH Level Output Voltage	$V_{CC} = Min, I_{OH} = Max$ $V_{II} = Max$	2.7	3.4		V
V _{OL}	LOW Level	$V_{CC} = Min, I_{OL} = Max$		0.35	0.5	V
Output Volta	Output Voltage	$V_{IH} = Min$ $I_{OL} = 4 \text{ mA}, V_{CC} = Min$			0.4	
II	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 7V$ $V_I = 10V$			0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max, V _I = 2.7V			20.0	μΑ
I _{IL}	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-0.4	mA
Ios	Short Circuit Output Current	V _{CC} = Max (Note 3)	-20		-100	mA
I _{CC}	Supply Current	V _{CC} = Max			28	mA

Note 2: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

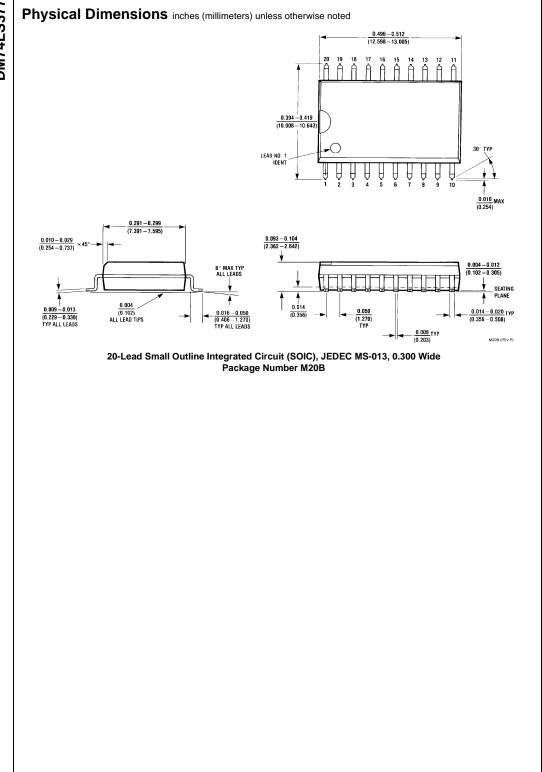
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

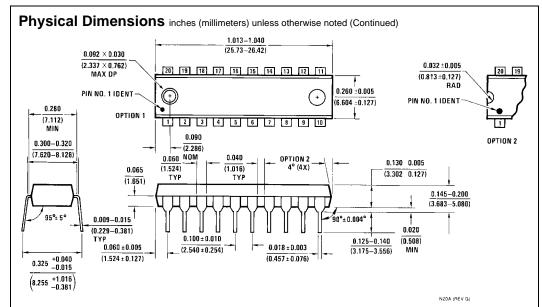
Switching Characteristics

 $V_{CC} = +5.0V, T_A = +25^{\circ}C$

Symbol	Parameter	$R_L = 2 k\Omega$	Units		
	T di diffetor	Min	Max	Cilita	
f _{MAX}	Maximum Clock Frequency	30		MHz	
t _{PLH}	Propagation Delay		25	ns	
t _{PHL}	CP to Q _n		25		

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20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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