FAIRCHILD SEMICONDUCTOR™

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DM74LS670
3-STATE 4-by-4 Register Files

General Description

These register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits writing into one location, and reading from another word location, simultaneously.

Four data inputs are available to supply the word to be stored. Location of the word is determined by the write select inputs A and B, in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data entry addressing separate from data read addressing and individual sense line — eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 ns typical) and the read time (24 ns typical). The register file has a non-volatile readout in that data is not lost when addressed.

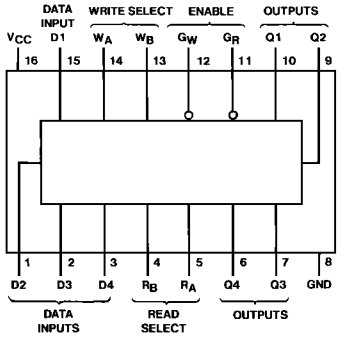
All inputs (except read enable and write enable) are buffered to lower the drive requirements to one normal Series 54LS/74LS load, and input clamping diodes minimize switching transients to simplify system design. High speed, double ended AND-OR-INVERT gates are employed for the read-address function and have high sink current, 3-STATE outputs. Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

Features

- Alternate Military/Aerospace device (54LS670) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.
- For use as:
  - Scratch pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Separate read/write addressing permits simultaneous reading and writing
- Organized as 4 words of 4 bits
- Expandable to 512 words of n-bits
- 3-STATE versions of DM54LS170/DM74LS170
- Fast access times 20 ns typ

Connection Diagram

Dual-In-Line Package



DS006436-1

Order Number 54LS670DMQB, 54LS670FMQB, 54LS670LMQB, DM54LS670J, DM54LS670W, DM74LS670M or DM74LS670N
See Package Number E20A, J16A, M16A, N16A or W16A

Function Tables

WRITE TABLE (Notes 1, 2, 3)

Write Inputs			Word			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ TABLE (Notes 1, 4)

Read Inputs			Outputs			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	WOB1	WOB2	WOB3	WOB4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

Note 1: H = High Level, L = Low Level, X = Don't Care, Z = High Impedance (Off).

Note 2: (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

Note 3: Q_0 = The level of Q before the indicated input conditions were established.

Note 4: WOB1 = The first bit of word 0, etc.

Absolute Maximum Ratings (Note 5)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter		DM54LS670			DM74LS670			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
t_W	Write Enable Pulse Width (Note 8)		25			25			ns
t_{SU}	Setup Time	Data	10			10			ns
	(Notes 6, 8)	W_A, W_B	15			15			
t_H	Hold Time	Data	15			15			ns
	(Notes 6, 8)	W_A, W_B	5			5			
t_{LATCH}	Latch Time for New Data (Notes 7, 8)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 5: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 6: Times are with respect to the Write-Enable input. Write-Select time will protect the data written into the previous address. If protection of data in the previous address, t_{SETUP} (W_A, W_B) can be ignored. As any address selection sustained for the final 30 ns of the Write-Enable pulse and during t_H (W_A, W_B) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

Note 7: Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

Note 8: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 9)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		I_{OL} = Max, V_{IH} = Min	DM74		0.34	0.5	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	D, R or W			0.1	mA
			G_W			0.2	
			G_R			0.3	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	D, R or W			20	µA
			G_W			40	
			G_R			60	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	D, R or W			−0.4	mA
			G_W			−0.8	
			G_R			−1.2	

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 9)	Max	Units
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 10)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 11)			30	50	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Read Select to Q		40		50	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Read Select to Q		45		55	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Write Enable to Q		45		55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Write Enable to Q		50		60	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Q		45		55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Q		40		50	ns
t_{PZH}	Output Enable Time to High Level Output	Read Enable to Any Q		35		45	ns
t_{PZL}	Output Enable Time to Low Level Output	Read Enable to Any Q		40		50	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 12)	Read Enable to Any Q		50			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 12)	Read Enable to Any Q		35			ns

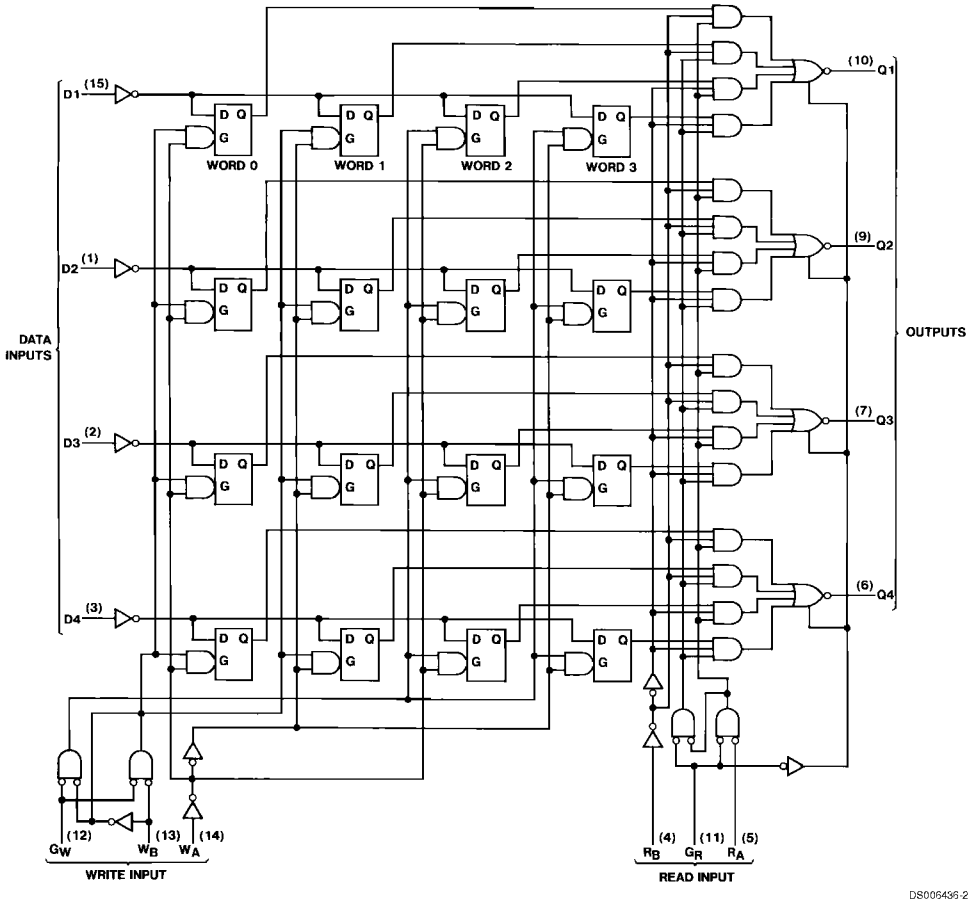
Note 9: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 10: Not more than one output should be shorted at a time, and the duration should not exceed one second.

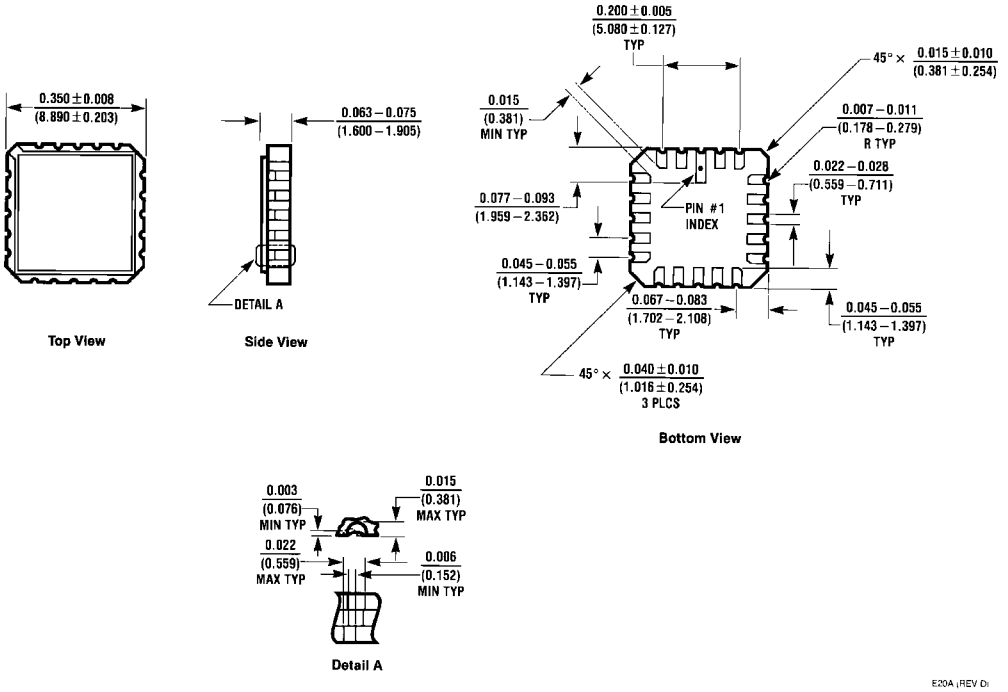
Note 11: I_{CC} is measured with 4.5V applied to all DATA inputs and both ENABLE inputs, all ADDRESS inputs are grounded and all outputs are open.

Note 12: C_L = 5 pF.

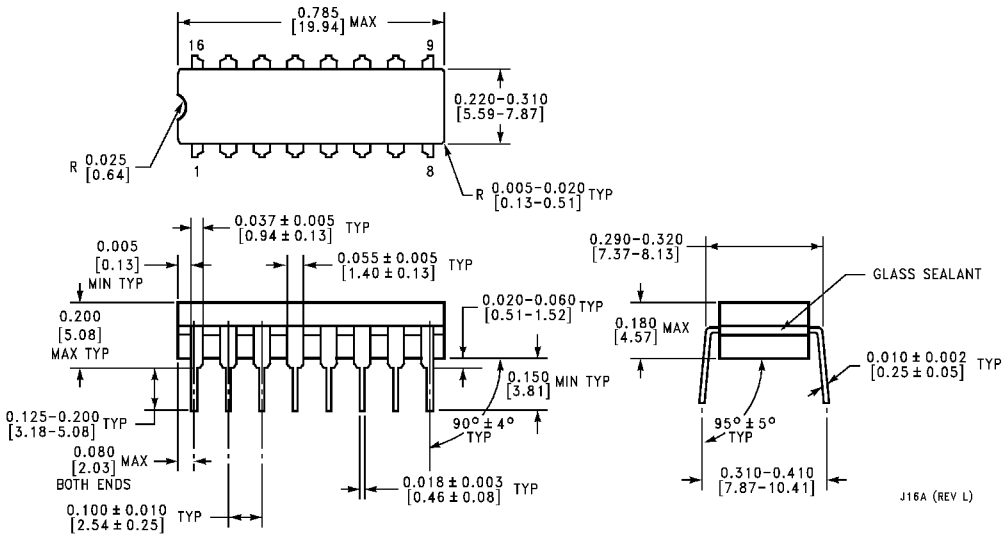
Logic Diagram



Physical Dimensions inches (millimeters) unless otherwise noted

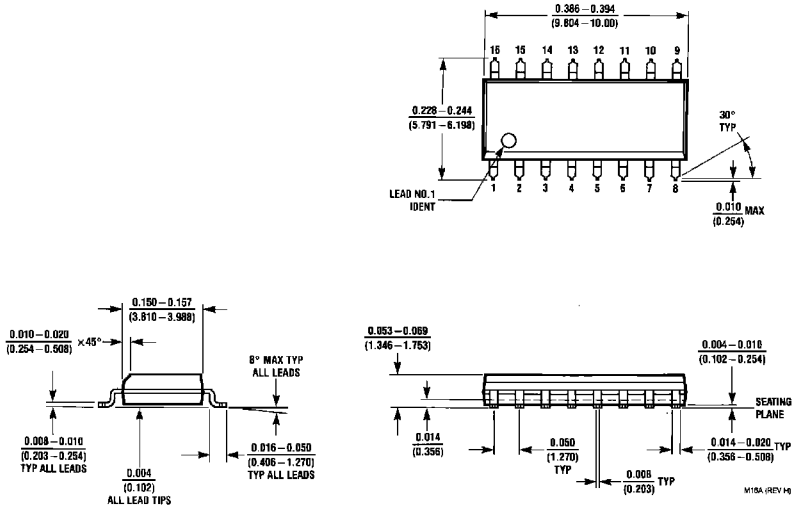


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS670LMQB
Package Number E20A

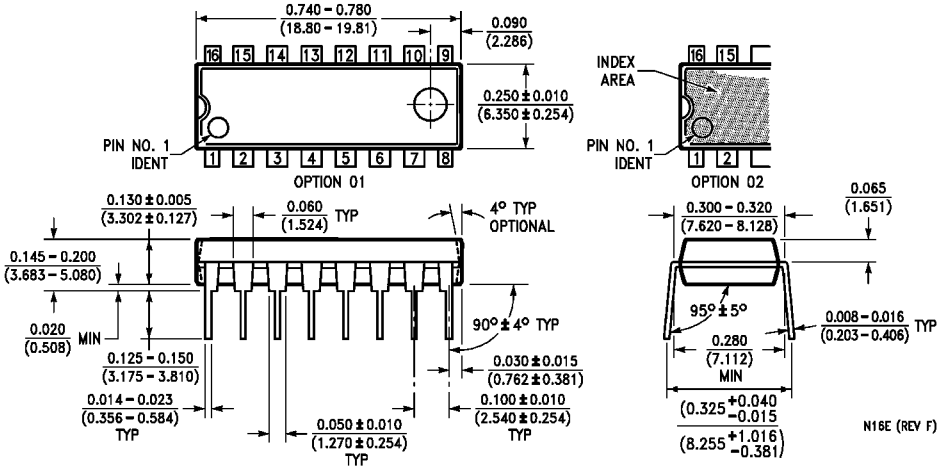


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS670DMQB or DM54LS670J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

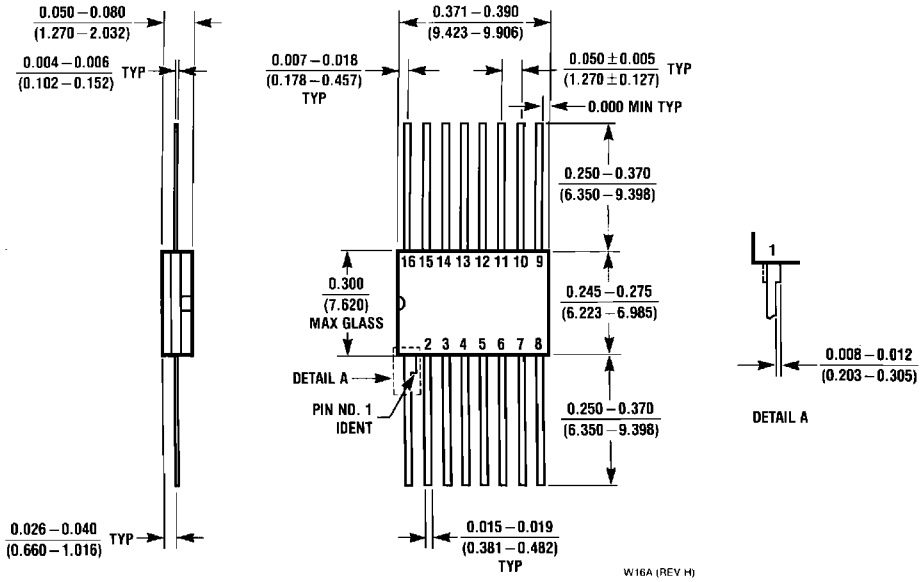


16-Lead Small Outline Molded Package (M)
Order Number DM74LS670M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS670N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (J)
Order Number 54LS670FMQB or DM54LS670W
Package Number W16A

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Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

www.fairchildsemi.com

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179