FEATURES

- Four (4) Completely Independent T1 or E1 Transceivers In One Small 27mm x 27mm Package
- Each Transceiver Contains a Short & Long Haul Line Interface Plus a Full Featured Framer with Alarm Detection/Generation, Elastic Stores, Hardware Based Signaling Support, Per DS0 Channel Control and HDLC Controller
- Each Multi-Chip Module (MCM) Contains Four Die of:
  DS21352 (DS21Q352)
  DS21552 (DS21Q552)
  DS21354 (DS21Q354)
  DS21554 (DS21Q554)
- Selection Guide:

	Supply	Device
T1	3.3V	DS21Q352
T1	5V	DS21Q552
E1	3.3V	DS21Q354
E1	5V	DS21Q554

- See the Specific DS21352/DS21552 and DS21354/DS21554 Data Sheets for Details on their Feature Set and Operation
- All Four T1 or E1 Transceivers Can be Concatenated into a Single 8.192MHz Backplane Data Stream
- IEEE 1149.1 JTAG-Boundary Scan Architecture
- DS21Q352/DS21Q552 and DS21Q354/DS21Q554 are Pin Compatible to Allow the Same Footprint to Support T1 and E1 Applications
- 256–lead MCM BGA package (27mm X 27mm)
- Low Power 5V CMOS or Low Power 3.3V CMOS with 5V Tolerant Input & Outputs

DESCRIPTION

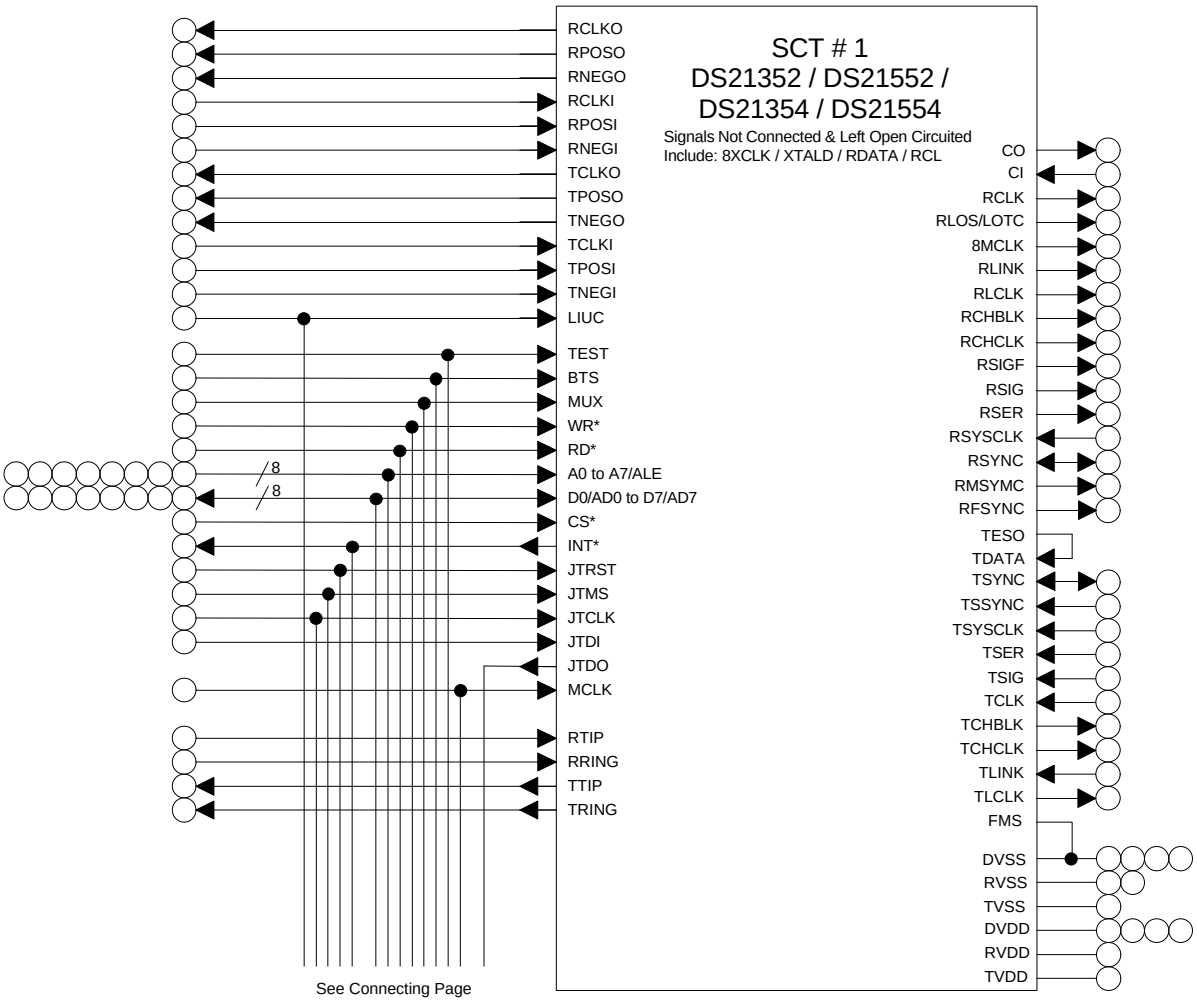
The Quad T1 and E1 Transceiver MCMs offer a high density packaging arrangement for the DS21352/DS21552 T1 Single-Chip Transceivers and the DS21354/DS21554 E1 Single-Chip Transceivers. Four silicon die of one of these devices is packaged in a Multi-Chip Module (MCM) with the electrical connections as shown in Figure 1. All of the functions available on the DS21352/DS21552 and DS21354/DS21554 are also available in the MCM packaged version however in order to minimize package size, some signals have been deleted. These differences are detailed in Table 1.

This data sheet describes the electrical connections and the mechanical dimensions only. Please see the DS21352/DS21552 and DS21354/DS21554 data sheets for full details on all of the features and the operating characteristics of the device.

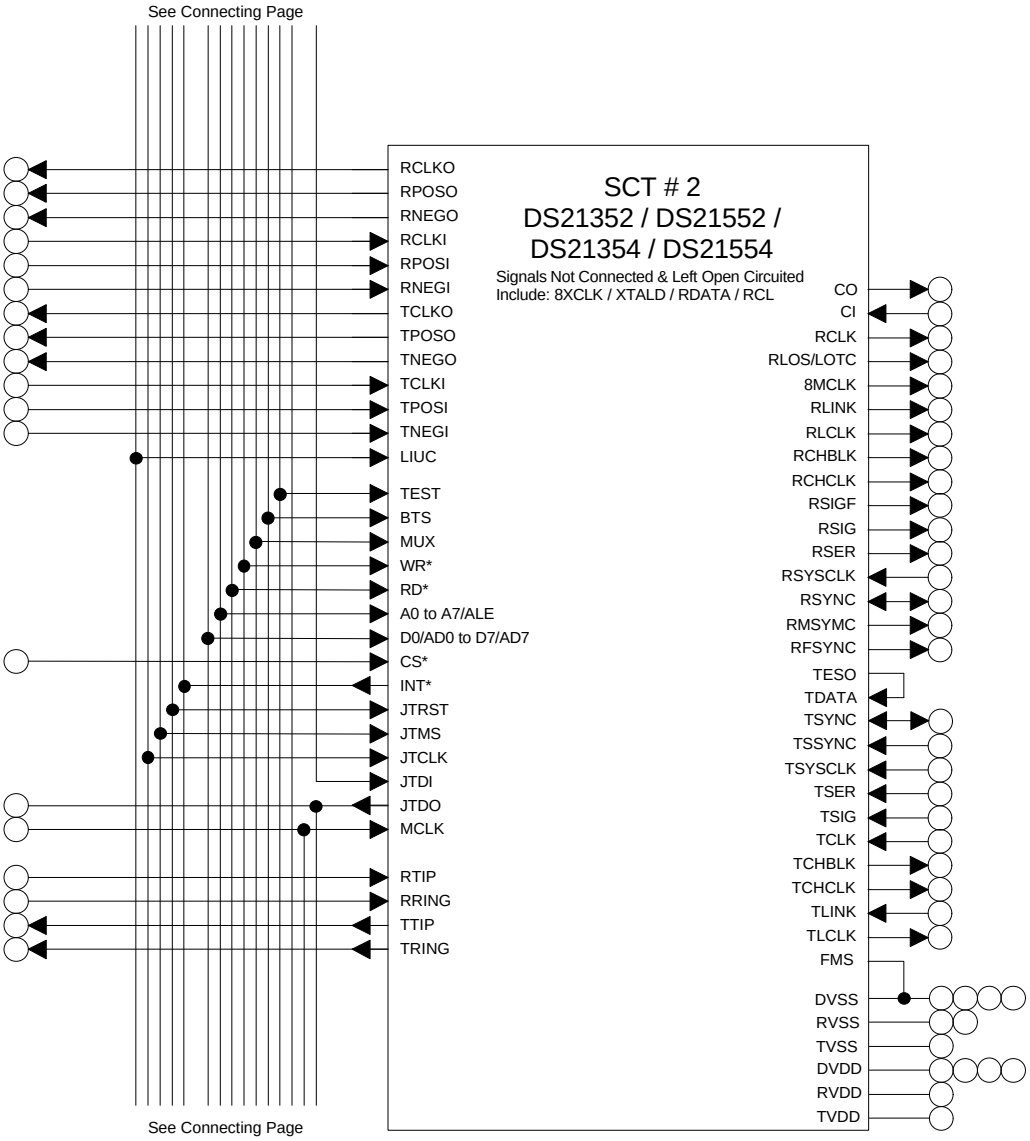
Changes from Normal DS21Q352/DS21Q552 & DS21Q354/DS21Q554 Configuration Table 1

1. The following signals are not available: XTALD / 8XCLK / TESO / TDATA / RCL / RDATA

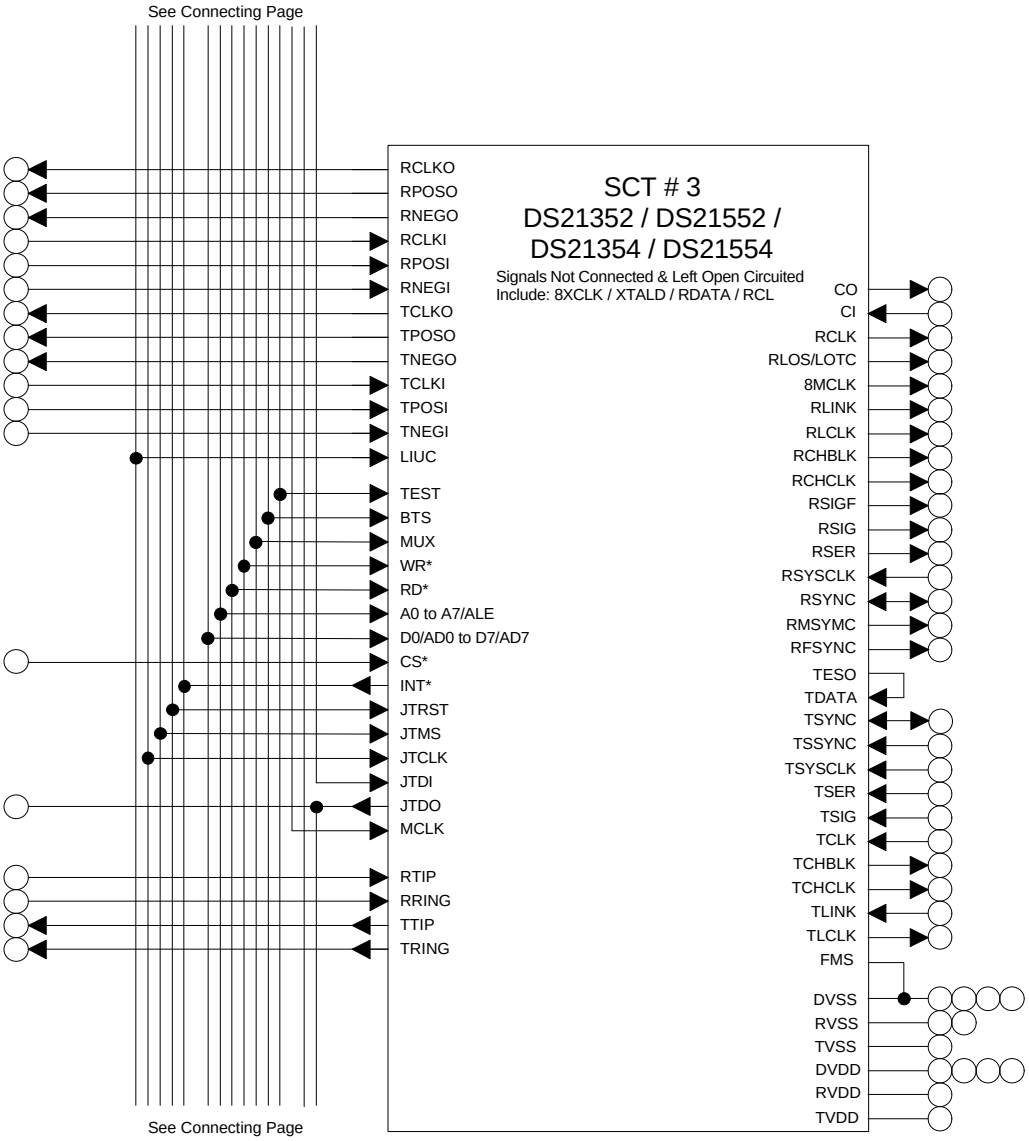
DS21Q352 / DS21Q552 / DS21Q354 / DS21Q554 Schematic Figure 1



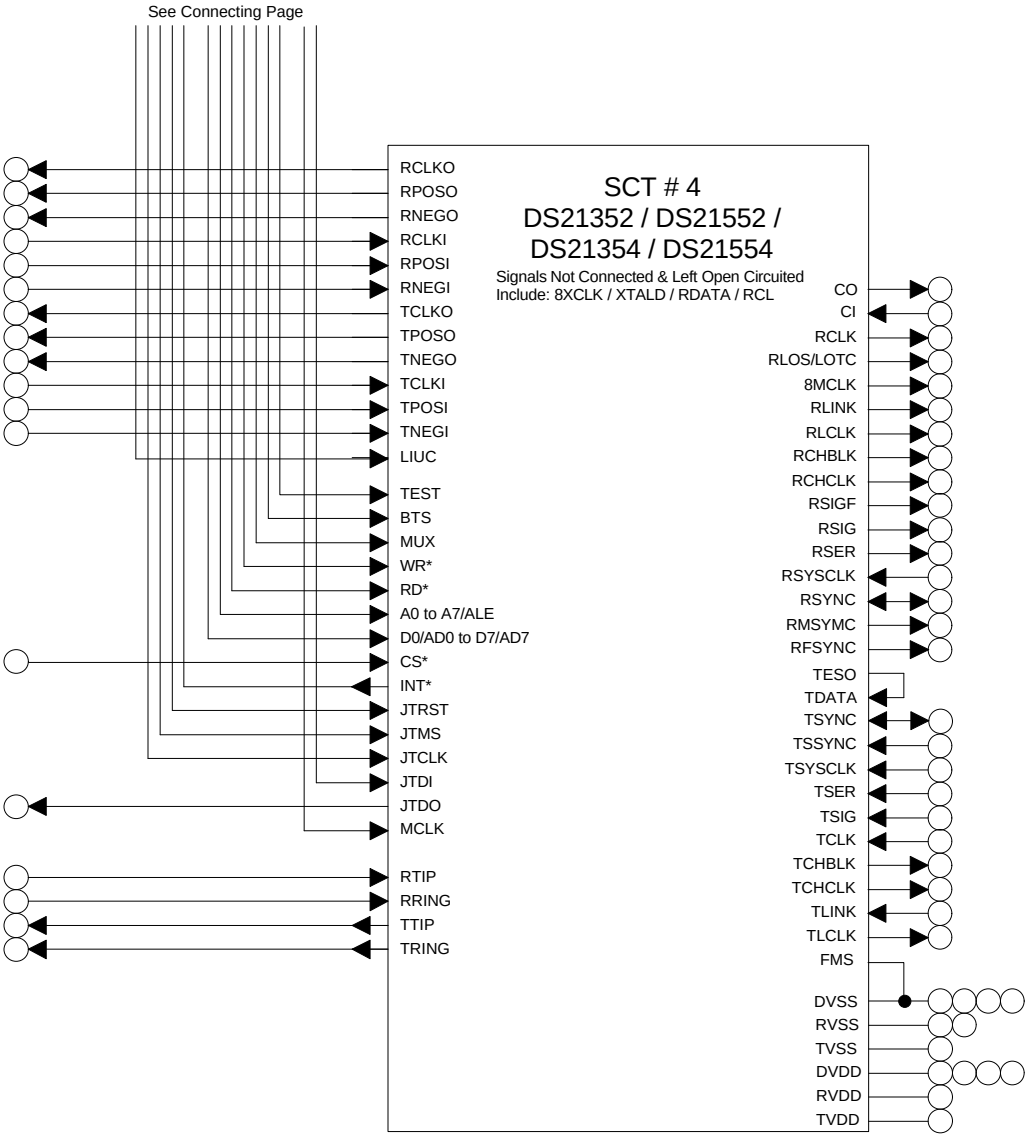
DS21Q352 / DS21Q552 / DS21Q354 / DS21Q554 Schematic Figure 1 (continued)



DS21Q352 / DS21Q552 / DS21Q354 / DS21Q554 Schematic Figure 1 (continued)



DS21Q352 / DS21Q552 / DS21Q354 / DS21Q554 Schematic Figure 1 (continued)



Lead Description Sorted by Symbol Table 2

Lead	Symbol	I/O	Description
M1	8MCLK1	O	8.192 MHz Clock Based on RCLK1.
H17	8MCLK2	O	8.192 MHz Clock Based on RCLK2.
F4	8MCLK3	O	8.192 MHz Clock Based on RCLK3.
V13	8MCLK4	O	8.192 MHz Clock Based on RCLK4.
U3	A0	I	Address Bus Bit 0 (lsb).
L17	A1	I	Address Bus Bit 1.
V2	A2	I	Address Bus Bit 2.
T4	A3	I	Address Bus Bit 3.
V8	A4	I	Address Bus Bit 4.
H4	A5	I	Address Bus Bit 5.
U8	A6	I	Address Bus Bit 6.
P4	A7/ALE	I	Address Bus Bit 7 (msb) / Address Latch Enable.
P2	BTS	I	Bus Type Select (0 = Intel / 1 = Motorola),
W6	CI1	I	Carry Input for Interleaved Bus Operation for SCT1.
F18	CI2	I	Carry Input for Interleaved Bus Operation for SCT2.
D7	CI3	I	Carry Input for Interleaved Bus Operation for SCT3.
T20	CI4	I	Carry Input for Interleaved Bus Operation for SCT4.
V9	CO1	O	Carry Output for Interleaved Bus Operation for SCT1.
B17	CO2	O	Carry Output for Interleaved Bus Operation for SCT2.
A6	CO3	O	Carry Output for Interleaved Bus Operation for SCT3.
J20	CO4	O	Carry Output for Interleaved Bus Operation for SCT4.
P3	CS1*	I	Chip Select for SCT1.
A14	CS2*	I	Chip Select for SCT2.
B5	CS3*	I	Chip Select for SCT3.
K17	CS4*	I	Chip Select for SCT4.
U11	D0/AD0	I/O	Data Bus Bit 0/ Address/Data Bus Bit 0 (lsb).
J19	D1/AD1	I/O	Data Bus Bit 1/ Address/Data Bus Bit 1.
W15	D2/AD2	I/O	Data Bus Bit 2/Address/Data Bus Bit 2.
U7	D3/AD3	I/O	Data Bus Bit 3/Address/Data Bus Bit 3.
U9	D4/AD4	I/O	Data Bus Bit 4/Address/Data Bus Bit 4.
U5	D5/AD5	I/O	Data Bus Bit 5/Address/Data Bus Bit 5.
V4	D6/AD6	I/O	Data Bus Bit 6/Address/Data Bus Bit 6.
U4	D7/AD7	I/O	Data Bus Bit 7/Address/Data Bus Bit 7 (msb).
J3	DVDD1	–	Digital Positive Supply.
N4	DVDD1	–	Digital Positive Supply.
U2	DVDD1	–	Digital Positive Supply.
V5	DVDD1	–	Digital Positive Supply.
B12	DVDD2	–	Digital Positive Supply.
C12	DVDD2	–	Digital Positive Supply.
C16	DVDD2	–	Digital Positive Supply.
D18	DVDD2	–	Digital Positive Supply.
A9	DVDD3	–	Digital Positive Supply.
B3	DVDD3	–	Digital Positive Supply.
B6	DVDD3	–	Digital Positive Supply.
C4	DVDD3	–	Digital Positive Supply.
G20	DVDD4	–	Digital Positive Supply.
M17	DVDD4	–	Digital Positive Supply.
M20	DVDD4	–	Digital Positive Supply.
P18	DVDD4	–	Digital Positive Supply.
H3	DVSS1	–	Digital Signal Ground.
J4	DVSS1	–	Digital Signal Ground.
U6	DVSS1	–	Digital Signal Ground.
W8	DVSS1	–	Digital Signal Ground.

A17	DVSS2	–	Digital Signal Ground.
A20	DVSS2	–	Digital Signal Ground.
B11	DVSS2	–	Digital Signal Ground.
C13	DVSS2	–	Digital Signal Ground.
A5	DVSS3	–	Digital Signal Ground.
B7	DVSS3	–	Digital Signal Ground.
B9	DVSS3	–	Digital Signal Ground.
C3	DVSS3	–	Digital Signal Ground.
H20	DVSS4	–	Digital Signal Ground
L20	DVSS4	–	Digital Signal Ground
N17	DVSS4	–	Digital Signal Ground
U13	DVSS4	–	Digital Signal Ground
U1	INT*	O	Interrupt for all four SCTs.
Y15	JTCLK	I	JTAG Clock.
N1	JTDI	I	JTAG Data Input.
H18	JTDO2	O	JTAG Data Output from SCT2.
V17	JTDO3	O	JTAG Data Output from SCT3.
V19	JTDO4	O	JTAG Data Output from SCT4.
W13	JTMS	I	JTAG Test Mode Select.
V18	JTRST*	I	JTAG Reset.
K2	LIUC	I	Line Interface Connect for all Four SCTs.
T1	MCLK1	I	Master Clock for SCT1 and SCT3.
W20	MCLK2	I	Master Clock for SCT2 and SCT4.
U10	MUX	I	Mux Bus Select.
M2	RCHBLK1	O	Receive Channel Block for SCT1.
G17	RCHBLK2	O	Receive Channel Block for SCT2.
G4	RCHBLK3	O	Receive Channel Block for SCT3.
Y12	RCHBLK4	O	Receive Channel Block for SCT4.
J1	RCHCLK1	O	Receive Channel Clock for SCT1.
D14	RCHCLK2	O	Receive Channel Clock for SCT2.
F3	RCHCLK3	O	Receive Channel Clock for SCT3.
U14	RCHCLK4	O	Receive Channel Clock for SCT4.
N3	RCLK1	O	Receive Clock Output from the Framer on SCT1.
B13	RCLK2	O	Receive Clock Output from the Framer on SCT2.
E3	RCLK3	O	Receive Clock Output from the Framer on SCT3.
M18	RCLK4	O	Receive Clock Output from the Framer on SCT4.
M4	RCLKI1	I	Receive Clock Input for the LIU on SCT1.
A15	RCLKI2	I	Receive Clock Input for the LIU on SCT2.
A4	RCLKI3	I	Receive Clock Input for the LIU on SCT3.
R17	RCLKI4	I	Receive Clock Input for the LIU on SCT4.
M3	RCLKO1	O	Receive Clock Output from the LIU on SCT1.
C14	RCLKO2	O	Receive Clock Output from the LIU on SCT2.
B4	RCLKO3	O	Receive Clock Output from the LIU on SCT3.
T17	RCLKO4	O	Receive Clock Output from the LIU on SCT4.
N2	RD*(DS*)	I	Read Input (Data Strobe)
K4	RFSYNC1	O	Receive Frame Sync (before the receive elastic store) for SCT1.
D17	RFSYNC2	O	Receive Frame Sync (before the receive elastic store) for SCT2.
A2	RFSYNC3	O	Receive Frame Sync (before the receive elastic store) for SCT3.
V14	RFSYNC4	O	Receive Frame Sync (before the receive elastic store) for SCT4.
F1	RLCLK1	O	Receive Link Clock for SCT1.
A12	RLCLK2	O	Receive Link Clock for SCT2.
D3	RLCLK3	O	Receive Link Clock for SCT3.
K18	RLCLK4	O	Receive Link Clock for SCT4.
G2	RLINK1	O	Receive Link Data for SCT1.
A13	RLINK2	O	Receive Link Data for SCT2.
A3	RLINK3	O	Receive Link Data for SCT3.
U12	RLINK4	O	Receive Link Data for SCT4.

H2	RLOS/LOTC1	O	Receive Loss Of Sync / Loss Of Transmit Clock for SCT1.
E17	RLOS/LOTC2	O	Receive Loss Of Sync / Loss Of Transmit Clock for SCT2.
E1	RLOS/LOTC3	O	Receive Loss Of Sync / Loss Of Transmit Clock for SCT3.
V11	RLOS/LOTC4	O	Receive Loss Of Sync / Loss Of Transmit Clock for SCT4.
L1	RMSYNC1	O	Receive Multiframe Sync for SCT1.
D16	RMSYNC2	O	Receive Multiframe Sync for SCT2.
F2	RMSYNC3	O	Receive Multiframe Sync for SCT3.
W16	RMSYNC4	O	Receive Multiframe Sync for SCT4.
R3	RNEGI1	I	Receive Negative Data for the Framer on SCT1.
D13	RNEGI2	I	Receive Negative Data for the Framer on SCT2.
A1	RNEGI3	I	Receive Negative Data for the Framer on SCT3.
P17	RNEGI4	I	Receive Negative Data for the Framer on SCT4.
L3	RNEGO1	O	Receive Negative Data from the LIU on SCT1.
B15	RNEGO2	O	Receive Negative Data from the LIU on SCT2.
C2	RNEGO3	O	Receive Negative Data from the LIU on SCT3.
U17	RNEGO4	O	Receive Negative Data from the LIU on SCT4.
R4	RPOSI1	I	Receive Positive Data for the Framer on SCT1.
B14	RPOSI2	I	Receive Positive Data for the Framer on SCT2.
B2	RPOSI3	I	Receive Positive Data for the Framer on SCT3.
V15	RPOSI4	I	Receive Positive Data for the Framer on SCT4.
L4	RPOSO1	O	Receive Positive Data from the LIU on SCT1.
A16	RPOSO2	O	Receive Positive Data from the LIU on SCT2.
B1	RPOSO3	O	Receive Positive Data from the LIU on SCT3.
U15	RPOSO4	O	Receive Positive Data from the LIU on SCT4.
Y11	RRING1	I	Receive Analog Ring Input for SCT1.
Y14	RRING2	I	Receive Analog Ring Input for SCT2.
Y17	RRING3	I	Receive Analog Ring Input for SCT3.
Y20	RRING4	I	Receive Analog Ring Input for SCT4.
J2	RSER1	O	Receive Serial Data for SCT1.
D15	RSER2	O	Receive Serial Data for SCT2.
E2	RSER3	O	Receive Serial Data for SCT3.
W17	RSER4	O	Receive Serial Data for SCT4.
L2	RSIG1	O	Receive Signaling Output for SCT1.
B16	RSIG2	O	Receive Signaling Output for SCT2.
C1	RSIG3	O	Receive Signaling Output for SCT3.
Y18	RSIG4	O	Receive Signaling Output for SCT4.
K1	RSIGF1	O	Receive Signaling Freeze Output for SCT1.
C15	RSIGF2	O	Receive Signaling Freeze Output for SCT2.
D2	RSIGF3	O	Receive Signaling Freeze Output for SCT3.
V16	RSIGF4	O	Receive Signaling Freeze Output for SCT4.
G1	RSYNC1	I/O	Receive Sync for SCT1.
D12	RSYNC2	I/O	Receive Sync for SCT2.
D1	RSYNC3	I/O	Receive Sync for SCT3.
V12	RSYNC4	I/O	Receive Sync for SCT4.
H1	RSYSCLK1	I	Receive System Clock for SCT1.
F17	RSYSCLK2	I	Receive System Clock for SCT2.
G3	RSYSCLK3	I	Receive System Clock for SCT3.
W14	RSYSCLK4	I	Receive System Clock for SCT4.
Y10	RTIP1	I	Receive Analog Tip Input for SCT1.
Y13	RTIP2	I	Receive Analog Tip Input for SCT2.
Y16	RTIP3	I	Receive Analog Tip Input for SCT3.
Y19	RTIP4	I	Receive Analog Tip Input for SCT4.
P1	RVDD1	–	Receive Analog Positive Supply.
J17	RVDD2	–	Receive Analog Positive Supply.
E4	RVDD3	–	Receive Analog Positive Supply.
W18	RVDD4	–	Receive Analog Positive Supply.
R2	RVSS1	–	Receive Analog Signal Ground

T2	RVSS1	–	Receive Analog Signal Ground
H19	RVSS2	–	Receive Analog Signal Ground
J18	RVSS2	–	Receive Analog Signal Ground
D4	RVSS3	–	Receive Analog Signal Ground
D5	RVSS3	–	Receive Analog Signal Ground
V20	RVSS4	–	Receive Analog Signal Ground
W19	RVSS4	–	Receive Analog Signal Ground
W1	TCHBLK1	O	Transmit Channel Block for SCT1.
F20	TCHBLK2	O	Transmit Channel Block for SCT2.
C11	TCHBLK3	O	Transmit Channel Block for SCT3.
U20	TCHBLK4	O	Transmit Channel Block for SCT4.
V10	TCHCLK1	O	Transmit Channel Clock for SCT1.
A18	TCHCLK2	O	Transmit Channel Clock for SCT2.
B8	TCHCLK3	O	Transmit Channel Clock for SCT3.
L18	TCHCLK4	O	Transmit Channel Clock for SCT4.
Y9	TCLK1	I	Transmit Clock for SCT1.
B19	TCLK2	I	Transmit Clock for SCT2.
B10	TCLK3	I	Transmit Clock for SCT3.
M19	TCLK4	I	Transmit Clock for SCT4.
V6	TCLKI1	I	Transmit Clock Input for the LIU on SCT1.
D19	TCLKI2	I	Transmit Clock Input for the LIU on SCT2.
C8	TCLKI3	I	Transmit Clock Input for the LIU on SCT3.
P20	TCLKI4	I	Transmit Clock Input for the LIU on SCT4.
W7	TCLKO1	O	Transmit Clock Output from the Framer on SCT1.
E18	TCLKO2	O	Transmit Clock Output from the Framer on SCT2.
A7	TCLKO3	O	Transmit Clock Output from the Framer on SCT3.
P19	TCLKO4	O	Transmit Clock Output from the Framer on SCT4.
U16	TEST	I	Test (0 = normal operation / 1 = tri-state all outputs).
V3	TLCLK1	O	Transmit Link Clock for SCT1.
E20	TLCLK2	O	Transmit Link Clock for SCT2.
D6	TLCLK3	O	Transmit Link Clock for SCT3.
T18	TLCLK4	O	Transmit Link Clock for SCT4.
W5	TLINK1	I	Transmit Link Data for SCT1.
E19	TLINK2	I	Transmit Link Data for SCT2.
C6	TLINK3	I	Transmit Link Data for SCT3.
T19	TLINK4	I	Transmit Link Data for SCT4.
R1	TNEGI1	I	Transmit Negative Data Input for the LIU on SCT1.
F19	TNEGI2	I	Transmit Negative Data Input for the LIU on SCT2.
D8	TNEGI3	I	Transmit Negative Data Input for the LIU on SCT3.
R20	TNEGI4	I	Transmit Negative Data Input for the LIU on SCT4.
T3	TNEGO1	O	Transmit Negative Data Output from Framer on SCT1.
B20	TNEGO2	O	Transmit Negative Data Output from Framer on SCT2.
D9	TNEGO3	O	Transmit Negative Data Output from Framer on SCT3.
N20	TNEGO4	O	Transmit Negative Data Output from Framer on SCT4.
W3	TPOSI1	I	Transmit Positive Data Input for the LIU on SCT1.
C20	TPOSI2	I	Transmit Positive Data Input for the LIU on SCT2.
A8	TPOSI3	I	Transmit Positive Data Input for the LIU on SCT3.
R19	TPOSI4	I	Transmit Positive Data Input for the LIU on SCT4.
V7	TPOSO1	O	Transmit Positive Data Output from Framer on SCT1.
C19	TPOSO2	O	Transmit Positive Data Output from Framer on SCT2.
C9	TPOSO3	O	Transmit Positive Data Output from Framer on SCT3.
N19	TPOSO4	O	Transmit Positive Data Output from Framer on SCT4.
Y2	TRING1	O	Transmit Analog Ring Output for SCT1.
Y4	TRING2	O	Transmit Analog Ring Output for SCT2.
Y6	TRING3	O	Transmit Analog Ring Output for SCT3.
Y8	TRING4	O	Transmit Analog Ring Output for SCT4.
W9	TSER1	I	Transmit Serial Data for SCT1.

C17	TSER2	I	Transmit Serial Data for SCT2.
C10	TSER3	I	Transmit Serial Data for SCT3.
K20	TSER4	I	Transmit Serial Data for SCT4.
W10	TSIG1	I	Transmit Signaling Input for SCT1.
C18	TSIG2	I	Transmit Signaling Input for SCT2.
A10	TSIG3	I	Transmit Signaling Input for SCT3.
L19	TSIG4	I	Transmit Signaling Input for SCT4.
W12	TSSYNC1	I	Transmit System Sync for SCT1.
B18	TSSYNC2	I	Transmit System Sync for SCT2.
D10	TSSYNC3	I	Transmit System Sync for SCT3.
K19	TSSYNC4	I	Transmit System Sync for SCT4.
V1	TSYNC1	I/O	Transmit Sync for SCT1.
D20	TSYNC2	I/O	Transmit Sync for SCT2.
C7	TSYNC3	I/O	Transmit Sync for SCT3.
R18	TSYNC4	I/O	Transmit Sync for SCT4.
W11	TSYSCLK1	I	Transmit System Clock for SCT1.
A19	TSYSCLK2	I	Transmit System Clock for SCT2.
A11	TSYSCLK3	I	Transmit System Clock for SCT3.
N18	TSYSCLK4	I	Transmit System Clock for SCT4.
Y1	TTIP1	O	Transmit Analog Tip Output for SCT1.
Y3	TTIP2	O	Transmit Analog Tip Output for SCT2.
Y5	TTIP3	O	Transmit Analog Tip Output for SCT3.
Y7	TTIP4	O	Transmit Analog Tip Output for SCT4.
W2	TVDD1	–	Transmit Analog Positive Supply.
G19	TVDD2	–	Transmit Analog Positive Supply.
D11	TVDD3	–	Transmit Analog Positive Supply.
U19	TVDD4	–	Transmit Analog Positive Supply.
W4	TVSS1	–	Transmit Analog Signal Ground.
G18	TVSS2	–	Transmit Analog Signal Ground.
C5	TVSS3	–	Transmit Analog Signal Ground.
U18	TVSS4	–	Transmit Analog Signal Ground.
K3	WR* (R/W*)	I	Write Input (Read/Write).

DS21Q352 / DS21Q552 / DS21Q354 / DS21Q554 PCB Land Pattern Figure 2

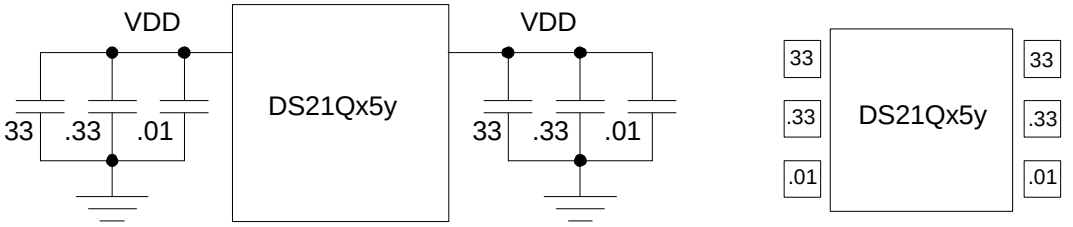
The diagram shown below is the lead pattern that will be placed on the target PCB. This is the same pattern that would be seen as viewed through the MCM from the top.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	rneg i 3	rf sync 3	rlink 3	rclk i 3	dvss 3	co 3	tclko 3	tpos i 3	dvdd 3	tsig 3	tsys clk 3	rlclk 3	rlink 2	cs 2*	rclki 2	rpos o 2	dvss 2	tch clk 2	tsys clk 2	dvss 2
B	rpos o 3	rposi 3	dvdd 3	rclk o 3	cs 3*	dvdd 3	dvss 3	tch clk 3	dvss 3	tclk 3	dvss 2	dvdd 2	rclk 2	rpos i 2	rneg o 2	rsig 2	co 2	ts sync 2	tclk 2	tneg o 2
C	rsig 3	rneg o 3	dvss 3	dvdd 3	tvss 3	tlink 3	tsync 3	tclk i 3	tpos o 3	tser 3	tch blk 3	dvdd 2	dvss 2	rclk o 2	rsigf 2	dvdd 2	tser 2	tsig 2	tpos o 2	tpos i 2
D	rsync 3	rsigf 3	rlclk 3	rvss 3	rvss 3	tlclk 3	ci 3	tneg i 3	tneg o 3	ts sync 3	tvdd 3	rsync 2	rneg i 2	rch clk 2	rser 2	rm sync 2	rf sync 2	dvdd 2	tclk i 2	tsync 2
E	rlos 3	rser 3	rclk 3	rvdd 3													rlos 2	tclk o 2	tlink 2	tlclk 2
F	rlclk 1	rm sync 3	rch clk 3	8m clk 3													rsys clk 2	ci 2	tneg i 2	tch blk 2
G	rsync 1	rlink 1	rsys clk 3	rch blk 3													rch blk 2	tvss 2	tvdd 2	dvdd 4
H	rsys clk 1	rlos 1	dvss 1	A5													8m clk 2	jtdo 2	rvss 2	dvss 4
J	rch clk 1	rser 1	dvdd 1	dvss 1													rvdd 2	rvss 2	D1/ AD1	co 4
K	rsigf 1	liuc	wr*	rf sync 1													cs 4*	rlclk 4	ts sync 4	tser 4
L	rm sync 1	rsig 1	rneg o 1	rpos o 1													A1	tch clk 4	tsig 4	dvss 4
M	8m clk 1	rch blk 1	rclk o 1	rclk i 1													dvdd 4	rclk 4	tclk 4	dvdd 4
N	jtdi	rd*	rclk 1	dvdd 1													dvss 4	tsys clk 4	tpos o 4	tneg o 4
P	rvdd 1	bts	cs 1*	A7/ ALE													rneg i 4	dvdd 4	tclk o 4	tclk i 4
R	tneg i 1	rvss 1	rneg i 1	rpos i 1													rclk i 4	tsync 4	tpos i 4	tneg i 4
T	mclk 1	rvss 1	tneg o 1	A3													rclk o 4	tlclk 4	tlink 4	ci 4
U	int*	dvdd 1	A0	D7/ AD7	D5/ AD5	dvss 1	D3/ AD3	A6	D4/ AD4	mux	D0/ AD0	rlink 4	dvss 4	rch clk 4	rpos o 4	test	rneg o 4	tvss 4	tvdd 4	tch blk 4
V	tsync 1	A2	tlclk 1	D6/ AD6	dvdd 1	tclk i 1	tpos o 1	A4	co 1	tch clk 1	rlos 4	rsync 4	8m clk 4	rf sync 4	rpos i 4	rsigf 4	jtdo3	jtrst*	jtdo4	rvss 4
W	tch blk 1	tvdd 1	tpos i 1	tvss 1	tlink 1	ci 1	tclk o 1	dvss 1	tser 1	tsig 1	tsys clk 1	ts sync 1	jtms	rsys clk 4	D2/ AD2	rm sync 4	rser 4	rvdd 4	rvss 4	mclk 2
Y	ttip 1	tring 1	ttip 2	tring 2	ttip 3	tring 3	ttip 4	tring 4	tclk 1	rtip 1	rring 1	rch blk 4	rtip 2	rring 2	jtclk	rtip 3	rring 3	rsig 4	rtip 4	rring 4

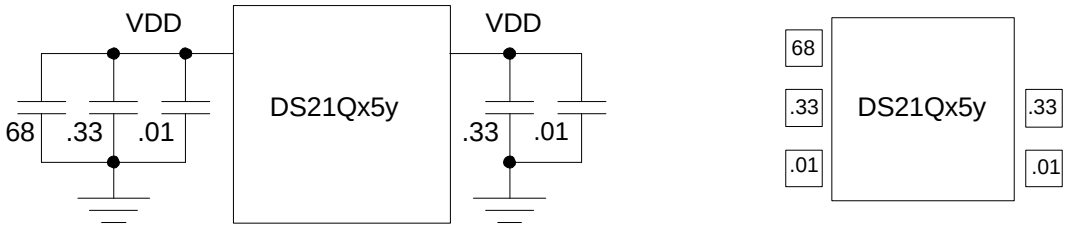
POWER SUPPLY DE-COUPLING

In a typical PCB layout for the DS21x5y, all of the VDD pins will connect to a common power plane and all the VSS lines will connect to a common ground plane. There are three recommended methods for de-coupling shown below in both schematic and pictorial form. As shown in the pictorials, the capacitors should be symmetrically located about the device. The first shown in figure 3 uses standard capacitors, two 33uf tantalums, two .33uf ceramics and two .01uf ceramics. The second method shown in figure 4 uses a single 68uf tantalum, two .33uf ceramics and two .01uf ceramics. The third method shown in figure 5 uses only four capacitors, two 1.5uf MLC and two .01uf ceramics. The 1.5uf is an MLC (Multi Layer Ceramic) type. The MLC construction is a low inductance type, which allows a smaller value of capacitance to be used. Since VDD and VSS signals will typically pass vertically to the power and ground planes of a PCB, the de-coupling caps must be placed as close to the DS21Qx5y as possible and routed vertically to power and ground planes.

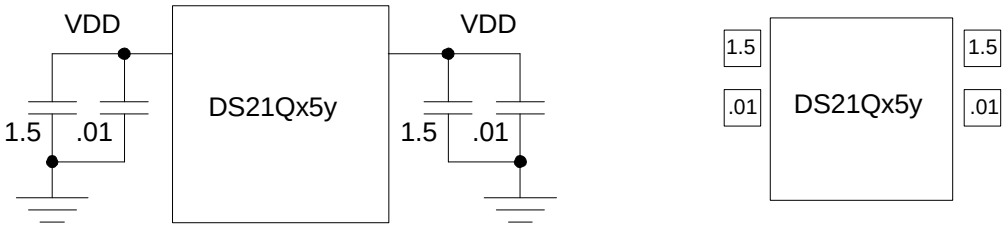
De-coupling scheme using standard tantalum caps. Figure 3



De-coupling scheme using single 68uf cap. Figure 4

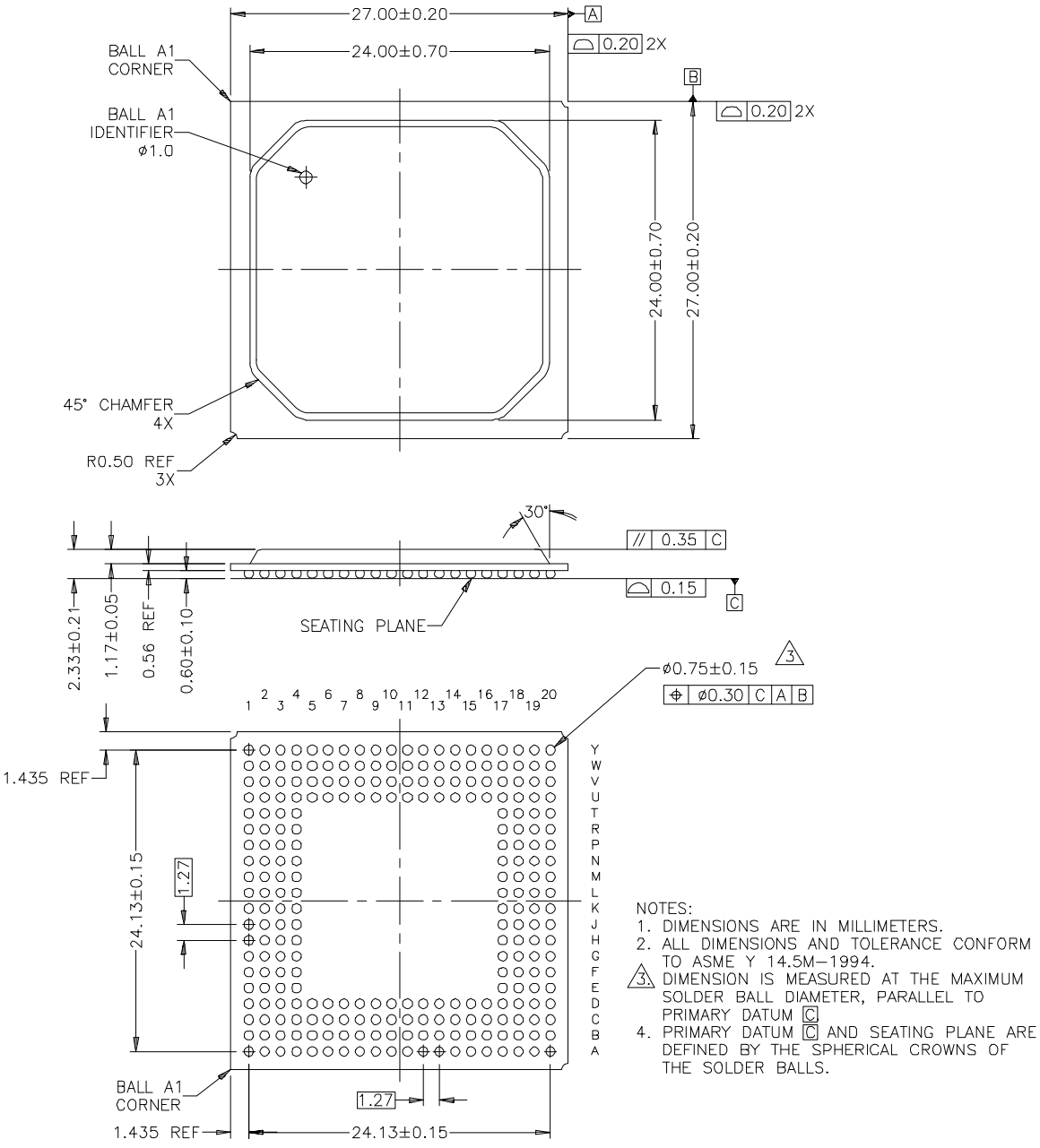


De-coupling scheme using MCL caps. Figure 5



All capacitor values in figures 3, 4 and 5 are in uf.

DS21Q352 / DS21Q552 / DS21Q354 / DS21Q554 Mechanical Dimensions



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