DS2406
Dual Addressable Switch Plus 1Kb Memory

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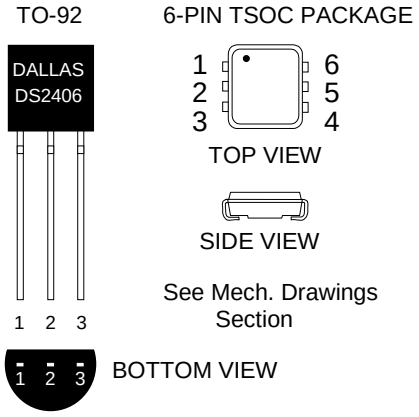
FEATURES

- Open drain PIO pins are controlled and their logic level can be determined over 1-Wire® bus for closed-loop control
- Replaces and is fully compatible with DS2407 but no user-programmable power-on settings and no Hidden Mode
- PIO channel A sink capability of 50mA at 0.4V with soft turn-on; channel B 8mA at 0.4V
- Maximum operating voltage of 13V at PIO-A, 6.5V at PIO-B
- 1024 bits user-programmable OTP EPROM
- User-programmable status memory to control the device
- Multiple DS2406's can be identified on a common 1-Wire bus and be turned on or off independently of other devices on the bus
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures error-free selection and absolute identity because no two parts are alike
- On-chip CRC16 generator allows detection of data transfer errors
- Built-in multidrop controller ensures compatibility with other 1-Wire net products
- Reduces control, address, data, programming and power to a single data pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 15.4 kbits/s
- Supports Conditional Search with user-selectable condition
- V_{cc} bondout for optional external supply to the device (TSOC package only)
- 1-Wire communication operates over a wide voltage range of 2.8V to 6.0V from -40°C to +85°C
- Low cost TO-92 and 6-pin TSOC packages

PIN ASSIGNMENT



PIN DESCRIPTION

	TO-92	TSOC
Pin 1	Ground	Ground
Pin 2	Data	Data
Pin 3	PIO-A	PIO-A
Pin 4	---	V_{cc}
Pin 5	---	NC
Pin 6	---	PIO-B

ORDERING INFORMATION

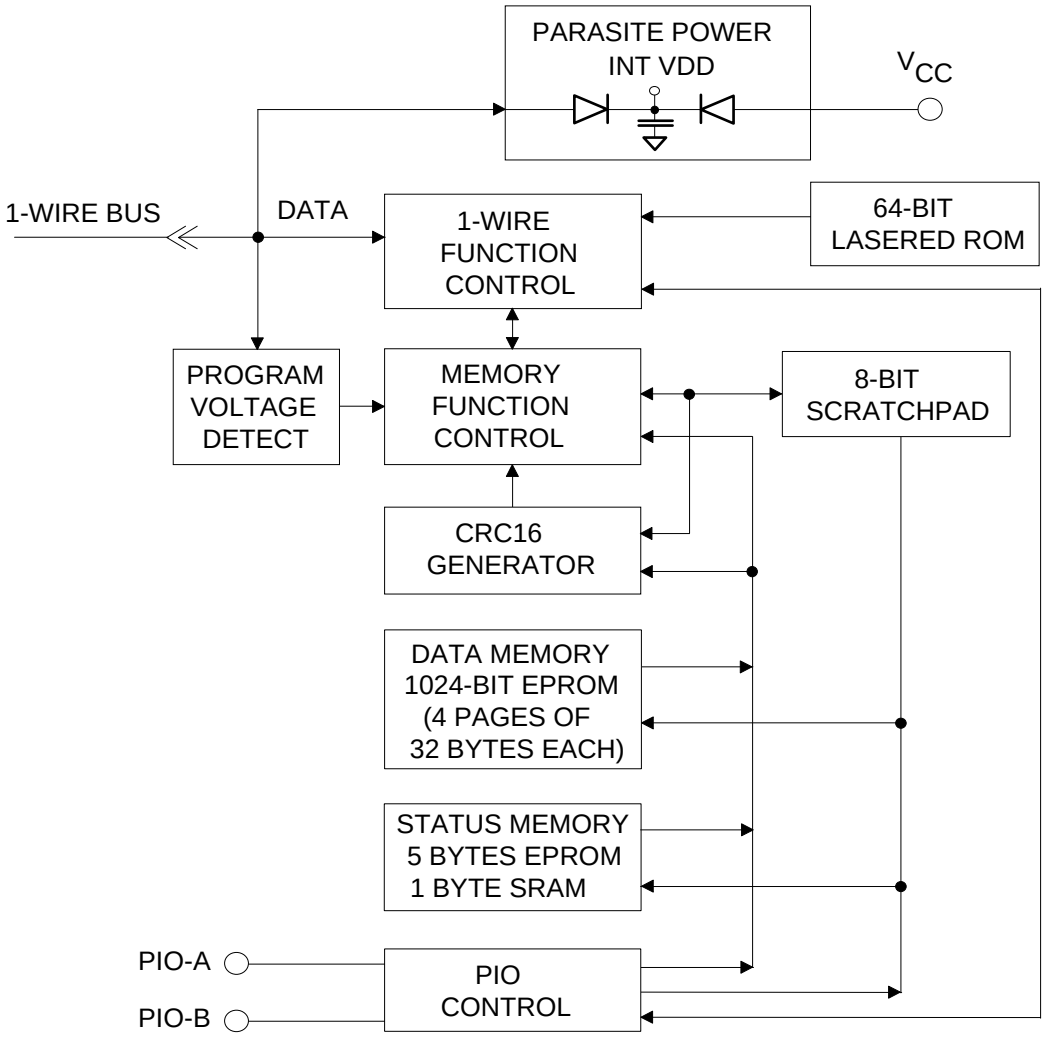
DS2406+	TO-92 Package
DS2406+T&R	TO-92 Package, Tape & Reel
DS2406P+	6-pin TSOC Package
DS2406P+T&R	TSOC Package, Tape & Reel

+ Indicates lead-free compliance.

ADDRESSABLE SWITCH DESCRIPTION

The DS2406 Dual Addressable Switch Plus Memory offers a simple way to remotely control a pair of open drain transistors and to monitor the logic level at each transistor's output via the 1-Wire bus for closed loop control. Each DS2406 has its own 64-bit ROM registration number that is factory lasered into the chip to provide a guaranteed unique identity for absolute traceability. The device's 1024 bits of EPROM can be used as electronic label to store information such as switch function, physical location, and installation date. Communication with the DS2406 follows the standard Dallas Semiconductor 1-Wire protocol and can be accomplished with minimal hardware such as a single port pin of a microcontroller. Multiple DS2406 devices can reside on a common 1-Wire network and be operated independently of each other. Individual devices will respond to a Conditional Search command if they qualify for certain user-specified conditions, which include the state of the output transistor, the static logic level or a voltage transition at the transistor's output.

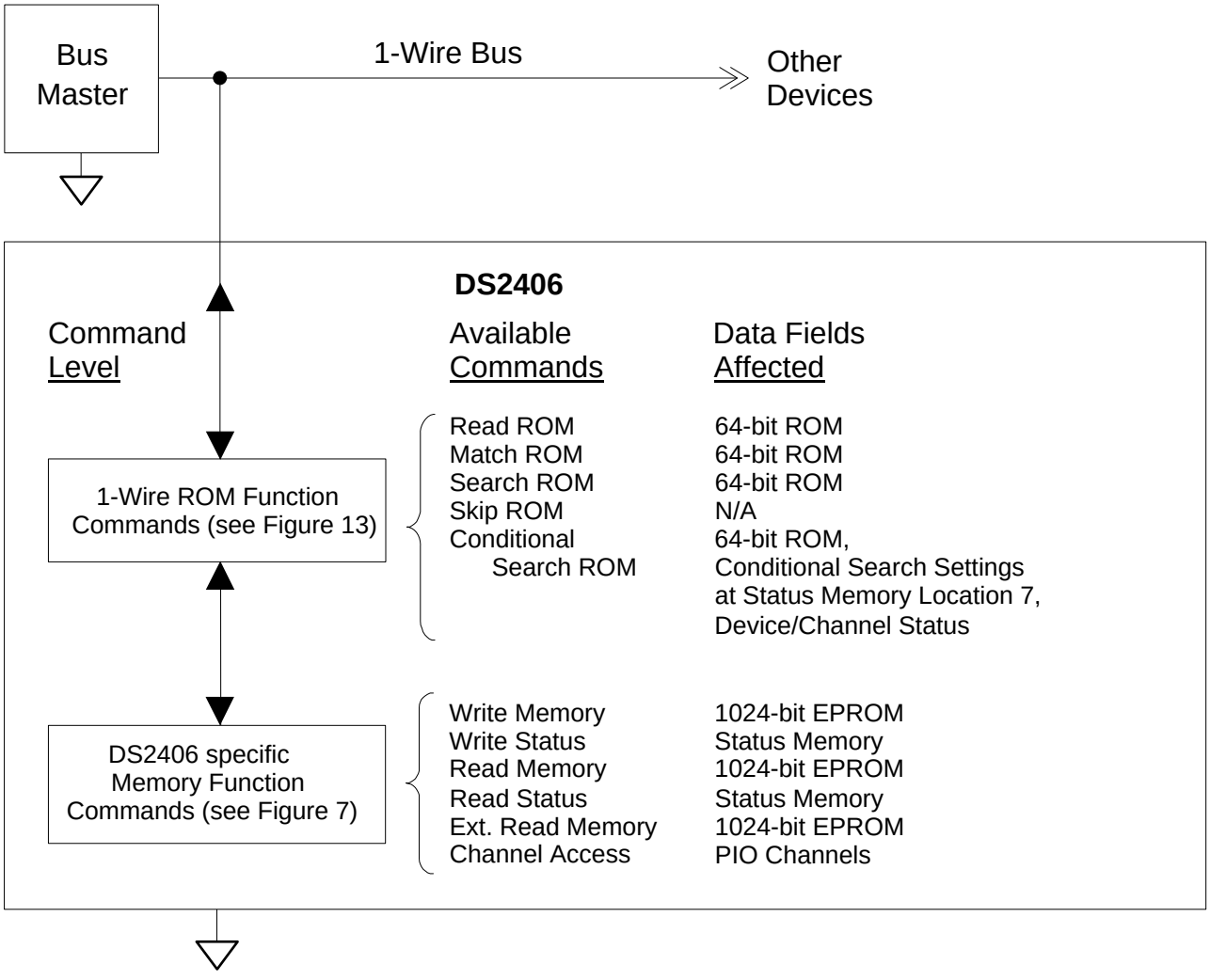
DS2406 BLOCK DIAGRAM Figure 1



OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS2406. The device has four major data components: 64-bit lasered ROM, 1024 bits of EPROM data memory, status memory, and the PIO-control block. The hierarchical structure of the 1-Wire protocol is shown in Figure 2. The bus master must first provide one of the five ROM function commands: Read ROM, Match ROM, Search ROM, Skip ROM, or Conditional Search ROM. The protocol required for these ROM functions is described in Figure 13. After a ROM functions command is successfully executed, the PIO-control and memory functions become accessible and the master may provide any one of the six memory- and control function commands. The protocol for these functions is described in Figure 7. All data is read and written least significant bit first.

HIERARCHICAL STRUCTURE FOR 1-Wire PROTOCOL Figure 2



PARASITE POWER

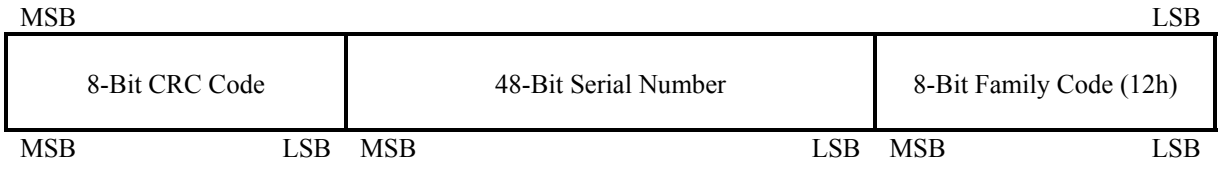
The DS2406 can derive its power entirely from the 1-Wire bus by storing energy on an internal capacitor during periods of time when the signal line is high. During low times the device continues to operate off of this "parasite" power source until the 1-Wire bus returns high to replenish the parasite (capacitor) supply. In applications where the device may be temporarily disconnected from the 1-Wire bus or where the low-times of the 1-Wire bus may be very long the V_{CC} pin may be connected to an external voltage supply to maintain the device status.

When writing to the EPROM memory, the 1-Wire communication occurs at normal voltage levels and then is pulsed momentarily to the programming voltage to cause the selected EPROM bits to be programmed. The bus master must be able to provide 12V and 10mA to adequately program the EPROM portions of the device. During programming, only EPROM-based devices are allowed to be present on the 1-Wire bus.

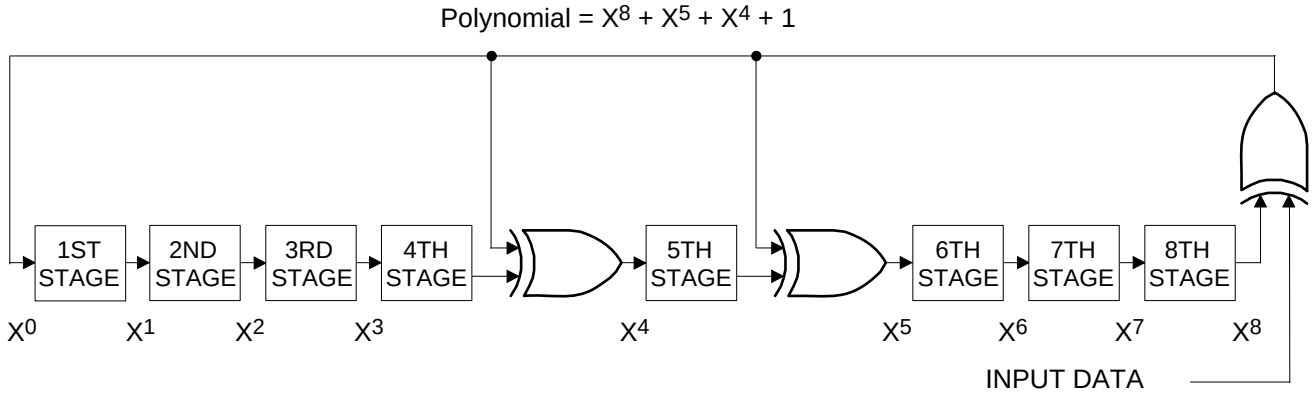
64-BIT LASERED ROM

Each DS2406 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (See Figure 3). The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in *Application Note 27*. The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, 1 bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all zeros. The 64-bit ROM and the 1-Wire Function Control section allow the DS2406 to operate as a 1-Wire device and follow the protocol detailed in the section "1-Wire Bus System".

64-BIT LASERED ROM Figure 3



1-WIRE CRC GENERATOR Figure 4



MEMORY MAP

The DS2406 has two memory sections, called data memory and status memory. The data memory consists of 1024 bits of one-time programmable EPROM organized as 4 pages of 32 bytes each. The address range of the device's status memory is 8 bytes. The first seven bytes of status memory (addresses 0 to 6) are implemented as EPROM. The eighth byte (address 7) consists of static RAM. The complete memory map is shown in Figure 5. The 8-bit scratchpad is an additional register that acts as a buffer when writing the memory. Data is first written to the scratchpad and then verified by reading a 16-bit CRC from the DS2406 that confirms proper receipt of the data and address. This process ensures data integrity when programming the memory. If the buffer contents are correct, the bus master should transmit a programming pulse (EPROM) or a dummy byte FFh (RAM) to transfer the data from the scratchpad to the addressed memory location. The details for reading and programming the DS2406 are given in the Memory Function Commands section.

DS2406 MEMORY MAP Figure 5

8-Bit Scratchpad

	Page #	Address Range	Description
1K-Bit EPROM	0	0000h to 001Fh	32-Byte final storage Data Memory
	1	0020h to 003Fh	32-Byte final storage Data Memory
	2	0040h to 005Fh	32-Byte final storage Data Memory
	3	0060h to 007Fh	32-Byte final storage Data Memory

8 Bytes Status Memory						
Valid Device Settings (SRAM)	00	Factory Test Byte	Redirection Bytes	Bitmap of Used Pages	Write-Protect Bits Data Memory	

DS2406 STATUS MEMORY MAP Figure 6

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0 (EPROM)	BM3	BM2	BM1	BM0	WP3	WP2	WP1	WP0
1 (EPROM)	1	1	1	1	1	1	Redir. 0	Redir. 0
2 (EPROM)	1	1	1	1	1	1	Redir. 1	Redir. 1
3 (EPROM)	1	1	1	1	1	1	Redir 2	Redir 2
4 (EPROM)	1	1	1	1	1	1	Redir 3	Redir 3
5 (EPROM)	EPROM Factory Test byte							
6 (EPROM)	Don't care, always reads 00							
7 (SRAM)	Supply Indication (read only)	PIO-B Channel Flip-flop	PIO-A Channel Flip-flop	CSS4 Channel Select	CSS3 Channel Select	CSS2 Source Select	CSS1 Source Select	CSS0 Polarity

STATUS MEMORY

The Status Memory can be read or written to indicate various conditions to the software interrogating the DS2406. These conditions include special features for the data memory, definition of the settings for the Conditional Search as well as the channel flip-flops and the external power supply indication. How these functions are assigned to the bits of the Status Memory is detailed in Figure 6.

The first 4 bits of the Status Memory (address 0, bits 0 to 3) contain the Write Protect Page bits which inhibit programming of the corresponding page in the 1024-bit data memory area if the appropriate write protection bit is programmed. Once a bit has been programmed in the Write Protect Page section of the Status Memory, the entire 32-byte page that corresponds to that bit can no longer be altered but may still be read. The remaining 4 bits of Status Memory location 0 are reserved for use by the 1-Wire File Structure, indicating which memory pages are already in use. Originally, all of these bits are unprogrammed, indicating that the device does not contain any data. As soon as data is written to any page of the device under control of TMEX, the bit inside this bitmap corresponding to that page will be programmed to 0, marking this page as used. These bits are application flags only and have no impact on the internal logic of the DS2406.

The next four bytes of the Status Memory (addresses 1 to 4) contain the Page Address Redirection Bytes which indicate if one or more of the pages of data in the 1024-bits EPROM memory section have been invalidated by software and redirected to the page address contained in the appropriate redirection byte. The hardware of the DS2406 makes no decisions based on the contents of the Page Address Redirection Bytes. Since with EPROM technology bits can only be changed from a logical 1 to a logical 0 by programming, it is not possible to simply rewrite a page if the data requires changing or updating. But with space permitting, an entire page of data can be redirected to another page within the DS2406. Under TMEX, a page is redirected by writing the one's complement of the new page address into the Page Address Redirection Byte that corresponds to the original (replaced) page. This architecture allows the user's software to make a "data patch" to the EPROM by indicating that a particular page or pages should be replaced with those indicated in the Page Address Redirection Bytes.

Under TMEX, if a Page Address Redirection Byte has a FFh value, the data in the main memory that corresponds to that page is valid. If a Page Address Redirection Byte has some other hex value than FFh, the data in the page corresponding to that redirection byte is invalid. According to the TMEX definitions, the valid data will now be found at the one's complement of the page address indicated by the hex value stored in the associated Page Address Redirection Byte. A value of FDh in the redirection byte for page 1, for example, would indicate that the updated data is now in page 2. Since the data memory consists of four pages only, the 6 most significant bits of the redirection bytes cannot be programmed to zeros.

Status Memory location 5 serves as a test byte and is programmed to 00h at the factory. Status Memory location 6 has no function with the DS2406. It is factory-programmed to 00h to distinguish the DS2406 from the DS2407, which both share the same family code. A DS2407 with Status Memory location 6 programmed to 00h will power-up into hidden mode and will only respond if the bus master addresses it by a Match ROM command followed by the correct device ROM code. Conversely, a device that does respond to a Read ROM command with family code 12h can only be a DS2406 if its Status Memory location 6 reads 00h.

Status Memory location 7 serves three purposes: 1) it holds the selection code for the Conditional Search function, 2) provides the bus master a memory mapped access to the channel flip-flops that control the PIO output transistors, and 3) allows the bus master to determine whether the device is hooked up to a V_{CC} power supply. Bit locations 0 to 4 store the conditional search settings. Their codes are explained in the section "ROM Function Commands" later in this document. The channel flip-flops are accessible through bit locations 5 and 6 as well as through the Channel Access function. The power-on default for the conditional search settings and the channel flip-flops is all 1's. Setting a channel flip-flop to 0 will make the associated PIO-transistor conducting or on; setting the flip-flop to 1 will switch the transistor off, which is identical to the power-on default. With the V_{CC} pin connected to a suitable power supply the power indicator bit 7 will read 1. The power supply indicator can also be read through the Channel Access function.

MEMORY FUNCTION COMMANDS

The "Memory Function Flow Chart" (Figure 7) describes the protocols necessary for accessing the various data fields and PIO channels within the DS2406. The Memory Function Control section, 8-bit scratchpad, and the Program Voltage Detect circuit combine to interpret the commands issued by the bus master and create the correct control signals within the device. A three-byte protocol is issued by the bus master. It is comprised of a command byte to determine the type of operation and two address bytes to determine the specific starting byte location within a data field or to supply and exchange setup and status data when accessing the PIO channels. The command byte indicates if the device is to be read or written or if the PIO channels are to be accessed. Writing data involves not only issuing the correct command sequence but also providing a 12-volt programming voltage at the appropriate times. To execute a write sequence, a byte of data is first loaded into the scratchpad and then programmed into the selected address. Write sequences always occur a byte at a time. To execute a read sequence, the starting address is issued by the bus master and data is read from the part beginning at that initial location and continuing to the end of the selected data field or until a reset sequence is issued. All bits transferred to the DS2406 and received back by the bus master are sent least significant bit first.

Read Memory [F0h]

The Read Memory command is used to read data from the 1024-bit EPROM data memory field. The bus master follows the command byte with a two-byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. Since the data memory contains 128 bytes, T15:T8 and T7 should all be zero. With every subsequent read data time slot the bus master receives data from the DS2406 starting at the initial address and continuing until the end of the 1024-bits data field is reached or until a Reset Pulse is issued. If reading occurs through the end of memory space, the bus master may issue sixteen additional read time slots and the DS2406 will respond with a 16-bit CRC of the command, address bytes and all data bytes read from the initial starting byte through the last byte of memory. This CRC is the result of clearing the CRC generator and then shifting in the command byte followed by the two address bytes and the data bytes beginning at the first addressed memory location and continuing through to the last byte of the EPROM data memory. After the CRC is received by the bus master, any subsequent read time slots will appear as logical 1s until a Reset Pulse is issued. Any reads ended by a Reset Pulse prior to reaching the end of memory will not have the 16-bit CRC available.

Typically the software controlling the device should store a 16-bit CRC with each page of data to insure rapid, error-free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (See *Application Note 114* for the recommended file structure). If CRC values are imbedded within the data it is unnecessary to read the end-of-memory CRC. The Read Memory command can be ended at any point by issuing a Reset Pulse.

Extended Read Memory [A5h]

The Extended Read Memory command supports page redirection when reading data from the 1024-bit EPROM data field. One major difference between the Extended Read Memory and the basic Read Memory command is that the bus master receives the Redirection Byte (see description of Status Memory) first before investing time in reading data from the addressed memory location. This allows the bus master to quickly decide whether to continue and access the data at the selected starting page or to terminate and restart the reading process at the redirected page address.

In addition to page redirection, the Extended Read Memory command also supports "bit-oriented" applications where the user cannot store a 16-bit CRC with the data itself. With bit-oriented applications the EPROM information may change over time within a page boundary making it impossible to include an accompanying CRC that will always be valid. Therefore, the Extended Read Memory command concludes each page with the DS2406 generating and supplying a 16-bit CRC that is based on and therefore always consistent with the current data stored in each page of the 1024-bit EPROM data field.

After having sent the command code of the Extended Read Memory command, the bus master sends a two-byte address (TA1=(T7:T0), TA2=(T15:T8)) that indicates a starting byte location within the data field. By sending eight read data time slots, the master receives the Redirection Byte associated with the page given by the starting address. With the next sixteen read data time slots, the bus master receives a 16-bit CRC of the command byte, address bytes and the Redirection Byte. This CRC is computed by the DS2406 and read back by the bus master to check if the command word, starting address and Redirection Byte were received correctly.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, the bus master issues read time slots and receives data from the DS2406 starting at the initial address and continuing until the end of a 32-byte page is reached. At that point the bus master will send sixteen additional read time slots and receive a 16-bit CRC that is the result of shifting into the CRC generator all of the data bytes from the initial starting byte to the last byte of the current page.

With the next 24 read data time slots the master will receive the Redirection Byte of the next page followed by a 16-bit CRC of the Redirection Byte. After this, data is again read from the 1024-bits EPROM data field starting at the beginning of the new page. This sequence will continue until the final page and its accompanying CRC are read by the bus master.

The Extended Read Memory command provides a 16-bit CRC at two locations within the transaction flow chart: 1) after the Redirection Byte and 2) at the end of each memory page. The CRC at the end of the memory page is always the result of clearing the CRC generator and shifting in the data bytes beginning at the first addressed memory location of the EPROM data page until the last byte of this page. With the initial pass through the Extended Read Memory flow chart the 16-bit CRC value after the Redirection Byte is the result of shifting the command byte into the cleared CRC generator, followed by the two address bytes and the Redirection Byte. Subsequent passes through the Extended Read Memory flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the Redirection Byte only. After the 16-bit CRC of the last page is read, the bus master will receive logical 1s from the DS2406 until a Reset Pulse is issued. The Extended Read Memory command sequence can be ended at any point by issuing a Reset Pulse.

WRITING EPROM MEMORY

The function flow for writing to the Data Memory and Status Memory is almost identical. After the appropriate write command has been issued, the bus master will send a two-byte starting address (TA1=(T7:T0), TA2=(T15:T8)) and a byte of data (D7:D0). A 16-bit CRC of the command byte, address bytes, and data byte is computed by the DS2406 and read back by the bus master to confirm that the correct command word, starting address, and data byte were received.

If the CRC read by the bus master is incorrect, a Reset Pulse must be issued and the entire sequence must be repeated. If the CRC received by the bus master is correct, a programming pulse (12V on the 1-Wire bus for 480 µs) is issued by the bus master. Prior to programming, the entire unprogrammed EPROM memory field will appear as logical 1s. For each bit in the data byte provided by the bus master that is set to a logical 0, the corresponding bit in the selected byte of the EPROM memory is programmed to a logical 0 after the programming pulse has been applied.

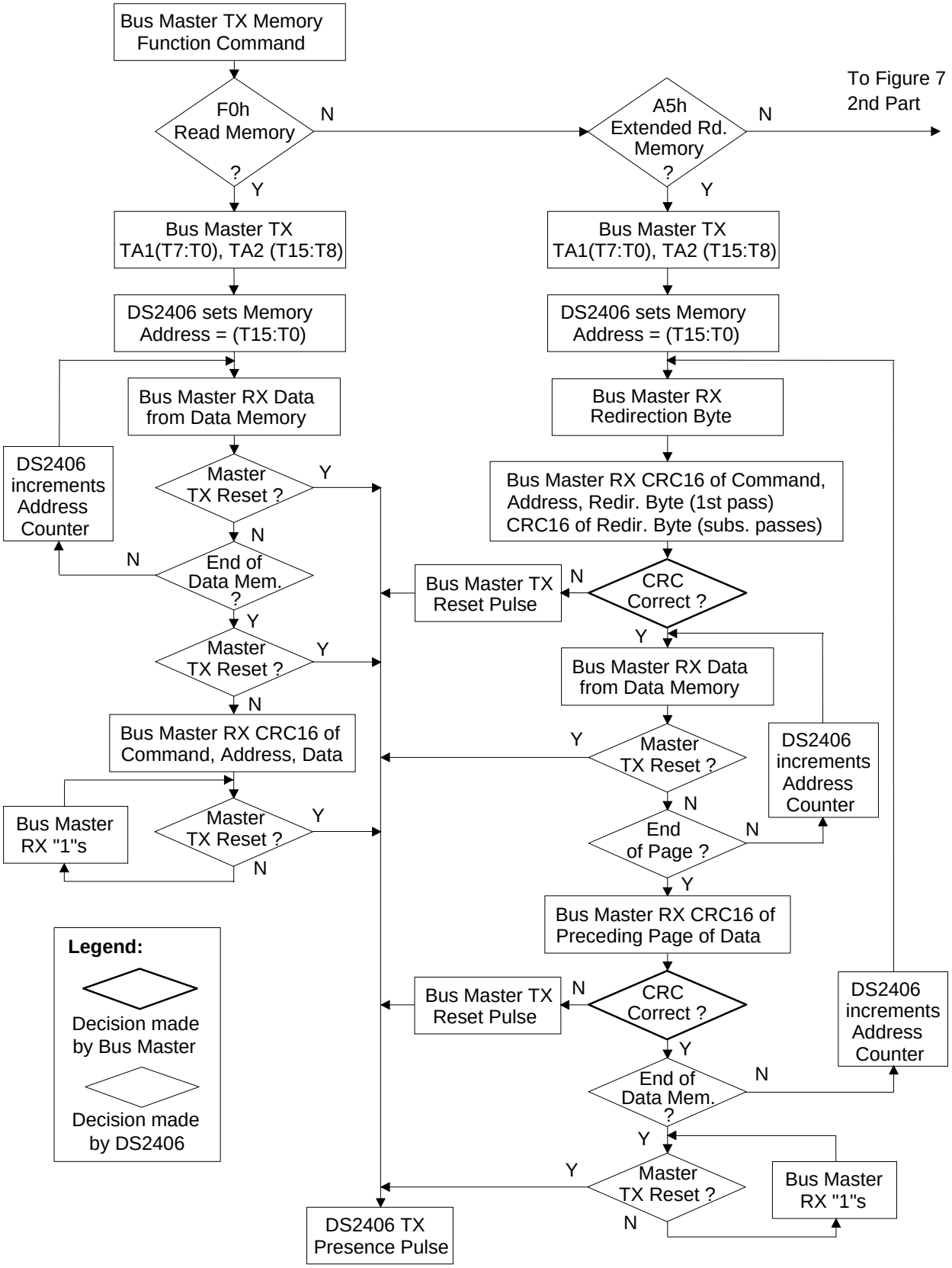
After the 480 µs programming pulse is applied and the data line returns to the idle level (5V), the bus master issues eight read time slots to verify that the appropriate bits have been programmed. The DS2406 responds with the data from the selected EPROM address sent least significant bit first. This byte contains the bit-wise logical AND of all data ever written to this address. If the EPROM byte contains 1s in bit positions where the byte issued by the master contained 0s, a Reset Pulse should be issued and the current byte address should be programmed again. If the DS2406 EPROM byte contains 0s in the same bit positions as the data byte, the programming was successful and the DS2406 will automatically increment its address counter to select the next byte in the EPROM memory field. The new two-byte address will also be loaded into the 16-bit CRC generator as a starting value. The bus master will issue the next byte of data using eight write time slots.

As the DS2406 receives this byte of data into the scratchpad, it also shifts the data into the CRC generator that has been preloaded with the current address and the result is a 16-bit CRC of the new data byte and the new address. After supplying the data byte, the bus master will read this 16-bit CRC from the DS2406 with sixteen read time slots to confirm that the address incremented properly and the data byte was received correctly. If the CRC is incorrect, a Reset Pulse must be issued and the write sequence must be restarted. If the CRC is correct, the bus master will issue a programming pulse and the selected byte in memory will be programmed.

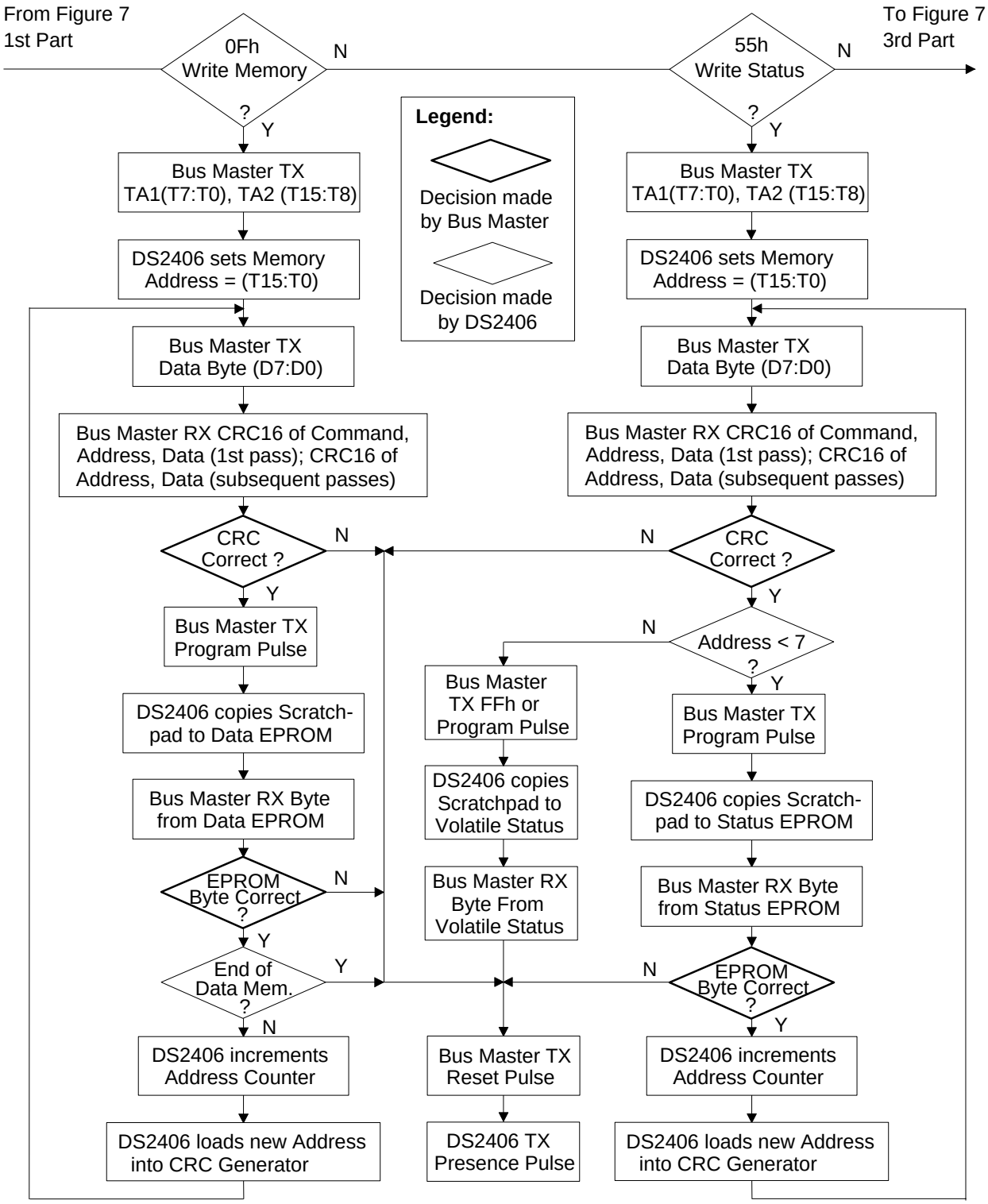
Note that the initial pass through the write flow chart will generate an 16-bit CRC value that is the result of shifting the command byte into the CRC generator, followed by the two address bytes, and finally the data byte. Subsequent passes through the write flow chart due to the DS2406 automatically incrementing its address counter will generate a 16-bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC generator and then shifting in the new data byte.

For both of these cases, the decision to continue (to apply a program pulse to the DS2406) is made entirely by the bus master, since the DS2406 will not be able to determine if the 16-bit CRC calculated by the bus master agrees with the 16-bit CRC calculated by the DS2406. If an incorrect CRC is ignored and the bus master applies a program pulse, incorrect programming could occur within the DS2406. Also note that the DS2406 will always increment its internal address counter after the receipt of the eight read time slots used to confirm the programming of the selected EPROM byte. The decision to continue is again made entirely by the bus master. Therefore if the EPROM data byte does not match the supplied data byte but the master continues with the write command, incorrect programming could occur within the DS2406. The write command sequence can be ended at any point by issuing a Reset Pulse.

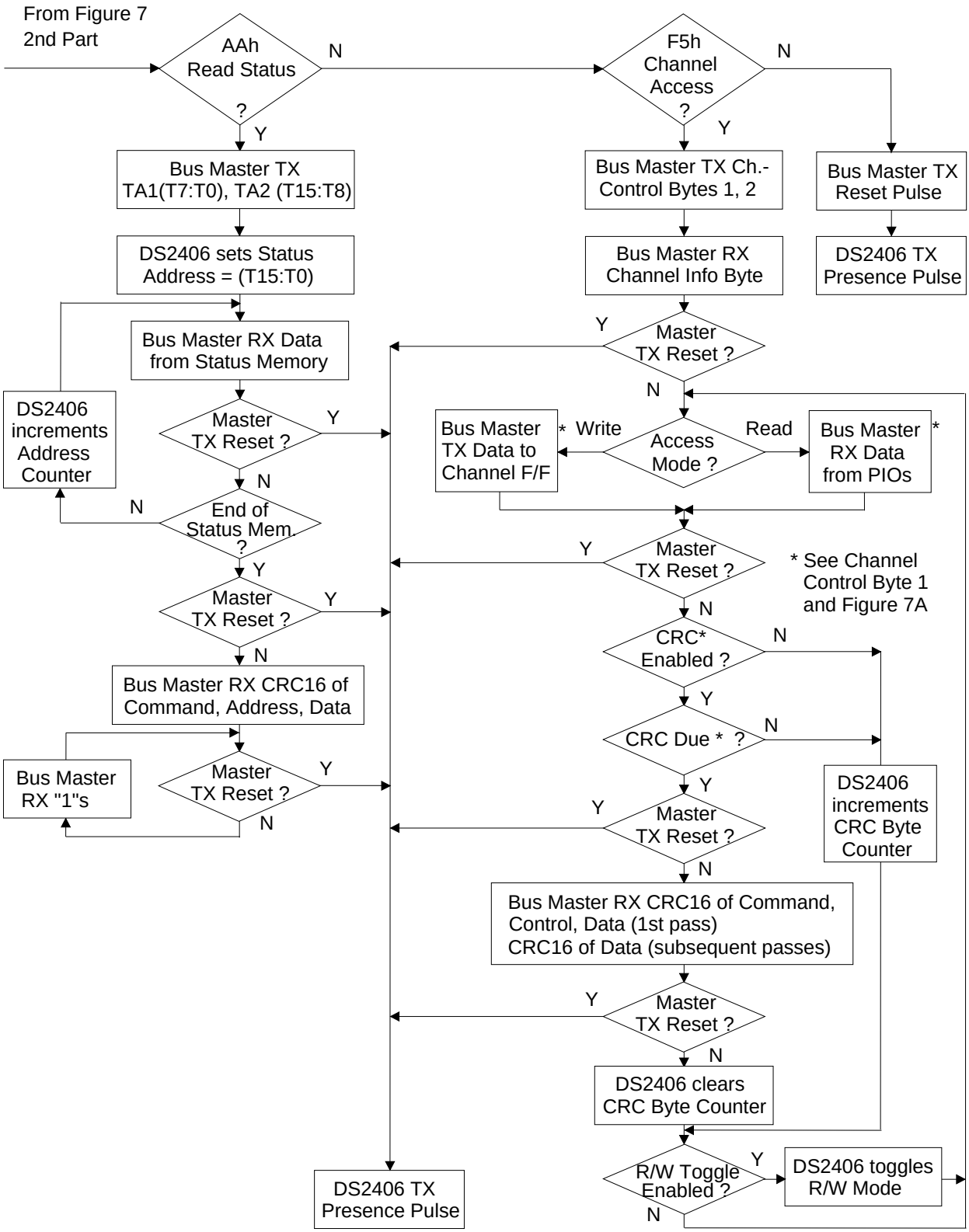
Memory Function Flow Chart Figure 7



Memory Function Flow Chart (continued) Figure 7



Memory Function Flow Chart (continued) Figure 7



Write Memory [0Fh]

The Write Memory command is used to program the 1024-bit EPROM data memory. The details of the functional flow chart are described in the section "Writing EPROM Memory". The data memory address range is 0000h to 007Fh. If the bus master sends a starting address higher than this, the nine most significant address bits are set to zeros by the internal circuitry of the chip. This will result in a mismatch between the CRC calculated by the DS2406 and the CRC calculated by the bus master, indicating an error condition.

Write Status [55h]

The Write Status command is used to program the Status Memory, which includes the specification of the Conditional Search Settings. The details of the functional flow chart are described in the section "Writing EPROM Memory".

The Status Memory address range is 0000h to 0007h. The general programming algorithm is valid for the EPROM section of the Status Memory (addresses 0 to 4) only. The Status memory locations 5 and 6 are already pre-programmed to 00h and therefore cannot be altered. Status memory location 7 consists of static RAM, which can be reprogrammed without limitation and does not require a 12V programming pulse. The supply indication (bit 7) is read-only; attempts to write to it are ignored. The function flow for writing to status memory location 7 is basically the same as for the other EPROM Status Memory Bytes. However, instead of a programming pulse the bus master may send a FFh byte (equivalent to 8 Write-One Time Slots) to transfer the new value from the scratchpad to the status memory.

If the bus master sends a starting address higher than 0007h, the nine most significant address bits are set to zeros by the internal circuitry of the chip. The address bits T3:T6 remain unchanged and will be ignored by the address decoder of the DS2406. Only if one or more of the address bits T8:T15 is set, the bus master will be able to discover an error condition based on the CRC16 that is calculated by the DS2406.

Read Status [AAh]

The Read Status command is used to read data from the Status Memory field. The functional flow chart of this command is identical to the Read Memory command. Since the Status Memory is only 8 bytes, the DS2406 will send the 16-bit CRC after the last byte of status information has been transmitted.

Channel Access [F5h]

The Channel Access command is used to access the PIO channels to sense the logical status of the output node and the output transistor and to change the status of the output transistor. The bus master will follow the command byte with two Channel Control Bytes and will receive back the Channel Info byte. The Channel Control bytes allow the master to select a PIO-channel to communicate with, to specify communication parameters, and to reset the activity latches. Figure 8 shows the details Channel Control Byte 1. The bit assignments of Channel Control Byte 2 are reserved for future development. The bus master should always send FFh for the second Channel Control Byte.

CHANNEL CONTROL BYTE 1 Figure 8

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ALR	IM	TOG	IC	CHS1	CHS0	CRC1	CRC0

Most easily understood are the bits CHS0 and CHS1, which select the channels to communicate with. One can select one of the two channels or both channels together. The selection codes are shown in the table below.

CHS1	CHS0	Description
0	0	(not allowed)
0	1	channel A only
1	0	channel B only
1	1	both channels interleaved

When reading only a single channel, the logic level at the selected PIO is sampled at the beginning of each read time slot (Figure 10a) and is immediately signaled through the 1-Wire line. Because the PIO logic levels are sensed at the beginning of the time slot, the bus master does not see transitions at the PIO that occur during the time slot. When writing to a single channel, the selected PIO will show the new status after (but not necessarily immediately after) the 1-Wire line has returned to its idle level of typically 5V (see Figure 10a). If the bus master transmits a 1 (Write One Time Slot), the output transistor of the selected channel will change its status after time td1, which is 15µs to 60µs after the beginning of the time slot. If the bus master transmits a 0 (Write Zero Time Slot), the output transistor will change its status with a delay of td0 after the 1-Wire line has returned to its idle level. The value of td0 may vary between 200 and 300 ns (see Figure 10a). Depending on the load conditions, there may be additional delay until the voltage at the PIO reaches a new logical level.

When communicating with both channels, the Interleave Control Bit IC controls when data is sampled and when data arrives at the PIO pins. There is an asynchronous mode (IC = 0) and a synchronous mode (IC = 1). For the asynchronous mode, both channels are accessed in an alternating way. For the synchronous mode, both channels are accessed simultaneously. For single-channel operation the Interleave Control Bit must be set to 0.

When reading in the asynchronous mode each channel is sampled alternately at the start of each Read Time Slot, beginning with channel A. The logic level detected at the PIO is immediately transmitted to the master during the same time slot. When reading in the synchronous mode, both channels will be sampled at the same time. The data bit from channel A will be sent to the master immediately during the same time slot while the data bit from channel B follows with the next time slot which does not sample the PIOs. Both channels will be sampled again with the time slot that follows the transmission of the data bit from PIO-B (Figure 10b).

When writing in the asynchronous mode, each channel will change its status independently of the other. The change of status occurs with the same timing relations as for communication with one channel. However, every second write time slot addresses the same channel. The first time slot is directed to channel A, the second to channel B, the next to channel A and so on. As a consequence, in asynchronous mode both PIOs can never change their status at the same time. When writing in the synchronous mode, both channels operate together. After the new values for both channels have arrived at the DS2406 the change of status at both channels occurs with the same timing relations as for communication with one channel. As with the asynchronous mode, every second write time slot contains data for the same channel. The first time slot addresses channel A, the second channel B and so on. Depending on the data values, in the synchronous mode both PIOs can change their status at the same time (Figure 10c). In any of these cases, the information of channel A and channel B will appear alternating on the 1-Wire line, always starting with channel A. By varying the idle-time between time slots on the 1-Wire line one has full control over the time points of sampling and the waveforms generated at the PIO-pins when writing to the device.

The TOG bit of Channel Control Byte 1 specifies if one is always reading or writing (TOG = 0) or if one is going to change from reading to writing or vice versa after every data byte that has been sent to or received from the DS2406 (TOG = 1). When accessing one channel, one byte is equivalent to eight reads from or writes to the selected PIO pin. When accessing two channels, one byte is equivalent to four reads or writes from/to each channel.

The initial mode (reading or writing) for accessing the PIO channels is specified in the IM bit. For reading, IM has to be set to 1, for writing IM needs to be 0. If the TOG bit is set to 0, the device will always read or write as specified by the IM bit. If TOG is 1, the device will use the setting of IM for the first byte to be transmitted and will alternate between reading and writing after every byte. Table 1 illustrates the effect of TOG and IM for one-channel as well as for two-channel operation.

THE EFFECT OF TOGGLE MODE AND INITIAL MODE Table 1

TOG	IM	CHANNELS	EFFECT
0	0	one channel	**Write** all bits to the selected channel
0	1	one channel	**Read** all bits from the selected channel
1	0	one channel	**Write** 8 bits, **read** 8 bits, write, read, etc. to/from the selected channel
1	1	one channel	**Read** 8 bits, **write** 8 bits, read, write, etc. from/to the selected channel
0	0	two channels	Repeat: four times (**write** A, **write** B)
0	1	two channels	Repeat: four times (**read** A, **read** B)
1	0	two channels	Four times: (**write** A, **write** B), four times: (**read** A, **read** B), write, read, etc.
1	1	two channels	Four times: (**read** A, **read** B), four times: (**write** A, **write** B), read, write, etc.

The ALR bit of Channel Control Byte 1 controls whether the activity latch of each channel gets reset. Both activity latches are cleared simultaneously if the ALR bit is 1. They are not changed if the ALR bit is 0. An activity latch is set with a negative or positive edge that occurs at its associated PIO channel.

Channel Control Byte 1 also controls the internal CRC generator to safeguard data transmission between the bus master and the DS2406 for channel access. It does not affect reading from or writing to the memory sections of the DS2406. The CRC control bits (bit 0 and bit 1) can be set to create and protect data packets that have the size of 8 bytes or 32 bytes. If desired, the device can safeguard even single bytes by a 16-bit CRC. This setting, however, limits the average PIO sampling rate to about one third of its maximum possible value. The codes for the CRC control are shown in the table below.

CRC1	CRC0	Description
0	0	CRC disabled (no CRC at all)
0	1	CRC after every byte
1	0	CRC after 8 bytes
1	1	CRC after 32 bytes

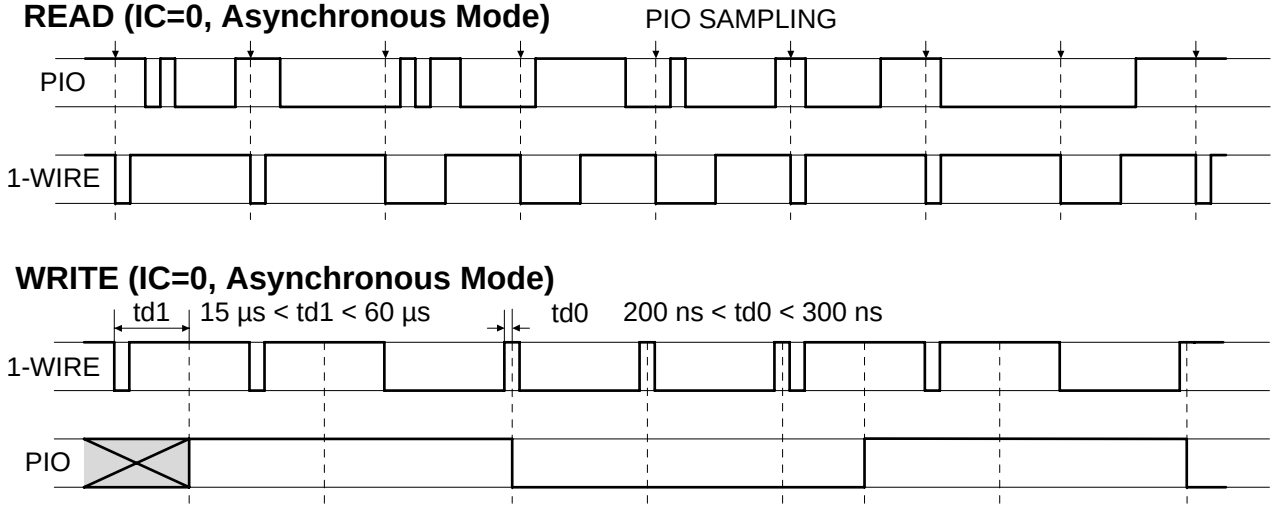
The CRC provides a high level of safeguarding data. A detailed description of CRCs is found in *Application Note 27*. If the CRC is disabled, the CRC-related sections in the flow chart are skipped.

After the Channel Control bytes have been transmitted the bus master receives the Channel Info byte (Figure 9). This byte indicates the status of the channel flip-flops, the PIO pins, the activity latches as well as the availability of channel B and external power supply. To be able to read from a PIO channel, the output transistor needs to be non-conducting, which is equivalent to a 1 for the channel flip-flop. Reading 0 for both the channel flip-flop and the sensed level indicates that the output transistor of the PIO is pulling the node low. For the Channel Info byte PIO A and B are sampled at the same time, as in the synchronous mode. If channel B is available, bit 6 of the Channel Info Byte reads 1. For 1-channel versions of the DS2406, the PIO B sensed level, channel flip-flop value, and activity latch value should be ignored. Without an external supply, the supply indication bit (bit 7) reads 0. As long as the voltage applied to the V_{CC} pin is high enough to operate the device this bit will read 1.

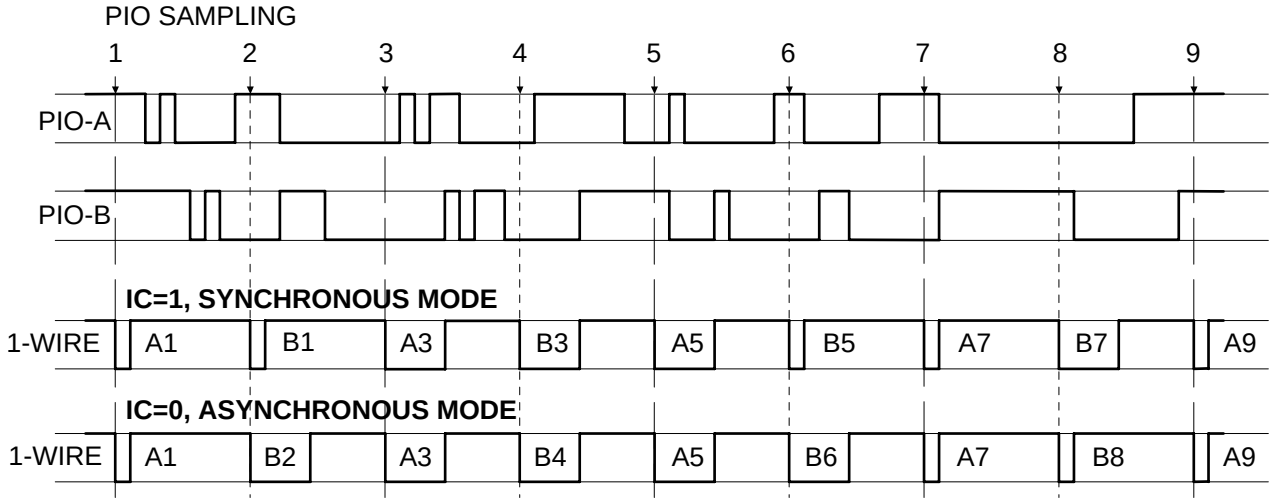
CHANNEL INFO BYTE Figure 9

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Supply Indication 0 = no supply	Number of Channels 0 = channel A only	PIO-B Activity Latch	PIO-A Activity Latch	PIO B Sensed Level	PIO A Sensed Level	PIO-B Channel Flip-Flop Q	PIO-A Channel Flip-Flop Q

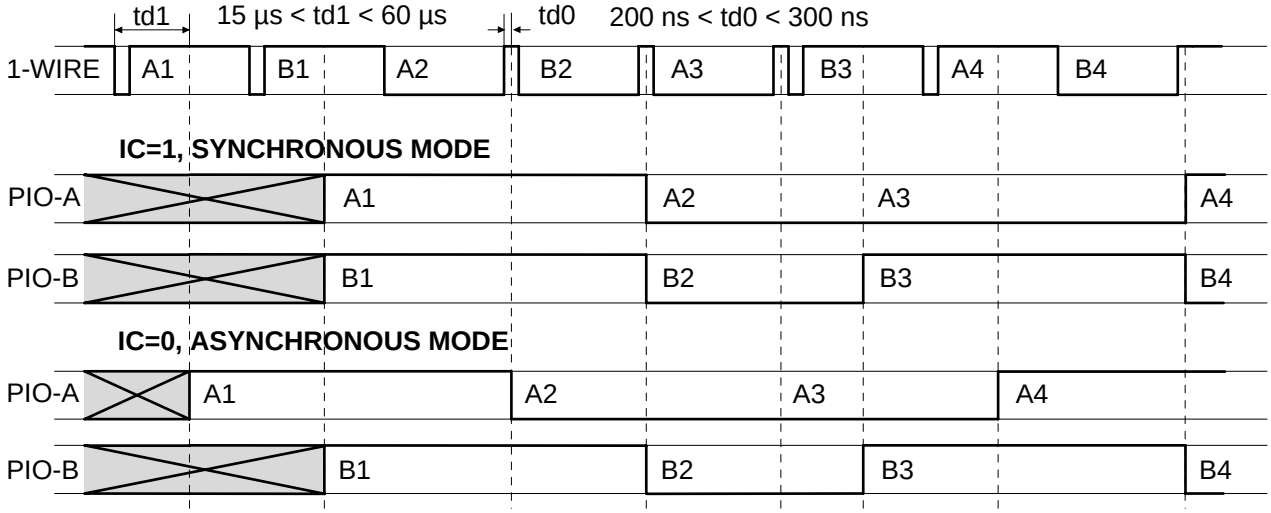
ONE-CHANNEL READ/WRITE Figure 10a



TWO-CHANNEL READ Figure 10b



TWO-CHANNEL WRITE Figure 10c



1-WIRE BUS SYSTEM

The 1-Wire bus is a system, which has a single bus master and one or more slaves. In all instances, the DS2406 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). A 1-Wire protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master.

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have an open drain or 3-state outputs. The 1-Wire port of the DS2406 is open drain with an internal circuit equivalent to that shown in Figure 11. Typical bus master ports are shown in Figure 12. If a bi-directional pin is not available, separate output and input pins can be tied together. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 15.4kbits/s. For normal communication excluding EPROM programming the 1-Wire bus requires only a pull-up resistor of approximately 5kΩ for short line lengths.

The idle state for the 1-Wire bus is high. If, for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120µs, one or more of the devices on the bus may be reset. If the 1-Wire bus remains low for more than 5ms any DS2406 that is not V_{CC} powered may perform a power-on reset and switch off both PIOs.

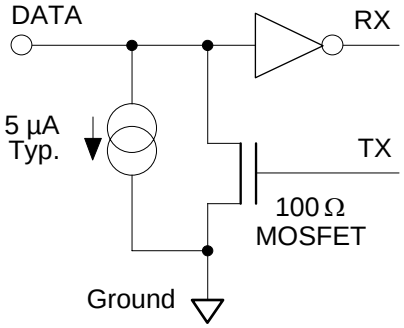
TRANSACTION SEQUENCE

The sequence for accessing the DS2406 via the 1-Wire port is as follows:

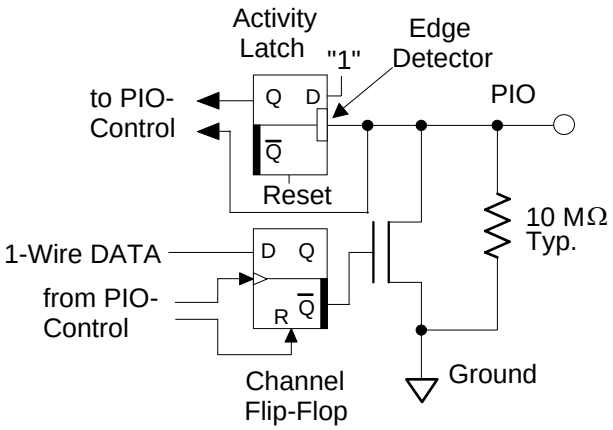
- Initialization
- ROM Function Command
- Memory or Channel Access Function Command
- Transaction/Data

DS2406 EQUIVALENT CIRCUIT Figure 11

1-Wire Interface

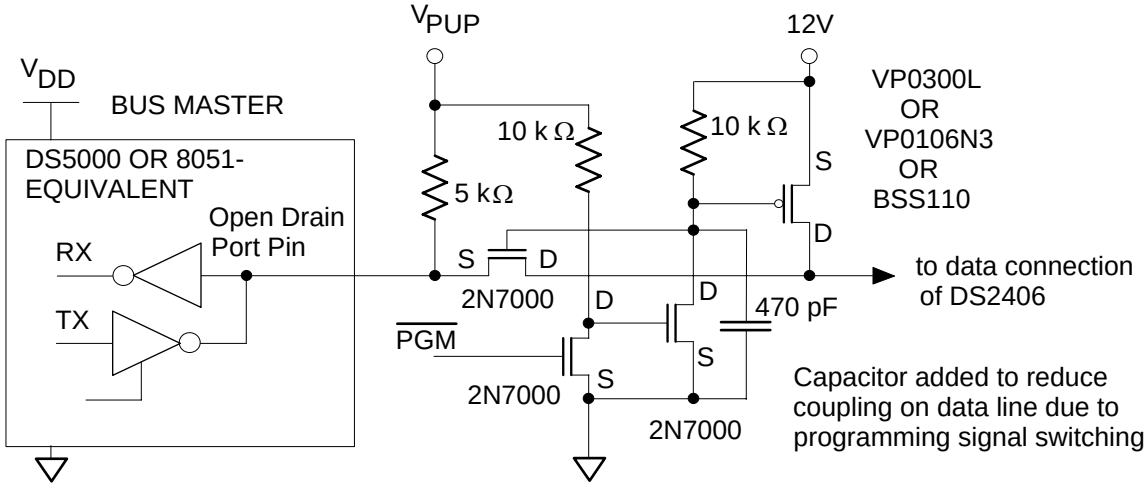


PIO Channel



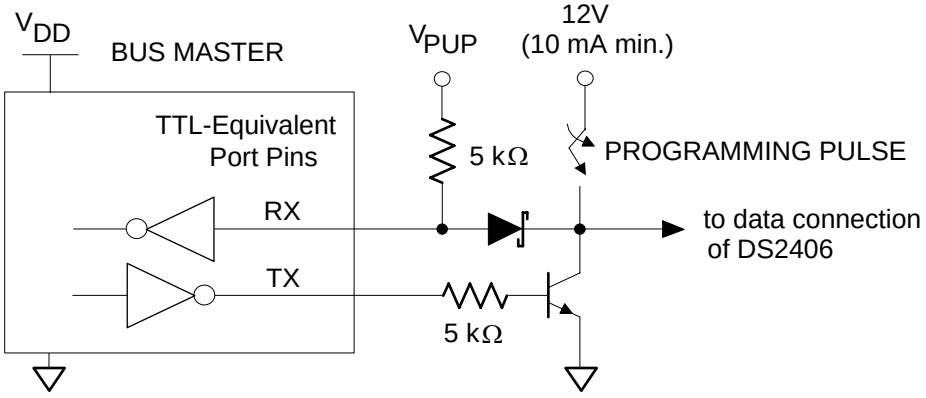
BUS MASTER CIRCUIT Figure 12

A) Open Drain



The interface is reduced to the 5kΩ pull-up resistor if one does not intend to program the EPROM cells.

B) Standard TTL



The diode and programming circuit are not required if one does not intend to program the EPROM cells.

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS2406 is on the bus and is ready to operate. For more details, see the "1-Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the five ROM function commands that the DS2406 supports. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 13).

Read ROM [33h]

This command allows the bus master to read the DS2406's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command should only be used only if there is a single slave on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The resultant family code and 48-bit serial number will be invalid.

Match ROM [55h]

The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS2406 on a multidrop bus. Only the DS2406 that exactly matches the 64-bit ROM sequence will respond to the subsequent memory function command. All slaves that do not match the 64-bit ROM sequence will wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

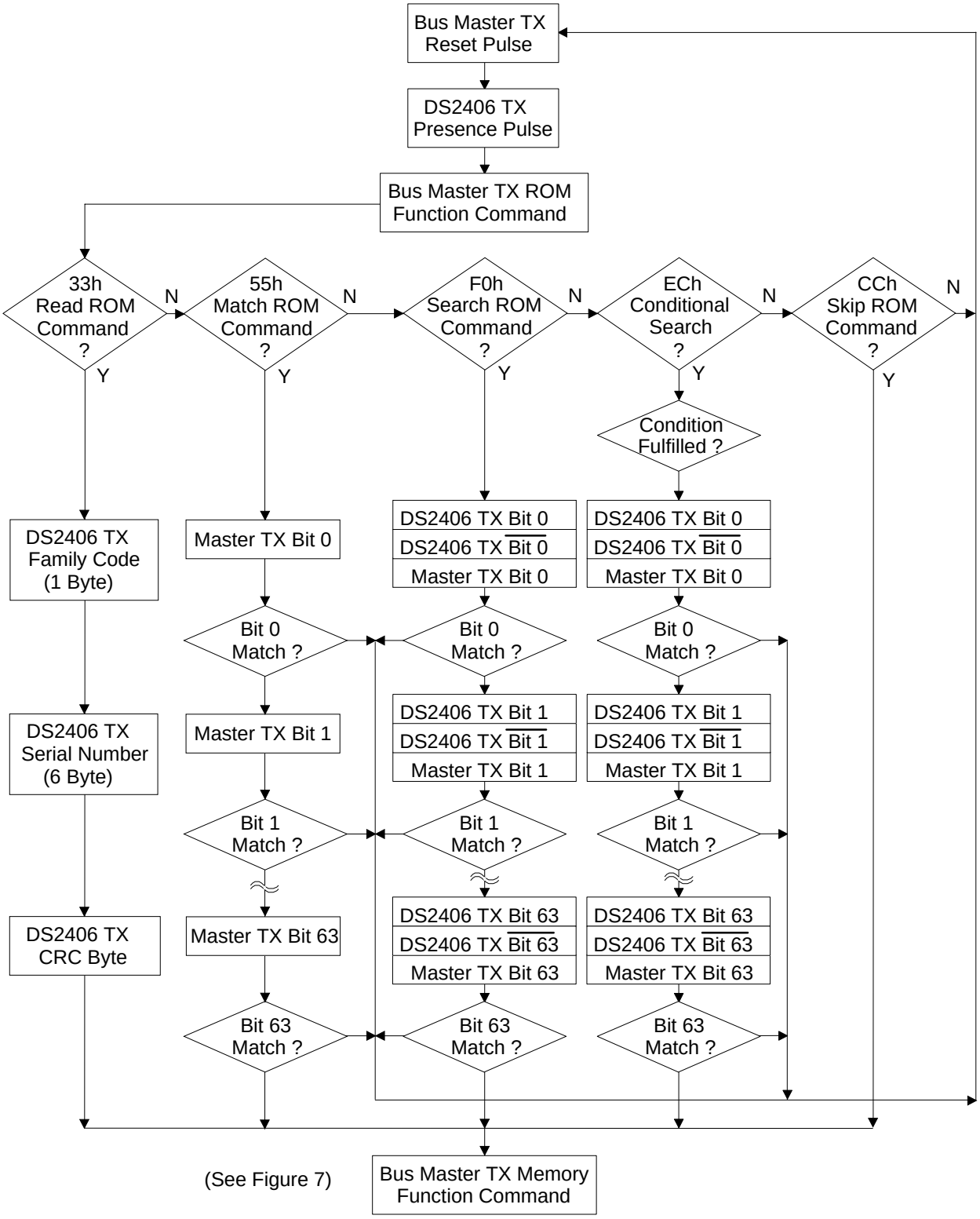
Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The Search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the 64-bit ROM code of one device. Additional passes will identify the ROM codes of the remaining devices. See *Application Note 187* for a comprehensive discussion of a search ROM, including an actual example.

Skip ROM [CCh]

This command can save time in a single drop bus system by allowing the bus master to access the memory and channel access functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open drain pull-downs will produce a wired-AND result).

ROM FUNCTIONS FLOW CHART Figure 13



Conditional Search ROM [ECh]

The Conditional Search ROM command operates similarly to the Search ROM command except that only devices fulfilling the specified condition will participate in the search. This command provides an efficient means for the bus master to identify devices in a multidrop system that have to signal a status change, e.g. the opening of a window in a building control application.

The condition is specified by the bit functions CSS0 to CSS4 in Status Memory location 7. At power-on all these bits are 1s. They can be changed by means of the Write Status command. As long as the device remains powered up, the modified search conditions are available for use at any time. For the conditional search, one can specify the polarity (HIGH or LOW; CSS0), the source (PIO-pin, channel flip flop or activity latch; CSS1, CSS2), and the channel of interest (A, B or the logical OR of A, B; CSS3, CSS4). Table 2 shows all qualifying conditions and the required settings for CSS0 to CSS4.

QUALIFYING CONDITIONS FOR CONDITIONAL SEARCH Table 2

DESCRIPTION		CONDITIONAL SEARCH SELECT CODE				
		CHANNEL SELECT		SOURCE SELECT		POLARITY
CONDITION	CHANNEL	CSS4	CSS3	CSS2	CSS1	CSS0
RESERVED		Don't care		0	0	0/1
Unconditional	neither one	0	0	At least one of these bits needs to be 1		0
Activity Latch = 0	A	0	1	0	1	0
Activity Latch = 1	A	0	1	0	1	1
Channel FF = 0 (transistor on)	A	0	1	1	0	0
Channel FF = 1 (transistor off)	A	0	1	1	0	1
PIO Low	A	0	1	1	1	0
PIO High	A	0	1	1	1	1
Activity Latch = 0	B	1	0	0	1	0
Activity Latch = 1	B	1	0	0	1	1
Channel FF = 0 (transistor on)	B	1	0	1	0	0
Channel FF = 1 (transistor off)	B	1	0	1	0	1
PIO Low	B	1	0	1	1	0
PIO High	B	1	0	1	1	1
Activity Latch = 0	A or B	1	1	0	1	0
Activity Latch = 1	A or B	1	1	0	1	1
Channel FF = 0 (transistor on)	A or B	1	1	1	0	0
Channel FF = 1 (transistor off)	A or B	1	1	1	0	1
PIO Low	A or B	1	1	1	1	0
PIO High	A or B	1	1	1	1	1

The activity latch (Figure 11) captures an event for interrogation by the bus master at a later time. This way, the bus master needs not interrogate devices continuously. The activity latch is set to 1 with the first negative or positive edge detected on the associated PIO channel. It can be cleared with the Channel Access command if the ALR bit of the Channel Control Byte 1 is set. The activity latch is automatically cleared when the DS2406 powers up. In order to use the activity latch the output transistor of the selected channel should be non-conducting. Otherwise signals applied to the PIO pin will be shorted to ground by the low impedance of the output transistor.

The Channel Select bits CSS3 and CSS4 specify the channel of interest. The sampling of the source within the selected channel will take place on completion of the Conditional Search command byte. The Channel selection codes are as follows:

CSS4	CSS3	Channel Selection
0	0	neither channel selected
0	1	channel A only
1	0	channel B only
1	1	channel A OR channel B

If both CSS3 and CSS4 are 1, the logical values of the selected signal source of both channels are ORed and the result is compared to specified polarity. If, for example, the specified polarity is 0, the signal source of both channels must be 0 for the device to respond to the Conditional Search. If both CSS3 and CSS4 are 0, neither channel is selected. Under this condition the device **will always respond** to the Conditional Search if the polarity bit CSS0 is 0, disregarding the source selection. If neither channel is selected and CSS0 = 1, the device will only respond to the regular Search ROM command.

The source selection for the Conditional Search is done through the Source Select bits CSS1 and CSS2. The codes for these bits are as follows:

CSS2	CSS1	Source Selection
0	0	RESERVED
0	1	Activity Latch
1	0	channel flip flop
1	1	PIO Status

The setting CSS1 = 0, CSS2 = 0 is reserved for future use. If programmed with this setting the device will respond to Conditional Search command as follows: if CSS0 = 0 the device will always respond to a Conditional Search, if CSS0 = 1 the device will never respond to a conditional search.

The Conditional Search Polarity is specified by CSS0. If CSS0 is 0, the DS2406 will respond to a Conditional Search command if the status of the selected source for the specified channel is logic 0. If CSS0 is set to 1, the source level needs to be logic 1.

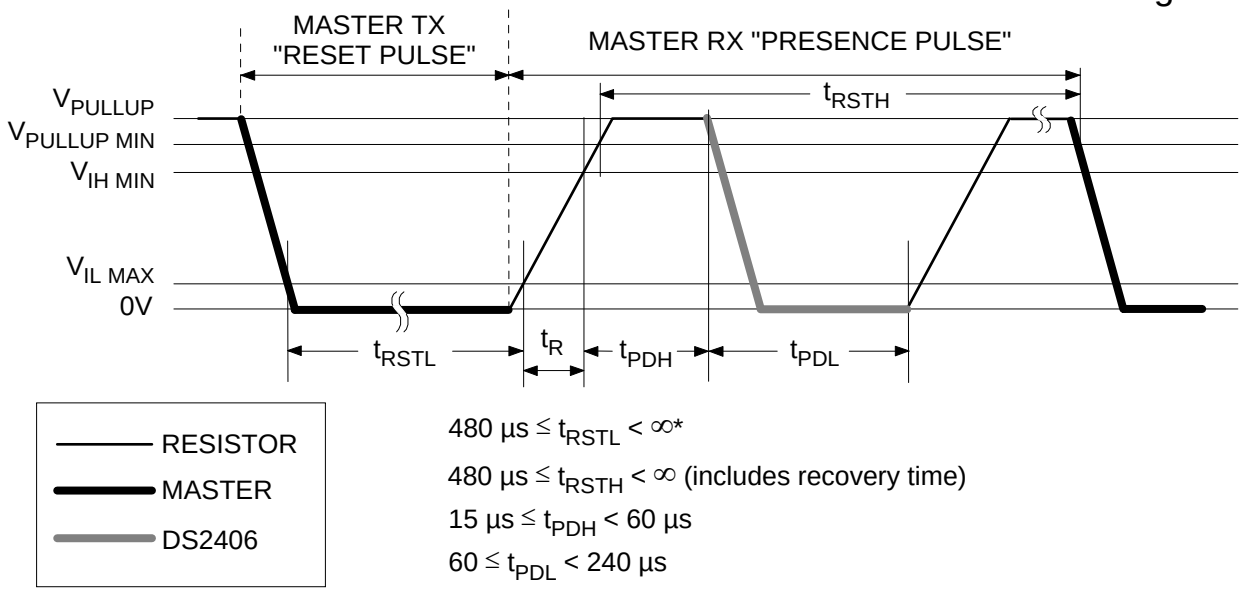
For 1-channel versions of the DS2406 the channel B input will always be logic 0. For this reason CSS4 should not be set to 1 to avoid unwanted influence from channel B. The bus master can determine the availability of channel B from bit 6 of the Channel Info byte.

1-WIRE SIGNALING

The DS2406 requires strict protocols to ensure data integrity. The protocol consists of five types of signaling on one line: Reset Sequence with Reset Pulse and Presence Pulse, Write 0, Write 1, Read Data, and Program Pulse. Except for the presence pulse the bus master initiates all these signals.

The initialization sequence required to begin any communication with the DS2406 is shown in Figure 14. A reset pulse followed by a presence pulse indicates the DS2406 is ready to send or receive data. The bus master transmits (TX) a reset pulse (t_{RSTL}, minimum 480µs). The bus master then releases the line and goes into receive mode (RX). The 1-Wire bus is pulled to a high state via the pull-up resistor. After detecting the rising edge on the data pin, the DS2406 waits (t_{PDH}, 15-60µs) and then transmits the presence pulse (t_{PDL}, 60-240µs).

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 14



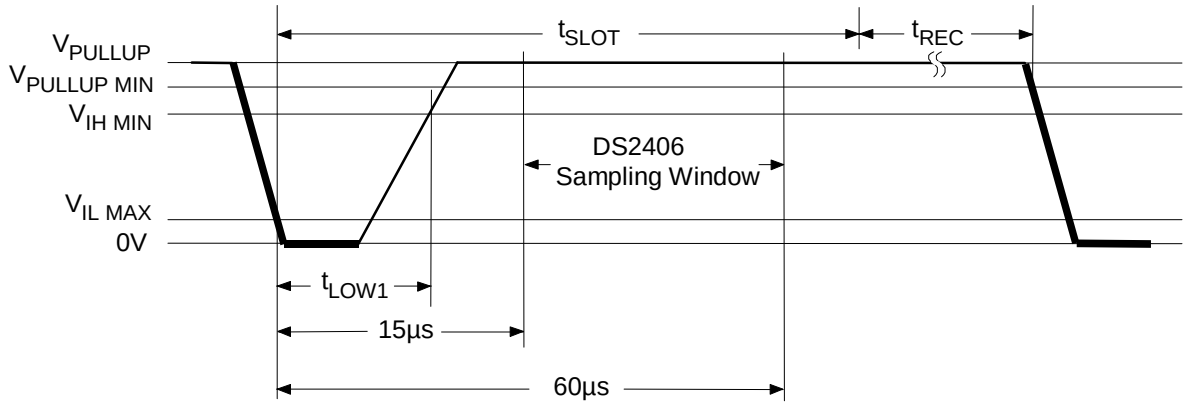
* In order not to mask interrupt signaling by other devices on the 1-Wire bus, t_{RSTL} + t_R should always be less than 960µs. In a parasitically powered environment t_{RSTL} should be limited to maximum 5ms. Otherwise the DS2406 may perform a power-on reset.

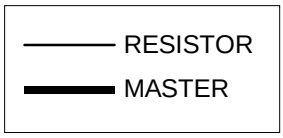
READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 15. The master initiates all time slots by driving the data line low. The falling edge of the data line synchronizes the DS2406 to the master by triggering an internal delay circuit. During write time slots, the delay circuit determines when the DS2406 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS2406 will hold the data line low. If the data bit is a "1", the DS2406 will not hold the data line low at all.

READ/WRITE TIMING DIAGRAM Figure 15

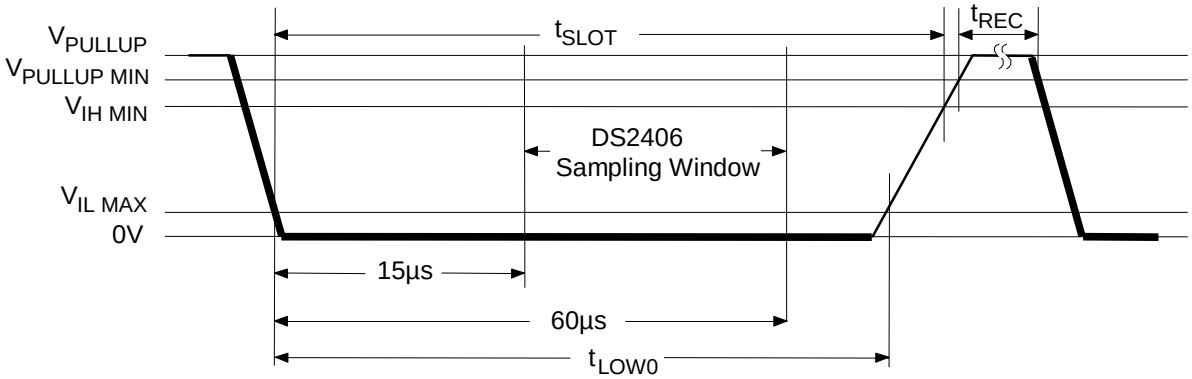
Write-one Time Slot





60 µs ≤ t_{SLOT} < 120 µs
1 µs ≤ t_{LOW1} < 15 µs
5 µs ≤ t_{REC} < ∞

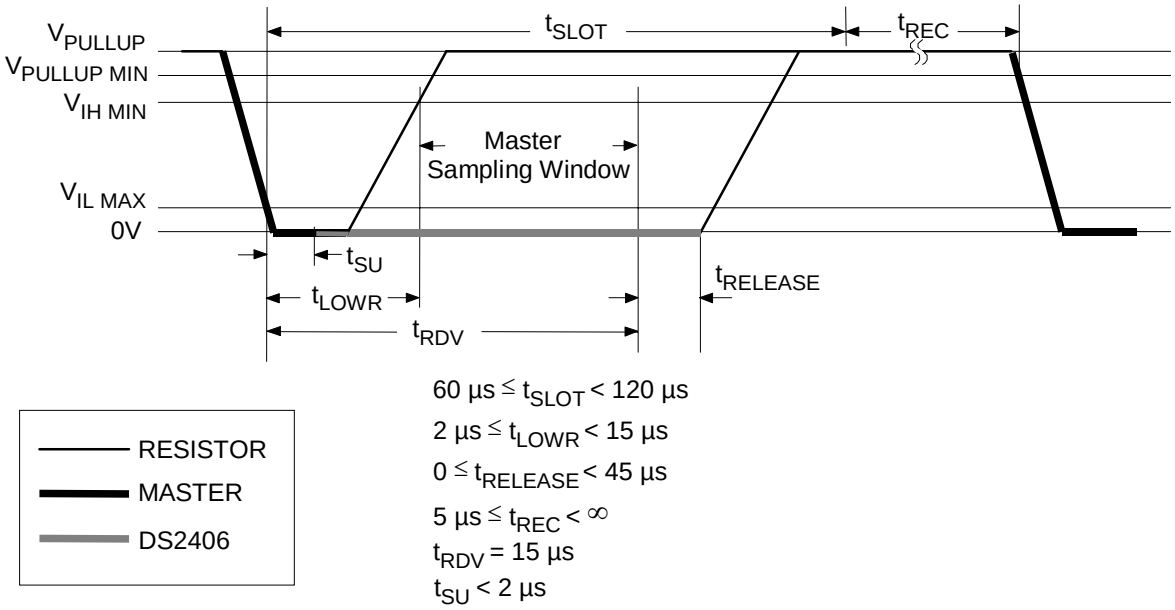
Write-zero Time Slot



60 µs ≤ t_{LOW0} < t_{SLOT} < 120 µs
5 µs ≤ t_{REC} < ∞

READ/WRITE TIMING DIAGRAM (continued) Figure 15

Read-data Time Slot

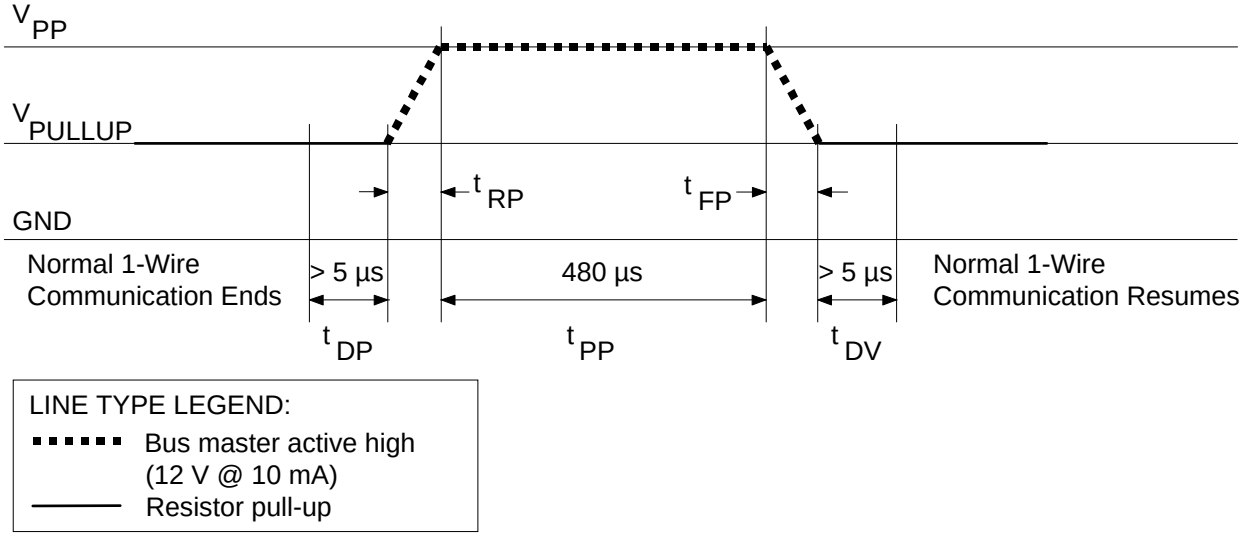


* The optimal sampling point for the master is as close as possible to the end time of the 15µs t_{RDV} period without exceeding t_{RDV}. For the case of a Read-one time slot, this maximizes the amount of time for the pull-up resistor to recover the line to a high level. For a Read-zero time slot it ensures that a read will occur before the fastest 1-Wire devices(s) release the line ($t_{RELEASE}$ = 0).

PROGRAM PULSE

To copy data from the 8-bit scratchpad to the EPROM data or status memory, a program pulse is applied to the data line after the bus master has confirmed that the CRC for the current byte is correct. During programming, the bus master controls the transition from a state where the data line is idling high via the pull-up resistor to a state where the data line is actively driven to a programming voltage of 12V providing a minimum of 10mA of current to the DS2406. This programming voltage (Figure 16) should be applied for 480µs, after which the bus master should return the data line to the idle high state. Note that due to the high voltage programming requirements for any 1-Wire EPROM device, it is not possible to multi-drop non-EPROM based 1-Wire devices with the DS2406 during programming. An internal diode within the non-EPROM based 1-Wire devices will attempt to clamp the data line at approximately 8V and could potentially damage these devices.

PROGRAM PULSE TIMING DIAGRAM Figure 16



CRC GENERATION

With the DS2406 there are two different types of CRCs (Cyclic Redundancy Checks). One CRC is an 8-bit type. It is computed at the factory and lasered into the most significant byte of the 64-bit ROM. The equivalent polynomial function of this CRC is $X^8 + X^5 + X^4 + 1$. To determine whether the ROM data has been read without error the bus master can compute the CRC value from the first 56 bits of the 64-bit ROM and compare it to the value read from the DS2406. This 8-bit CRC is received in the true form (non-inverted) when reading the ROM.

The other CRC is a 16-bit type, generated according to the standardized CRC16-polynomial function $X^{16} + X^{15} + X^2 + 1$. This CRC is used for error detection when reading Data Memory, Status Memory, or when communicating with PIO channels. In contrast to the 8-bit CRC, the 16-bit CRC is always returned in the complemented (inverted) form. A CRC-generator inside the DS2406 chip (Figure 17) will calculate a new 16-bit CRC as shown in the command flow chart of Figure 7. The bus master may compare the CRC value read from the device to the one it calculates from the data and decides whether to continue with an operation or to re-do the function that returned the CRC error.

When reading the data memory of the DS2406 with the Read Memory command, the 16-bit CRC is only transmitted at the end of the memory. This CRC is generated by clearing the CRC generator, shifting in the command, low address, high address, and every data byte starting at the first addressed memory location and continuing until the end of the physical data memory is reached.

When reading the Status Memory, the 16-bit CRC is transmitted at the end of the 8-byte Status Memory page. The 16-bit CRC will be generated by clearing the CRC generator, shifting in the command byte, low address, high address, and the data bytes beginning at the first addressed memory location and continuing until the last byte of the Status Memory is reached.

When reading the data memory of the DS2406 with the Extended Read Memory command, there are two situations where a 16-bit CRC is generated. One 16-bit CRC follows each Redirection Byte; another 16-bit CRC is transmitted after the last byte of a memory data page is read. The CRC at the end of the memory page is always the result of clearing the CRC generator and shifting in the data bytes beginning at the first addressed memory location of the EPROM data page until the last byte of this page. With the initial pass through the Extended Read Memory flow chart the 16-bit CRC value is the result of shifting

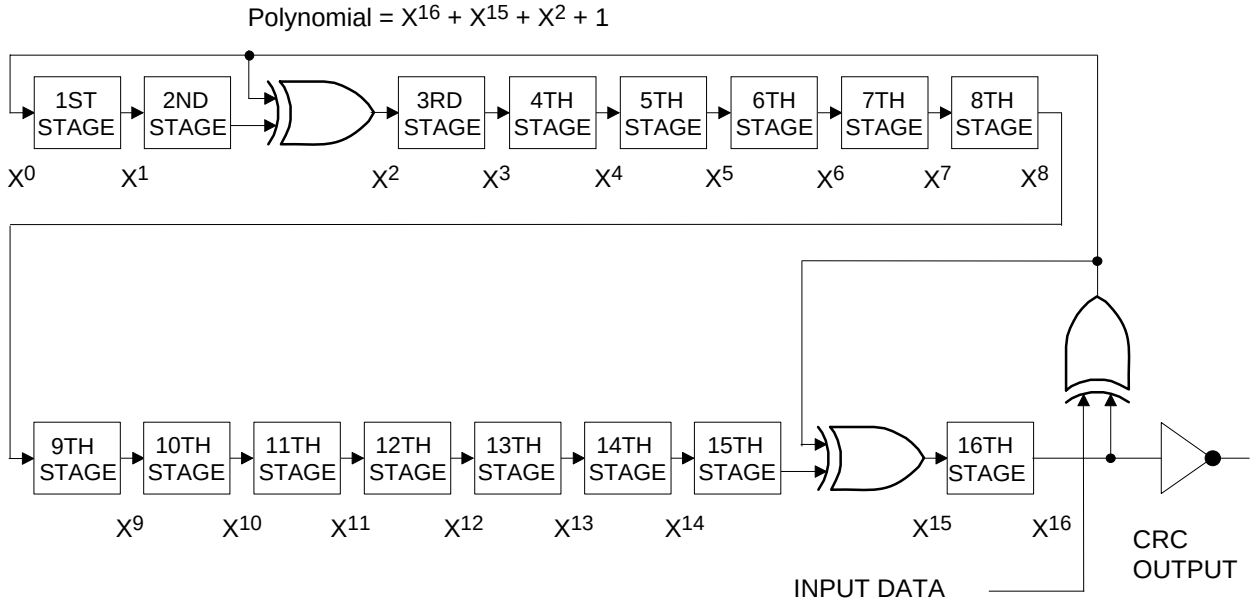
the command byte into the cleared CRC generator, followed by the two address bytes and the Redirection Byte. Subsequent passes through the Extended Read Memory flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in only the Redirection Byte.

When writing to the DS2406 (either data memory or status memory), the bus master receives a 16-bit CRC to verify that the data transfer was correct before applying the programming pulse. With the initial pass through the Write Memory/Status flow chart the 16-bit CRC will be generated by clearing the CRC-generator, shifting in the command, low address, high address and the data byte. Subsequent passes through the Write Memory/Status flow chart due to the DS2406 automatically incrementing its address counter will generate a 16-bit CRC that is the result of loading (not shifting) the new (incremented) address into the CRC generator and then shifting in the new data byte.

When communicating with a PIO channel using the Channel Access command, one can select whether and how often a 16-bit CRC will be added to the data stream. This CRC selection is specified in the Channel Control byte 1 and may be changed with every execution of the Channel Access command. Depending on the CRC selection, the device can generate a CRC after every byte that follows the Channel Info byte, after each block of eight bytes or after each block of 32 bytes. If the CRC is enabled, with the initial pass through the Channel Access flow chart the 16-bit CRC will be generated by clearing the CRC-generator, shifting in the command, Channel Control Bytes 1 and 2, Channel Info Byte and the specified amount of data bytes (1, 8, or 32). Subsequent passes through the Channel Access flow chart will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the new data byte(s). This algorithm is valid for all accesses to the PIO channels, continuous reading or writing as well as toggling between read and write.

The comparison of CRC values and decision to continue with an operation are determined entirely by the bus master. There is no circuitry on the DS2406 that prevents a command sequence from proceeding if a CRC error occurs. For more details on generating CRC values including example implementations in both hardware and software, see *Application Note 27*.

CRC-16 HARDWARE DESCRIPTION AND POLYNOMIAL Figure 17



ABSOLUTE MAXIMUM RATINGS*

Voltage on DATA or PIO-A to Ground	-0.5V to +13.0V
Voltage on V_{CC} or PIO-B to Ground	-0.5V to +6.5V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specifications

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS
DATA PIN (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
1-Wire Pullup Voltage	V_{PUP}	2.8		6.0	V	1, 2
1-Wire Input High	V_{IH}	2.2			V	1, 3
1-Wire Input Low	V_{IL}	-0.3		0.5	V	1
1-Wire Output Low @ 4mA	V_{OL}			0.4	V	1
Input Load Current	I_L		5		µA	4
Programming Voltage @ 10mA	V_{PP}	11.5		12.0	V	

DC ELECTRICAL CHARACTERISTICS
PIO PIN (V_{PUP} = 2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 (PIOA)	V_{IHA}	2.2		12	V	1, 3
Logic 0 (PIOA)	V_{ILA}	-0.3		0.3	V	1
Input Leakage Current, pin at 12V	I_{LA}	0.9		1.9	µA	5, 6
Output Sink Current @ 0.4V (PIOA)	I_{SA}	See graph on page 30			mA	6, 7, 8
PIOA Pullup Voltage	V_{PUPA}			12	V	1, 2, 6
Logic 1 (PIOB)	V_{IHB}	2.2		6.0	V	1, 3
Logic 0 (PIOB)	V_{ILB}	-0.3		0.4	V	1
Input Leakage Current, pin at 6V	I_{LB}	0.45		0.9	µA	5, 6
Output Sink Current @ 0.4V (PIOB)	I_{SB}	See graph on page 30			mA	6
PIOB Pullup Voltage	V_{PUPB}			6	V	1, 2, 6

DC ELECTRICAL CHARACTERISTICS V_{CC} (V_{PUP}=2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IHC}	2.8		6.0	V	1, 9
Logic 0	V_{ILC}	-0.3		0.8	V	1
Input Current	I_{CC}			6.0	µA	4

CAPACITANCES

(t_A = 25°C)

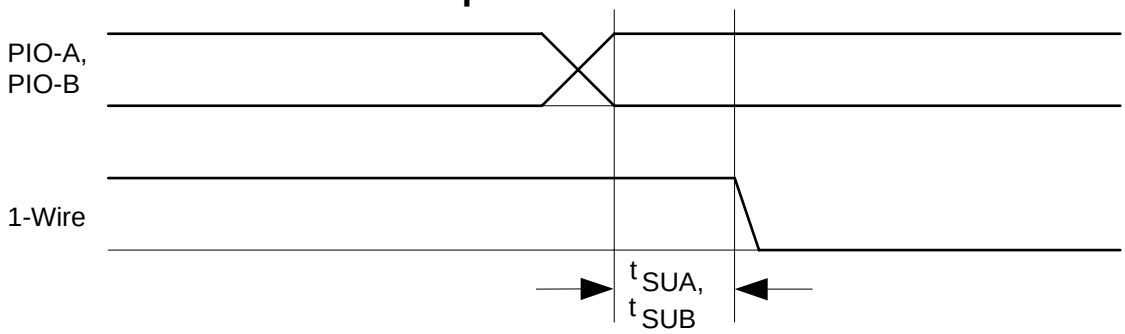
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance DATA Pin	C_D			800	pF	10
Capacitance PIO-A Pin	C_A		100		pF	
Capacitance PIO-B Pin	C_B		25		pF	
Capacitance V_{CC} Pin	C_C		10		pF	

AC ELECTRICAL CHARACTERISTICS

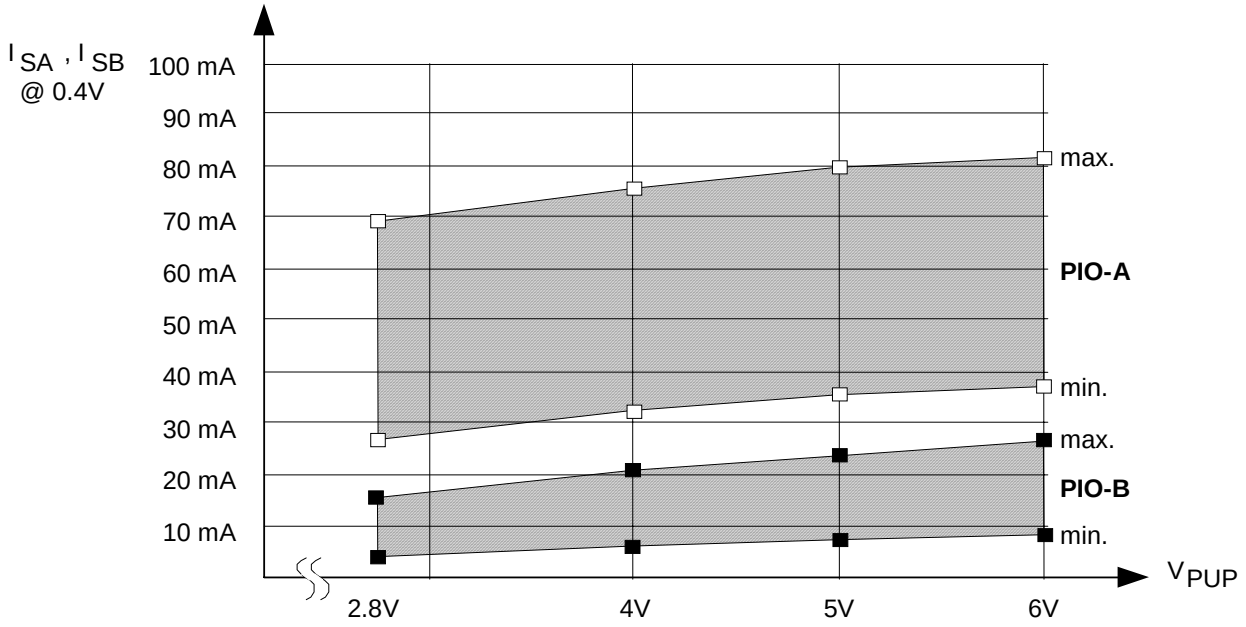
(V_{PUP}=2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	11
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Low Time	t_{LOWR}	2		15	µs	11
Read Data Valid	t_{RDV}		15		µs	12
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup 1-Wire	t_{SU}			2	µs	13
Recovery Time	t_{REC}	5			µs	
Reset High Time	t_{RSTH}	480			µs	14
Reset Low Time	t_{RSTL}	480		960	µs	15
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	
Read Data Setup PIO-A	t_{SUA}	0.5			µs	
Read Data Setup PIO-B	t_{SUB}	0.5			µs	
Delay to Program	t_{DP}	5			µs	
Delay to Verify	t_{DV}	5			µs	
Program Pulse Width	t_{PP}	480		5000	µs	16
Program Voltage Rise Time	t_{RP}	0.5		5.0	µs	
Program Voltage Fall Time	t_{FP}	0.5		5.0	µs	

Definition of PIO Read Data Setup Time



PIO SINK CURRENT



NOTE: The sink current is production-tested at V_{PUP} = 2.8V; the specification for V_{PUP} of 4V, 5V and 6V is guaranteed by design.

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP}, V_{PUPA}, V_{PUPB} = external pull-up voltage.
3. V_{IH} is a function of the chip-internal supply voltage. This voltage is determined by either the external pull-up resistor and V_{PUP} or the V_{CC} supply, whichever is higher. Without V_{CC} supply, V_{IH} for either PIO pin should always be greater than or equal to V_{PUP} -0.3V.
4. Input load is to ground.
5. Leakage current is to ground.
6. Guaranteed by design, not production tested.
7. If the current at PIO-A reaches 200mA the gate voltage of the output transistor will be reduced to limit the sink current to 200mA. The user-supplied circuitry should limit the current flow through the PIO-transistor to no more than 100mA. Otherwise the DS2406 may be damaged.
8. PIO-A has a controlled turn-on output. The indicated currents are DC values. At V_{PUP} = 4.0V or higher the sink current typically reaches 80% of its DC value 1 µs after turning on the transistor.
9. V_{CC} must be at least 4.0V if it is to be connected during a programming pulse.
10. Capacitance on the data pin could be 800pF when power is first applied. If a 5kΩ resistor is used to pull up the data line to V_{PUP}, 5µs after power has been applied the parasite capacitance will not affect normal communications.
11. The duration of the low pulse sent by the master should be a minimum of 2µs with a maximum value as short as possible to allow time for the pull-up resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write 1 Low Time, or before the master samples in the case of a Read Low Time.
12. The optimal sampling point for the master is as close as possible to the end time of the 15µs t_{RDV} period without exceeding t_{RDV}. For the case of a Read-one time slot, this maximizes the amount of time for the pull-up resistor to recover the line to a high level. For a Read-zero time slot it ensures that a read will occur before the fastest 1-Wire devices(s) release the line ($t_{RELEASE}$ = 0).

13. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 2µs of this falling edge and will remain valid for 15µs total from falling edge on 1-Wire bus.
14. An additional reset or communication sequence cannot begin until the reset high time has expired.
15. The Reset Low Time (t_{RSTL}) should be restricted to a maximum of 960µs to allow interrupt signaling; otherwise, it could mask or conceal interrupt pulses.
16. The accumulative duration of the programming pulses for each address must not exceed 5ms.

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
033109	Relocated V_{PUP} specification from headline to Data Pin parameter block in the *DC ELECTRICAL CHARACTERISTICS* table.	28
	Changed V_{ILmax} spec from 0.8V to 0.5V.	
	Removed V_{OH} spec for 1-Wire port.	
	Changed V_{ILAmax} spec from 0.6V to 0.3V.	
	Replaced input resistance RI with input leakage current ILA, ILB.	
	Replaced V_{OHA} with V_{PUPA}.	
	Replaced V_{OHB} with V_{PUPB}.	
	Added GBD note to I_{LA}, I_{LB}, I_{SA}, I_{SB}, V_{PUPA}, V_{PUPB}.	
	Changed I_{CCmax} from 4µA to 6µA.	
	Changed $t_{LOWRmin}$ from 1µs to 2µs.	29
	Changed t_{SUmax} from 1µs to 2µs.	
	Changed t_{RECmin} from 1µs to 5µs.	
	Updated PIO Sink Current graphic for 4mA (PIO-B) at 2.8V VPUP and added GBD note to graphic.	30
	Updated document text to match changes in EC table.	1, 17, 24. 25
	Removed leaded and flip-chip part numbers and references in the *Ordering Information* table.	1

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