

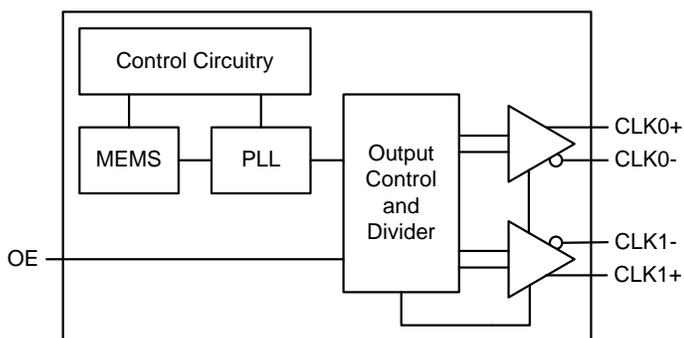


## General Description

The DSC557-03 is a crystal-less, two output PCI express clock generator meeting Gen1, Gen2, and Gen3 specifications. The clock generator uses proven silicon MEMS technology to provide 100MHz\* differential output clocks with excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the external quartz crystal, the DSSC557-03 significantly enhances reliability and accelerates product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSC557-03 has an Output Enable / Disable feature allowing it to disable the outputs when OE is low. The device is available in two different packages; a "drop-in" replacement 16 pin TSSOP or a space saving 14 pin QFN (77% less board space). Additional output formats are also available in any combination of LVPECL, LVDS, and HCSL.

## Block Diagram



\* Clk0+/- and Clk1+/- are 100 MHz as per PCIe standards. For other frequencies, please contact the factory.

## Features

- **Meets PCIe Gen1, Gen2 & Gen3 specs.**
- **Available Output Formats:**
  - HCSL, LVPECL, or LVDS
  - HCSL/LVPECL, HCSL/LVDS, LVPECL/LVDS
- **Wide Temperature Range**
  - Ext. Industrial: -40° to 105° C
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **Supply Range of 2.25 to 3.6 V**
- **Low Power Consumption**
  - 30% lower than competing devices
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **Available Footprints:**
  - 16 TSSOP
  - 14 QFN
- **Lead Free & RoHS Compliant**
- **Short Lead Time: 2 Weeks**

## Applications

- **Communications/Networking**
  - Ethernet
  - 1G, 10GBASE-T/KR/LR/SR, and FcoE
  - Routers and Switches
  - Gateways, VoIP, Wireless AP's
  - Passive Optical Networks
- **Storage**
  - SAN, NAS, SSD, JBOD
- **Embedded Applications**
  - Industrial, Medical, and Avionics
  - Security Systems and Office Automation
  - Digital Sinage, POS and others
- **Consumer Electronics**
  - Smart TV, Bluray, STB

## Specifications (Unless specified otherwise: T=25° C, VDD =3.3V)

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage <sup>1</sup>	V <sub>DD</sub>		2.25		3.6	V
Supply Current	I <sub>DD</sub>	EN pin low – outputs are disabled		21	23	mA
Supply Current <sup>2</sup> (Two HCSL Outputs)	I <sub>DD</sub>	EN pin high – outputs are enabled R <sub>L</sub> =50 Ω, F <sub>O1</sub> =F <sub>O2</sub> =100 MHz		60		mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±100	ppm
					±50	
Startup Time <sup>3</sup>	t <sub>SU</sub>				5	ms
Input Logic Levels Input logic high Input logic low	V <sub>IH</sub>		0.75xV <sub>DD</sub>		-	V
	V <sub>IL</sub>		-		0.25xV <sub>DD</sub>	
Output Disable Time <sup>4</sup>	t <sub>DA</sub>				5	ns
Output Enable Time	t <sub>EN</sub>				20	ns
Pull-Up Resistor <sup>2</sup>		Pull-up on OE pin		40		kΩ

HCSL Outputs <sup>6</sup>						
Parameter		Condition	Min.	Typ.	Max.	Unit
Output Logic Levels Output logic high Output logic low	V <sub>OH</sub>	R <sub>L</sub> =50Ω	0.725		-	V
	V <sub>OL</sub>		-		0.1	
Pk to Pk Output Swing		Single-Ended		750		mV
Output Transition time <sup>4</sup> Rise Time Fall Time	t <sub>R</sub>	20% to 80% R <sub>L</sub> =50Ω, C <sub>L</sub> = 2pF	200		400	ps
	t <sub>F</sub>					
Frequency	f <sub>0</sub>	Single Frequency	2.3	100 <sup>7</sup>	460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter <sup>5</sup>	J <sub>PER</sub>	F <sub>O1</sub> =F <sub>O2</sub> =100 MHz		2.5		ps <sub>RMS</sub>
Jitter, Phase (Common Clock Architecture)	R <sub>J</sub>	PCIe Gen 1.1 T <sub>J</sub> =D <sub>J</sub> + 14.069 x R <sub>J</sub> (BER 10-12)		0.540		ps <sub>RMS</sub>
	D <sub>J</sub> T <sub>J</sub>	PCIe Gen 1.1 T <sub>J</sub> =D <sub>J</sub> + 14.069 x R <sub>J</sub> (BER 10-12)		0.832 8.536	41.9 <sup>8</sup> 86.0 <sup>8</sup>	ps <sub>P-P</sub>
	J <sub>RMS-CCHF</sub>	PCIe Gen 2.1, 1.5 MHz to Nyquist		0.458	3.1 <sup>8</sup>	ps <sub>RMS</sub>
	J <sub>RMS-CCLF</sub>	PCIe Gen 2.1, 10 kHz to 1.5 MHz		0.030	3.0 <sup>8</sup>	ps <sub>RMS</sub>
	J <sub>RMS-CC</sub>	PCIe Gen 3.0		0.165	1.0 <sup>8</sup>	ps <sub>RMS</sub>
Integrated Phase Noise (Data Clock Architecture)	J <sub>RMS-DCHF</sub>	PCIe Gen 2.1, 1.5 MHz to Nyquist		0.561	4.0 <sup>8</sup>	ps <sub>RMS</sub>
	J <sub>RMS-DCLF</sub>	PCIe Gen 2.1, 10 kHz to 1.5 MHz		1.778	7.5 <sup>8</sup>	ps <sub>RMS</sub>
	J <sub>RMS-DC</sub>	PCIe Gen 3.0		0.147	1.0 <sup>8</sup>	ps <sub>RMS</sub>

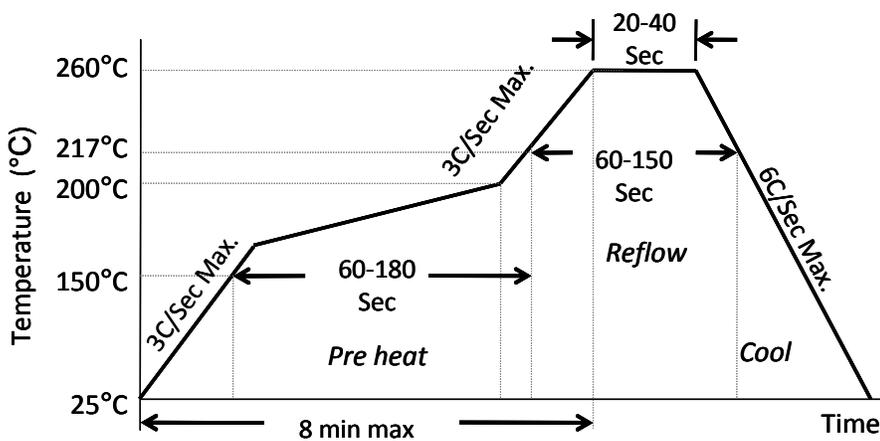
### Notes:

- V<sub>DD</sub> should be filtered with 0.01uf capacitor.
- Output is enabled if OE pin is floated or not connected.
- t<sub>SU</sub> is time to 100PPM stable output frequency after V<sub>DD</sub> is applied and outputs are enabled.
- Output Waveform and Connection Diagram define the parameters.
- Period Jitter includes crosstalk from adjacent output.
- Contact [Sales@Discera.com](mailto:Sales@Discera.com) for alternate output options (LVPECL, LVDS, LVCMOS).
- Contact [Sales@Discera.com](mailto:Sales@Discera.com) for alternate frequency options
- Jitter limits established by Gen 1.1, Gen 2.1, and Gen 3.0 PCIe standards.

## Absolute Maximum Ratings

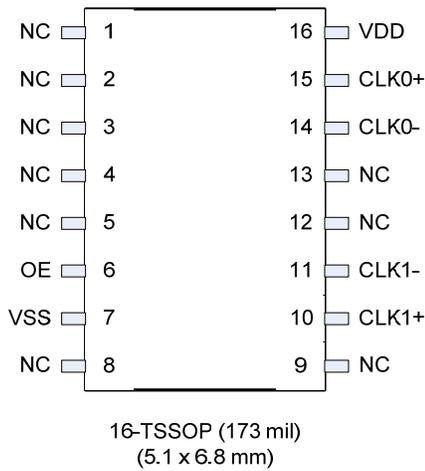
Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	$V_{DD}+0.3$	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD	-		V	
HBM		4000		
MM		400		
CDM		1500		

## Solder Reflow Profile

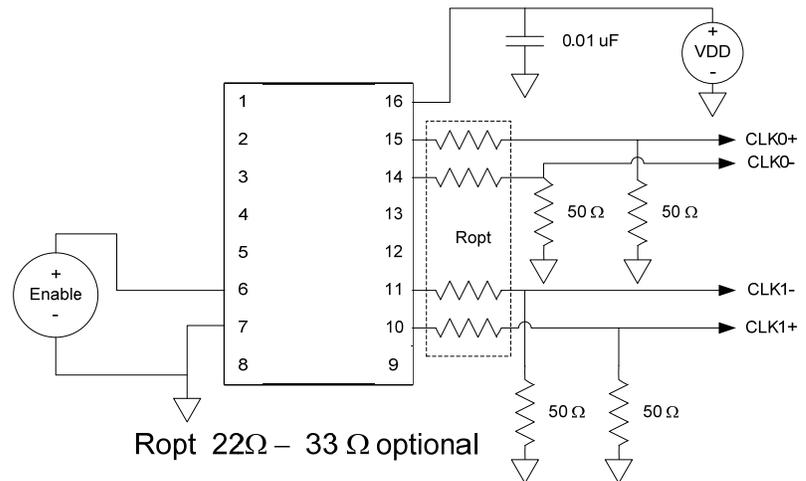


<b>14 QFN MSL 1 @ 260°C refer to JSTD-020C</b> <b>16 TSSOP MSL 3 @ 260°C refer to JSTD-020C</b>	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

## Pin Diagram (16 TSSOP)



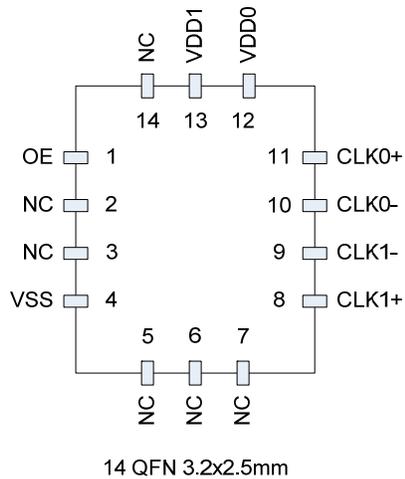
## Connection Diagram (16 TSSOP Two HCSL Outputs)



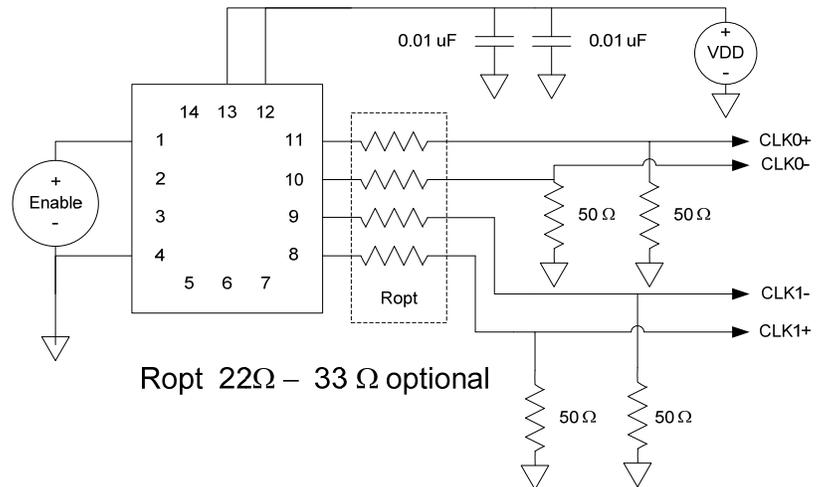
## Pin Description (16 TSSOP)

Pin No.	Pin Name <sup>9</sup>	Pin Type	Description
1	NC	NA	No connect
2	NC	NA	No connect
3	NC	NA	No connect
4	NC	NA	No connect
5	NC	NA	No connect
6	OE	I	Output Enable; active high
7	VSS	Power	Ground
8	NC	NA	No connect
9	NC	NA	No connect
10	CLK1+	O	True output of differential pair
11	CLK1-	O	Complement output of differential pair
12	NC	NA	No connect
13	NC	NA	No connect
14	CLK0-	O	Complement output of differential pair
15	CLK0+	O	True output of differential pair
16	VDD	Power	Power Supply

## Pin Diagram (14 QFN)



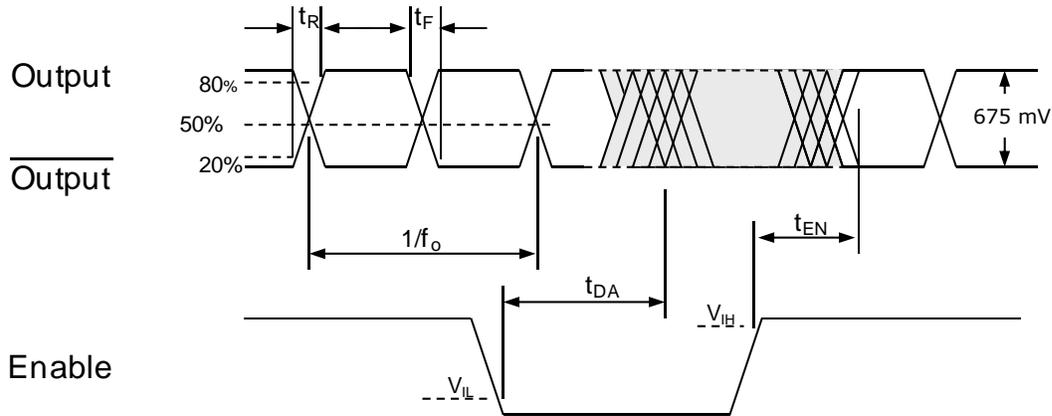
## Connection Diagram (14 QFN Two HCSL Outputs)



## Pin Description (14 QFN)

Pin No.	Pin Name	Pin Type	Description
1	OE	I	Output Enable; active high
2	NC	NA	Ground recommended or leave as a NC
3	NC	NA	Ground recommended or leave as a NC
4	VSS	Power	Ground
5	NC	NA	Ground recommended or leave as a NC
6	NC	NA	Ground recommended or leave as a NC
7	NC	NA	Ground recommended or leave as a NC
8	CLK1+	O	True output of differential pair
9	CLK1-	O	Complement output of differential pair
10	CLK0-	O	Complement output of differential pair
11	CLK0+	O	True output of differential pair
12	VDD1	Power	Power Supply for Core and Output 1 (CLK0+/-)
13	VDD0	Power	Power Supply for Output 0 (CLK1+/-)
14	NC	NA	Ground recommended or leave as a NC

## OE Function and Output Waveform: HCSL



## Ordering Information<sup>9</sup>

**DSC557-03 4 4 F I 0 - T**

CLK 1 Output Format  
 1: LVCMOS  
 2: LVPECL  
 3: LVDS  
 4: HCSL

CLK 0 Output Format  
 1: LVCMOS  
 2: LVPECL  
 3: LVDS  
 4: HCSL

- Packing  
T: Tape & Reel
- Stability  
0: ±100ppm  
1: ±50ppm
- Temp Range  
E: -20 to 70  
I: -40 to 85  
L: -40 to 105
- Package  
F: 14 QFN  
S: 16 TSSOP

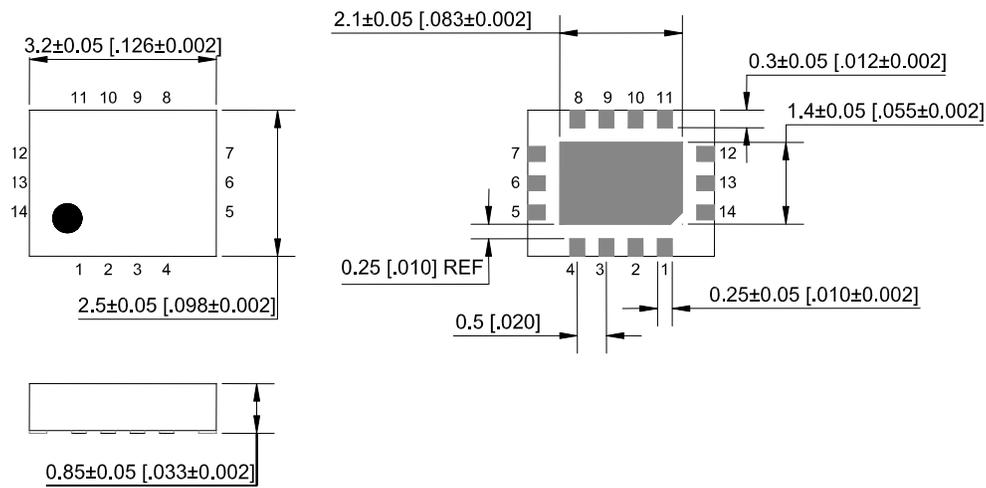
Note 9. CLK0 and CLK1 are configured at the factory to 100 MHz. (For other frequencies, contact the factory at sales@discera.com.)

## Package Dimensions

### F: 14 QFN, 3.2 x 2.5 mm

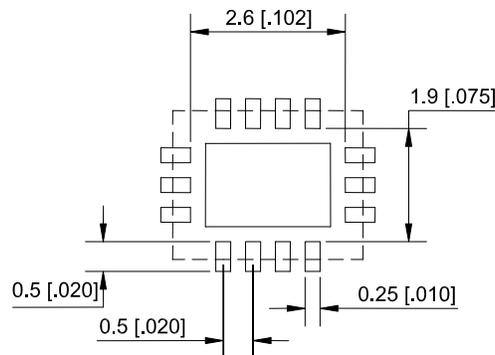
#### External Dimensions

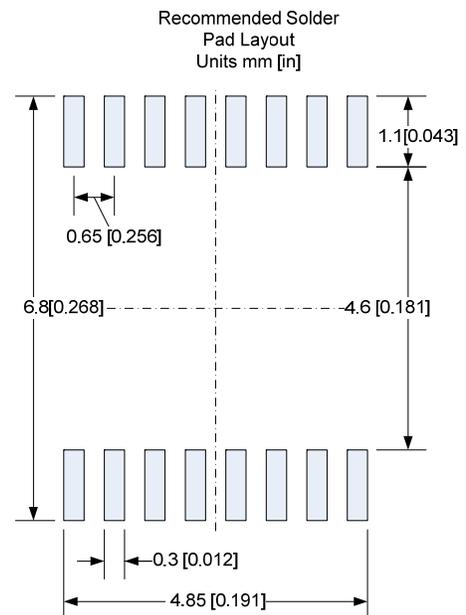
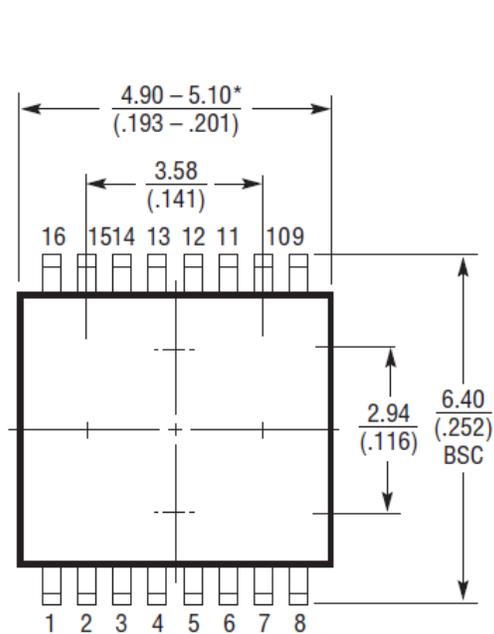
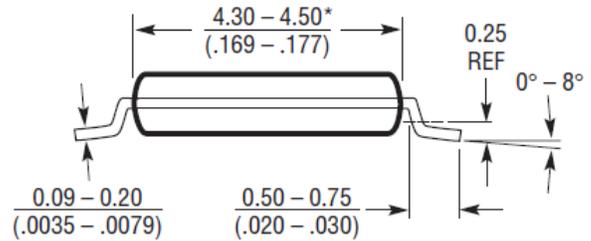
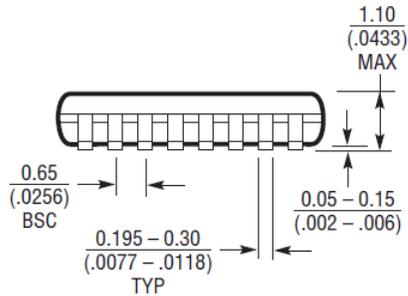
units: mm[inch]



#### Recommended Solder Pad Layout

units: mm[inch]



**S: 16 TSSOP (173 mil body width)****NOTE:**

1. CONTROLLING DIMENSION: MILLIMETERS

2. DIMENSIONS ARE IN  $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$ 

3. DRAWING NOT TO SCALE

4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

\*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

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