# dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814

# 16-Bit Microcontrollers and Digital Signal Controllers with High-Speed PWM, USB and Advanced Analog

## Operating Conditions

- 3.0V to 3.6V, -40ºC to +125ºC, DC to 60 MIPS
- 3.0V to 3.6V, -40ºC to +85ºC, DC to 70 MIPS

## Core: 16-Bit dsPIC33E/PIC24E CPU

- Code-Efficient (C and Assembly) architecture
- Two 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle Mixed-Sign MUL Plus Hardware Divide
- 32-Bit Multiply Support

## Clock Management

- 2% Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer
- Fast Wake-up and Start-up

## Power Management

- Low-Power Management modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset
- 1.0 mA/MHz Dynamic Current (typical)
- 60 µA $I_{PD}$ Current (typical)

## High-Speed PWM

- Up to Seven PWM Pairs with Independent Timing
- Dead Time for Rising and Falling Edges
- 8.32 ns PWM Resolution
- PWM Support for:
  - DC/DC, AC/DC, Inverters, PFC, Lighting
  - BLDC, PMSM, ACIM, SRM
- Programmable Fault Inputs
- Flexible Trigger Configurations for ADC Conversions

## Advanced Analog Features

- Two Independent ADC modules:
  - One ADC configurable as 10-bit, 1.1 Msps with four S&H or 12-bit, 500 ksps with one S&H
  - One 10-bit ADC, 1.1 Msps with four S&H
  - Eight S&H using both ADC 10-bit modules
  - 24 analog channels (64-pin devices) up to 32 analog channels (100/121/144-pin devices)
- Flexible and Independent ADC Trigger Sources
- Comparators:
  - Up to three Analog Comparator modules
  - Programmable references with 32 voltage points

## Timers/Output Compare/Input Capture

- 27 General Purpose Timers:
  - Nine 16-bit and up to four 32-bit Timers/Counters
  - 16 OC modules configurable as Timers/Counters
  - Two 32-bit Quadrature Encoder Interface (QEI) modules configurable as Timers/Counters
- 16 IC modules
- Peripheral Pin Select (PPS) to allow Function Remap
- Real-Time Clock and Calendar (RTCC) module

## Communication Interfaces

- USB 2.0 OTG-Compliant Full-Speed Interface
- Four UART modules (15 Mbps)
  - Supports LIN/J2602 protocols and IrDA®
- Four 4-Wire SPI modules (15 Mbps)
- Two ECAN™ modules (1 Mbaud) CAN 2.0B Support
- Two $I^2C$ modules (up to 1 Mbaud) with SMBus Support
- Data Converter Interface (DCI) module with Support for $I^2S$ and Audio Codecs
- PPS to allow Function Remap
- Parallel Master Port (PMP)
- Programmable Cyclic Redundancy Check (CRC)

## Direct Memory Access (DMA)

- 15-Channel DMA with User-Selectable Priority Arbitration
- UART, USB, SPI, ADC, ECAN™, IC, OC, Timers, DCI/$I^2S$, PMP

## Input/Output

- Sink/Source 10 mA on All Pins
- 5V Tolerant Pins
- Selectable Open-Drain, Pull-ups and Pull-Downs
- Up to 5 mA Overvoltage Clamp Current
- External Interrupts on All I/O pins

## Qualification and Class B Support

- AEC-Q100 REVG (Grade 1 -40ºC to +125ºC) Planned
- AEC-Q100 REVG (Grade 0 -40ºC to +150ºC) Planned
- Class B Safety Library, IEC 60730

## Debugger Development Support

- In-Circuit and In-Application Programming
- Five Program and Three Complex Data Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

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## dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. Their pinout diagrams appear on the following pages.

**TABLE 1: dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 CONTROLLER FAMILIES**

| Device | Pins | Packages | Program Flash Memory (Kbyte)(1) | RAM (Kbyte)(2) | Remappable Peripherals | | | | | | | | | | | | RTCC | $I^2C$™ | CRC Generator | 10-Bit/12-Bit ADC(8) | USB | Parallel Master Port | I/O Pins |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 16-Bit Timer(3,4) | Input Capture | Output Compare (with PWM) | Motor Control PWM (Channels)(5) | QEI | UART with IrDA® | SPI | ECAN™ | External Interrupts(6) | DMA Controller (Channels) | DCI | Analog Comparators/ Inputs Per Comparator(7) | | | | | | | |
| dsPIC33EP256MU806 | 64 | QFN, TQFP | 280 | 28 | 9 | 16 | 16 | 8 | 2 | 4 | 4 | 2 | 5 | 15 | 1 | 3/4 | 1 | 2 | 1 | 2 ADC, 24 ch | 1 | Y | 51 |
| dsPIC33EP256MU810 | 100 | TQFP | 280 | 28 | 9 | 16 | 16 | 12 | 2 | 4 | 4 | 2 | 5 | 15 | 1 | 3/4 | 1 | 2 | 1 | 2 ADC, 32 ch | 1 | Y | 83 |
| | 121 | TFBGA | | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EP256MU814 | 144 | TQFP, LQFP | 280 | 28 | 9 | 16 | 16 | 14 | 2 | 4 | 4 | 2 | 5 | 15 | 1 | 3/4 | 1 | 2 | 1 | 2 ADC, 32 ch | 1 | Y | 122 |
| dsPIC33EP512GP806 | 64 | QFN, TQFP | 536 | 52 | 9 | 16 | 16 | — | — | 4 | 4 | 2 | 5 | 15 | 1 | 3/4 | 1 | 2 | 1 | 2 ADC, 24 ch | — | Y | 53 |
| dsPIC33EP512MC806 | 64 | QFN, TQFP | 536 | 52 | 9 | 16 | 16 | 8 | 2 | 4 | 4 | 2 | 5 | 15 | 1 | 3/4 | 1 | 2 | 1 | 2 ADC, 24 ch | — | Y | 53 |
| dsPIC33EP512MU810 | 100 | TQFP | 536 | 52 | 9 | 16 | 16 | 12 | 2 | 4 | 4 | 2 | 5 | 15 | 1 | 3/4 | 1 | 2 | 1 | 2 ADC, 32 ch | 1 | Y | 83 |
| | 121 | TFBGA | | | | | | | | | | | | | | | | | | | | | |
| dsPIC33EP512MU814 | 144 | TQFP, LQFP | 536 | 52 | 9 | 16 | 16 | 14 | 2 | 4 | 4 | 2 | 5 | 15 | 1 | 3/4 | 1 | 2 | 1 | 2 ADC, 32 ch | 1 | Y | 122 |
| PIC24EP256GU810 | 100 | TQFP | 280 | 28 | 9 | 16 | 16 | 0 | 0 | 4 | 4 | 2 | 5 | 15 | 1 | 3/4 | 1 | 2 | 1 | 2 ADC, 32 ch | 1 | Y | 83 |
| | 121 | TFBGA | | | | | | | | | | | | | | | | | | | | | |
| PIC24EP256GU814 | 144 | TQFP, LQFP | 280 | 28 | 9 | 16 | 16 | 0 | 0 | 4 | 4 | 2 | 5 | 15 | 1 | 3/4 | 1 | 2 | 1 | 2 ADC, 32 ch | 1 | Y | 122 |
| PIC24EP512GP806 | 64 | QFN, TQFP | 586 | 52 | 9 | 16 | 16 | — | — | 4 | 4 | 2 | 5 | 15 | 1 | 3/4 | 1 | 2 | 1 | 2 ADC, 24 ch | — | Y | 53 |
| PIC24EP512GU810 | 100 | TQFP | 536 | 52 | 9 | 16 | 16 | 0 | 0 | 4 | 4 | 2 | 5 | 15 | 1 | 3/4 | 1 | 2 | 1 | 2 ADC, 32 ch | 1 | Y | 83 |
| | 121 | TFBGA | | | | | | | | | | | | | | | | | | | | | |
| PIC24EP512GU814 | 144 | TQFP,LQFP | 536 | 52 | 9 | 16 | 16 | 0 | 0 | 4 | 4 | 2 | 5 | 15 | 1 | 3/4 | 1 | 2 | 1 | 2 ADC, 32 ch | 1 | Y | 122 |

**Note 1:** Flash size is inclusive of 24 Kbytes of auxiliary Flash. Auxiliary Flash supports simultaneous code execution and self-erase/programming. Refer to **Section 5. "Flash Programming"** (DS70609) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

**2:** RAM size is inclusive of 4 Kbytes of DMA RAM (DPSRAM) for all devices.

**3:** Up to eight of these timers can be combined into four 32-bit timers.

**4:** Eight out of nine timers are remappable.

**5:** PWM Faults and Sync signals are remappable.

**6:** Four out of five interrupts are remappable.

**7:** Comparator output is remappable.

**8:** The ADC2 module supports 10-bit mode only.


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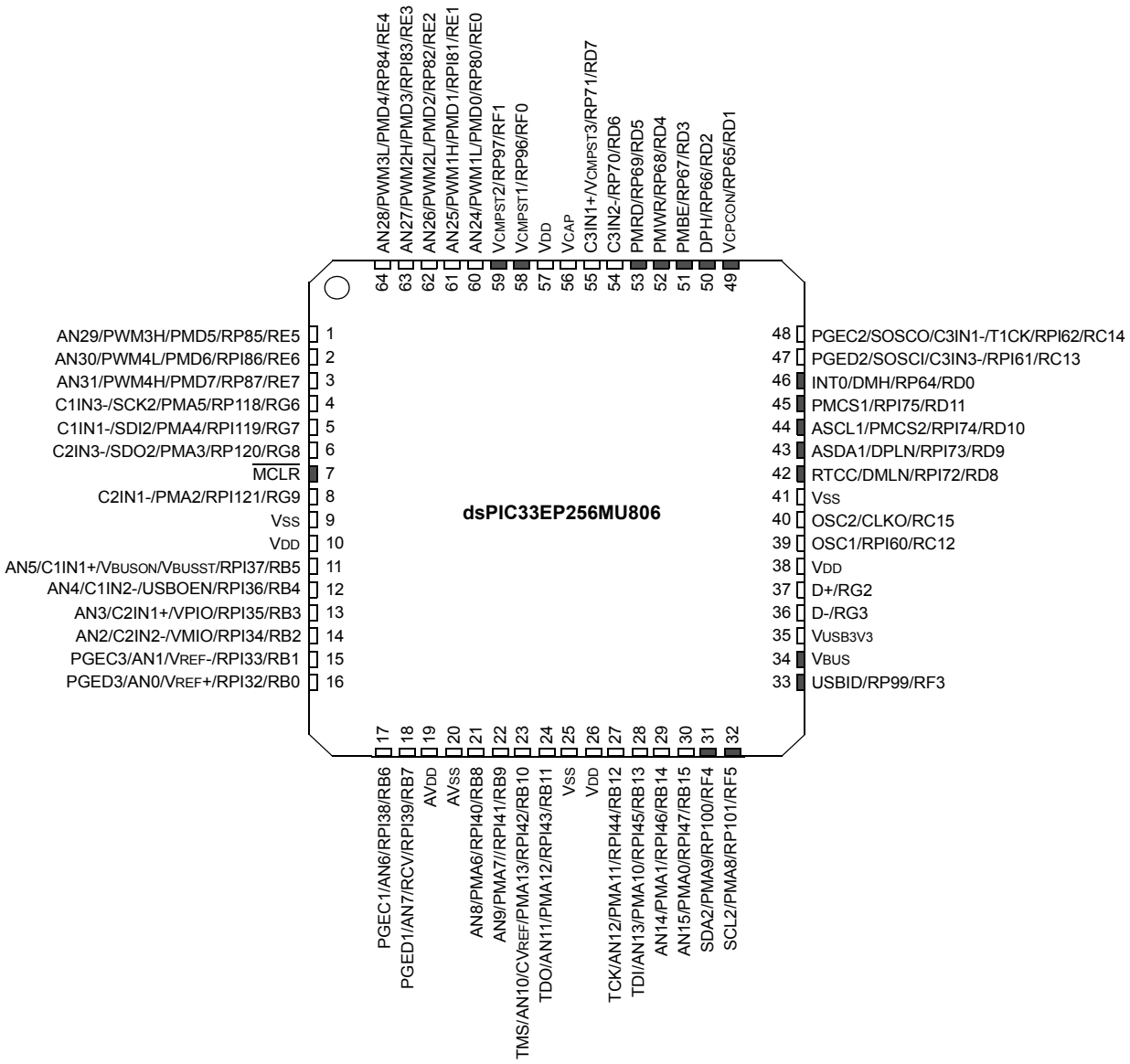
## Pin Diagrams

**64-Pin QFN**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

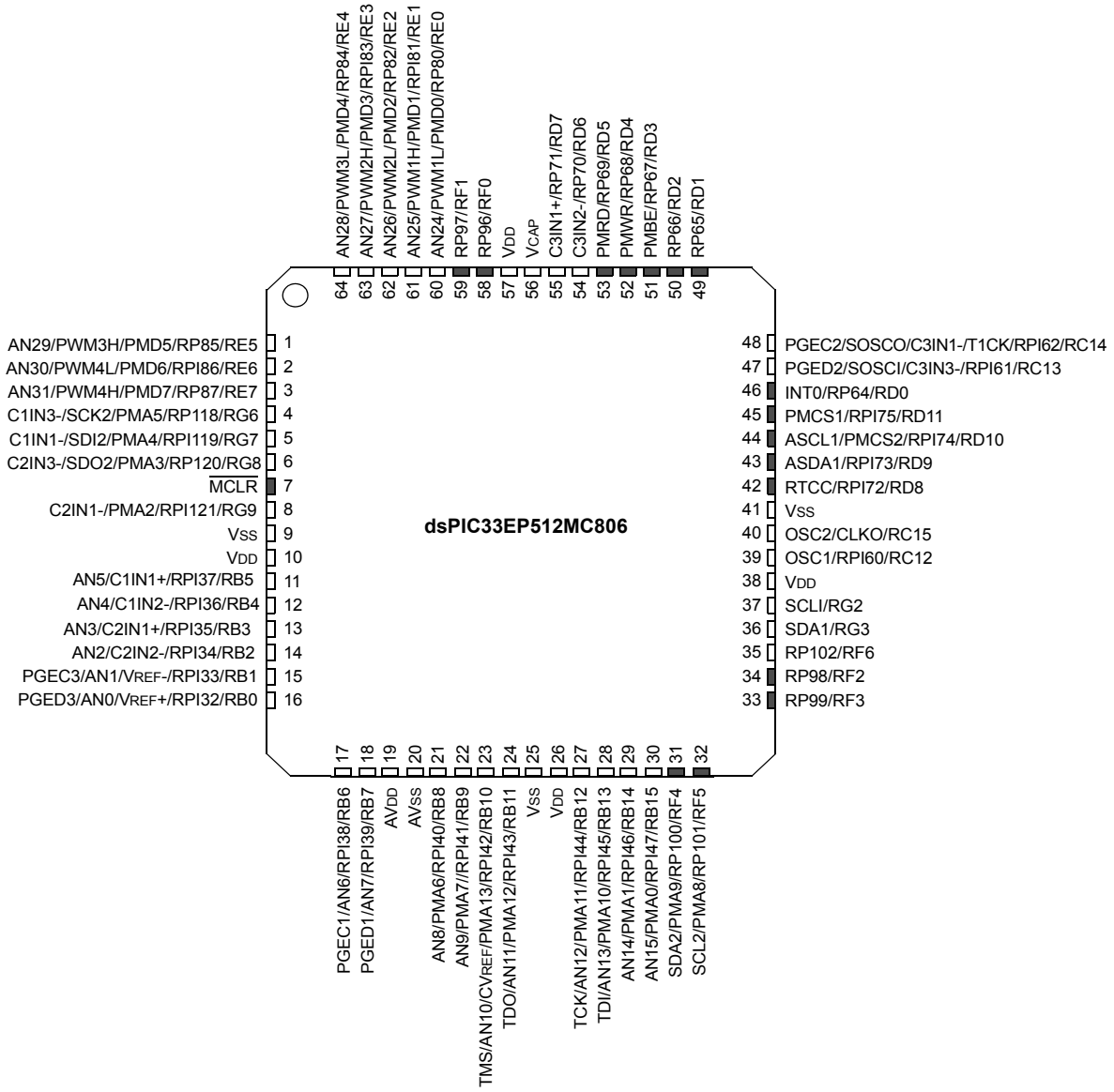
**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

## Pin Diagrams

**64-Pin QFN**

■ = Pins are up to 5V tolerant

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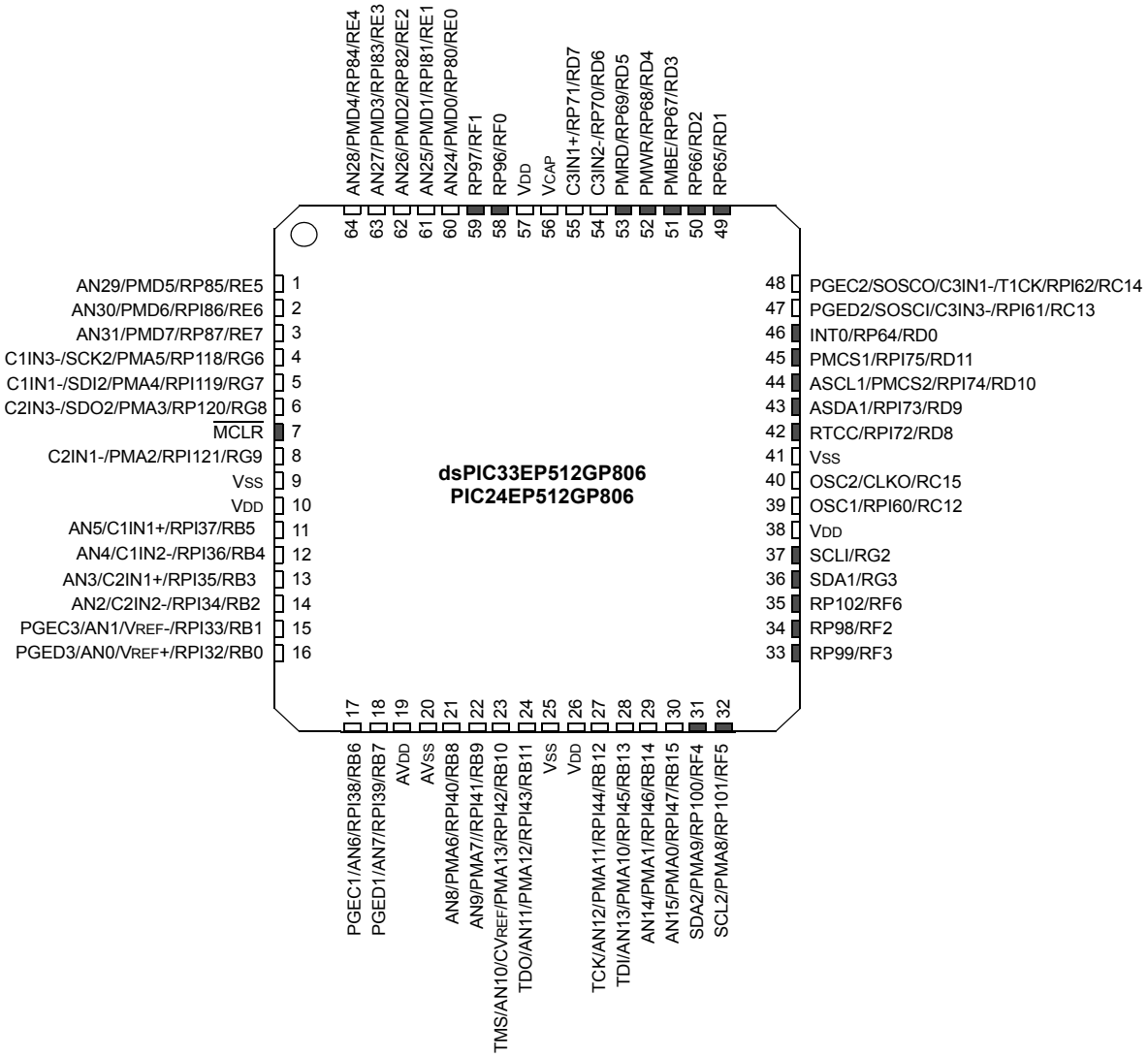
## Pin Diagrams

**64-Pin QFN**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

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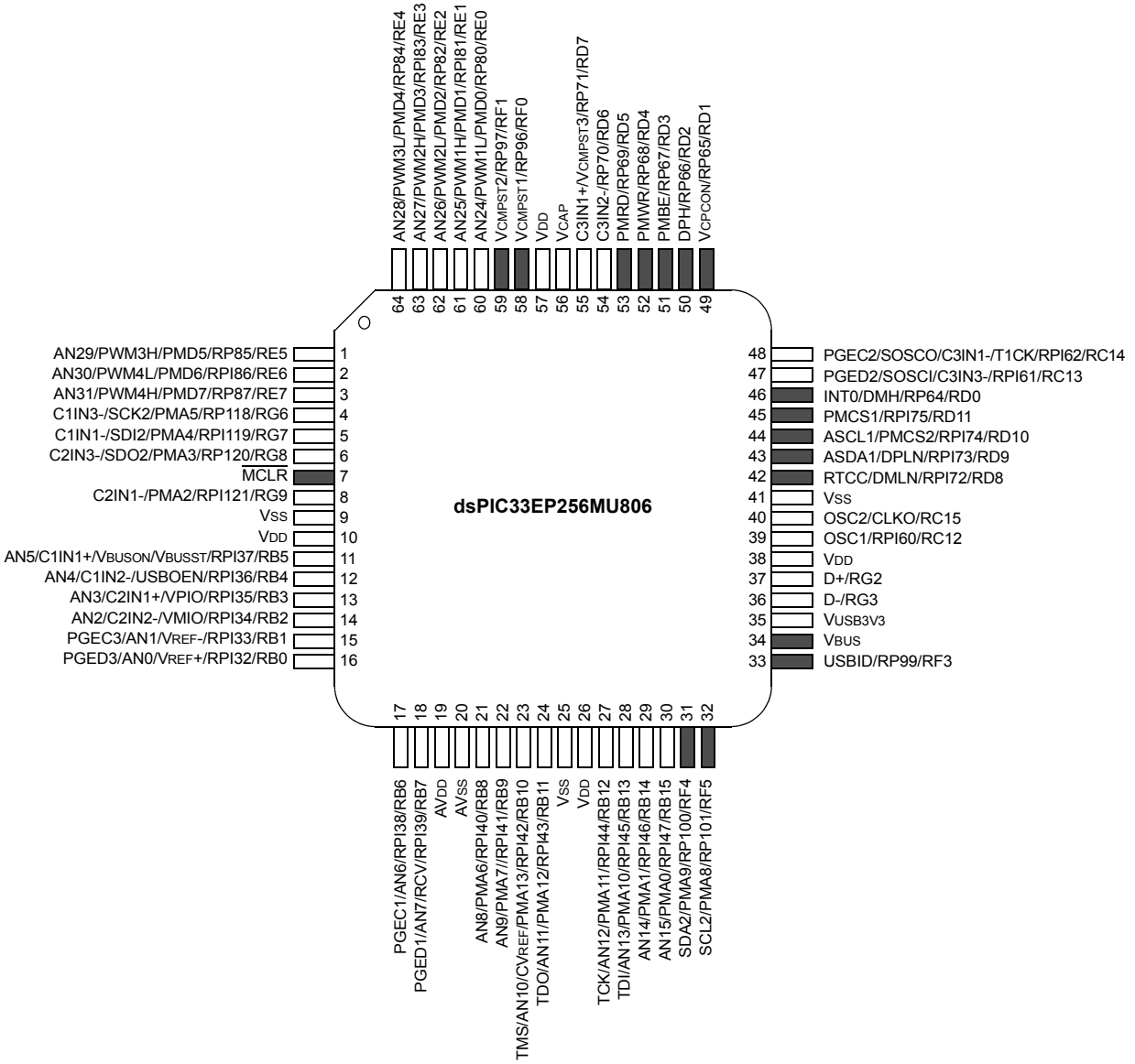
## Pin Diagrams (Continued)

**64-Pin TQFP**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

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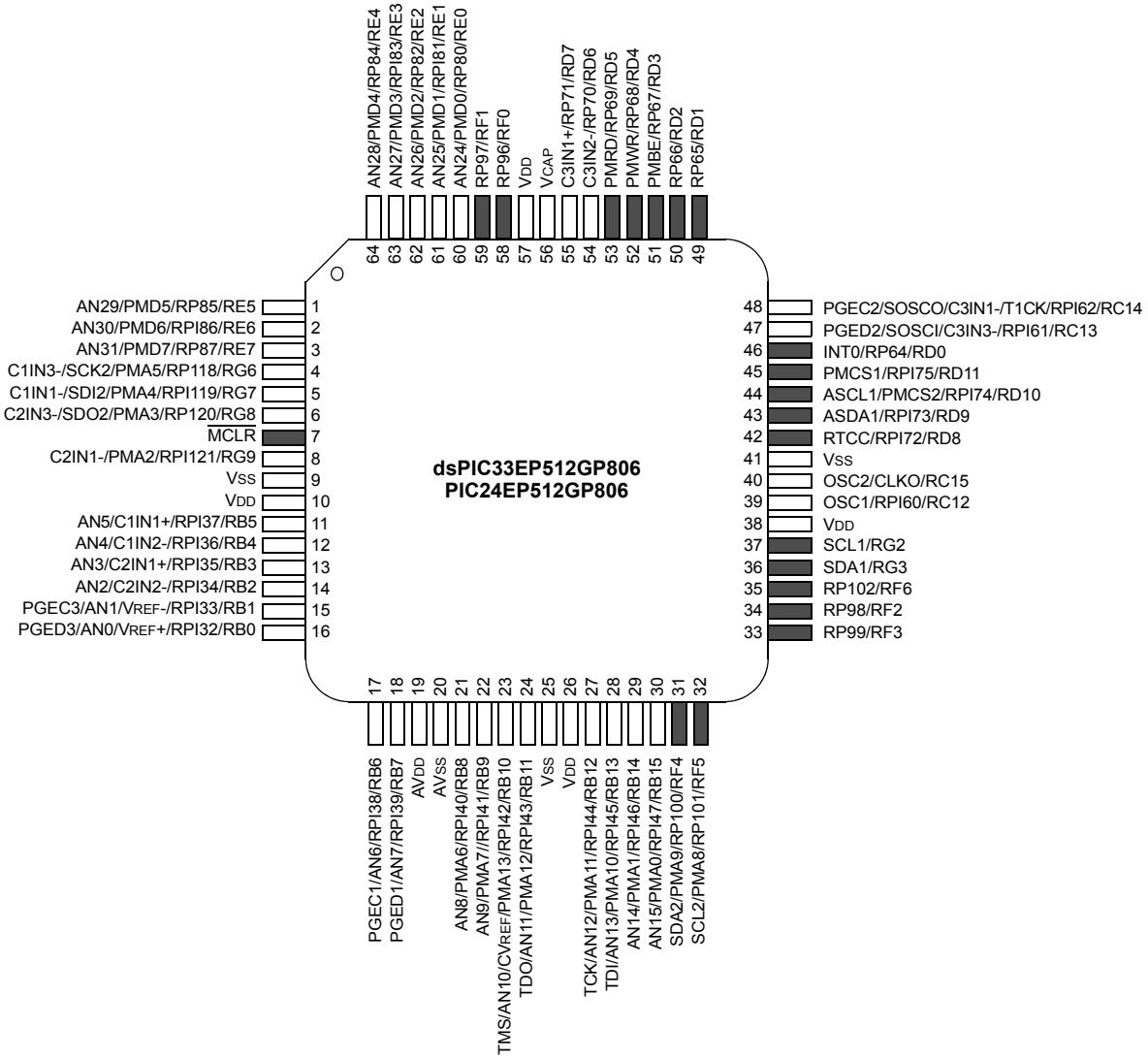
## Pin Diagrams (Continued)

**64-Pin TQFP**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

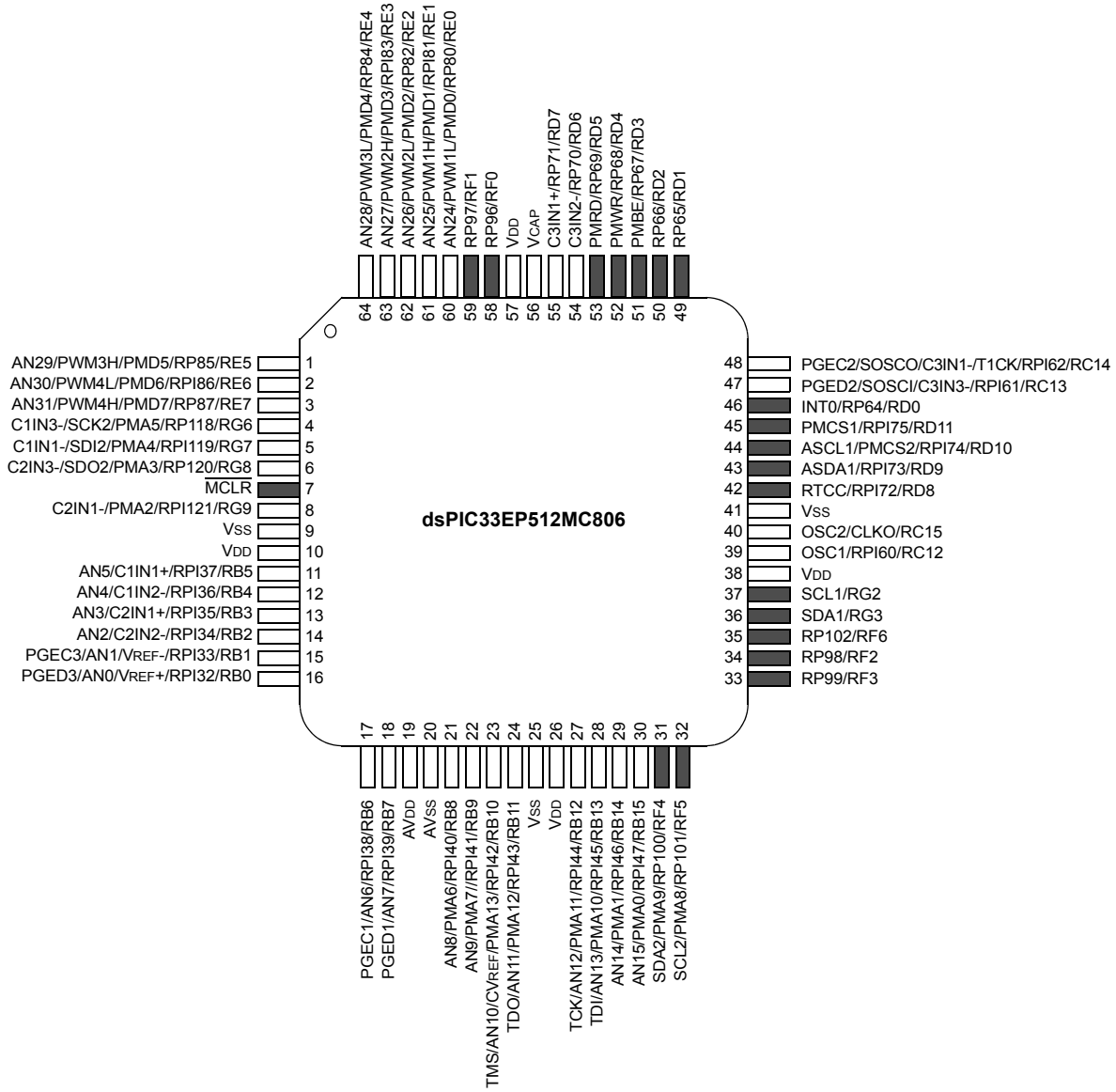
**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

## Pin Diagrams (Continued)

**64-Pin TQFP**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.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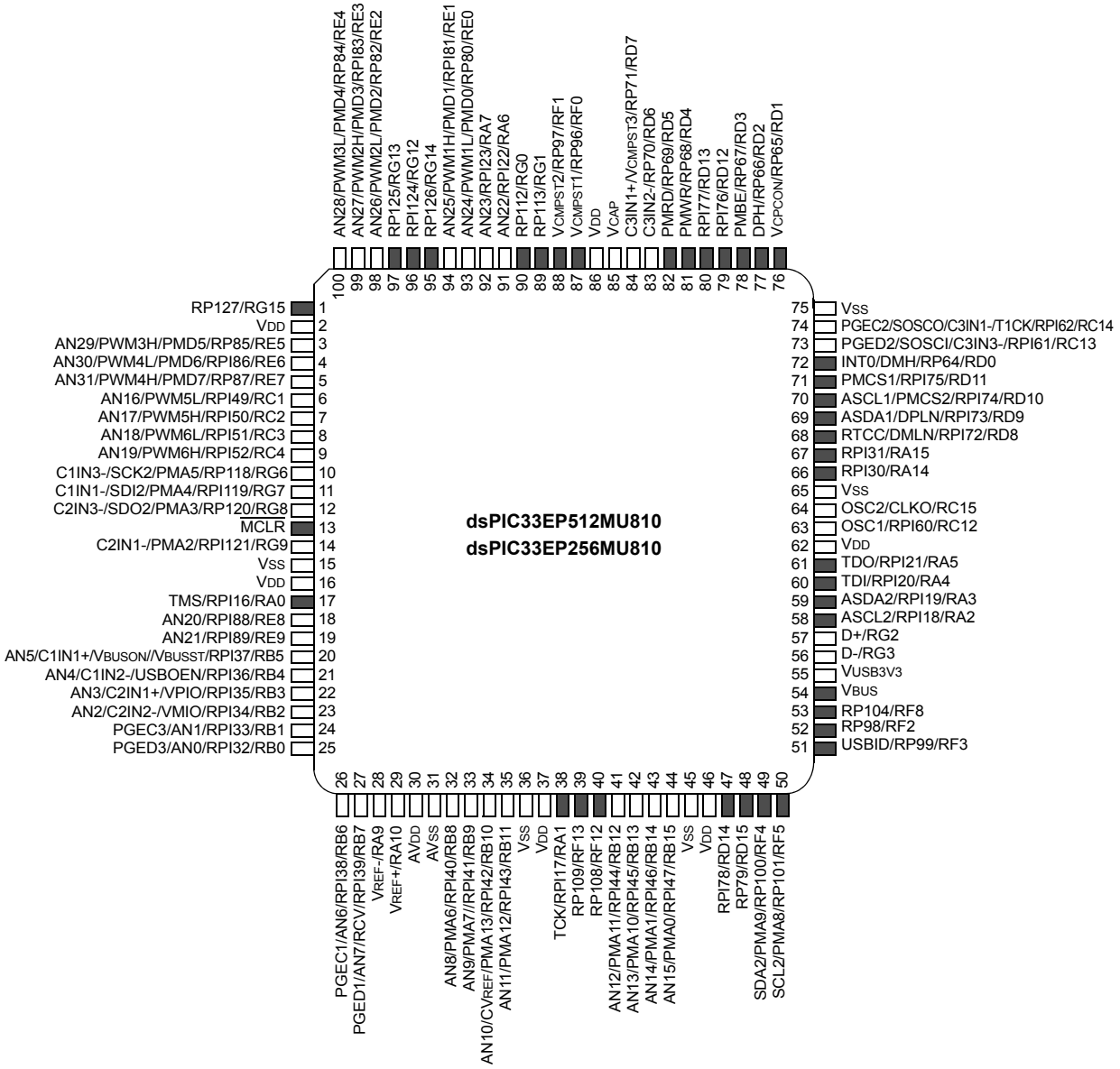
## Pin Diagrams (Continued)

**100-Pin TQFP**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

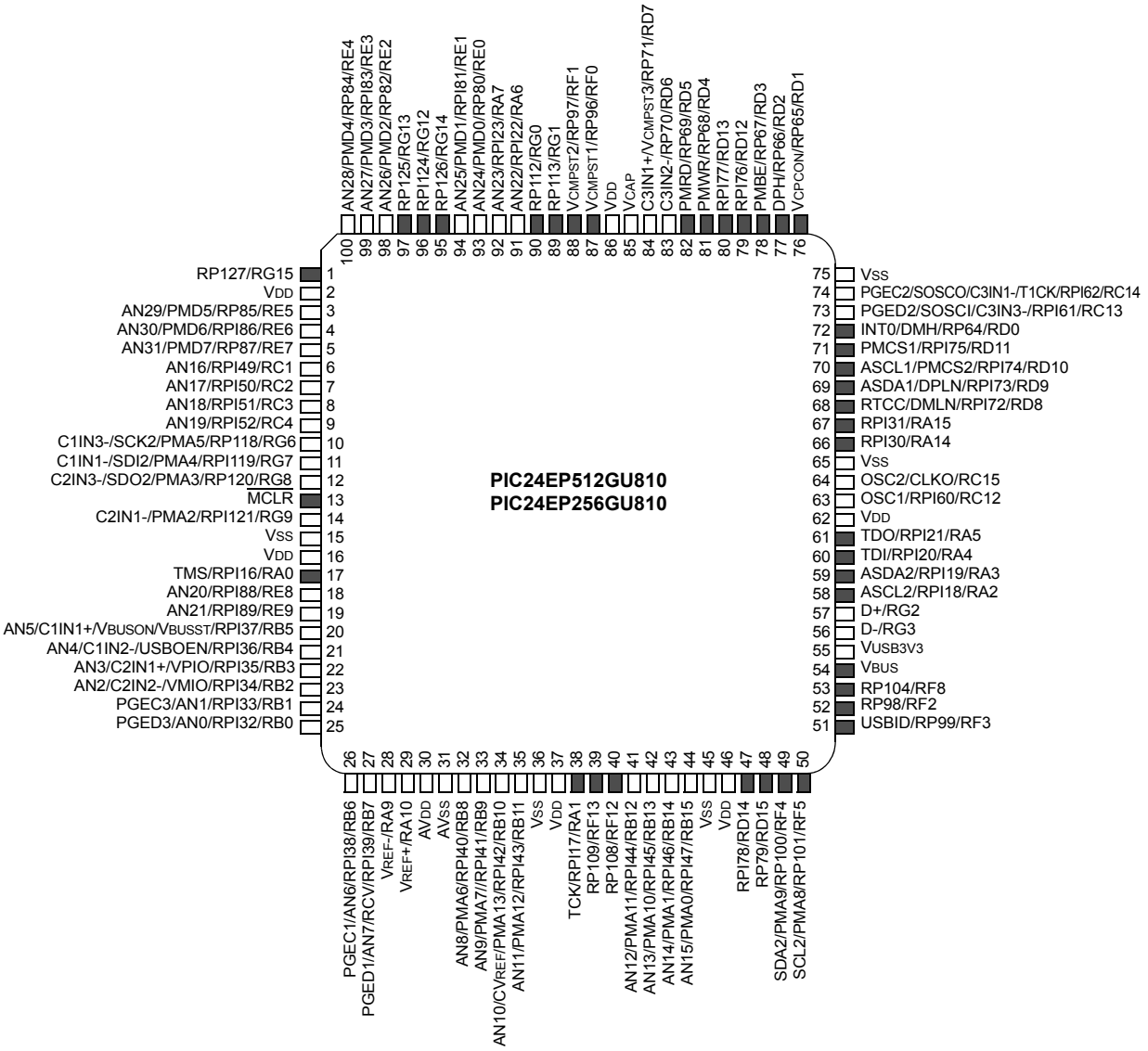
**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

## Pin Diagrams (Continued)

**100-Pin TQFP**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.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## Pin Diagrams (Continued)

**121-Pin TFBGA(1)**

● = Pins are up to 5V tolerant

**dsPIC33EP256MU810**
**dsPIC33EP512MU810**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | RE4 | RE3 | RG13 | RE0 | RG0 | RF1 | VDD | NC | RD12 | RD2 | RD1 |
| B | NC | RG15 | RE2 | RE1 | RA7 | RF0 | VCAP | RD5 | RD3 | VSS | RC14 |
| C | RE6 | VDD | RG12 | RG14 | RA6 | NC | RD7 | RD4 | NC | RC13 | RD11 |
| D | RC1 | RE7 | RE5 | NC | NC | NC | RD6 | RD13 | RD0 | NC | RD10 |
| E | RC4 | RC3 | RG6 | RC2 | NC | RG1 | NC | RA15 | RD8 | RD9 | RA14 |
| F | MCLR | RG8 | RG9 | RG7 | VSS | NC | NC | VDD | RC12 | VSS | RC15 |
| G | RE8 | RE9 | RA0 | NC | VDD | VSS | VSS | NC | RA5 | RA3 | RA4 |
| H | RB5 | RB4 | NC | NC | NC | VDD | NC | VBUS | VUSB3V3 | RG2 | RA2 |
| J | RB3 | RB2 | RB7 | AVDD | RB11 | RA1 | RB12 | NC | NC | RF8 | RG3 |
| K | RB1 | RB0 | RA10 | RB8 | NC | RF12 | RB14 | VDD | RD15 | RF3 | RF2 |
| L | RB6 | RA9 | AVSS | RB9 | RB10 | RF13 | RB13 | RB15 | RD14 | RF4 | RF5 |

**Note 1:** Refer to Table 2 for full pin names.

**TABLE 2: PIN NAMES: dsPIC33EP256MU810 AND dsPIC33EP512MU810 DEVICES(1,2)**

| Pin Number | Full Pin Name |
|---|---|
| A1 | AN28/PWM3L/PMD4/RP84/RE4 |
| A2 | AN27/PWM2H/PMD3/RPI83/RE3 |
| A3 | RP125/RG13 |
| A4 | AN24/PWM1L/PMD0/RP80/RE0 |
| A5 | RP112/RG0 |
| A6 | VCMPST2/RP97/RF1 |
| A7 | VDD |
| A8 | No Connect |
| A9 | RPI76/RD12 |
| A10 | DPH/RP66/RD2 |
| A11 | VCPCON/RP65/RD1 |
| B1 | No Connect |
| B2 | RP127/RG15 |
| B3 | AN26/PWM2L/PMD2/RP82/RE2 |
| B4 | AN25/PWM1H/PMD1/RPI81/RE1 |
| B5 | AN23/RPI23/RA7 |
| B6 | VCMPST1/RP96/RF0 |
| B7 | VCAP |
| B8 | PMRD/RP69/RD5 |
| B9 | PMBE/RP67/RD3 |
| B10 | VSS |
| B11 | PGEC2/SOSCO/C3IN1-/T1CK/RPI62/RC14 |
| C1 | AN30/PWM4L/PMD6/RPI86/RE6 |
| C2 | VDD |
| C3 | RPI124/RG12 |
| C4 | RP126/RG14 |
| C5 | AN22/RPI22/RA6 |
| C6 | No Connect |
| C7 | C3IN1+/VCMPST3/RP71/RD7 |
| C8 | PMWR/RP68/RD4 |
| C9 | No Connect |
| C10 | PGED2/SOSCI/C3IN3-/RPI61/RC13 |
| C11 | PMCS1/RPI75/RD11 |
| D1 | AN16/PWM5L/RPI49/RC1 |
| D2 | AN31/PWM4H/PMD7/RP87/RE7 |
| D3 | AN29/PWM3H/PMD5/RP85/RE5 |
| D4 | No Connect |
| D5 | No Connect |
| D6 | No Connect |
| D7 | C3IN2-/RP70/RD6 |
| D8 | RPI77/RD13 |
| D9 | INT0/DMH/RP64/RD0 |
| D10 | No Connect |
| D11 | ASCL1(3)/PMCS2/RPI74/RD10 |

| Pin Number | Full Pin Name |
|---|---|
| E8 | RPI31/RA15 |
| E9 | RTCC/DMLN/RPI72/RD8 |
| E10 | ASDA1(3)/DPLN/RPI73/RD9 |
| E11 | RPI30/RA14 |
| F1 | $\overline{\text{MCLR}}$ |
| F2 | C2IN3-/SDO2/PMA3/RP120/RG8 |
| F3 | C2IN1-/PMA2/RPI121/RG9 |
| F4 | C1IN1-/SDI2/PMA4/RPI119/RG7 |
| F5 | VSS |
| F6 | No Connect |
| F7 | No Connect |
| F8 | VDD |
| F9 | OSC1/RPI60/RC12 |
| F10 | VSS |
| F11 | OSC2/CLKO/RC15 |
| G1 | AN20/RPI88/RE8 |
| G2 | AN21/RPI89/RE9 |
| G3 | TMS/RPI16/RA0 |
| G4 | No Connect |
| G5 | VDD |
| G6 | VSS |
| G7 | VSS |
| G8 | No Connect |
| G9 | TDO/RPI21/RA5 |
| G10 | ASDA2(3)/RPI19/RA3 |
| G11 | TDI/RPI20/RA4 |
| H1 | AN5/C1IN1+/VBUSON/VBUSST/RPI37/RB5 |
| H2 | AN4/C1IN2-/USBOEN/RPI36/RB4 |
| H3 | No Connect |
| H4 | No Connect |
| H5 | No Connect |
| H6 | VDD |
| H7 | No Connect |
| H8 | VBUS |
| H9 | VUSB3V3 |
| H10 | D+/RG2(4) |
| H11 | ASCL2(3)/RPI18/RA2 |
| J1 | AN3/C2IN1+/VPIO/RPI35/RB3 |
| J2 | AN2/C2IN2-/VMIO/RPI34/RB2 |
| J3 | PGED1/AN7/RCV/RPI39/RB7 |
| J4 | AVDD |
| J5 | AN11/PMA12/RPI43/RB11 |
| J6 | TCK/RPI17/RA1 |
| J7 | AN12/PMA11/RPI44/RB12 |

**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

**4:** The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

**5:** The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.


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**TABLE 2: PIN NAMES: dsPIC33EP256MU810 AND dsPIC33EP512MU810 DEVICES(1,2) (CONTINUED)**

| Pin Number | Full Pin Name | Pin Number | Full Pin Name |
|---|---|---|---|
| E1 | AN19/PWM6H/RPI52/RC4 | J8 | No Connect |
| E2 | AN18/PWM6L/RPI51/RC3 | J9 | No Connect |
| E3 | C1IN3-/SCK2/PMA5/RP118/RG6 | J10 | RP104/RF8 |
| E4 | AN17/PWM5H/RPI50/RC2 | J11 | D-/RG3(5) |
| E5 | No Connect | K1 | PGEC3/AN1/RPI33/RB1 |
| E6 | RP113/RG1 | K2 | PGED3/AN0/RPI32/RB0 |
| E7 | No Connect | K3 | VREF+/RA10 |
| K4 | AN8/PMA6/RPI40/RB8 | L3 | AVSS |
| K5 | No Connect | L4 | AN9/PMA7//RPI41/RB9 |
| K6 | RP108/RF12 | L5 | AN10/CVREF/PMA13/RPI42/RB10 |
| K7 | AN14/PMA1/RPI46/RB14 | L6 | RP109/RF13 |
| K8 | VDD | L7 | AN13/PMA10/RPI45/RB13 |
| K9 | RP79/RD15 | L8 | AN15/PMA0/RPI47/RB15 |
| K10 | USBID/RP99/RF3 | L9 | RPI78/RD14 |
| K11 | RP98/RF2 | L10 | SDA2(3)/PMA9/RP100/RF4 |
| L1 | PGEC1/AN6/RPI38/RB6 | L11 | SCL2(3)/PMA8/RP101/RF5 |
| L2 | VREF-/RA9 | | |

**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

**4:** The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

**5:** The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

## Pin Diagrams (Continued)

**121-Pin TFBGA(1)**

● = Pins are up to 5V tolerant

**PIC24EP256GU810**
**PIC24EP512GU810**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | RE4 | RE3 | RG13 | RE0 | RG0 | RF1 | VDD | NC | RD12 | RD2 | RD1 |
| B | NC | RG15 | RE2 | RE1 | RA7 | RF0 | VCAP | RD5 | RD3 | VSS | RC14 |
| C | RE6 | VDD | RG12 | RG14 | RA6 | NC | RD7 | RD4 | NC | RC13 | RD11 |
| D | RC1 | RE7 | RE5 | NC | NC | NC | RD6 | RD13 | RD0 | NC | RD10 |
| E | RC4 | RC3 | RG6 | RC2 | NC | RG1 | NC | RA15 | RD8 | RD9 | RA14 |
| F | $\overline{\text{MCLR}}$ | RG8 | RG9 | RG7 | VSS | NC | NC | VDD | RC12 | VSS | RC15 |
| G | RE8 | RE9 | RA0 | NC | VDD | VSS | VSS | NC | RA5 | RA3 | RA4 |
| H | RB5 | RB4 | NC | NC | NC | VDD | NC | VBUS | VUSB3V3 | RG2 | RA2 |
| J | RB3 | RB2 | RB7 | AVDD | RB11 | RA1 | RB12 | NC | NC | RF8 | RG3 |
| K | RB1 | RB0 | RA10 | RB8 | NC | RF12 | RB14 | VDD | RD15 | RF3 | RF2 |
| L | RB6 | RA9 | AVSS | RB9 | RB10 | RF13 | RB13 | RB15 | RD14 | RF4 | RF5 |

**Note 1:** Refer to Table 3 for full pin names.


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**TABLE 3: PIN NAMES: PIC24EP256GU810 AND PIC24EP512GU810 DEVICES(1,2)**

| Pin Number | Full Pin Name |
|---|---|
| A1 | AN28/PMD4/RP84/RE4 |
| A2 | AN27/PMD3/RPI83/RE3 |
| A3 | RP125/RG13 |
| A4 | AN24/PMD0/RP80/RE0 |
| A5 | RP112/RG0 |
| A6 | VCMPST2/RP97/RF1 |
| A7 | VDD |
| A8 | No Connect |
| A9 | RPI76/RD12 |
| A10 | DPH/RP66/RD2 |
| A11 | VCPCON/RP65/RD1 |
| B1 | No Connect |
| B2 | RP127/RG15 |
| B3 | AN26/PMD2/RP82/RE2 |
| B4 | AN25/PMD1/RPI81/RE1 |
| B5 | AN23/RPI23/RA7 |
| B6 | VCMPST1/RP96/RF0 |
| B7 | VCAP |
| B8 | PMRD/RP69/RD5 |
| B9 | PMBE/RP67/RD3 |
| B10 | VSS |
| B11 | PGEC2/SOSCO/C3IN1-/T1CK/RPI62/RC14 |
| C1 | AN30/PMD6/RPI86/RE6 |
| C2 | VDD |
| C3 | RPI124/RG12 |
| C4 | RP126/RG14 |
| C5 | AN22/RPI22/RA6 |
| C6 | No Connect |
| C7 | C3IN1+/VCMPST3/RP71/RD7 |
| C8 | PMWR/RP68/RD4 |
| C9 | No Connect |
| C10 | PGED2/SOSCI/C3IN3-/RPI61/RC13 |
| C11 | PMCS1/RPI75/RD11 |
| D1 | AN16/RPI49/RC1 |
| D2 | AN31/PMD7/RP87/RE7 |
| D3 | AN29/PMD5/RP85/RE5 |
| D4 | No Connect |
| D5 | No Connect |
| D6 | No Connect |
| D7 | C3IN2-/RP70/RD6 |
| D8 | RPI77/RD13 |
| D9 | INT0/DMH/RP64/RD0 |
| D10 | No Connect |
| D11 | ASCL1(3)/PMCS2/RPI74/RD10 |

| Pin Number | Full Pin Name |
|---|---|
| E8 | RPI31/RA15 |
| E9 | RTCC/DMLN/RPI72/RD8 |
| E10 | ASDA1(3)/DPLN/RPI73/RD9 |
| E11 | RPI30/RA14 |
| F1 | $\overline{\text{MCLR}}$ |
| F2 | C2IN3-/SDO2/PMA3/RP120/RG8 |
| F3 | C2IN1-/PMA2/RPI121/RG9 |
| F4 | C1IN1-/SDI2/PMA4/RPI119/RG7 |
| F5 | VSS |
| F6 | No Connect |
| F7 | No Connect |
| F8 | VDD |
| F9 | OSC1/RPI60/RC12 |
| F10 | VSS |
| F11 | OSC2/CLKO/RC15 |
| G1 | AN20/RPI88/RE8 |
| G2 | AN21/RPI89/RE9 |
| G3 | TMS/RPI16/RA0 |
| G4 | No Connect |
| G5 | VDD |
| G6 | VSS |
| G7 | VSS |
| G8 | No Connect |
| G9 | TDO/RPI21/RA5 |
| G10 | ASDA2(3)/RPI19/RA3 |
| G11 | TDI/RPI20/RA4 |
| H1 | AN5/C1IN1+/VBUSON/VBUSST/RPI37/RB5 |
| H2 | AN4/C1IN2-/USBOEN/RPI36/RB4 |
| H3 | No Connect |
| H4 | No Connect |
| H5 | No Connect |
| H6 | VDD |
| H7 | No Connect |
| H8 | VBUS |
| H9 | VUSB3V3 |
| H10 | D+/RG2(4) |
| H11 | ASCL2(3)/RPI18/RA2 |
| J1 | AN3/C2IN1+/VPIO/RPI35/RB3 |
| J2 | AN2/C2IN2-/VMIO/RPI34/RB2 |
| J3 | PGED1/AN7/RCV/RPI39/RB7 |
| J4 | AVDD |
| J5 | AN11/PMA12/RPI43/RB11 |
| J6 | TCK/RPI17/RA1 |
| J7 | AN12/PMA11/RPI44/RB12 |

**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

**4:** The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

**5:** The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

**TABLE 3: PIN NAMES: PIC24EP256GU810 AND PIC24EP512GU810 DEVICES(1,2) (CONTINUED)**

| Pin Number | Full Pin Name |
|---|---|
| E1 | AN19/RPI52/RC4 |
| E2 | AN18/RPI51/RC3 |
| E3 | C1IN3-/SCK2/PMA5/RP118/RG6 |
| E4 | AN17/RPI50/RC2 |
| E5 | No Connect |
| E6 | RP113/RG1 |
| E7 | No Connect |
| K4 | AN8/PMA6/RPI40/RB8 |
| K5 | No Connect |
| K6 | RP108/RF12 |
| K7 | AN14/PMA1/RPI46/RB14 |
| K8 | VDD |
| K9 | RP79/RD15 |
| K10 | USBID/RP99/RF3 |
| K11 | RP98/RF2 |
| L1 | PGEC1/AN6/RPI38/RB6 |
| L2 | VREF-/RA9 |

| Pin Number | Full Pin Name |
|---|---|
| J8 | No Connect |
| J9 | No Connect |
| J10 | RP104/RF8 |
| J11 | D-/RG3(5) |
| K1 | PGEC3/AN1/RPI33/RB1 |
| K2 | PGED3/AN0/RPI32/RB0 |
| K3 | VREF+/RA10 |
| L3 | AVSS |
| L4 | AN9/PMA7/RPI41/RB9 |
| L5 | AN10/CVREF/PMA13/RPI42/RB10 |
| L6 | RP109/RF13 |
| L7 | AN13/PMA10/RPI45/RB13 |
| L8 | AN15/PMA0/RPI47/RB15 |
| L9 | RPI78/RD14 |
| L10 | SDA2(3)/PMA9/RP100/RF4 |
| L11 | SCL2(3)/PMA8/RP101/RF5 |

**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as change notification (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

**4:** The pin name is SCL1/RG2 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.

**5:** The pin name is SDA1/RG3 for the dsPIC33EP512(GP/MC)806 and PIC24EP512GP806 devices.


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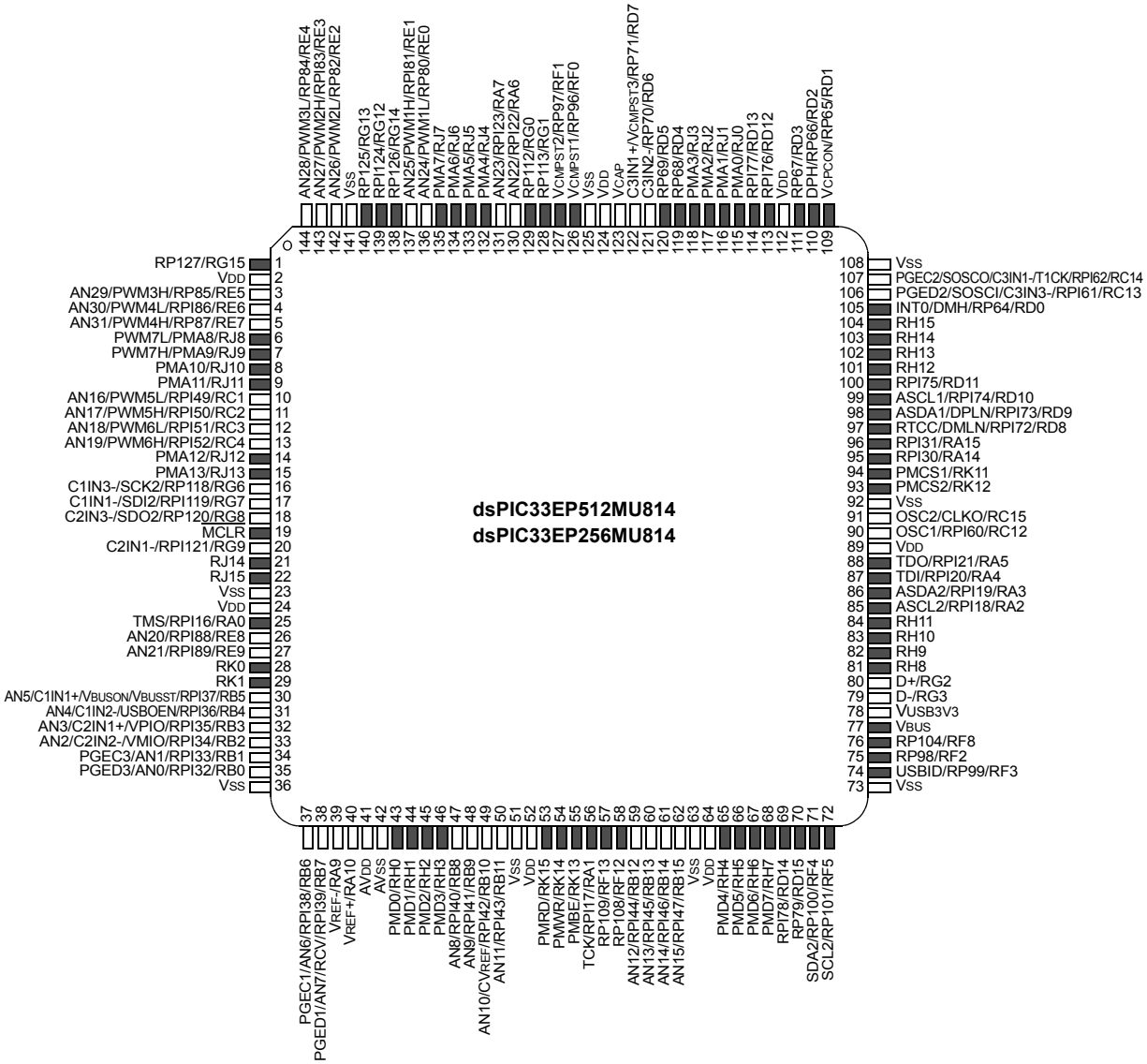
## Pin Diagrams (Continued)

**144-Pin TQFP, 144-pin LQFP**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

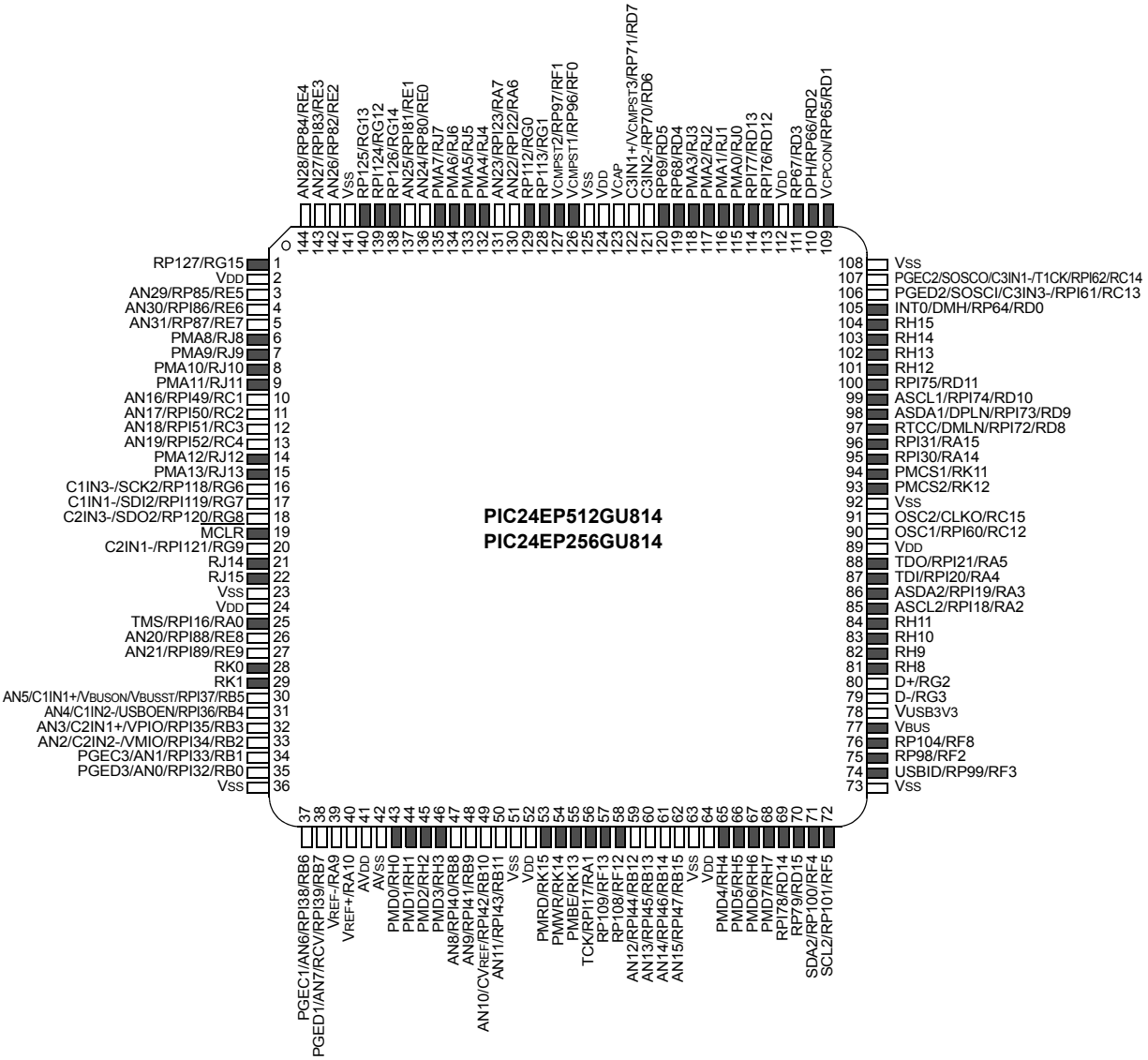
**2:** Every I/O port pin (RAx-RKx) can be used as change notification (CNAx-CNKx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

## Pin Diagrams (Continued)

**144-Pin TQFP, 144-pin LQFP**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RKx) can be used as change notification (CNAx-CNKx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.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## Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33E/PIC24E Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

**Note:** To access the documents listed below, browse to the documentation section of the dsPIC33EP512MU814 product page on the Microchip web site (www.microchip.com).

In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310#1

- **Section 1. "Introduction"** (DS70573)
- **Section 2. "CPU"** (DS70359)
- **Section 3. "Data Memory"** (DS70595)
- **Section 4. "Program Memory"** (DS70613)
- **Section 5. "Flash Programming"** (DS70609)
- **Section 6. "Interrupts"** (DS70600)
- **Section 7. "Oscillator"** (DS70580)
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- **Section 12. "Input Capture"** (DS70352)
- **Section 13. "Output Compare"** (DS70358)
- **Section 14. "High-Speed PWM"** (DS70645)
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- **Section 16. "Analog-to-Digital Converter (ADC)"** (DS70621)
- **Section 17. "UART"** (DS70582)
- **Section 18. "Serial Peripheral Interface (SPI)"** (DS70569)
- **Section 19. "Inter-Integrated Circuit™ ($I^2C$™)"** (DS70330)
- **Section 20. "Data Converter Interface (DCI)"** (DS70356)
- **Section 21. "Enhanced Controller Area Network (ECAN™)"** (DS70353)
- **Section 22. "Direct Memory Access (DMA)"** (DS70348)
- **Section 23. "CodeGuard™ Security"** (DS70634)
- **Section 24. "Programming and Diagnostics"** (DS70608)
- **Section 25. "USB On-The-Go (OTG)"** (DS70571)
- **Section 26. "Op Amp/Comparator"** (DS70357)
- **Section 27. "Programmable Cyclic Redundancy Check (CRC)"** (DS70346)
- **Section 28. "Parallel Master Port (PMP)"** (DS70576)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS70584)
- **Section 30. "Device Configuration"** (DS70618)

**NOTES:**


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# 1.0 DEVICE OVERVIEW

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com)

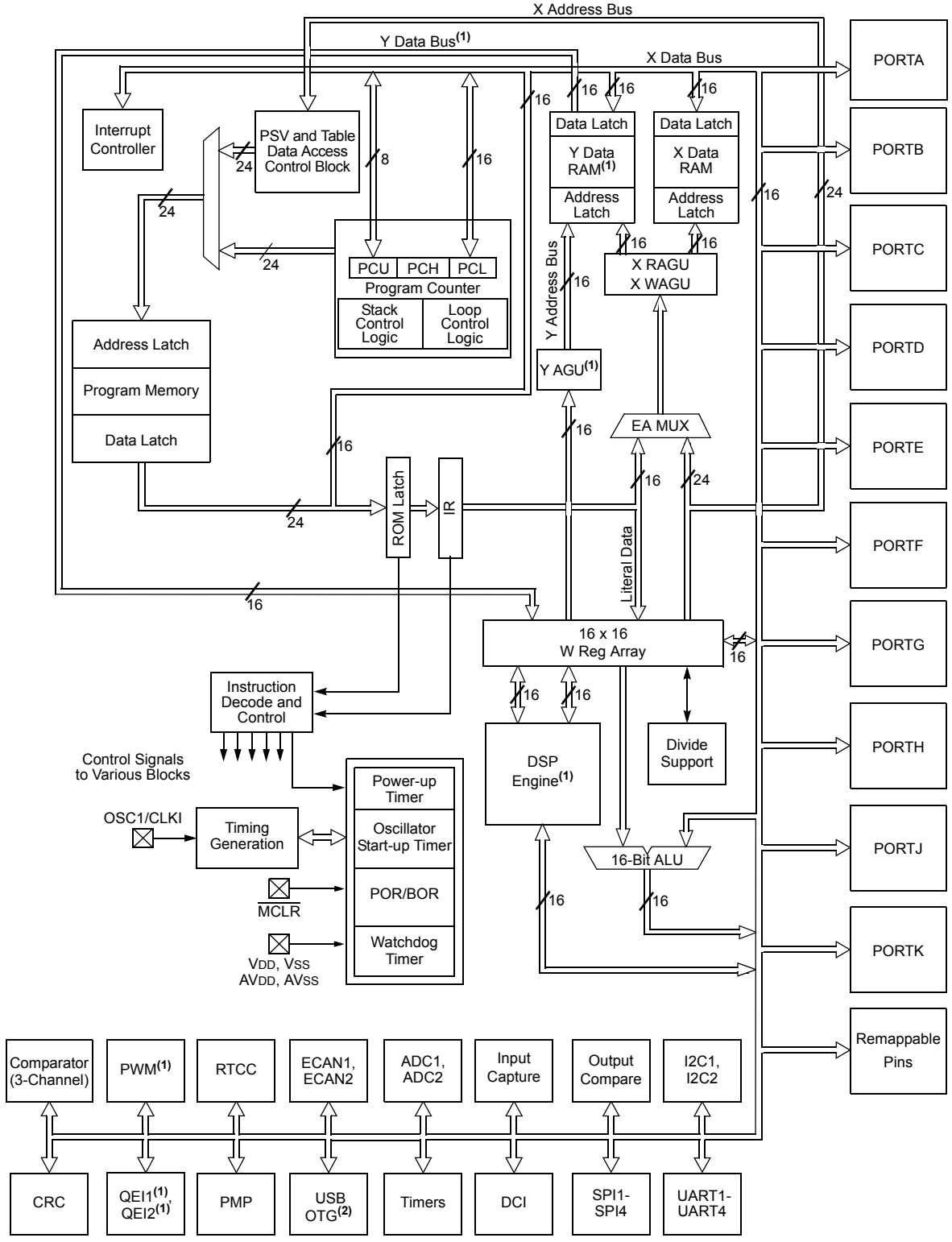
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 Digital Signal Controller (DSC) and Microcontroller (MCU) devices. The dsPIC33EPXXX(GP/MC/MU)806/810/814 devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance 16-bit MCU architecture.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 BLOCK DIAGRAM**




**Note 1:** This feature or peripheral is only available on dsPIC33EPXXX(MC/MU)806/810/814 devices.

**2:** This feature or peripheral is only available on dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU806/810/814 devices.


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**TABLE 1-1: PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| AN0-AN31 | I | Analog | No | Analog input channels. |
| CLKI | I | ST/ CMOS | No | External clock source input. Always associated with OSC1 pin function. |
| CLKO | O | — | No | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function. |
| OSC1 | I | ST/ CMOS | No | Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. |
| OSC2 | I/O | — | No | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. |
| SOSCI | I | ST/ CMOS | No | 32.768 kHz low-power oscillator crystal input; CMOS otherwise. |
| SOSCO | O | — | No | 32.768 kHz low-power oscillator crystal output. |
| IC1-IC16 | I | ST | Yes | Capture Inputs 1 through 16. |
| OCFA | I | ST | Yes | Compare Fault A input (for Compare channels). |
| OCFB | I | ST | Yes | Compare Fault B input (for Compare channels). |
| OCFC | I | ST | Yes | Compare Fault C input (for Compare channels). |
| OC1-OC16 | O | — | Yes | Compare Outputs 1 through 16. |
| INT0 | I | ST | No | External Interrupt 0. |
| INT1 | I | ST | Yes | External Interrupt 1. |
| INT2 | I | ST | Yes | External Interrupt 2. |
| INT3 | I | ST | Yes | External Interrupt 3. |
| INT4 | I | ST | Yes | External Interrupt 4. |
| RA0-RA7, RA9, RA10, RA14, RA15 | I/O | ST | No | PORTA is a bidirectional I/O port. |
| RB0-RB15 | I/O | ST | No | PORTB is a bidirectional I/O port. |
| RC1-RC4, RC12-RC15 | I/O | ST | No | PORTC is a bidirectional I/O port. |
| RD0-RD15 | I/O | ST | No | PORTD is a bidirectional I/O port. |
| RE0-RE9 | I/O | ST | No | PORTE is a bidirectional I/O port. |
| RF0-RF6, RF8 RF12, RF13 | I/O | ST | No | PORTF is a bidirectional I/O port. |
| RG0, RG1 | I/O | ST | No | PORTG is a bidirectional I/O port. |
| RG2, RG3(3) | I/O | ST | No | PORTG is a bidirectional I/O port. |
| RG6-RG9, RG12-RG15 | I/O | ST | No | PORTG is a bidirectional I/O port. |
| RH0-RH15 | I/O | ST | No | PORTH is a bidirectional I/O port. |
| RJ0-RJ15 | I/O | ST | No | PORTJ is a bidirectional I/O port. |
| RK0-RK1, RK11-RK15 | I/O | ST | No | PORTK is a bidirectional I/O port. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

**Note 1:** This pin is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**2:** AVDD must be connected at all times.

**3:** These pins are input only on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

**4:** These pins are only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

**5:** The availability of $I^2C$™ interfaces varies by device. Refer to the **"Pin Diagrams"** section for availability. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

**6:** Analog functionality is activated by enabling the USB module and is not controlled by the ANSEL register.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| T1CK | I | ST | No | Timer1 external clock input. |
| T2CK | I | ST | Yes | Timer2 external clock input. |
| T3CK | I | ST | Yes | Timer3 external clock input. |
| T4CK | I | ST | Yes | Timer4 external clock input. |
| T5CK | I | ST | Yes | Timer5 external clock input. |
| T6CK | I | ST | Yes | Timer6 external clock input. |
| T7CK | I | ST | Yes | Timer7 external clock input. |
| T8CK | I | ST | Yes | Timer8 external clock input. |
| T9CK | I | ST | Yes | Timer9 external clock input. |
| $\overline{U1CTS}$ | I | ST | Yes | UART1 Clear-to-Send. |
| $\overline{U1RTS}$ | O | — | Yes | UART1 Ready-to-Send. |
| U1RX | I | ST | Yes | UART1 receive. |
| U1TX | O | — | Yes | UART1 transmit. |
| $\overline{U2CTS}$ | I | ST | Yes | UART2 Clear-to-Send. |
| $\overline{U2RTS}$ | O | — | Yes | UART2 Ready-to-Send. |
| U2RX | I | ST | Yes | UART2 receive. |
| U2TX | O | — | Yes | UART2 transmit. |
| $\overline{U3CTS}$ | I | ST | Yes | UART3 Clear-to-Send. |
| $\overline{U3RTS}$ | O | — | Yes | UART3 Ready-to-Send. |
| U3RX | I | ST | Yes | UART3 receive. |
| U3TX | O | — | Yes | UART3 transmit. |
| $\overline{U4CTS}$ | I | ST | Yes | UART4 Clear-to-Send. |
| $\overline{U4RTS}$ | O | — | Yes | UART4 Ready-to-Send. |
| U4RX | I | ST | Yes | UART4 receive. |
| U4TX | O | — | Yes | UART4 transmit. |
| SCK1 | I/O | ST | Yes | Synchronous serial clock input/output for SPI1. |
| SDI1 | I | ST | Yes | SPI1 data in. |
| SDO1 | O | — | Yes | SPI1 data out. |
| $\overline{SS1}$ | I/O | ST | Yes | SPI1 slave synchronization or frame pulse I/O. |
| SCK2 | I/O | ST | No | Synchronous serial clock input/output for SPI2. |
| SDI2 | I | ST | No | SPI2 data in. |
| SDO2 | O | — | No | SPI2 data out. |
| $\overline{SS2}$ | I/O | ST | Yes | SPI2 slave synchronization or frame pulse I/O. |
| SCK3 | I/O | ST | Yes | Synchronous serial clock input/output for SPI3. |
| SDI3 | I | ST | Yes | SPI3 data in. |
| SDO3 | O | — | Yes | SPI3 data out. |
| $\overline{SS3}$ | I/O | ST | Yes | SPI3 slave synchronization or frame pulse I/O. |
| SCK4 | I/O | ST | Yes | Synchronous serial clock input/output for SPI4. |
| SDI4 | I | ST | Yes | SPI4 data in. |
| SDO4 | O | — | Yes | SPI4 data out. |
| $\overline{SS4}$ | I/O | ST | Yes | SPI4 slave synchronization or frame pulse I/O. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

**Note 1:** This pin is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**2:** AVDD must be connected at all times.

**3:** These pins are input only on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

**4:** These pins are only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

**5:** The availability of $I^2C$™ interfaces varies by device. Refer to the **"Pin Diagrams"** section for availability. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

**6:** Analog functionality is activated by enabling the USB module and is not controlled by the ANSEL register.


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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| SCL1(5) | I/O | ST | No | Synchronous serial clock input/output for I2C1. |
| SDA1(5) | I/O | ST | No | Synchronous serial data input/output for I2C1. |
| ASCL1(5) | I/O | ST | No | Alternate synchronous serial clock input/output for I2C1. |
| ASDA1(5) | I/O | ST | No | Alternate synchronous serial data input/output for I2C1. |
| SCL2(5) | I/O | ST | No | Synchronous serial clock input/output for I2C2. |
| SDA2(5) | I/O | ST | No | Synchronous serial data input/output for I2C2. |
| ASCL2(5) | I/O | ST | No | Alternate synchronous serial clock input/output for I2C2. |
| ASDA2(5) | I/O | ST | No | Alternate synchronous serial data input/output for I2C2. |
| TMS | I | ST | No | JTAG Test mode select pin. |
| TCK | I | ST | No | JTAG test clock input pin. |
| TDI | I | ST | No | JTAG test data input pin. |
| TDO | O | — | No | JTAG test data output pin. |
| INDX1(1) | I | ST | Yes | Quadrature Encoder Index1 pulse input. |
| HOME1(1) | I | ST | Yes | Quadrature Encoder Home1 pulse input. |
| QEA1(1) | I | ST | Yes | Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer external clock input in Timer mode. |
| QEB1(1) | I | ST | Yes | Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer external gate input in Timer mode. |
| CNTCMP1(1) | O | — | Yes | Quadrature Encoder Compare Output 1. |
| INDX2(1) | I | ST | Yes | Quadrature Encoder Index2 pulse input. |
| HOME2(1) | I | ST | Yes | Quadrature Encoder Home2 pulse input. |
| QEA2(1) | I | ST | Yes | Quadrature Encoder Phase A input in QEI2 mode. Auxiliary timer external clock input in Timer mode. |
| QEB2(1) | I | ST | Yes | Quadrature Encoder Phase B input in QEI2 mode. Auxiliary timer external gate input in Timer mode. |
| CNTCMP2(1) | O | — | Yes | Quadrature Encoder Compare Output 2. |
| COFS | I/O | ST | Yes | Data Converter Interface frame synchronization pin. |
| CSCK | I/O | ST | Yes | Data Converter Interface serial clock input/output pin. |
| CSDI | I | ST | Yes | Data Converter Interface serial data input pin. |
| CSDO | O | — | Yes | Data Converter Interface serial data output pin. |
| C1RX | I | ST | Yes | ECAN1 bus receive pin. |
| C1TX | O | — | Yes | ECAN1 bus transmit pin. |
| C2RX | I | ST | Yes | ECAN2 bus receive pin. |
| C2TX | O | — | Yes | ECAN2 bus transmit pin. |
| RTCC | O | — | No | Real-Time Clock alarm output. |
| CVREF | O | Analog | No | Comparator voltage reference output. |
| C1IN1+, C1IN2-, C1IN1-, C1IN3- | I | Analog | No | Comparator 1 inputs |
| C1OUT | O | — | Yes | Comparator 1 output. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

**Note 1:** This pin is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**2:** AVDD must be connected at all times.

**3:** These pins are input only on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

**4:** These pins are only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

**5:** The availability of I2C™ interfaces varies by device. Refer to the **"Pin Diagrams"** section for availability. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

**6:** Analog functionality is activated by enabling the USB module and is not controlled by the ANSEL register.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| C2IN1+, C2IN2-, C2IN1-, C2IN3- | I | Analog | No | Comparator 2 inputs. |
| C2OUT | O | — | Yes | Comparator 2 output. |
| C3IN1+, C3IN2-, C2IN1-, C3IN3- | I | Analog | No | Comparator 3 inputs. |
| C3OUT | O | — | Yes | Comparator 3 output. |
| PMA0 | I/O | TTL/ST | No | Parallel Master Port Address Bit 0 input (Buffered Slave modes) and output (Master modes). |
| PMA1 | I/O | TTL/ST | No | Parallel Master Port Address Bit 1 input (Buffered Slave modes) and output (Master modes). |
| PMA2 -PMA13 | O | — | No | Parallel Master Port Address Bits 2-13 (Demultiplexed Master modes). |
| PMBE | O | — | No | Parallel Master Port byte enable strobe. |
| PMCS1, PMCS2 | O | — | No | Parallel Master Port Chip Select 1 and 2 strobe. |
| PMD0-PMD7 | I/O | TTL/ST | No | Parallel Master Port data (Demultiplexed Master mode) or address/data (Multiplexed Master modes). |
| PMRD | O | — | No | Parallel Master Port read strobe. |
| PMWR | O | — | No | Parallel Master Port write strobe. |
| $\overline{FLT1}$-$\overline{FLT7}$(1) | I | ST | Yes | PWM Fault Input 1 through 7. |
| DTCMP1-DTCMP7(1) | I | ST | Yes | PWM dead-time compensation input. |
| PWM1L-PWM7L(1) | O | — | No | PWM Low Output 1 through 7. |
| PWM1H-PWM7H(1) | O | — | No | PWM High Output 1 through 7. |
| SYNCI1, SYNCI2(1) | I | ST | Yes | PWM Synchronization Inputs 1 and 2. |
| SYNCO1, SYNCO2(1) | O | — | Yes | PWM Synchronization Outputs 1 and 2. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

**Note 1:** This pin is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**2:** AVDD must be connected at all times.

**3:** These pins are input only on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

**4:** These pins are only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

**5:** The availability of $I^2C$™ interfaces varies by device. Refer to the **"Pin Diagrams"** section for availability. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

**6:** Analog functionality is activated by enabling the USB module and is not controlled by the ANSEL register.


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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| VBUS(4,6) | I | Analog | No | USB bus power monitor. |
| VUSB3V3(4) | P | — | No | USB internal transceiver supply. If the USB module is not being used, this pin must be connected to VDD. |
| VBUSON(4) | O | — | No | USB host and On-The-Go (OTG) bus power control output. |
| D+(4,6) | I/O | Analog | No | D+ pin of internal USB transceiver. |
| D-(4,6) | I/O | Analog | No | D- pin of internal USB transceiver. |
| USBID(4) | I | ST | No | USB OTG ID detect. |
| USBOEN(4) | O | — | No | USB output enabled control (for external transceiver). |
| VBUSST(4) | I | ST | No | USB boost controller overcurrent detection. |
| VCPCON(4) | O | — | No | USB boost controller PWM signal. |
| VCMPST1(4) | I | ST | No | USB External Comparator 1 input. |
| VCMPST2(4) | I | ST | No | USB External Comparator 2 input. |
| VCMPST3(4) | I | ST | No | USB External Comparator 3 input. |
| VMIO(4) | I/O | ST | No | USB differential minus input/output (external transceiver). |
| VPIO(4) | I/O | ST | No | USB differential plus input/output (external transceiver). |
| DMH(4) | O | — | No | D- external pull-up control output. |
| DPH(4) | O | — | No | D+ external pull-up control output. |
| DMLN(4) | O | — | No | D- external pull-down control output. |
| DPLN(4) | O | — | No | D+ External Pull-down Control Output. |
| RCV(4) | I | ST | No | USB receive input (from external transceiver). |
| PGED1 | I/O | ST | No | Data I/O pin for Programming/Debugging Communication Channel 1. |
| PGEC1 | I | ST | No | Clock input pin for Programming/Debugging Communication Channel 1. |
| PGED2 | I/O | ST | No | Data I/O pin for Programming/Debugging Communication Channel 2. |
| PGEC2 | I | ST | No | Clock input pin for Programming/Debugging Communication Channel 2. |
| PGED3 | I/O | ST | No | Data I/O pin for Programming/Debugging Communication Channel 3. |
| PGEC3 | I | ST | No | Clock input pin for Programming/Debugging Communication Channel 3. |
| $\overline{MCLR}$ | I/P | ST | No | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| AVDD(2) | P | P | No | Positive supply for analog modules. This pin must be connected at all times. |
| AVSS | P | P | No | Ground reference for analog modules. |
| VDD | P | — | No | Positive supply for peripheral logic and I/O pins. |
| VCAP | P | — | No | CPU logic filter capacitor connection. |
| VSS | P | — | No | Ground reference for logic and I/O pins. |
| VREF+ | I | Analog | No | Analog voltage reference (high) input. |
| VREF- | I | Analog | No | Analog voltage reference (low) input. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

**Note 1:** This pin is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**2:** AVDD must be connected at all times.

**3:** These pins are input only on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

**4:** These pins are only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

**5:** The availability of $I^2C$™ interfaces varies by device. Refer to the **"Pin Diagrams"** section for availability. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.

**6:** Analog functionality is activated by enabling the USB module and is not controlled by the ANSEL register.

**NOTES:**


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# 2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS AND MICROCONTROLLERS

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com)

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

## 2.1 Basic Connection Requirements

Getting started with the 16-bit DSCs and microcontrollers requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used) (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used (see **Section 2.6 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VUSB3V3 pin is used when utilizing the USB module. If the USB module is not used, VUSB3V3 must be connected to VDD.
- VREF+/VREF- pin is used when external voltage reference for ADC module is implemented

**Note:** The AVDD and AVSS pins must be connected independent of the ADC voltage reference source. The voltage difference between AVDD and VDD cannot exceed 300 mV at any time during operation or start-up.

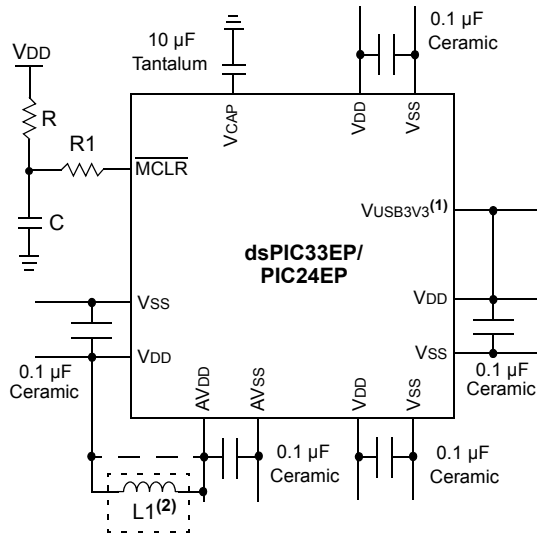
## 2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, VUSB3V3, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

**FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION**




**Note 1:** If the USB module is not used, VUSB3V3 must be connected to VDD, as shown.

**2:** As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{FCNV}{2}$$ (i.e., ADC conversion rate/2)

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

### 2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

## 2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor greater than 4.7 µF (10 µF is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 32.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 29.2 "On-Chip Voltage Regulator"** for details.

## 2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

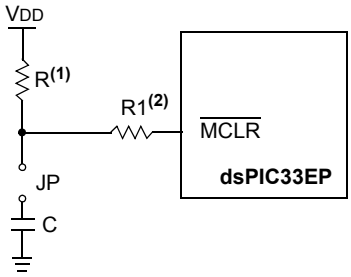
- Device Reset
- Device Programming and Debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

**FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS**




**Note 1:** R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

**2:** R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.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## 2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high ($V_{IH}$) and input low ($V_{IL}$) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICkit™ 3, MPLAB ICD 3, or MPLAB REAL ICE™.

For more information on MPLAB ICD 3 and MPLAB REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

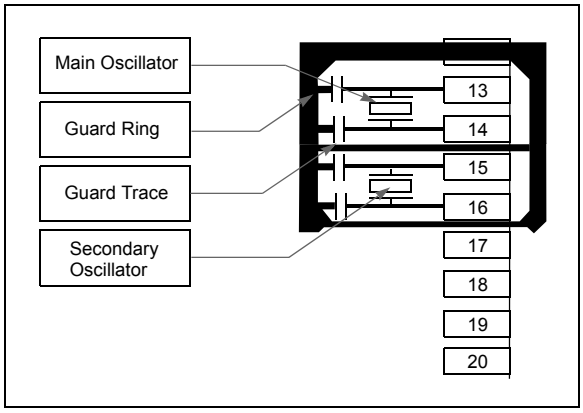
- *"Using MPLAB® ICD 3"* (poster) DS51765
- *"MPLAB® ICD 3 Design Advisory"* DS51764
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* DS51616
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) DS51749

## 2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For details, see **Section 9.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

**FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT**




## 2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 3 MHz < $F_{IN}$ < 5.5 MHz to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLDBF to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

## 2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic-low state.

Alternatively, connect a 1k to 10k resistor between $V_{SS}$ and unused pins and drive the output to logic low.

## 2.9 Application Examples

- Induction heating
- Uninterruptable Power Supplies (UPS)
- DC/AC inverters
- Compressor motor control
- Washing machine 3-phase motor control
- BLDC motor control
- Automotive HVAC, cooling fans, fuel pumps
- Stepper motor control
- Audio and fluid sensor monitoring
- Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- Consumer audio
- Industrial and building control (security systems and access control)
- Barcode reading
- Networking: LAN switches, gateways
- Data storage device management
- Smart cards and smart card readers

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

**FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION**

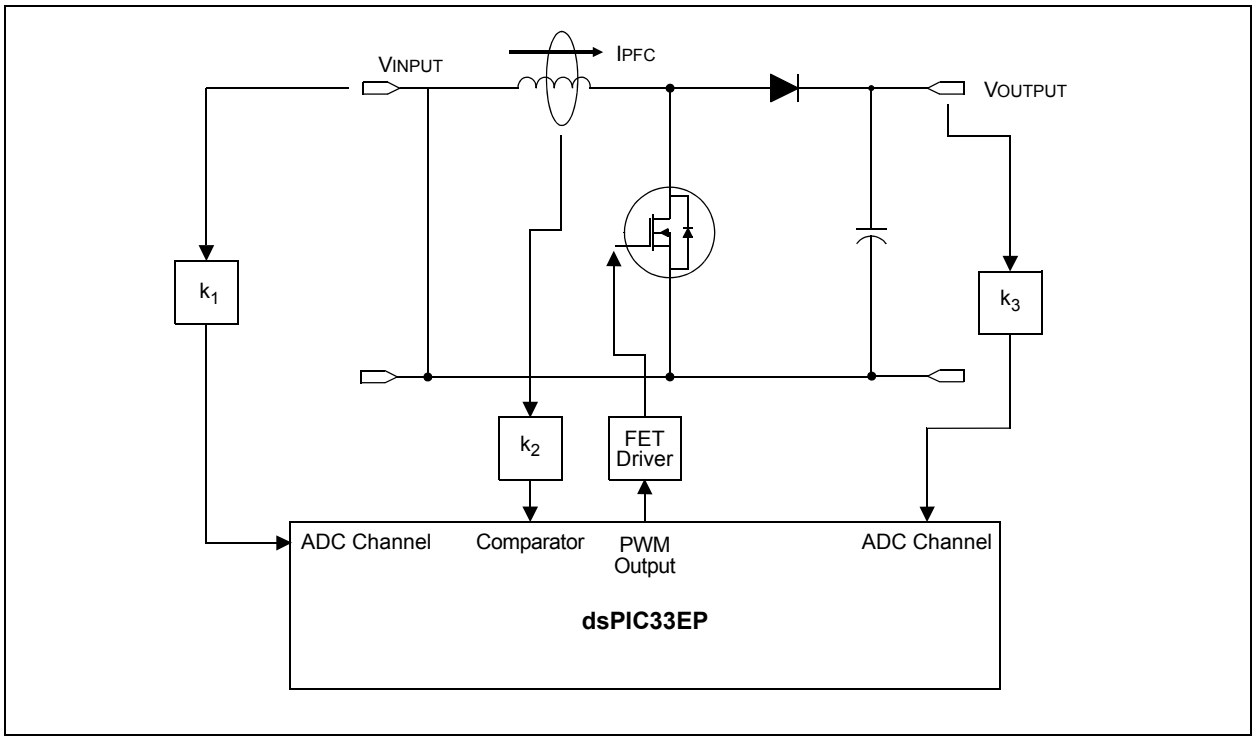




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**FIGURE 2-5: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER**

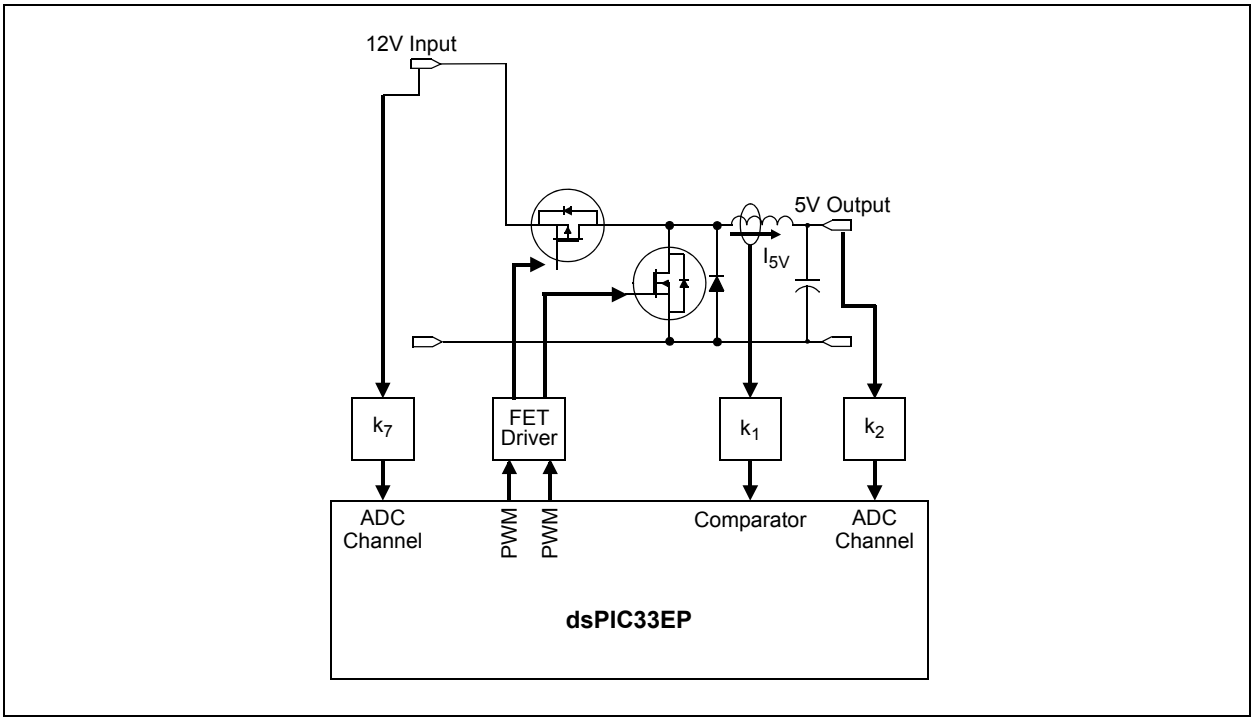



**FIGURE 2-6: MULTI-PHASE SYNCHRONOUS BUCK CONVERTER**

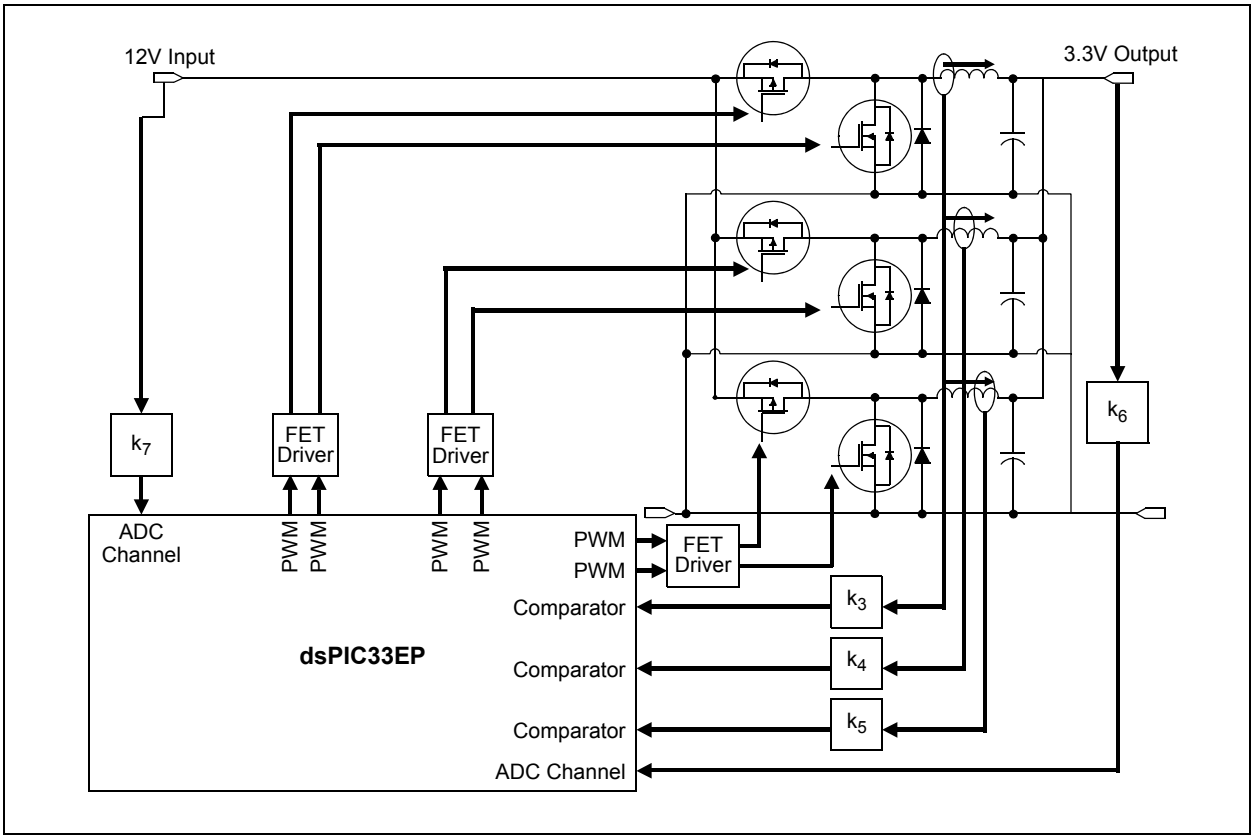


**FIGURE 2-7: INTERLEAVED PFC**

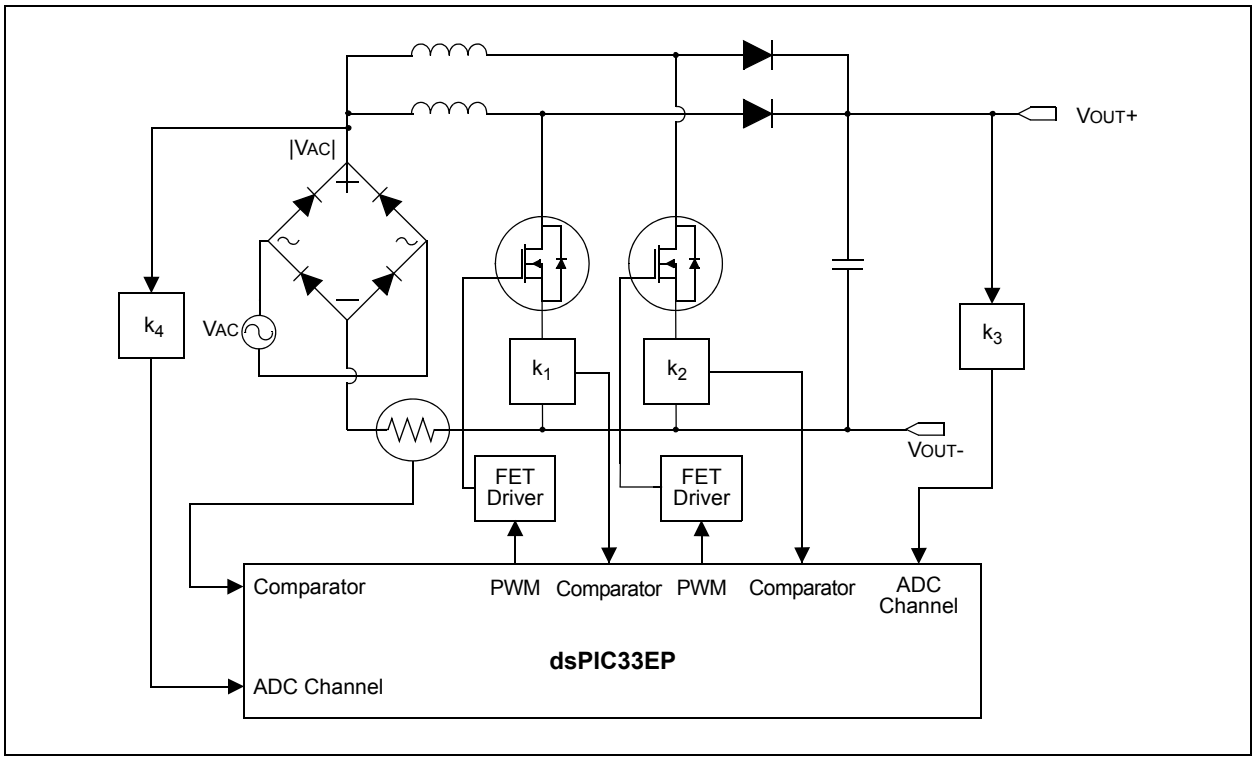
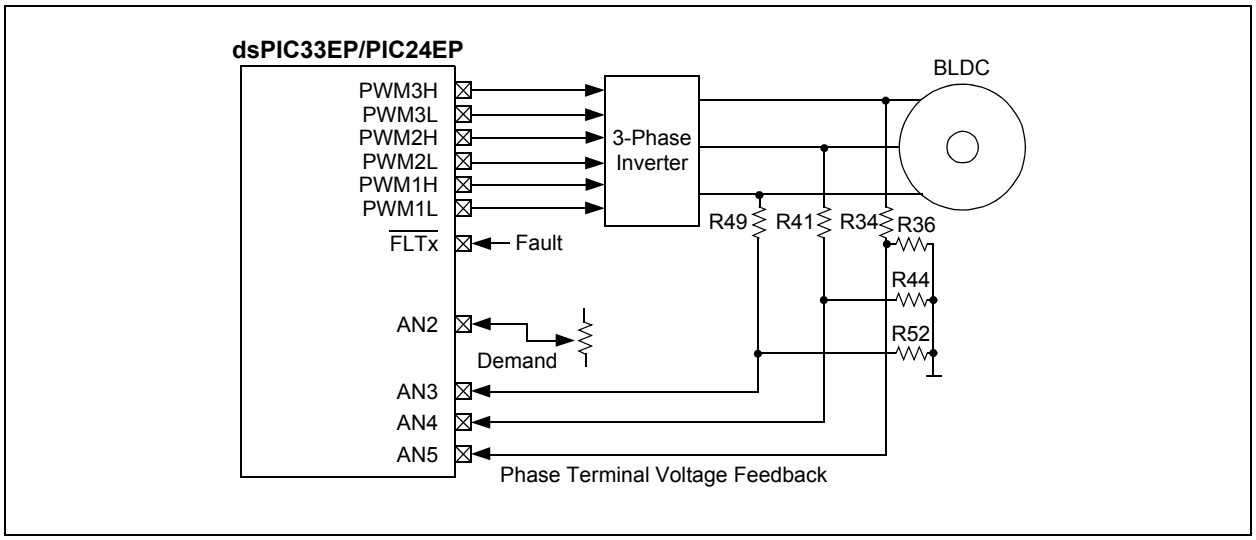



**FIGURE 2-8: BEMF VOLTAGE MEASURED USING THE ADC MODULE**





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# 3.0 CPU

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "CPU"** (DS70359) in the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word, with a variable length opcode field. The Program Counter (PC) is 24 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction, PSV accesses and the table instructions. Overhead free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

## 3.1 Registers

Devices have sixteen 16-bit working registers in the programmer's model. Each of the working registers can act as a Data, Address or Address Offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls. The working registers, W0 through W3, and selected bits from the STATUS register, have shadow registers for fast context saves and restores using a single `POP.S` or `PUSH.S` instruction.

## 3.2 Instruction Set

The dsPIC33EPXXXMU806/810/814 instruction set has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The PIC24EPXXX(GP/GU)810/814 instruction set has the MCU class of instructions and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

## 3.3 Data Space Addressing

The Base Data Space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operate solely through the X memory AGU, which accesses the entire memory map as one linear data space. On dsPIC33EPXXX(GP/MC/MU)806/810/814 devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

The upper 32 Kbytes of the data space memory map can optionally be mapped into Program Space at any 16K program word boundary. The program-to-data space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were data space. Moreover, the Base Data Space address is used in conjunction with a read or write page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to **Section 3. "Data Memory"** (DS70595) and **Section 4. "Program Memory"** (DS70613) in the *"dsPIC33E/PIC24E Family Reference Manual"* for more details on EDS, PSV and table accesses.

On dsPIC33EPXXX(GP/MC/MU)806/810/814 devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms. PIC24EPXXX(GP/GU)810/814 devices do not support Modulo and Bit-Reversed Addressing.

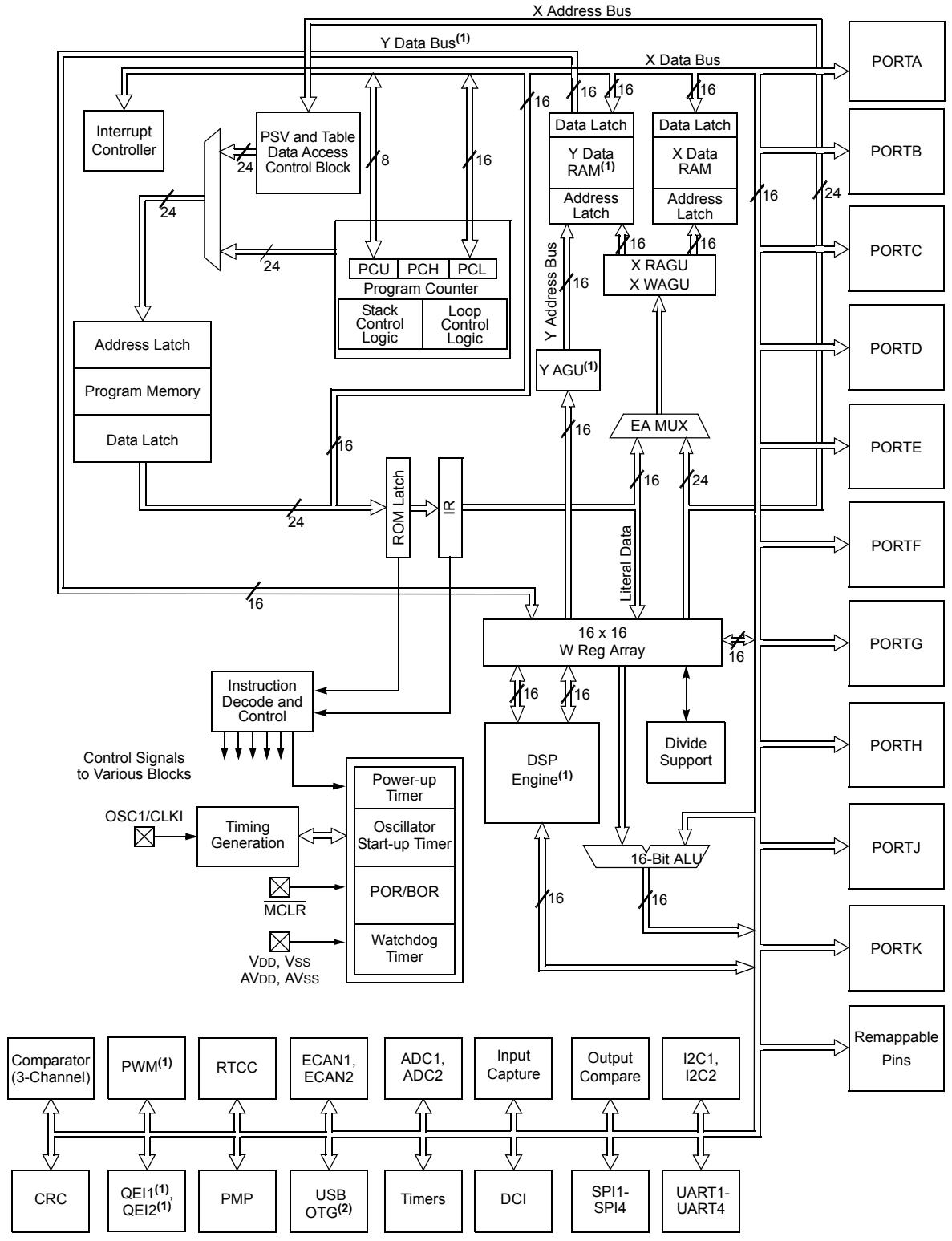
## 3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

**FIGURE 3-1: dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 CPU BLOCK DIAGRAM**




**Note 1:** This feature or peripheral is only available on dsPIC33EPXXX(MC/MU)806/810/814 devices.

**2:** This feature or peripheral is only available on dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU806/810/814 devices.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## 3.5 Programmer's Model

The programmer's model is shown in Figure 3-2. All registers in the programmer's model are memory mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, all devices in this family contain control registers for interrupts, while the dsPIC33EPXXX(GP/MC/MU)806/810/814 devices contain control registers for Modulo and Bit-reversed Addressing. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory mapped, as shown in Table 4-1.

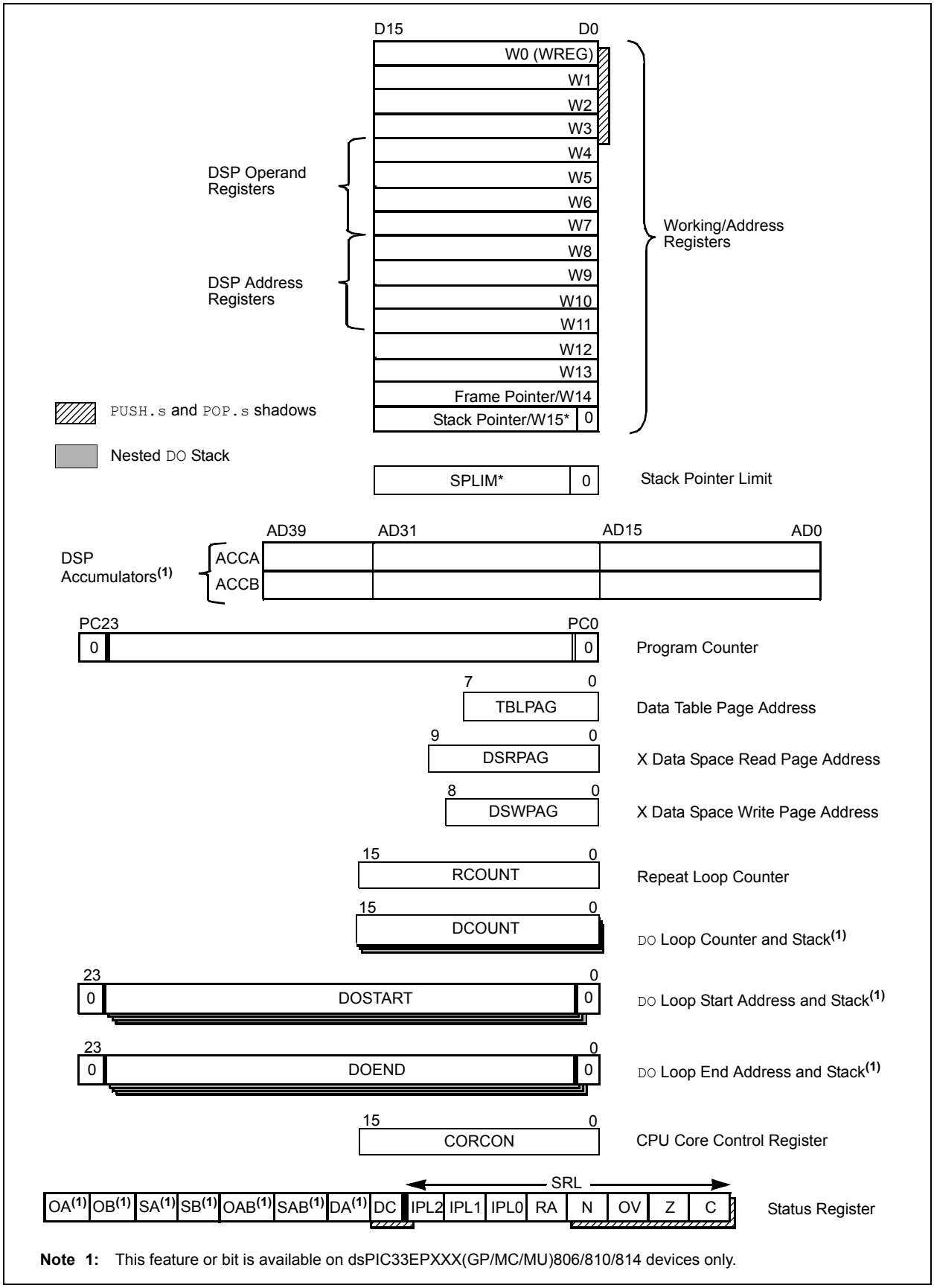
**TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS**

| Register(s) Name | Description |
|---|---|
| W0 through W15 | Working Register Array |
| ACCA, ACCB | 40-Bit DSP Accumulators |
| PC | 23-Bit Program Counter |
| SR | ALU and DSP Engine Status register |
| SPLIM | Stack Pointer Limit Value register |
| TBLPAG | Table Memory Page Address register |
| DSRPAG | Extended Data Space (EDS) Read Page register |
| DSWPAG | Extended Data Space (EDS) Write Page register |
| RCOUNT | REPEAT Loop Count register |
| DCOUNT(1) | DO Loop Count register |
| DOSTARTH(1,2), DOSTARTL(1,2) | DO Loop Start Address register (High and Low) |
| DOENDH(1), DOENDL(1) | DO Loop End Address register (High and Low) |
| CORCON | Contains DSP Engine, DO Loop Control and Trap Status bits |

**Note 1:** This register is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

**2:** The DOSTARTH and DOSTARTL registers are read-only.

**FIGURE 3-2: PROGRAMMER'S MODEL**




**Note 1:** This feature or bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.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## 3.6 CPU Resources

Many useful resources related to the CPU are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 3.6.1 KEY RESOURCES

- See **Section 16. "CPU"** (DS70359) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 3.7 CPU Control Registers

**REGISTER 3-1: SR: CPU STATUS REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/C-0 | R/C-0 | R -0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OA(1) | OB(1) | SA(1,4) | SB(1,4) | OAB(1) | SAB(1) | DA(1) | DC |
| bit 15 | | | | | | | bit 8 |

| R/W-0(2,3) | R/W-0(2,3) | R/W-0(2,3) | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| | IPL<2:0> | | RA | N | OV | Z | C |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | U = Unimplemented bit, read as '0' | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | C = Clearable bit | |
| -n = Value at POR | '1'= Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **OA:** Accumulator A Overflow Status bit(1)
1 = Accumulator A has overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit(1)
1 = Accumulator B has overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit(1,4)
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit(1,4)
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit(1)
1 = Accumulators A or B have overflowed
0 = Neither Accumulators A or B have overflowed

bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit(1)
1 = Accumulators A or B are saturated or have been saturated at some time
0 = Neither Accumulator A or B are saturated

bit 9 **DA:** DO Loop Active bit(1)
1 = DO loop in progress
0 = DO loop not in progress

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low order bit (for byte-sized data) or 8th low order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low order bit (for byte-sized data) or 8th low order bit (for word-sized data) of the result occurred

**Note 1:** This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

**2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1.

**3:** The IPL<2:0> bits are read-only when NSTDIS = 1 (INTCON1<15>).

**4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.


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**REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)**

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(2,3)
111 = CPU Interrupt Priority Level is 7 (15, user interrupts are disabled)
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit
1 = REPEAT loop in progress
0 = REPEAT loop not in progress

bit 3 **N:** MCU ALU Negative bit
1 = Result was negative
0 = Result was non-negative (zero or positive)

bit 2 **OV:** MCU ALU Overflow bit
This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = No overflow occurred

bit 1 **Z:** MCU ALU Zero bit
1 = An operation that affects the Z bit has set it at some time in the past
0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)

bit 0 **C:** MCU ALU Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

**Note 1:** This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

**2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1.

**3:** The IPL<2:0> bits are read-only when NSTDIS = 1 (INTCON1<15>).

**4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

**REGISTER 3-2: CORCON: CORE CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VAR | — | US<1:0>(1) | | EDT(1,2) | DL<2:0>(1) | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SATA(1) | SATB(1) | SATDW(1) | ACCSAT(1) | IPL3(3) | SFA | RND(1) | IF(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing is enabled
0 = Fixed exception processing is enabled

bit 14 **Unimplemented:** Read as '0'

bit 13-12 **US<1:0>:** DSP Multiply Unsigned/Signed Control bits(1)
11 = Reserved
10 = DSP engine multiplies are mixed-sign
01 = DSP engine multiplies are unsigned
00 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit(1,2)
1 = Terminates executing DO loop at end of current loop iteration
0 = No effect

bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits(1)
111 = 7 DO loops are active
•
•
•
001 = 1 DO loop is active
000 = 0 DO loops are active

bit 7 **SATA:** ACCA Saturation Enable bit(1)
1 = Accumulator A saturation is enabled
0 = Accumulator A saturation is disabled

bit 6 **SATB:** ACCB Saturation Enable bit(1)
1 = Accumulator B saturation is enabled
0 = Accumulator B saturation is disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit(1)
1 = Data space write saturation is enabled
0 = Data space write saturation is disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit(1)
1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(3)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

**Note 1:** This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.
**2:** This bit is always read as '0'.
**3:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.


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**REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)**

bit 2 **SFA:** Stack Frame Active Status bit
- 1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
- 0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1 **RND:** Rounding Mode Select bit(1)
- 1 = Biased (conventional) rounding is enabled
- 0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit(1)
- 1 = Integer mode is enabled for DSP multiply
- 0 = Fractional mode is enabled for DSP multiply

**Note 1:** This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

**2:** This bit is always read as '0'.

**3:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

## 3.8 Arithmetic Logic Unit (ALU)

The ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

### 3.8.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed, or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

### 3.8.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

1. 32-bit signed/16-bit signed divide
2. 32-bit unsigned/16-bit unsigned divide
3. 16-bit signed/16-bit signed divide
4. 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

## 3.9 DSP Engine (dsPIC33EPXXX(GP/MC/MU)806/810/814 Devices Only)

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are: `ADD`, `SUB` and `NEG`.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- Signed, unsigned or mixed-sign DSP multiply (US)
- Conventional or convergent rounding (RND)
- Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

**TABLE 3-2: DSP INSTRUCTIONS SUMMARY**

| Instruction | Algebraic Operation | ACC Write Back |
|---|---|---|
| CLR | $A = 0$ | Yes |
| ED | $A = (x - y)^2$ | No |
| EDAC | $A = A + (x - y)^2$ | No |
| MAC | $A = A + (x \bullet y)$ | Yes |
| MAC | $A = A + x^2$ | No |
| MOVSAC | No change in A | Yes |
| MPY | $A = x \bullet y$ | No |
| MPY | $A = x^2$ | No |
| MPY.N | $A = -x \bullet y$ | No |
| MSC | $A = A - x \bullet y$ | Yes |


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# 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4. "Program Memory"** (DS70613) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

The device architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the data space during code execution.

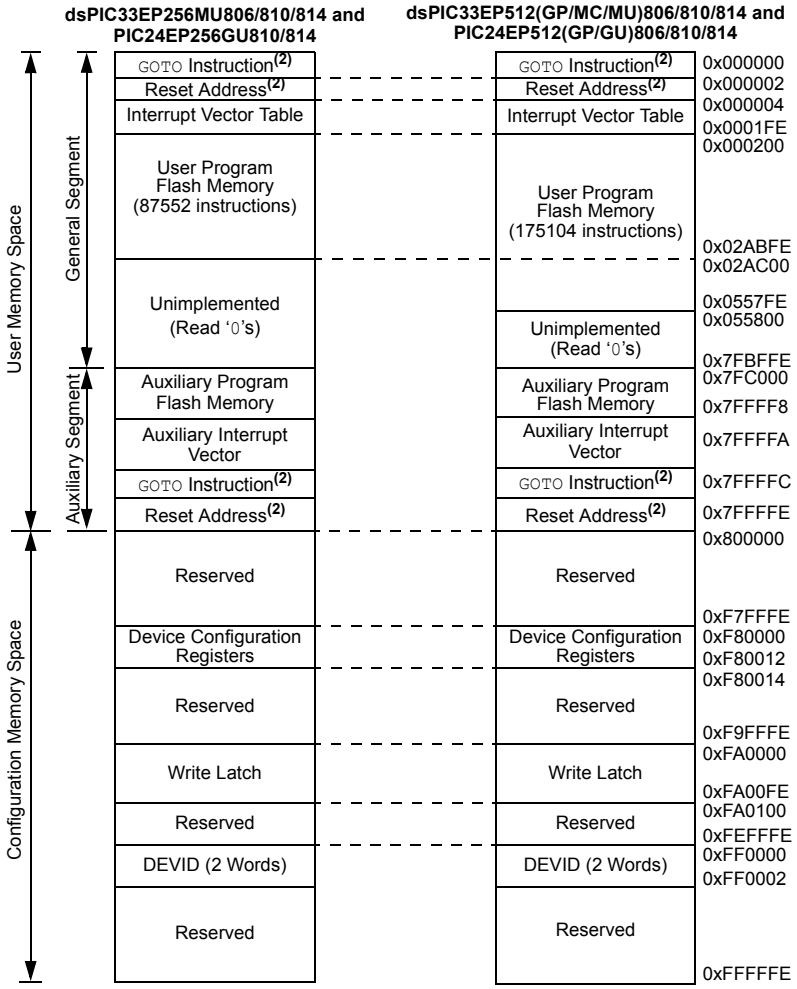
## 4.1 Program Address Space

The device program address memory space is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or data space remapping as described in **Section 4.8 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD/TBLWT operations, which use TBLPAG<7> to permit access to the Configuration bits and Device ID sections of the configuration memory space.

The device program memory map is shown in Figure 4-1.

**FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 DEVICES(1)**




**Note 1:** Memory areas are not shown to scale.

**2:** The Reset location is controlled by the Reset Target Vector Select bit, RSTPRI (FICD<2>). See **Section 29.0 "Special Features"** for more information.

### 4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-2).

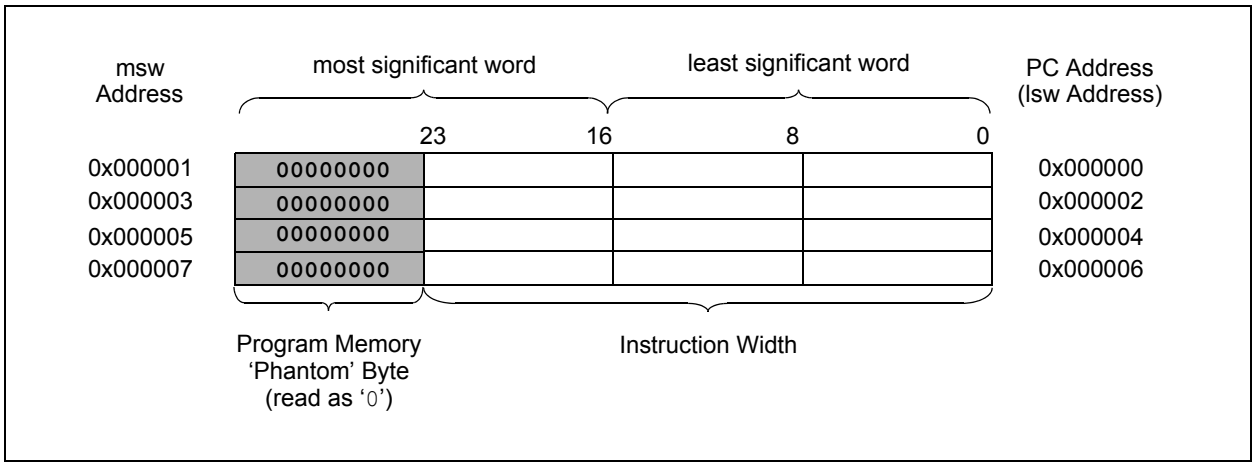
Program memory addresses are always word-aligned on the lower word and addresses are incremented or decremented by two during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

### 4.1.2 INTERRUPT AND TRAP VECTORS

All devices reserve the addresses between 0x00000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address 0x000000 of the primary Flash memory or at address 0x7FFFFC of the auxiliary Flash memory, with the actual address for the start of code at address 0x000002 of the primary Flash memory or at address 0x7FFFFE of the auxiliary Flash memory. Reset Target Vector Select bit (RSTPRI) in the FPOR Configuration register controls whether primary or auxiliary Flash Reset location is used.

A more detailed discussion of the interrupt vector tables is provided in **Section 7.1 "Interrupt Vector Table"**.

**FIGURE 4-2: PROGRAM MEMORY ORGANIZATION**





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## 4.2 Data Address Space

The CPU has a separate 16-bit wide data memory space. The data space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps are shown in Figure 4-3, Figure 4-4, Figure 4-5 and Figure 4-6.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the data space. This arrangement gives a Base Data Space address range of 64 Kbytes or 32K words.

The Base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space, which has a total address range of 16 MBytes.

dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices implement up to 56 Kbytes of data memory. If an EA point to a location outside of this area, an all-zero word or byte is returned.

### 4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte-addressable, 16-bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all data space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

### 4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® MCU devices and improve data space memory usage efficiency, the device instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB. The MSB is not modified.

A Sign-Extend instruction (`SE`) is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (`ZE`) instruction on the appropriate address.

### 4.2.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

| **Note:** | The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information. |
|---|---|

### 4.2.4 NEAR DATA SPACE

The 8-Kbyte area between 0x0000 and 0x1FFF is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole data space is addressable using `MOV` instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a working register as an Address Pointer.

**FIGURE 4-3: DATA MEMORY MAP FOR dsPIC33EP512(GP/MC/MU)806/810/814 DEVICES WITH 52-KBYTE RAM**

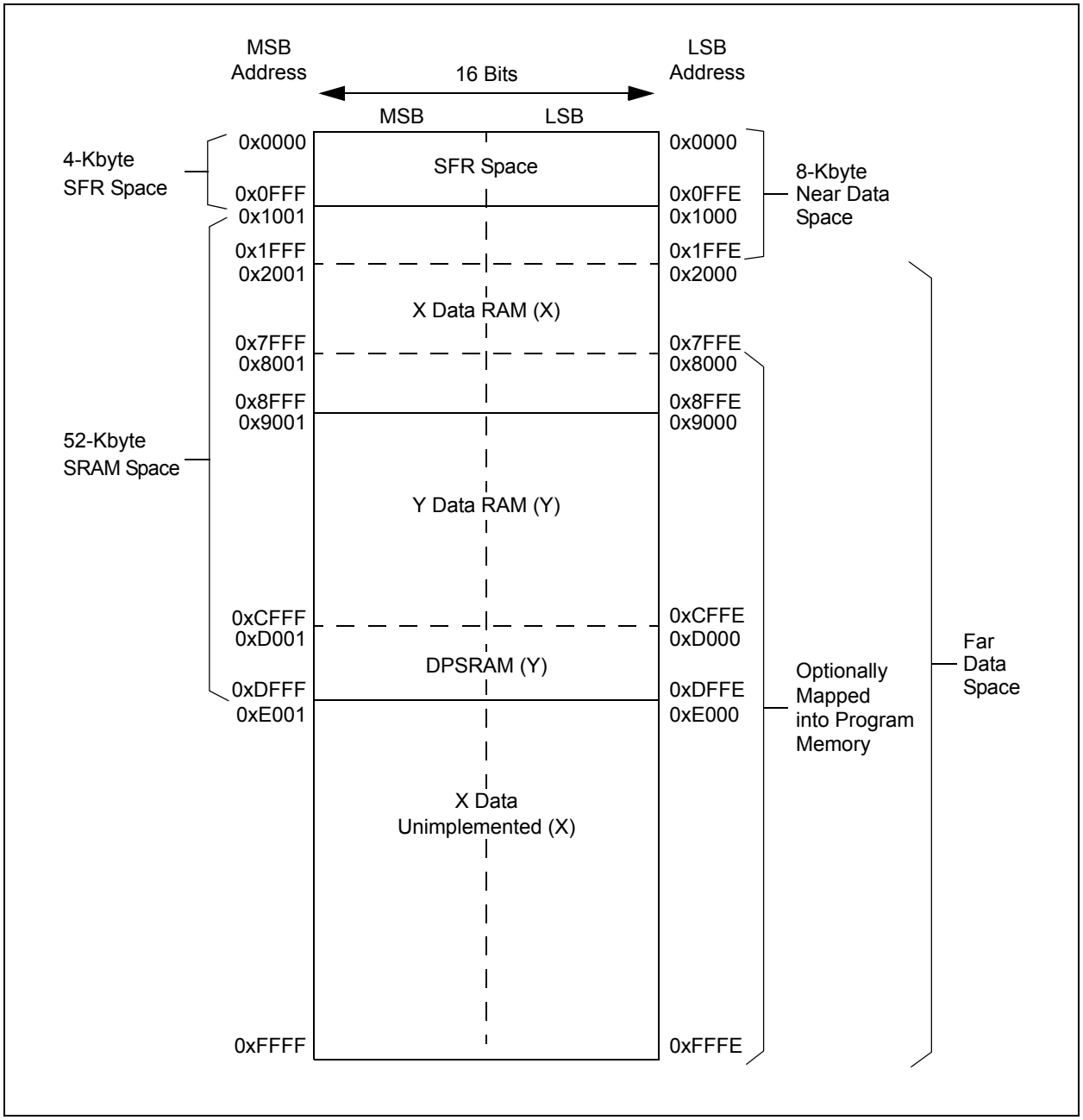



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**FIGURE 4-4: DATA MEMORY MAP FOR PIC24EP512(GP/GU)806/810/814 DEVICES WITH 52-KBYTE RAM**

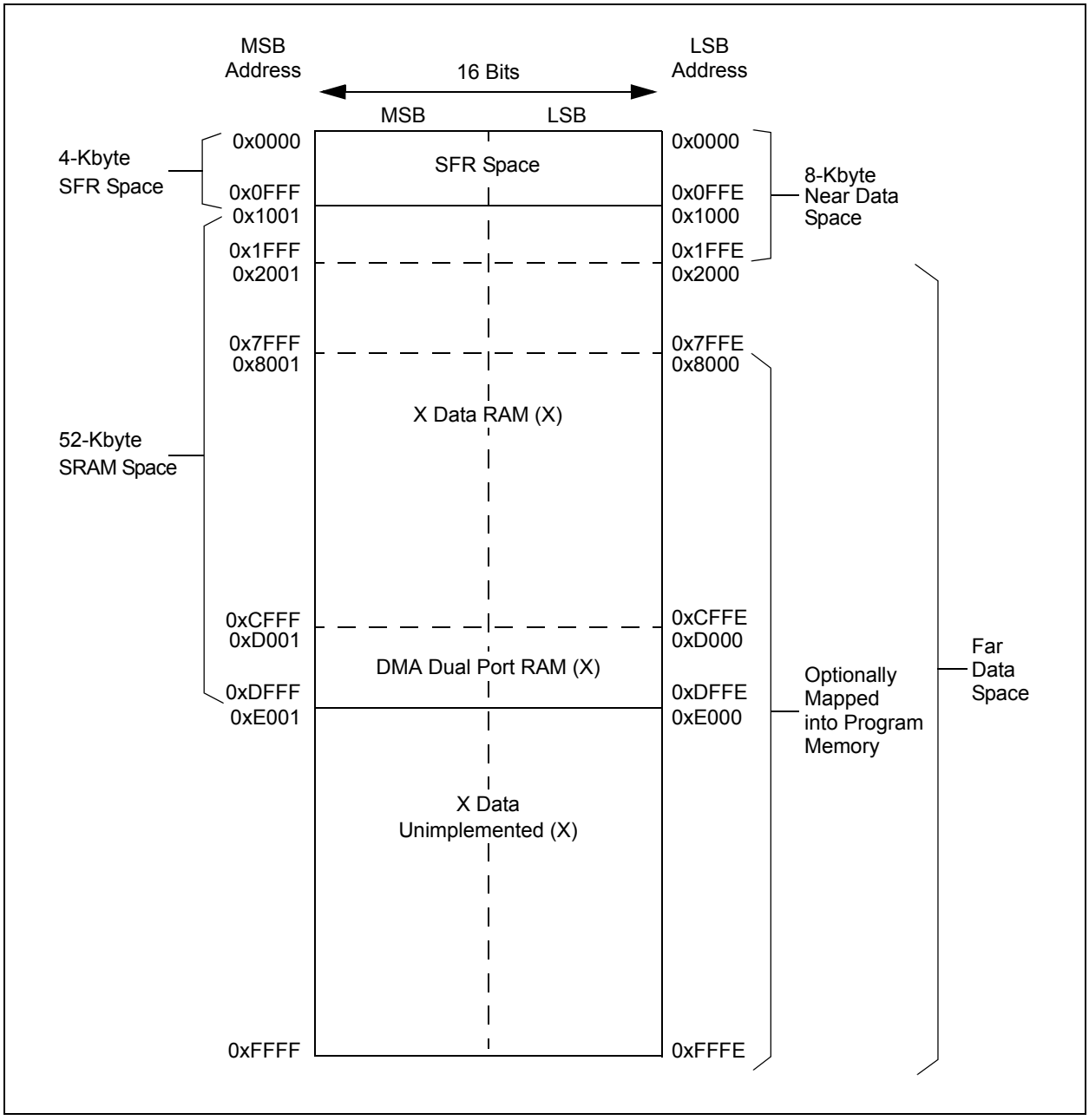

**FIGURE 4-5: DATA MEMORY MAP FOR dsPIC33EP256MU806/810/814 DEVICES WITH 28-KBYTE RAM**

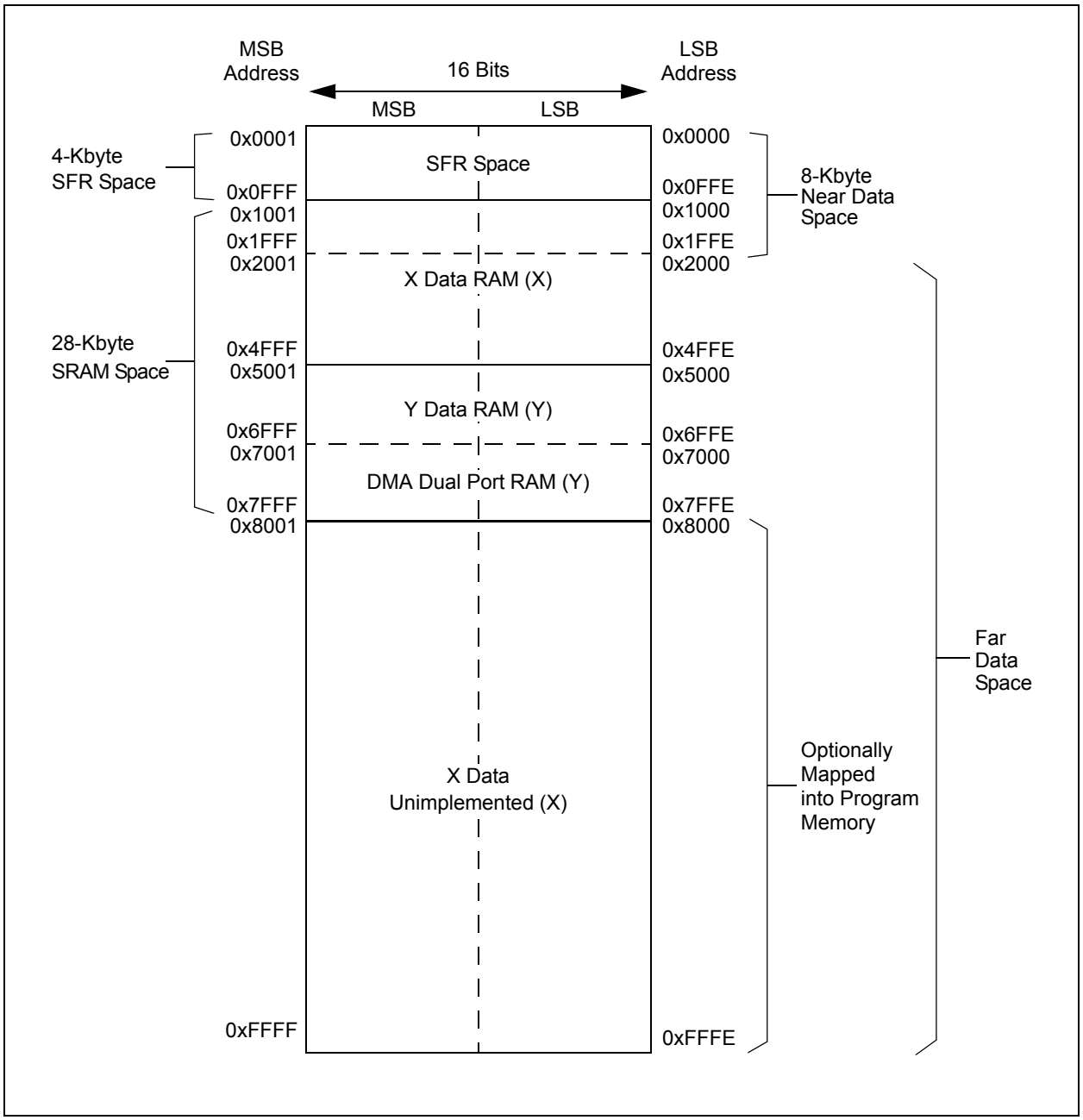



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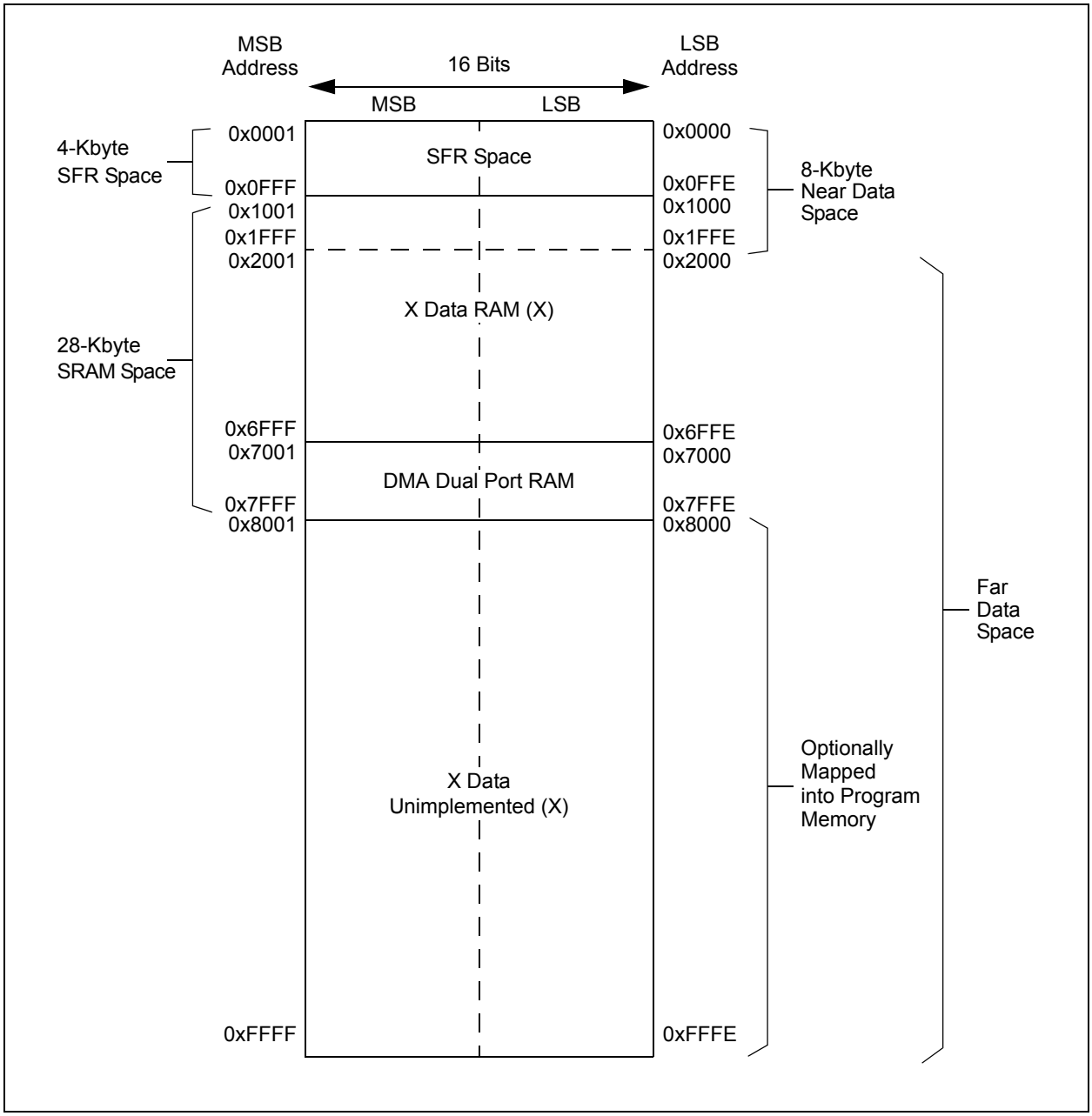
**FIGURE 4-6: DATA MEMORY MAP FOR PIC24EP256GU810/814 DEVICES WITH 28-KBYTE RAM**



### 4.2.5 X AND Y DATA SPACES

The dsPIC33EPXXX(GP/MC/MU)806/810/814 core has two data spaces, X and Y. These data spaces can be considered either separate (for some DSP instructions), or as one unified linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The PIC24EPXXX(GP/GU)806/810/814 devices do not have a Y data space and a Y AGU. For these devices, the entire data space is treated as X data space.

The X data space is used by all instructions and supports all addressing modes. X data space has separate read and write data buses. The X read data bus is the read data path for all instructions that view data space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (`MAC` class).

The Y data space is used in concert with the X data space by the `MAC` class of instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MOVSAC`, `MPY`, `MPY.N` and `MSC`) to provide two concurrent data read paths.

Both the X and Y data spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X data space. Modulo Addressing and Bit-Reversed Addressing are not present in PIC24EPXXX(GP/GU)806/810/814 devices.

All data memory writes, including in DSP instructions, view data space as combined X and Y address space. The boundary between the X and Y data spaces is device-dependent and is not user-programmable.

### 4.2.6 DMA RAM

Each dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 device contains 4 Kbytes of dual ported DMA RAM located at the end of Y data RAM and is part of Y data space. Memory locations in the DMA RAM space are accessible simultaneously by the CPU and the DMA Controller module. DMA RAM is utilized by the DMA controller to store data to be transferred to various peripherals using DMA, as well as data transferred from various peripherals using DMA. The DMA RAM can be accessed by the DMA controller without having to steal cycles from the CPU.

When the CPU and the DMA controller attempt to concurrently write to the same DMA RAM location, the hardware ensures that the CPU is given precedence in accessing the DMA RAM location. Therefore, the DMA RAM provides a reliable means of transferring DMA data without ever having to stall the CPU.

| | |
|---|---|
| **Note 1:** | DMA RAM can be used for general purpose data storage if the DMA function is not required in an application. |
| **2:** | On PIC24EPXXX(GP/GU)806/810/814 devices, DMA RAM is located at the end of X data RAM and is part of X data space. |

## 4.3 Program Memory Resources

Many useful resources related to the Program Memory are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 4.3.1 KEY RESOURCES

- **Section 4. "Program Memory"** (DS70612) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 4.4 Special Function Register Maps

Table 4-1 through Table 4-72 provide mapping tables for all Special Function Registers (SFRs).


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**TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806/810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W0 | 0000 | W0 (WREG) | | | | | | | | | | | | | | | | 0000 |
| W1 | 0002 | W1 | | | | | | | | | | | | | | | | 0000 |
| W2 | 0004 | W2 | | | | | | | | | | | | | | | | 0000 |
| W3 | 0006 | W3 | | | | | | | | | | | | | | | | 0000 |
| W4 | 0008 | W4 | | | | | | | | | | | | | | | | 0000 |
| W5 | 000A | W5 | | | | | | | | | | | | | | | | 0000 |
| W6 | 000C | W6 | | | | | | | | | | | | | | | | 0000 |
| W7 | 000E | W7 | | | | | | | | | | | | | | | | 0000 |
| W8 | 0010 | W8 | | | | | | | | | | | | | | | | 0000 |
| W9 | 0012 | W9 | | | | | | | | | | | | | | | | 0000 |
| W10 | 0014 | W10 | | | | | | | | | | | | | | | | 0000 |
| W11 | 0016 | W11 | | | | | | | | | | | | | | | | 0000 |
| W12 | 0018 | W12 | | | | | | | | | | | | | | | | 0000 |
| W13 | 001A | W13 | | | | | | | | | | | | | | | | 0000 |
| W14 | 001C | W14 | | | | | | | | | | | | | | | | 0000 |
| W15 | 001E | W15 | | | | | | | | | | | | | | | | 1000 |
| SPLIM | 0020 | SPLIM | | | | | | | | | | | | | | | | 0000 |
| ACCAL | 0022 | ACCAL | | | | | | | | | | | | | | | | 0000 |
| ACCAH | 0024 | ACCAH | | | | | | | | | | | | | | | | 0000 |
| ACCAU | 0026 | Sign-Extension of ACCA<39> | | | | | | | | ACCAU | | | | | | | | 0000 |
| ACCBL | 0028 | ACCBL | | | | | | | | | | | | | | | | 0000 |
| ACCBH | 002A | ACCBH | | | | | | | | | | | | | | | | 0000 |
| ACCBU | 002C | Sign-Extension of ACCB<39> | | | | | | | | ACCBU | | | | | | | | 0000 |
| PCL | 002E | PCL | | | | | | | | | | | | | | | — | 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | — | PCH | | | | | | | 0000 |
| DSRPAG | 0032 | — | — | — | — | — | — | DSRPAG | | | | | | | | | | 0001 |
| DSWPAG | 0034 | — | — | — | — | — | — | — | DSWPAG | | | | | | | | | 0001 |
| RCOUNT | 0036 | RCOUNT | | | | | | | | | | | | | | | | 0000 |
| DCOUNT | 0038 | DCOUNT | | | | | | | | | | | | | | | | 0000 |
| DOSTARTL | 003A | DOSTARTL | | | | | | | | | | | | | | | — | 0000 |
| DOSTARTH | 003C | — | — | — | — | — | — | — | — | — | — | DOSTARTH | | | | | | 0000 |
| DOENDL | 003E | DOENDL | | | | | | | | | | | | | | | — | 0000 |
| DOENDH | 0040 | — | — | — | — | — | — | — | — | — | — | DOENDH | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806/810/814 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SR | 0042 | OA | OB | SA | SB | OAB | SAB | DA | DC | IPL2 | IPL1 | IPL0 | RA | N | OV | Z | C | 0000 |
| CORCON | 0044 | VAR | — | US<1:0> | | EDT | DL<2:0> | | | SATA | SATB | SATDW | ACCSAT | IPL3 | SFA | RND | IF | 0020 |
| MODCON | 0046 | XMODEN | YMODEN | — | — | BWM<3:0> | | | | YWM<3:0> | | | | XWM<3:0> | | | | 0000 |
| XMODSRT | 0048 | XMODSRT<15:1> | | | | | | | | | | | | | | | 0 | 0000 |
| XMODEND | 004A | XMODEND<15:1> | | | | | | | | | | | | | | | 1 | 0001 |
| YMODSRT | 004C | YMODSRT<15:1> | | | | | | | | | | | | | | | 0 | 0000 |
| YMODEND | 004E | YMODEND<15:1> | | | | | | | | | | | | | | | 1 | 0001 |
| XBREV | 0050 | BREN | XBREV<14:0> | | | | | | | | | | | | | | | 0000 |
| DISICNT | 0052 | — | — | DISICNT<13:0> | | | | | | | | | | | | | | 0000 |
| TBLPAG | 0054 | — | — | — | — | — | — | — | — | TBLPAG<7:0> | | | | | | | | 0000 |
| MSTRPR | 0058 | MSTRPR<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-2: CPU CORE REGISTER MAP FOR PIC24EPXXX(GP/GU)810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W0 | 0000 | W0 (WREG) | | | | | | | | | | | | | | | | 0000 |
| W1 | 0002 | W1 | | | | | | | | | | | | | | | | 0000 |
| W2 | 0004 | W2 | | | | | | | | | | | | | | | | 0000 |
| W3 | 0006 | W3 | | | | | | | | | | | | | | | | 0000 |
| W4 | 0008 | W4 | | | | | | | | | | | | | | | | 0000 |
| W5 | 000A | W5 | | | | | | | | | | | | | | | | 0000 |
| W6 | 000C | W6 | | | | | | | | | | | | | | | | 0000 |
| W7 | 000E | W7 | | | | | | | | | | | | | | | | 0000 |
| W8 | 0010 | W8 | | | | | | | | | | | | | | | | 0000 |
| W9 | 0012 | W9 | | | | | | | | | | | | | | | | 0000 |
| W10 | 0014 | W10 | | | | | | | | | | | | | | | | 0000 |
| W11 | 0016 | W11 | | | | | | | | | | | | | | | | 0000 |
| W12 | 0018 | W12 | | | | | | | | | | | | | | | | 0000 |
| W13 | 001A | W13 | | | | | | | | | | | | | | | | 0000 |
| W14 | 001C | W14 | | | | | | | | | | | | | | | | 0000 |
| W15 | 001E | W15 | | | | | | | | | | | | | | | | 1000 |
| SPLIM | 0020 | SPLIM | | | | | | | | | | | | | | | | 0000 |
| PCL | 002E | PCL | | | | | | | | | | | | | | | — | 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | — | PCH | | | | | | | 0000 |
| DSRPAG | 0032 | — | — | — | — | — | — | DSRPAG<9:0> | | | | | | | | | | 0001 |
| DSWPAG | 0034 | — | — | — | — | — | — | — | DSWPAG<8:0> | | | | | | | | | 0001 |
| RCOUNT | 0036 | RCOUNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| SR | 0042 | — | — | — | — | — | — | — | DC | IPL2 | IPL1 | IPL0 | RA | N | OV | Z | C | 0000 |
| CORCON | 0044 | VAR | — | — | — | — | — | — | — | — | — | — | — | IPL3 | SFA | — | — | 0020 |
| DISICNT | 0052 | — | — | DISICNT<13:0> | | | | | | | | | | | | | | 0000 |
| TBLPAG | 0054 | — | — | — | — | — | — | — | — | TBLPAG<7:0> | | | | | | | | 0000 |
| MSTRPR | 0058 | MSTRPR<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | NVMIF | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | IC8IF | IC7IF | AD2IF | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | T6IF | DMA4IF | PMPIF | OC8IF | OC7IF | OC6IF | OC5IF | IC6IF | IC5IF | IC4IF | IC3IF | DMA3IF | C1IF | C1RXIF | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | RTCIF | DMA5IF | DCIIF | DCIEIF | QEI1IF | PSEMIF | C2IF | C2RXIF | INT4IF | INT3IF | T9IF | T8IF | MI2C2IF | SI2C2IF | T7IF | 0000 |
| IFS4 | 0808 | — | — | — | — | QEI2IF | — | PSESMIF | — | C2TXIF | C1TXIF | DMA7IF | DMA6IF | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS5 | 080A | PWM2IF | PWM1IF | IC9IF | OC9IF | SPI3IF | SPI3EIF | U4TXIF | U4RXIF | U4EIF | USB1IF | — | — | U3TXIF | U3RXIF | U3EIF | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | PWM7IF | PWM6IF | PWM5IF | PWM4IF | PWM3IF | 0000 |
| IFS7 | 080E | IC11IF | OC11IF | IC10IF | OC10IF | SPI4IF | SPI4EIF | DMA11IF | DMA10IF | DMA9IF | DMA8IF | — | — | — | — | — | — | 0000 |
| IFS8 | 0810 | — | ICDIF | IC16IF | OC16IF | IC15IF | OC15IF | IC14IF | OC14IF | IC13IF | OC13IF | — | DMA14IF | DMA13IF | DMA12IF | IC12IF | OC12IF | 0000 |
| IEC0 | 0820 | NVMIE | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | IC8IE | IC7IE | AD2IE | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | T6IE | DMA4IE | PMPIE | OC8IE | OC7IE | OC6IE | OC5IE | IC6IE | IC5IE | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | RTCIE | DMA5IE | DCIIE | DCIEIE | QEI1IE | PSEMIE | C2IE | C2RXIE | INT4IE | INT3IE | T9IE | T8IE | MI2C2IE | SI2C2IE | T7IE | 0000 |
| IEC4 | 0828 | — | — | — | — | QEI2IE | — | PSESMIE | — | C2TXIE | C1TXIE | DMA7IE | DMA6IE | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC5 | 082A | PWM2IE | PWM1IE | IC9IE | OC9IE | SPI3IE | SPI3EIE | U4TXIE | U4RXIE | U4EIE | USB1IE | — | — | U3TXIE | U3RXIE | U3EIE | — | 0000 |
| IEC6 | 082C | — | — | — | — | — | — | — | — | — | — | — | PWM7IE | PWM6IE | PWM5IE | PWM4IE | PWM3IE | 0000 |
| IEC7 | 082E | IC11IE | OC11IE | IC10IE | OC10IE | SPI4IE | SPI4EIE | DMA11IE | DMA10IE | DMA9IE | DMA8IE | — | — | — | — | — | — | 0000 |
| IEC8 | 0830 | — | ICDIE | IC16IE | OC16IE | IC15IE | OC15IE | IC14IE | OC14IE | IC13IE | OC13IE | — | DMA14IE | DMA13IE | DMA12IE | IC12IE | OC12IE | 0000 |
| IPC0 | 0840 | — | T1IP<2:0> | | | — | OC1IP<2:0> | | | — | IC1IP<2:0> | | | — | INT0IP<2:0> | | | 4444 |
| IPC1 | 0842 | — | T2IP<2:0> | | | — | OC2IP<2:0> | | | — | IC2IP<2:0> | | | — | DMA0IP<2:0> | | | 4444 |
| IPC2 | 0844 | — | U1RXIP<2:0> | | | — | SPI1IP<2:0> | | | — | SPI1EIP<2:0> | | | — | T3IP<2:0> | | | 4444 |
| IPC3 | 0846 | — | NVMIP<2:0> | | | — | DMA1IP<2:0> | | | — | AD1IP<2:0> | | | — | U1TXIP<2:0> | | | 4444 |
| IPC4 | 0848 | — | CNIP<2:0> | | | — | CMIP<2:0> | | | — | MI2C1IP<2:0> | | | — | SI2C1IP<2:0> | | | 4444 |
| IPC5 | 084A | — | IC8IP<2:0> | | | — | IC7IP<2:0> | | | — | AD2IP<2:0> | | | — | INT1IP<2:0> | | | 4444 |
| IPC6 | 084C | — | T4IP<2:0> | | | — | OC4IP<2:0> | | | — | OC3IP<2:0> | | | — | DMA2IP<2:0> | | | 4444 |
| IPC7 | 084E | — | U2TXIP<2:0> | | | — | U2RXIP<2:0> | | | — | INT2IP<2:0> | | | — | T5IP<2:0> | | | 4444 |
| IPC8 | 0850 | — | C1IP<2:0> | | | — | C1RXIP<2:0> | | | — | SPI2IP<2:0> | | | — | SPI2EIP<2:0> | | | 4444 |
| IPC9 | 0852 | — | IC5IP<2:0> | | | — | IC4IP<2:0> | | | — | IC3IP<2:0> | | | — | DMA3IP<2:0> | | | 4444 |
| IPC10 | 0854 | — | OC7IP<2:0> | | | — | OC6IP<2:0> | | | — | OC5IP<2:0> | | | — | IC6IP<2:0> | | | 4444 |
| IPC11 | 0856 | — | T6IP<2:0> | | | — | DMA4IP<2:0> | | | — | PMPIP<2:0> | | | — | OC8IP<2:0> | | | 4444 |
| IPC12 | 0858 | — | T8IP<2:0> | | | — | MI2C2IP<2:0> | | | — | SI2C2IP<2:0> | | | — | T7IP<2:0> | | | 4444 |
| IPC13 | 085A | | C2RXIP<2:0> | | | — | INT4IP<2:0> | | | — | INT3IP<2:0> | | | — | T9IP<2:0> | | | 4444 |
| IPC14 | 085C | — | DCIEIP<2:0> | | | — | QEI1IP<2:0> | | | — | PSEMIP<2:0> | | | — | C2IP<2:0> | | | 4444 |
| IPC15 | 085E | — | — | — | — | — | RTCIP<2:0> | | | — | DMA5IP<2:0> | | | — | DCIIP<2:0> | | | 0444 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU814 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IPC16 | 0860 | — | CRCIP<2:0> | | | — | U2EIP<2:0> | | | — | U1EIP<2:0> | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | C2TXIP<2:0> | | | — | C1TXIP<2:0> | | | — | DMA7IP<2:0> | | | — | DMA6IP<2:0> | | | 4444 |
| IPC18 | 0864 | — | QEI2IP<2:0> | | | — | — | — | — | — | PSESMIP<2:0> | | | — | — | — | — | 4040 |
| IPC20 | 0868 | — | U3TXIP<2:0> | | | — | U3RXIP<2:0> | | | — | U3EIP<2:0> | | | — | — | — | — | 4440 |
| IPC21 | 086A | — | U4EIP<2:0> | | | — | USB1IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC22 | 086C | — | SPI3IP<2:0> | | | — | SPI3EIP<2:0> | | | — | U4TXIP<2:0> | | | — | U4RXIP<2:0> | | | 4444 |
| IPC23 | 086E | — | PWM2IP<2:0> | | | — | PWM1IP<2:0> | | | — | IC9IP<2:0> | | | — | OC9IP<2:0> | | | 4444 |
| IPC24 | 0870 | — | PWM6IP<2:0> | | | — | PWM5IP<2:0> | | | — | PWM4IP<2:0> | | | — | PWM3IP<2:0> | | | 4444 |
| IPC25 | 0872 | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM7IP<2:0> | | | 0004 |
| IPC29 | 087A | — | DMA9IP<2:0> | | | — | DMA8IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC30 | 087C | — | SPI4IP<2:0> | | | — | SPI4EIP<2:0> | | | — | DMA11IP<2:0> | | | — | DMA10IP<2:0> | | | 4444 |
| IPC31 | 087E | — | IC11IP<2:0> | | | — | OC11IP<2:0> | | | — | IC10IP<2:0> | | | — | OC10IP<2:0> | | | 4444 |
| IPC32 | 0880 | — | DMA13IP<2:0> | | | — | DMA12IP<2:0> | | | — | IC12IP<2:0> | | | — | OC12IP<2:0> | | | 4444 |
| IPC33 | 0882 | — | IC13IP<2:0> | | | — | OC13IP<2:0> | | | — | — | — | — | — | DMA14IP<2:0> | | | 4404 |
| IPC34 | 0884 | — | IC15IP<2:0> | | | — | OC15IP<2:0> | | | — | IC14IP<2:0> | | | — | OC14IP<2:0> | | | 4444 |
| IPC35 | 0886 | — | — | — | — | — | ICDIP<2:0> | | | — | IC16IP<2:0> | | | — | OC16IP<2:0> | | | 0444 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE | SFTACERR | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | UAE | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | ILR<3:0> | | | | VECNUM<7:0> | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU810 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | NVMIF | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | IC8IF | IC7IF | AD2IF | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | T6IF | DMA4IF | PMPIF | OC8IF | OC7IF | OC6IF | OC5IF | IC6IF | IC5IF | IC4IF | IC3IF | DMA3IF | C1IF | C1RXIF | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | RTCIF | DMA5IF | DCIIF | DCIEIF | QEI1IF | PSEMIF | C2IF | C2RXIF | INT4IF | INT3IF | T9IF | T8IF | MI2C2IF | SI2C2IF | T7IF | 0000 |
| IFS4 | 0808 | — | — | — | — | QEI2IF | — | PSESMIF | — | C2TXIF | C1TXIF | DMA7IF | DMA6IF | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS5 | 080A | PWM2IF | PWM1IF | IC9IF | OC9IF | SPI3IF | SPI3EIF | U4TXIF | U4RXIF | U4EIF | USB1IF | — | — | U3TXIF | U3RXIF | U3EIF | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | — | PWM6IF | PWM5IF | PWM4IF | PWM3IF | 0000 |
| IFS7 | 080E | IC11IF | OC11IF | IC10IF | OC10IF | SPI4IF | SPI4EIF | DMA11IF | DMA10IF | DMA9IF | DMA8IF | — | — | — | — | — | — | 0000 |
| IFS8 | 0810 | — | ICDIF | IC16IF | OC16IF | IC15IF | OC15IF | IC14IF | OC14IF | IC13IF | OC13IF | — | DMA14IF | DMA13IF | DMA12IF | IC12IF | OC12IF | 0000 |
| IEC0 | 0820 | NVMIE | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | IC8IE | IC7IE | AD2IE | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | T6IE | DMA4IE | PMPIE | OC8IE | OC7IE | OC6IE | OC5IE | IC6IE | IC5IE | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | RTCIE | DMA5IE | DCIIE | DCIEIE | QEI1IE | PSEMIE | C2IE | C2RXIE | INT4IE | INT3IE | T9IE | T8IE | MI2C2IE | SI2C2IE | T7IE | 0000 |
| IEC4 | 0828 | — | — | — | — | QEI2IE | — | PSESMIE | — | C2TXIE | C1TXIE | DMA7IE | DMA6IE | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC5 | 082A | PWM2IE | PWM1IE | IC9IE | OC9IE | SPI3IE | SPI3EIE | U4TXIE | U4RXIE | U4EIE | USB1IE | — | — | U3TXIE | U3RXIE | U3EIE | — | 0000 |
| IEC6 | 082C | — | — | — | — | — | — | — | — | — | — | — | — | PWM6IE | PWM5IE | PWM4IE | PWM3IE | 0000 |
| IEC7 | 082E | IC11IE | OC11IE | IC10IE | OC10IE | SPI4IE | SPI4EIE | DMA11IE | DMA10IE | DMA9IE | DMA8IE | — | — | — | — | — | — | 0000 |
| IEC8 | 0830 | — | ICDIE | IC16IE | OC16IE | IC15IE | OC15IE | IC14IE | OC14IE | IC13IE | OC13IE | — | DMA14IE | DMA13IE | DMA12IE | IC12IE | OC12IE | 0000 |
| IPC0 | 0840 | — | T1IP<2:0> | | | — | OC1IP<2:0> | | | — | IC1IP<2:0> | | | — | INT0IP<2:0> | | | 4444 |
| IPC1 | 0842 | — | T2IP<2:0> | | | — | OC2IP<2:0> | | | — | IC2IP<2:0> | | | — | DMA0IP<2:0> | | | 4444 |
| IPC2 | 0844 | — | U1RXIP<2:0> | | | — | SPI1IP<2:0> | | | — | SPI1EIP<2:0> | | | — | T3IP<2:0> | | | 4444 |
| IPC3 | 0846 | — | NVMIP<2:0> | | | — | DMA1IP<2:0> | | | — | AD1IP<2:0> | | | — | U1TXIP<2:0> | | | 4444 |
| IPC4 | 0848 | — | CNIP<2:0> | | | — | CMIP<2:0> | | | — | MI2C1IP<2:0> | | | — | SI2C1IP<2:0> | | | 4444 |
| IPC5 | 084A | — | IC8IP<2:0> | | | — | IC7IP<2:0> | | | — | AD2IP<2:0> | | | — | INT1IP<2:0> | | | 4444 |
| IPC6 | 084C | — | T4IP<2:0> | | | — | OC4IP<2:0> | | | — | OC3IP<2:0> | | | — | DMA2IP<2:0> | | | 4444 |
| IPC7 | 084E | — | U2TXIP<2:0> | | | — | U2RXIP<2:0> | | | — | INT2IP<2:0> | | | — | T5IP<2:0> | | | 4444 |
| IPC8 | 0850 | — | C1IP<2:0> | | | — | C1RXIP<2:0> | | | — | SPI2IP<2:0> | | | — | SPI2EIP<2:0> | | | 4444 |
| IPC9 | 0852 | — | IC5IP<2:0> | | | — | IC4IP<2:0> | | | — | IC3IP<2:0> | | | — | DMA3IP<2:0> | | | 4444 |
| IPC10 | 0854 | — | OC7IP<2:0> | | | — | OC6IP<2:0> | | | — | OC5IP<2:0> | | | — | IC6IP<2:0> | | | 4444 |
| IPC11 | 0856 | — | T6IP<2:0> | | | — | DMA4IP<2:0> | | | — | PMPIP<2:0> | | | — | OC8IP<2:0> | | | 4444 |
| IPC12 | 0858 | — | T8IP<2:0> | | | — | MI2C2IP<2:0> | | | — | SI2C2IP<2:0> | | | — | T7IP<2:0> | | | 4444 |
| IPC13 | 085A | | C2RXIP<2:0> | | | — | INT4IP<2:0> | | | — | INT3IP<2:0> | | | — | T9IP<2:0> | | | 4444 |
| IPC14 | 085C | — | DCIEIP<2:0> | | | — | QEI1IP<2:0> | | | — | PSEMIP<2:0> | | | — | C2IP<2:0> | | | 4444 |
| IPC15 | 085E | — | — | — | — | — | RTCIP<2:0> | | | — | DMA5IP<2:0> | | | — | DCIIP<2:0> | | | 0444 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU810 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IPC16 | 0860 | — | CRCIP<2:0> | | | — | U2EIP<2:0> | | | — | U1EIP<2:0> | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | C2TXIP<2:0> | | | — | C1TXIP<2:0> | | | — | DMA7IP<2:0> | | | — | DMA6IP<2:0> | | | 4444 |
| IPC18 | 0864 | — | QEI2IP<2:0> | | | — | — | — | — | — | PSESMIP<2:0> | | | — | — | — | — | 4040 |
| IPC20 | 0868 | — | U3TXIP<2:0> | | | — | U3RXIP<2:0> | | | — | U3EIP<2:0> | | | — | — | — | — | 4440 |
| IPC21 | 086A | — | U4EIP<2:0> | | | — | USB1IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC22 | 086C | — | SPI3IP<2:0> | | | — | SPI3EIP<2:0> | | | — | U4TXIP<2:0> | | | — | U4RXIP<2:0> | | | 4444 |
| IPC23 | 086E | — | PWM2IP<2:0> | | | — | PWM1IP<2:0> | | | — | IC9IP<2:0> | | | — | OC9IP<2:0> | | | 4444 |
| IPC24 | 0870 | — | PWM6IP<2:0> | | | — | PWM5IP<2:0> | | | — | PWM4IP<2:0> | | | — | PWM3IP<2:0> | | | 4444 |
| IPC29 | 087A | — | DMA9IP<2:0> | | | — | DMA8IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC30 | 087C | — | SPI4IP<2:0> | | | — | SPI4EIP<2:0> | | | — | DMA11IP<2:0> | | | — | DMA10IP<2:0> | | | 4444 |
| IPC31 | 087E | — | IC11IP<2:0> | | | — | OC11IP<2:0> | | | — | IC10IP<2:0> | | | — | OC10IP<2:0> | | | 4444 |
| IPC32 | 0880 | — | DMA13IP<2:0> | | | — | DMA12IP<2:0> | | | — | IC12IP<2:0> | | | — | OC12IP<2:0> | | | 4444 |
| IPC33 | 0882 | — | IC13IP<2:0> | | | — | OC13IP<2:0> | | | — | — | — | — | — | DMA14IP<2:0> | | | 4404 |
| IPC34 | 0884 | — | IC15IP<2:0> | | | — | OC15IP<2:0> | | | — | IC14IP<2:0> | | | — | OC14IP<2:0> | | | 4444 |
| IPC35 | 0886 | — | — | — | — | — | ICDIP<2:0> | | | — | IC16IP<2:0> | | | — | OC16IP<2:0> | | | 0444 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE | SFTACERR | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | UAE | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | — | ILR<3:0> | | | | VECNUM<7:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | NVMIF | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | IC8IF | IC7IF | AD2IF | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | T6IF | DMA4IF | PMPIF | OC8IF | OC7IF | OC6IF | OC5IF | IC6IF | IC5IF | IC4IF | IC3IF | DMA3IF | C1IF | C1RXIF | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | RTCIF | DMA5IF | DCIIF | DCIEIF | QEI1IF | PSEMIF | C2IF | C2RXIF | INT4IF | INT3IF | T9IF | T8IF | MI2C2IF | SI2C2IF | T7IF | 0000 |
| IFS4 | 0808 | — | — | — | — | QEI2IF | — | PSESMIF | — | C2TXIF | C1TXIF | DMA7IF | DMA6IF | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS5 | 080A | PWM2IF | PWM1IF | IC9IF | OC9IF | SPI3IF | SPI3EIF | U4TXIF | U4RXIF | U4EIF | USB1IF | — | — | U3TXIF | U3RXIF | U3EIF | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM4IF | PWM3IF | 0000 |
| IFS7 | 080E | IC11IF | OC11IF | IC10IF | OC10IF | SPI4IF | SPI4EIF | DMA11IF | DMA10IF | DMA9IF | DMA8IF | — | — | — | — | — | — | 0000 |
| IFS8 | 0810 | — | ICDIF | IC16IF | OC16IF | IC15IF | OC15IF | IC14IF | OC14IF | IC13IF | OC13IF | — | DMA14IF | DMA13IF | DMA12IF | IC12IF | OC12IF | 0000 |
| IEC0 | 0820 | NVMIE | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | IC8IE | IC7IE | AD2IE | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | T6IE | DMA4IE | PMPIE | OC8IE | OC7IE | OC6IE | OC5IE | IC6IE | IC5IE | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | RTCIE | DMA5IE | DCIIE | DCIEIE | QEI1IE | PSEMIE | C2IE | C2RXIE | INT4IE | INT3IE | T9IE | T8IE | MI2C2IE | SI2C2IE | T7IE | 0000 |
| IEC4 | 0828 | — | — | — | — | QEI2IE | — | PSESMIE | — | C2TXIE | C1TXIE | DMA7IE | DMA6IE | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC5 | 082A | PWM2IE | PWM1IE | IC9IE | OC9IE | SPI3IE | SPI3EIE | U4TXIE | U4RXIE | U4EIE | USB1IE | — | — | U3TXIE | U3RXIE | U3EIE | — | 0000 |
| IEC6 | 082C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM4IE | PWM3IE | 0000 |
| IEC7 | 082E | IC11IE | OC11IE | IC10IE | OC10IE | SPI4IE | SPI4EIE | DMA11IE | DMA10IE | DMA9IE | DMA8IE | — | — | — | — | — | — | 0000 |
| IEC8 | 0830 | — | ICDIE | IC16IE | OC16IE | IC15IE | OC15IE | IC14IE | OC14IE | IC13IE | OC13IE | — | DMA14IE | DMA13IE | DMA12IE | IC12IE | OC12IE | 0000 |
| IPC0 | 0840 | — | T1IP<2:0> | | | — | OC1IP<2:0> | | | — | IC1IP<2:0> | | | — | INT0IP<2:0> | | | 4444 |
| IPC1 | 0842 | — | T2IP<2:0> | | | — | OC2IP<2:0> | | | — | IC2IP<2:0> | | | — | DMA0IP<2:0> | | | 4444 |
| IPC2 | 0844 | — | U1RXIP<2:0> | | | — | SPI1IP<2:0> | | | — | SPI1EIP<2:0> | | | — | T3IP<2:0> | | | 4444 |
| IPC3 | 0846 | — | NVMIP<2:0> | | | — | DMA1IP<2:0> | | | — | AD1IP<2:0> | | | — | U1TXIP<2:0> | | | 4444 |
| IPC4 | 0848 | — | CNIP<2:0> | | | — | CMIP<2:0> | | | — | MI2C1IP<2:0> | | | — | SI2C1IP<2:0> | | | 4444 |
| IPC5 | 084A | — | IC8IP<2:0> | | | — | IC7IP<2:0> | | | — | AD2IP<2:0> | | | — | INT1IP<2:0> | | | 4444 |
| IPC6 | 084C | — | T4IP<2:0> | | | — | OC4IP<2:0> | | | — | OC3IP<2:0> | | | — | DMA2IP<2:0> | | | 4444 |
| IPC7 | 084E | — | U2TXIP<2:0> | | | — | U2RXIP<2:0> | | | — | INT2IP<2:0> | | | — | T5IP<2:0> | | | 4444 |
| IPC8 | 0850 | — | C1IP<2:0> | | | — | C1RXIP<2:0> | | | — | SPI2IP<2:0> | | | — | SPI2EIP<2:0> | | | 4444 |
| IPC9 | 0852 | — | IC5IP<2:0> | | | — | IC4IP<2:0> | | | — | IC3IP<2:0> | | | — | DMA3IP<2:0> | | | 4444 |
| IPC10 | 0854 | — | OC7IP<2:0> | | | — | OC6IP<2:0> | | | — | OC5IP<2:0> | | | — | IC6IP<2:0> | | | 4444 |
| IPC11 | 0856 | — | T6IP<2:0> | | | — | DMA4IP<2:0> | | | — | PMPIP<2:0> | | | — | OC8IP<2:0> | | | 4444 |
| IPC12 | 0858 | — | T8IP<2:0> | | | — | MI2C2IP<2:0> | | | — | SI2C2IP<2:0> | | | — | T7IP<2:0> | | | 4444 |
| IPC13 | 085A | | C2RXIP<2:0> | | | — | INT4IP<2:0> | | | — | INT3IP<2:0> | | | — | T9IP<2:0> | | | 4444 |
| IPC14 | 085C | — | DCIEIP<2:0> | | | — | QEI1IP<2:0> | | | — | PSEMIP<2:0> | | | — | C2IP<2:0> | | | 4444 |
| IPC15 | 085E | — | — | — | — | — | RTCIP<2:0> | | | — | DMA5IP<2:0> | | | — | DCIIP<2:0> | | | 0444 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IPC16 | 0860 | — | CRCIP<2:0> | | | — | U2EIP<2:0> | | | — | U1EIP<2:0> | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | C2TXIP<2:0> | | | — | C1TXIP<2:0> | | | — | DMA7IP<2:0> | | | — | DMA6IP<2:0> | | | 4444 |
| IPC18 | 0864 | — | QEI2IP<2:0> | | | — | — | — | — | — | PSESMIP<2:0> | | | — | — | — | — | 4040 |
| IPC20 | 0868 | — | U3TXIP<2:0> | | | — | U3RXIP<2:0> | | | — | U3EIP<2:0> | | | — | — | — | — | 4440 |
| IPC21 | 086A | — | U4EIP<2:0> | | | — | USB1IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC22 | 086C | — | SPI3IP<2:0> | | | — | SPI3EIP<2:0> | | | — | U4TXIP<2:0> | | | — | U4RXIP<2:0> | | | 4444 |
| IPC23 | 086E | — | PWM2IP<2:0> | | | — | PWM1IP<2:0> | | | — | IC9IP<2:0> | | | — | OC9IP<2:0> | | | 4444 |
| IPC24 | 0870 | — | — | — | — | — | — | — | — | — | PWM4IP<2:0> | | | — | PWM3IP<2:0> | | | 0044 |
| IPC29 | 087A | — | DMA9IP<2:0> | | | — | DMA8IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC30 | 087C | — | SPI4IP<2:0> | | | — | SPI4EIP<2:0> | | | — | DMA11IP<2:0> | | | — | DMA10IP<2:0> | | | 4444 |
| IPC31 | 087E | — | IC11IP<2:0> | | | — | OC11IP<2:0> | | | — | IC10IP<2:0> | | | — | OC10IP<2:0> | | | 4444 |
| IPC32 | 0880 | — | DMA13IP<2:0> | | | — | DMA12IP<2:0> | | | — | IC12IP<2:0> | | | — | OC12IP<2:0> | | | 4444 |
| IPC33 | 0882 | — | IC13IP<2:0> | | | — | OC13IP<2:0> | | | — | — | — | — | — | DMA14IP<2:0> | | | 4404 |
| IPC34 | 0884 | — | IC15IP<2:0> | | | — | OC15IP<2:0> | | | — | IC14IP<2:0> | | | — | OC14IP<2:0> | | | 4444 |
| IPC35 | 0886 | — | — | — | — | — | ICDIP<2:0> | | | — | IC16IP<2:0> | | | — | OC16IP<2:0> | | | 0444 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE | SFTACERR | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | UAE | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | — | ILR<3:0> | | | | VECNUM<7:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | NVMIF | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | IC8IF | IC7IF | AD2IF | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | T6IF | DMA4IF | PMPIF | OC8IF | OC7IF | OC6IF | OC5IF | IC6IF | IC5IF | IC4IF | IC3IF | DMA3IF | C1IF | C1RXIF | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | RTCIF | DMA5IF | DCIIF | DCIEIF | QEI1IF | PSEMIF | C2IF | C2RXIF | INT4IF | INT3IF | T9IF | T8IF | MI2C2IF | SI2C2IF | T7IF | 0000 |
| IFS4 | 0808 | — | — | — | — | QEI2IF | — | PSESMIF | — | C2TXIF | C1TXIF | DMA7IF | DMA6IF | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS5 | 080A | PWM2IF | PWM1IF | IC9IF | OC9IF | SPI3IF | SPI3EIF | U4TXIF | U4RXIF | U4EIF | — | — | — | U3TXIF | U3RXIF | U3EIF | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM4IF | PWM3IF | 0000 |
| IFS7 | 080E | IC11IF | OC11IF | IC10IF | OC10IF | SPI4IF | SPI4EIF | DMA11IF | DMA10IF | DMA9IF | DMA8IF | — | — | — | — | — | — | 0000 |
| IFS8 | 0810 | — | ICDIF | IC16IF | OC16IF | IC15IF | OC15IF | IC14IF | OC14IF | IC13IF | OC13IF | — | DMA14IF | DMA13IF | DMA12IF | IC12IF | OC12IF | 0000 |
| IEC0 | 0820 | NVMIE | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | IC8IE | IC7IE | AD2IE | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | T6IE | DMA4IE | PMPIE | OC8IE | OC7IE | OC6IE | OC5IE | IC6IE | IC5IE | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | RTCIE | DMA5IE | DCIIE | DCIEIE | QEI1IE | PSEMIE | C2IE | C2RXIE | INT4IE | INT3IE | T9IE | T8IE | MI2C2IE | SI2C2IE | T7IE | 0000 |
| IEC4 | 0828 | — | — | — | — | QEI2IE | — | PSESMIE | — | C2TXIE | C1TXIE | DMA7IE | DMA6IE | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC5 | 082A | PWM2IE | PWM1IE | IC9IE | OC9IE | SPI3IE | SPI3EIE | U4TXIE | U4RXIE | U4EIE | — | — | — | U3TXIE | U3RXIE | U3EIE | — | 0000 |
| IEC6 | 082C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM4IE | PWM3IE | 0000 |
| IEC7 | 082E | IC11IE | OC11IE | IC10IE | OC10IE | SPI4IE | SPI4EIE | DMA11IE | DMA10IE | DMA9IE | DMA8IE | — | — | — | — | — | — | 0000 |
| IEC8 | 0830 | — | ICDIE | IC16IE | OC16IE | IC15IE | OC15IE | IC14IE | OC14IE | IC13IE | OC13IE | — | DMA14IE | DMA13IE | DMA12IE | IC12IE | OC12IE | 0000 |
| IPC0 | 0840 | — | T1IP<2:0> | | | — | OC1IP<2:0> | | | — | IC1IP<2:0> | | | — | INT0IP<2:0> | | | 4444 |
| IPC1 | 0842 | — | T2IP<2:0> | | | — | OC2IP<2:0> | | | — | IC2IP<2:0> | | | — | DMA0IP<2:0> | | | 4444 |
| IPC2 | 0844 | — | U1RXIP<2:0> | | | — | SPI1IP<2:0> | | | — | SPI1EIP<2:0> | | | — | T3IP<2:0> | | | 4444 |
| IPC3 | 0846 | — | NVMIP<2:0> | | | — | DMA1IP<2:0> | | | — | AD1IP<2:0> | | | — | U1TXIP<2:0> | | | 4444 |
| IPC4 | 0848 | — | CNIP<2:0> | | | — | CMIP<2:0> | | | — | MI2C1IP<2:0> | | | — | SI2C1IP<2:0> | | | 4444 |
| IPC5 | 084A | — | IC8IP<2:0> | | | — | IC7IP<2:0> | | | — | AD2IP<2:0> | | | — | INT1IP<2:0> | | | 4444 |
| IPC6 | 084C | — | T4IP<2:0> | | | — | OC4IP<2:0> | | | — | OC3IP<2:0> | | | — | DMA2IP<2:0> | | | 4444 |
| IPC7 | 084E | — | U2TXIP<2:0> | | | — | U2RXIP<2:0> | | | — | INT2IP<2:0> | | | — | T5IP<2:0> | | | 4444 |
| IPC8 | 0850 | — | C1IP<2:0> | | | — | C1RXIP<2:0> | | | — | SPI2IP<2:0> | | | — | SPI2EIP<2:0> | | | 4444 |
| IPC9 | 0852 | — | IC5IP<2:0> | | | — | IC4IP<2:0> | | | — | IC3IP<2:0> | | | — | DMA3IP<2:0> | | | 4444 |
| IPC10 | 0854 | — | OC7IP<2:0> | | | — | OC6IP<2:0> | | | — | OC5IP<2:0> | | | — | IC6IP<2:0> | | | 4444 |
| IPC11 | 0856 | — | T6IP<2:0> | | | — | DMA4IP<2:0> | | | — | PMPIP<2:0> | | | — | OC8IP<2:0> | | | 4444 |
| IPC12 | 0858 | — | T8IP<2:0> | | | — | MI2C2IP<2:0> | | | — | SI2C2IP<2:0> | | | — | T7IP<2:0> | | | 4444 |
| IPC13 | 085A | | C2RXIP<2:0> | | | — | INT4IP<2:0> | | | — | INT3IP<2:0> | | | — | T9IP<2:0> | | | 4444 |
| IPC14 | 085C | — | DCIEIP<2:0> | | | — | QEI1IP<2:0> | | | — | PSEMIP<2:0> | | | — | C2IP<2:0> | | | 4444 |
| IPC15 | 085E | — | — | — | — | — | RTCIP<2:0> | | | — | DMA5IP<2:0> | | | — | DCIIP<2:0> | | | 0444 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC806 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IPC16 | 0860 | — | CRCIP<2:0> | | | — | U2EIP<2:0> | | | — | U1EIP<2:0> | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | C2TXIP<2:0> | | | — | C1TXIP<2:0> | | | — | DMA7IP<2:0> | | | — | DMA6IP<2:0> | | | 4444 |
| IPC18 | 0864 | — | QEI2IP<2:0> | | | — | — | — | — | — | PSESMIP<2:0> | | | — | — | — | — | 4040 |
| IPC20 | 0868 | — | U3TXIP<2:0> | | | — | U3RXIP<2:0> | | | — | U3EIP<2:0> | | | — | — | — | — | 4440 |
| IPC21 | 086A | — | U4EIP<2:0> | | | — | — | — | — | — | — | — | — | — | — | — | — | 4400 |
| IPC22 | 086C | — | SPI3IP<2:0> | | | — | SPI3EIP<2:0> | | | — | U4TXIP<2:0> | | | — | U4RXIP<2:0> | | | 4444 |
| IPC23 | 086E | — | PWM2IP<2:0> | | | — | PWM1IP<2:0> | | | — | IC9IP<2:0> | | | — | OC9IP<2:0> | | | 4444 |
| IPC24 | 0870 | — | — | — | — | — | — | — | — | — | PWM4IP<2:0> | | | — | PWM3IP<2:0> | | | 0044 |
| IPC29 | 087A | — | DMA9IP<2:0> | | | — | DMA8IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC30 | 087C | — | SPI4IP<2:0> | | | — | SPI4EIP<2:0> | | | — | DMA11IP<2:0> | | | — | DMA10IP<2:0> | | | 4444 |
| IPC31 | 087E | — | IC11IP<2:0> | | | — | OC11IP<2:0> | | | — | IC10IP<2:0> | | | — | OC10IP<2:0> | | | 4444 |
| IPC32 | 0880 | — | DMA13IP<2:0> | | | — | DMA12IP<2:0> | | | — | IC12IP<2:0> | | | — | OC12IP<2:0> | | | 4444 |
| IPC33 | 0882 | — | IC13IP<2:0> | | | — | OC13IP<2:0> | | | — | — | — | — | — | DMA14IP<2:0> | | | 4404 |
| IPC34 | 0884 | — | IC15IP<2:0> | | | — | OC15IP<2:0> | | | — | IC14IP<2:0> | | | — | OC14IP<2:0> | | | 4444 |
| IPC35 | 0886 | — | — | — | — | — | ICDIP<2:0> | | | — | IC16IP<2:0> | | | — | OC16IP<2:0> | | | 0444 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE | SFTACERR | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | UAE | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | — | ILR<3:0> | | | | VECNUM<7:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP806 AND PIC24EPXXXGP806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | NVMIF | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | IC8IF | IC7IF | AD2IF | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | T6IF | DMA4IF | PMPIF | OC8IF | OC7IF | OC6IF | OC5IF | IC6IF | IC5IF | IC4IF | IC3IF | DMA3IF | C1IF | C1RXIF | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | RTCIF | DMA5IF | DCIIF | DCIEIF | — | PSEMIF | C2IF | C2RXIF | INT4IF | INT3IF | T9IF | T8IF | MI2C2IF | SI2C2IF | T7IF | 0000 |
| IFS4 | 0808 | — | — | — | — | — | — | PSESMIF | — | C2TXIF | C1TXIF | DMA7IF | DMA6IF | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS5 | 080A | — | — | IC9IF | OC9IF | SPI3IF | SPI3EIF | U4TXIF | U4RXIF | U4EIF | — | — | — | U3TXIF | U3RXIF | U3EIF | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS7 | 080E | IC11IF | OC11IF | IC10IF | OC10IF | SPI4IF | SPI4EIF | DMA11IF | DMA10IF | DMA9IF | DMA8IF | — | — | — | — | — | — | 0000 |
| IFS8 | 0810 | — | ICDIF | IC16IF | OC16IF | IC15IF | OC15IF | IC14IF | OC14IF | IC13IF | OC13IF | — | DMA14IF | DMA13IF | DMA12IF | IC12IF | OC12IF | 0000 |
| IEC0 | 0820 | NVMIE | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | IC8IE | IC7IE | AD2IE | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | T6IE | DMA4IE | PMPIE | OC8IE | OC7IE | OC6IE | OC5IE | IC6IE | IC5IE | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | RTCIE | DMA5IE | DCIIE | DCIEIE | — | PSEMIE | C2IE | C2RXIE | INT4IE | INT3IE | T9IE | T8IE | MI2C2IE | SI2C2IE | T7IE | 0000 |
| IEC4 | 0828 | — | — | — | — | — | — | PSESMIE | — | C2TXIE | C1TXIE | DMA7IE | DMA6IE | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC5 | 082A | — | — | IC9IE | OC9IE | SPI3IE | SPI3EIE | U4TXIE | U4RXIE | U4EIE | — | — | — | U3TXIE | U3RXIE | U3EIE | — | 0000 |
| IEC6 | 082C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC7 | 082E | IC11IE | OC11IE | IC10IE | OC10IE | SPI4IE | SPI4EIE | DMA11IE | DMA10IE | DMA9IE | DMA8IE | — | — | — | — | — | — | 0000 |
| IEC8 | 0830 | — | ICDIE | IC16IE | OC16IE | IC15IE | OC15IE | IC14IE | OC14IE | IC13IE | OC13IE | — | DMA14IE | DMA13IE | DMA12IE | IC12IE | OC12IE | 0000 |
| IPC0 | 0840 | — | T1IP<2:0> | | | — | OC1IP<2:0> | | | — | IC1IP<2:0> | | | — | INT0IP<2:0> | | | 4444 |
| IPC1 | 0842 | — | T2IP<2:0> | | | — | OC2IP<2:0> | | | — | IC2IP<2:0> | | | — | DMA0IP<2:0> | | | 4444 |
| IPC2 | 0844 | — | U1RXIP<2:0> | | | — | SPI1IP<2:0> | | | — | SPI1EIP<2:0> | | | — | T3IP<2:0> | | | 4444 |
| IPC3 | 0846 | — | NVMIP<2:0> | | | — | DMA1IP<2:0> | | | — | AD1IP<2:0> | | | — | U1TXIP<2:0> | | | 4444 |
| IPC4 | 0848 | — | CNIP<2:0> | | | — | CMIP<2:0> | | | — | MI2C1IP<2:0> | | | — | SI2C1IP<2:0> | | | 4444 |
| IPC5 | 084A | — | IC8IP<2:0> | | | — | IC7IP<2:0> | | | — | AD2IP<2:0> | | | — | INT1IP<2:0> | | | 4444 |
| IPC6 | 084C | — | T4IP<2:0> | | | — | OC4IP<2:0> | | | — | OC3IP<2:0> | | | — | DMA2IP<2:0> | | | 4444 |
| IPC7 | 084E | — | U2TXIP<2:0> | | | — | U2RXIP<2:0> | | | — | INT2IP<2:0> | | | — | T5IP<2:0> | | | 4444 |
| IPC8 | 0850 | — | C1IP<2:0> | | | — | C1RXIP<2:0> | | | — | SPI2IP<2:0> | | | — | SPI2EIP<2:0> | | | 4444 |
| IPC9 | 0852 | — | IC5IP<2:0> | | | — | IC4IP<2:0> | | | — | IC3IP<2:0> | | | — | DMA3IP<2:0> | | | 4444 |
| IPC10 | 0854 | — | OC7IP<2:0> | | | — | OC6IP<2:0> | | | — | OC5IP<2:0> | | | — | IC6IP<2:0> | | | 4444 |
| IPC11 | 0856 | — | T6IP<2:0> | | | — | DMA4IP<2:0> | | | — | PMPIP<2:0> | | | — | OC8IP<2:0> | | | 4444 |
| IPC12 | 0858 | — | T8IP<2:0> | | | — | MI2C2IP<2:0> | | | — | SI2C2IP<2:0> | | | — | T7IP<2:0> | | | 4444 |
| IPC13 | 085A | | C2RXIP<2:0> | | | — | INT4IP<2:0> | | | — | INT3IP<2:0> | | | — | T9IP<2:0> | | | 4444 |
| IPC14 | 085C | — | DCIEIP<2:0> | | | — | — | — | — | — | PSEMIP<2:0> | | | — | C2IP<2:0> | | | 4444 |
| IPC15 | 085E | — | — | — | — | — | RTCIP<2:0> | | | — | DMA5IP<2:0> | | | — | DCIIP<2:0> | | | 0444 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP806 AND PIC24EPXXXGP806 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IPC16 | 0860 | — | CRCIP<2:0> | | | — | U2EIP<2:0> | | | — | U1EIP<2:0> | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | C2TXIP<2:0> | | | — | C1TXIP<2:0> | | | — | DMA7IP<2:0> | | | — | DMA6IP<2:0> | | | 4444 |
| IPC18 | 0864 | — | — | — | — | — | — | — | — | — | PSESMIP<2:0> | | | — | — | — | — | 4040 |
| IPC20 | 0868 | — | U3TXIP<2:0> | | | — | U3RXIP<2:0> | | | — | U3EIP<2:0> | | | — | — | — | — | 4440 |
| IPC21 | 086A | — | U4EIP<2:0> | | | — | — | — | — | — | — | — | — | — | — | — | — | 4400 |
| IPC22 | 086C | — | SPI3IP<2:0> | | | — | SPI3EIP<2:0> | | | — | U4TXIP<2:0> | | | — | U4RXIP<2:0> | | | 4444 |
| IPC23 | 086E | — | — | — | — | — | — | — | — | — | IC9IP<2:0> | | | — | OC9IP<2:0> | | | 4444 |
| IPC24 | 0870 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0044 |
| IPC29 | 087A | — | DMA9IP<2:0> | | | — | DMA8IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC30 | 087C | — | SPI4IP<2:0> | | | — | SPI4EIP<2:0> | | | — | DMA11IP<2:0> | | | — | DMA10IP<2:0> | | | 4444 |
| IPC31 | 087E | — | IC11IP<2:0> | | | — | OC11IP<2:0> | | | — | IC10IP<2:0> | | | — | OC10IP<2:0> | | | 4444 |
| IPC32 | 0880 | — | DMA13IP<2:0> | | | — | DMA12IP<2:0> | | | — | IC12IP<2:0> | | | — | OC12IP<2:0> | | | 4444 |
| IPC33 | 0882 | — | IC13IP<2:0> | | | — | OC13IP<2:0> | | | — | — | — | — | — | DMA14IP<2:0> | | | 4404 |
| IPC34 | 0884 | — | IC15IP<2:0> | | | — | OC15IP<2:0> | | | — | IC14IP<2:0> | | | — | OC14IP<2:0> | | | 4444 |
| IPC35 | 0886 | — | — | — | — | — | ICDIP<2:0> | | | — | IC16IP<2:0> | | | — | OC16IP<2:0> | | | 0444 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE | SFTACERR | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | UAE | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | — | ILR<3:0> | | | | VECNUM<7:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-8: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | NVMIF | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | IC8IF | IC7IF | AD2IF | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | T6IF | DMA4IF | PMPIF | OC8IF | OC7IF | OC6IF | OC5IF | IC6IF | IC5IF | IC4IF | IC3IF | DMA3IF | C1IF | C1RXIF | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | RTCIF | DMA5IF | DCIIF | DCIEIF | — | — | C2IF | C2RXIF | INT4IF | INT3IF | T9IF | T8IF | MI2C2IF | SI2C2IF | T7IF | 0000 |
| IFS4 | 0808 | — | — | — | — | — | — | — | — | C2TXIF | C1TXIF | DMA7IF | DMA6IF | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS5 | 080A | — | — | IC9IF | OC9IF | SPI3IF | SPI3EIF | U4TXIF | U4RXIF | U4EIF | USB1IF | — | — | U3TXIF | U3RXIF | U3EIF | — | 0000 |
| IFS7 | 080E | IC11IF | OC11IF | IC10IF | OC10IF | SPI4IF | SPI4EIF | DMA11IF | DMA10IF | DMA9IF | DMA8IF | — | — | — | — | — | — | 0000 |
| IFS8 | 0810 | — | ICDIF | IC16IF | OC16IF | IC15IF | OC15IF | IC14IF | OC14IF | IC13IF | OC13IF | — | DMA14IF | DMA13IF | DMA12IF | IC12IF | OC12IF | 0000 |
| IEC0 | 0820 | NVMIE | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | IC8IE | IC7IE | AD2IE | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | T6IE | DMA4IE | PMPIE | OC8IE | OC7IE | OC6IE | OC5IE | IC6IE | IC5IE | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | RTCIE | DMA5IE | DCIIE | DCIEIE | — | — | C2IE | C2RXIE | INT4IE | INT3IE | T9IE | T8IE | MI2C2IE | SI2C2IE | T7IE | 0000 |
| IEC4 | 0828 | — | — | — | — | — | — | — | — | C2TXIE | C1TXIE | DMA7IE | DMA6IE | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC5 | 082A | — | — | IC9IE | OC9IE | SPI3IE | SPI3EIE | U4TXIE | U4RXIE | U4EIE | USB1IE | — | — | U3TXIE | U3RXIE | U3EIE | — | 0000 |
| IEC7 | 082E | IC11IE | OC11IE | IC10IE | OC10IE | SPI4IE | SPI4EIE | DMA11IE | DMA10IE | DMA9IE | DMA8IE | — | — | — | — | — | — | 0000 |
| IEC8 | 0830 | — | ICDIE | IC16IE | OC16IE | IC15IE | OC15IE | IC14IE | OC14IE | IC13IE | OC13IE | — | DMA14IE | DMA13IE | DMA12IE | IC12IE | OC12IE | 0000 |
| IPC0 | 0840 | — | T1IP<2:0> | | | — | OC1IP<2:0> | | | — | IC1IP<2:0> | | | — | INT0IP<2:0> | | | 4444 |
| IPC1 | 0842 | — | T2IP<2:0> | | | — | OC2IP<2:0> | | | — | IC2IP<2:0> | | | — | DMA0IP<2:0> | | | 4444 |
| IPC2 | 0844 | — | U1RXIP<2:0> | | | — | SPI1IP<2:0> | | | — | SPI1EIP<2:0> | | | — | T3IP<2:0> | | | 4444 |
| IPC3 | 0846 | — | NVMIP<2:0> | | | — | DMA1IP<2:0> | | | — | AD1IP<2:0> | | | — | U1TXIP<2:0> | | | 4444 |
| IPC4 | 0848 | — | CNIP<2:0> | | | — | CMIP<2:0> | | | — | MI2C1IP<2:0> | | | — | SI2C1IP<2:0> | | | 4444 |
| IPC5 | 084A | — | IC8IP<2:0> | | | — | IC7IP<2:0> | | | — | AD2IP<2:0> | | | — | INT1IP<2:0> | | | 4444 |
| IPC6 | 084C | — | T4IP<2:0> | | | — | OC4IP<2:0> | | | — | OC3IP<2:0> | | | — | DMA2IP<2:0> | | | 4444 |
| IPC7 | 084E | — | U2TXIP<2:0> | | | — | U2RXIP<2:0> | | | — | INT2IP<2:0> | | | — | T5IP<2:0> | | | 4444 |
| IPC8 | 0850 | — | C1IP<2:0> | | | — | C1RXIP<2:0> | | | — | SPI2IP<2:0> | | | — | SPI2EIP<2:0> | | | 4444 |
| IPC9 | 0852 | — | IC5IP<2:0> | | | — | IC4IP<2:0> | | | — | IC3IP<2:0> | | | — | DMA3IP<2:0> | | | 4444 |
| IPC10 | 0854 | — | OC7IP<2:0> | | | — | OC6IP<2:0> | | | — | OC5IP<2:0> | | | — | IC6IP<2:0> | | | 4444 |
| IPC11 | 0856 | — | T6IP<2:0> | | | — | DMA4IP<2:0> | | | — | PMPIP<2:0> | | | — | OC8IP<2:0> | | | 4444 |
| IPC12 | 0858 | — | T8IP<2:0> | | | — | MI2C2IP<2:0> | | | — | SI2C2IP<2:0> | | | — | T7IP<2:0> | | | 4444 |
| IPC13 | 085A | | C2RXIP<2:0> | | | — | INT4IP<2:0> | | | — | INT3IP<2:0> | | | — | T9IP<2:0> | | | 4444 |
| IPC14 | 085C | — | DCIEIP<2:0> | | | — | — | — | — | — | — | — | — | — | C2IP<2:0> | | | 4004 |
| IPC15 | 085E | — | — | — | — | — | RTCIP<2:0> | | | — | DMA5IP<2:0> | | | — | DCIIP<2:0> | | | 0444 |
| IPC16 | 0860 | — | CRCIP<2:0> | | | — | U2EIP<2:0> | | | — | U1EIP<2:0> | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | C2TXIP<2:0> | | | — | C1TXIP<2:0> | | | — | DMA7IP<2:0> | | | — | DMA6IP<2:0> | | | 4444 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-8: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGU810/814 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IPC20 | 0868 | — | U3TXIP<2:0> | | | — | U3RXIP<2:0> | | | — | U3EIP<2:0> | | | — | — | — | — | 4440 |
| IPC21 | 086A | — | U4EIP<2:0> | | | — | USB1IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC22 | 086C | — | SPI3IP<2:0> | | | — | SPI3EIP<2:0> | | | — | U4TXIP<2:0> | | | — | U4RXIP<2:0> | | | 4444 |
| IPC23 | 086E | — | — | — | — | — | — | — | — | — | IC9IP<2:0> | | | — | OC9IP<2:0> | | | 0044 |
| IPC29 | 087A | — | DMA9IP<2:0> | | | — | DMA8IP<2:0> | | | — | — | — | — | — | — | — | — | 4400 |
| IPC30 | 087C | — | SPI4IP<2:0> | | | — | SPI4EIP<2:0> | | | — | DMA11IP<2:0> | | | — | DMA10IP<2:0> | | | 4444 |
| IPC31 | 087E | — | IC11IP<2:0> | | | — | OC11IP<2:0> | | | — | IC10IP<2:0> | | | — | OC10IP<2:0> | | | 4444 |
| IPC32 | 0880 | — | DMA13IP<2:0> | | | — | DMA12IP<2:0> | | | — | IC12IP<2:0> | | | — | OC12IP<2:0> | | | 4444 |
| IPC33 | 0882 | — | IC13IP<2:0> | | | — | OC13IP<2:0> | | | — | — | — | — | — | DMA14IP<2:0> | | | 4404 |
| IPC34 | 0884 | — | IC15IP<2:0> | | | — | OC15IP<2:0> | | | — | IC14IP<2:0> | | | — | OC14IP<2:0> | | | 4444 |
| IPC35 | 0886 | — | — | — | — | — | ICDIP<2:0> | | | — | IC16IP<2:0> | | | — | OC16IP<2:0> | | | 4444 |
| INTCON1 | 08C0 | NSTDIS | — | — | — | — | — | — | — | — | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | UAE | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | — | ILR<3:0> | | | | VECNUM<7:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-9: TIMER1 THROUGH TIMER9 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMR1 | 0100 | Timer1 Register | | | | | | | | | | | | | | | | xxxx |
| PR1 | 0102 | Period Register 1 | | | | | | | | | | | | | | | | FFFF |
| T1CON | 0104 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS<1:0> | | — | TSYNC | TCS | — | 0000 |
| TMR2 | 0106 | Timer2 Register | | | | | | | | | | | | | | | | xxxx |
| TMR3HLD | 0108 | Timer3 Holding Register (for 32-bit timer operations only) | | | | | | | | | | | | | | | | xxxx |
| TMR3 | 010A | Timer3 Register | | | | | | | | | | | | | | | | xxxx |
| PR2 | 010C | Period Register 2 | | | | | | | | | | | | | | | | FFFF |
| PR3 | 010E | Period Register 3 | | | | | | | | | | | | | | | | FFFF |
| T2CON | 0110 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS<1:0> | | T32 | — | TCS | — | 0000 |
| T3CON | 0112 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS<1:0> | | — | — | TCS | — | 0000 |
| TMR4 | 0114 | Timer4 Register | | | | | | | | | | | | | | | | xxxx |
| TMR5HLD | 0116 | Timer5 Holding Register (for 32-bit operations only) | | | | | | | | | | | | | | | | xxxx |
| TMR5 | 0118 | Timer5 Register | | | | | | | | | | | | | | | | xxxx |
| PR4 | 011A | Period Register 4 | | | | | | | | | | | | | | | | FFFF |
| PR5 | 011C | Period Register 5 | | | | | | | | | | | | | | | | FFFF |
| T4CON | 011E | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS<1:0> | | T32 | — | TCS | — | 0000 |
| T5CON | 0120 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS<1:0> | | — | — | TCS | — | 0000 |
| TMR6 | 0122 | Timer6 Register | | | | | | | | | | | | | | | | xxxx |
| TMR7HLD | 0124 | Timer7 Holding Register (for 32-bit operations only) | | | | | | | | | | | | | | | | xxxx |
| TMR7 | 0126 | Timer7 Register | | | | | | | | | | | | | | | | xxxx |
| PR6 | 0128 | Period Register 6 | | | | | | | | | | | | | | | | FFFF |
| PR7 | 012A | Period Register 7 | | | | | | | | | | | | | | | | FFFF |
| T6CON | 012C | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS<1:0> | | T32 | — | TCS | — | 0000 |
| T7CON | 012E | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS<1:0> | | — | — | TCS | — | 0000 |
| TMR8 | 0130 | Timer8 Register | | | | | | | | | | | | | | | | xxxx |
| TMR9HLD | 0132 | Timer9 Holding Register (for 32-bit operations only) | | | | | | | | | | | | | | | | xxxx |
| TMR9 | 0134 | Timer9 Register | | | | | | | | | | | | | | | | xxxx |
| PR8 | 0136 | Period Register 8 | | | | | | | | | | | | | | | | FFFF |
| PR9 | 0138 | Period Register 9 | | | | | | | | | | | | | | | | FFFF |
| T8CON | 013A | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS<1:0> | | T32 | — | TCS | — | 0000 |
| T9CON | 013C | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS<1:0> | | — | — | TCS | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-10: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 16 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IC1CON1 | 0140 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC1CON2 | 0142 | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC1BUF | 0144 | Input Capture 1 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC1TMR | 0146 | Input Capture 1 Timer | | | | | | | | | | | | | | | | 0000 |
| IC2CON1 | 0148 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC2CON2 | 014A | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC2BUF | 014C | Input Capture 2 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC2TMR | 014E | Input Capture 2 Timer | | | | | | | | | | | | | | | | 0000 |
| IC3CON1 | 0150 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC3CON2 | 0152 | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC3BUF | 0154 | Input Capture 3 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC3TMR | 0156 | Input Capture 3 Timer | | | | | | | | | | | | | | | | 0000 |
| IC4CON1 | 0158 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC4CON2 | 015A | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC4BUF | 015C | Input Capture 4 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC4TMR | 015E | Input Capture 4 Timer | | | | | | | | | | | | | | | | 0000 |
| IC5CON1 | 0160 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC5CON2 | 0162 | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC5BUF | 0164 | Input Capture 5 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC5TMR | 0166 | Input Capture 5 Timer | | | | | | | | | | | | | | | | 0000 |
| IC6CON1 | 0168 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC6CON2 | 016A | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC6BUF | 016C | Input Capture 6 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC6TMR | 016E | Input Capture 6 Timer | | | | | | | | | | | | | | | | 0000 |
| IC7CON1 | 0170 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC7CON2 | 0172 | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC7BUF | 0174 | Input Capture 7 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC7TMR | 0176 | Input Capture 7 Timer | | | | | | | | | | | | | | | | 0000 |
| IC8CON1 | 0178 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC8CON2 | 017A | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC8BUF | 017C | Input Capture 8 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC8TMR | 017E | Input Capture 8 Timer | | | | | | | | | | | | | | | | 0000 |

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**TABLE 4-10: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 16 REGISTER MAP (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IC9CON1 | 0180 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC9CON2 | 0182 | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC9BUF | 0184 | Input Capture 9 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC9TMR | 0186 | Input Capture 9 Timer | | | | | | | | | | | | | | | | 0000 |
| IC10CON1 | 0188 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC10CON2 | 018A | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC10BUF | 018C | Input Capture 10 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC10TMR | 018E | Input Capture 10 Timer | | | | | | | | | | | | | | | | 0000 |
| IC11CON1 | 0190 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC11CON2 | 0192 | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC11BUF | 0194 | Input Capture 11 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC11TMR | 0196 | Input Capture 11 Timer | | | | | | | | | | | | | | | | 0000 |
| IC12CON1 | 0198 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC12CON2 | 019A | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC12BUF | 019C | Input Capture 12 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC12TMR | 019E | Input Capture 12 Timer | | | | | | | | | | | | | | | | 0000 |
| IC13CON1 | 01A0 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC13CON2 | 01A2 | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC13BUF | 01A4 | Input Capture 13 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC13TMR | 01A6 | Input Capture 13 Timer | | | | | | | | | | | | | | | | 0000 |
| IC14CON1 | 01A8 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC14CON2 | 01AA | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC14BUF | 01AC | Input Capture 14 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC14TMR | 01AE | Input Capture 14 Timer | | | | | | | | | | | | | | | | 0000 |
| IC15CON1 | 01B0 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC15CON2 | 01B2 | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC15BUF | 01B4 | Input Capture 15 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC15TMR | 01B6 | Input Capture 15 Timer | | | | | | | | | | | | | | | | 0000 |
| IC16CON1 | 01B8 | — | — | ICSIDL | ICTSEL<2:0> | | | — | — | — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| IC16CON2 | 01BA | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL<4:0> | | | | | 000D |
| IC16BUF | 01BC | Input Capture 16 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC16TMR | 01BE | Input Capture 16 Timer | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-11: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 16 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OC1CON1 | 0900 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC1CON2 | 0902 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC1RS | 0904 | Output Compare 1 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC1R | 0906 | Output Compare 1 Register | | | | | | | | | | | | | | | | xxxx |
| OC1TMR | 0908 | Timer Value 1 Register | | | | | | | | | | | | | | | | xxxx |
| OC2CON1 | 090A | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC2CON2 | 090C | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC2RS | 090E | Output Compare 2 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC2R | 0910 | Output Compare 2 Register | | | | | | | | | | | | | | | | xxxx |
| OC2TMR | 0912 | Timer Value 2 Register | | | | | | | | | | | | | | | | xxxx |
| OC3CON1 | 0914 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC3CON2 | 0916 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC3RS | 0918 | Output Compare 3 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC3R | 091A | Output Compare 3 Register | | | | | | | | | | | | | | | | xxxx |
| OC3TMR | 091C | Timer Value 3 Register | | | | | | | | | | | | | | | | xxxx |
| OC4CON1 | 091E | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC4CON2 | 0920 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC4RS | 0922 | Output Compare 4 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC4R | 0924 | Output Compare 4 Register | | | | | | | | | | | | | | | | xxxx |
| OC4TMR | 0926 | Timer Value 4 Register | | | | | | | | | | | | | | | | xxxx |
| OC5CON1 | 0928 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC5CON2 | 092A | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC5RS | 092C | Output Compare 5 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC5R | 092D | Output Compare 5 Register | | | | | | | | | | | | | | | | xxxx |
| OC5TMR | 0930 | Timer Value 5 Register | | | | | | | | | | | | | | | | xxxx |
| OC6CON1 | 0932 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC6CON2 | 0934 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC6RS | 0936 | Output Compare 6 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC6R | 0938 | Output Compare 6 Register | | | | | | | | | | | | | | | | xxxx |
| OC6TMR | 093A | Timer Value 6 Register | | | | | | | | | | | | | | | | xxxx |
| OC7CON1 | 093C | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC7CON2 | 093E | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC7RS | 0940 | Output Compare 7 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC7R | 0942 | Output Compare 7 Register | | | | | | | | | | | | | | | | xxxx |
| OC7TMR | 0944 | Timer Value 7 Register | | | | | | | | | | | | | | | | xxxx |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-11: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 16 REGISTER MAP (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OC8CON1 | 0946 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC8CON2 | 0948 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC8RS | 094A | Output Compare 8 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC8R | 094C | Output Compare 8 Register | | | | | | | | | | | | | | | | xxxx |
| OC8TMR | 094E | Timer Value 8 Register | | | | | | | | | | | | | | | | xxxx |
| OC9CON1 | 0950 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC9CON2 | 0952 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC9RS | 0954 | Output Compare 9 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC9R | 0956 | Output Compare 9 Register | | | | | | | | | | | | | | | | xxxx |
| OC9TMR | 0958 | Timer Value 9 Register | | | | | | | | | | | | | | | | xxxx |
| OC10CON1 | 095A | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC10CON2 | 095C | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC10RS | 095E | Output Compare 10 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC10R | 0960 | Output Compare 10 Register | | | | | | | | | | | | | | | | xxxx |
| OC10TMR | 0962 | Timer Value 10 Register | | | | | | | | | | | | | | | | xxxx |
| OC11CON1 | 0964 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC11CON2 | 0966 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC11RS | 0968 | Output Compare 11 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC11R | 096A | Output Compare 11 Register | | | | | | | | | | | | | | | | xxxx |
| OC11TMR | 096C | Timer Value 11 Register | | | | | | | | | | | | | | | | xxxx |
| OC12CON1 | 096E | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC12CON2 | 0970 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC12RS | 0972 | Output Compare 12 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC12R | 0974 | Output Compare 12 Register | | | | | | | | | | | | | | | | xxxx |
| OC12TMR | 0976 | Timer Value 12 Register | | | | | | | | | | | | | | | | xxxx |
| OC13CON1 | 0978 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC13CON2 | 097A | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC13RS | 097C | Output Compare 13 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC13R | 097E | Output Compare 13 Register | | | | | | | | | | | | | | | | xxxx |
| OC13TMR | 0980 | Timer Value 13 Register | | | | | | | | | | | | | | | | xxxx |
| OC14CON1 | 0982 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC14CON2 | 0984 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC14RS | 0986 | Output Compare 14 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC14R | 0988 | Output Compare 14 Register | | | | | | | | | | | | | | | | xxxx |
| OC14TMR | 098A | Timer Value 14 Register | | | | | | | | | | | | | | | | xxxx |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-11: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 16 REGISTER MAP (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OC15CON1 | 098C | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC15CON2 | 098E | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC15RS | 0990 | Output Compare 15 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC15R | 0992 | Output Compare 15 Register | | | | | | | | | | | | | | | | xxxx |
| OC15TMR | 0994 | Timer Value 15 Register | | | | | | | | | | | | | | | | xxxx |
| OC16CON1 | 0996 | — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB | ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | | 0000 |
| OC16CON2 | 0998 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | | 000C |
| OC16RS | 099A | Output Compare 16 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC16R | 099C | Output Compare 16 Register | | | | | | | | | | | | | | | | xxxx |
| OC16TMR | 099E | Timer Value 16 Register | | | | | | | | | | | | | | | | xxxx |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-12: PWM REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PTCON | 0C00 | PTEN | — | PTSIDL | SESTAT | SEIEN | EIPU | SYNCPOL | SYNCOEN | SYNCEN | SYNCSRC<2:0> | | | SEVTPS<3:0> | | | | 0000 |
| PTCON2 | 0C02 | — | — | — | — | — | — | — | — | — | — | — | — | — | PCLKDIV<2:0> | | | 0000 |
| PTPER | 0C04 | PTPER<15:0> | | | | | | | | | | | | | | | | FFF8 |
| SEVTCMP | 0C06 | SEVTCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| MDC | 0C0A | MDC<15:0> | | | | | | | | | | | | | | | | 0000 |
| STCON | 0C0E | — | — | — | SESTAT | SEIEN | EIPU | SYNCPOL | SYNCOEN | SYNCEN | SYNCSRC<2:0> | | | SEVTPS<3:0> | | | | 0000 |
| STCON2 | 0C10 | — | — | — | — | — | — | — | — | — | — | — | — | — | PCLKDIV<2:0> | | | 0000 |
| STPER | 0C12 | STPER<15:0> | | | | | | | | | | | | | | | | FFF8 |
| SSEVTCMP | 0C14 | SSEVTCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| CHOP | 0C1A | CHPCLKEN | — | — | — | — | — | CHOPCLK<9:0> | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-13: PWM GENERATOR 1 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON1 | 0C20 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC<1:0> | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON1 | 0C22 | PENH | PENL | POLH | POLL | PMOD<1:0> | | OVRENH | OVRENL | OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC | 0000 |
| FCLCON1 | 0C24 | IFLTMOD | CLSRC<4:0> | | | | | CLPOL | CLMOD | FLTSRC<4:0> | | | | | FLTPOL | FLTMOD<1:0> | | 0000 |
| PDC1 | 0C26 | PDC1<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE1 | 0C28 | PHASE1<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR1 | 0C2A | — | — | DTR1<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR1 | 0C2C | — | — | ALTDTR1<13:0> | | | | | | | | | | | | | | 0000 |
| SDC1 | 0C2E | SDC1<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE1 | 0C30 | SPHASE1<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG1 | 0C32 | TRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON1 | 0C34 | TRGDIV<3:0> | | | | — | — | — | — | — | — | TRGSTRT<5:0> | | | | | | 0000 |
| PWMCAP1 | 0C38 | PWMCAP1<15:0> | | | | | | | | | | | | | | | | 0000 |
| LEBCON1 | 0C3A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY1 | 0C3C | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON1 | 0C3E | — | — | — | — | BLANKSEL<3:0> | | | | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-14: PWM GENERATOR 2 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON2 | 0C40 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC<1:0> | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON2 | 0C42 | PENH | PENL | POLH | POLL | PMOD<1:0> | | OVRENH | OVRENL | OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC | 0000 |
| FCLCON2 | 0C44 | IFLTMOD | CLSRC<4:0> | | | | | CLPOL | CLMOD | FLTSRC<4:0> | | | | | FLTPOL | FLTMOD<1:0> | | 0000 |
| PDC2 | 0C46 | PDC2<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE2 | 0C48 | PHASE2<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR2 | 0C4A | — | — | DTR2<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR2 | 0C4C | — | — | ALTDTR2<13:0> | | | | | | | | | | | | | | 0000 |
| SDC2 | 0C4E | SDC2<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE2 | 0C50 | SPHASE2<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG2 | 0C52 | TRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON2 | 0C54 | TRGDIV<3:0> | | | | — | — | — | — | — | — | TRGSTRT<5:0> | | | | | | 0000 |
| PWMCAP2 | 0C58 | PWMCAP2<15:0> | | | | | | | | | | | | | | | | 0000 |
| LEBCON2 | 0C5A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY2 | 0C5C | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON2 | 0C5E | — | — | — | — | BLANKSEL<3:0> | | | | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-15: PWM GENERATOR 3 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON3 | 0C60 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC<1:0> | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON3 | 0C62 | PENH | PENL | POLH | POLL | PMOD<1:0> | | OVRENH | OVRENL | OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC | 0000 |
| FCLCON3 | 0C64 | IFLTMOD | CLSRC<4:0> | | | | | CLPOL | CLMOD | FLTSRC<4:0> | | | | | FLTPOL | FLTMOD<1:0> | | 0000 |
| PDC3 | 0C66 | PDC3<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE3 | 0C68 | PHASE3<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR3 | 0C6A | — | — | DTR3<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR3 | 0C6C | — | — | ALTDTR3<13:0> | | | | | | | | | | | | | | 0000 |
| SDC3 | 0C6E | SDC3<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE3 | 0C70 | SPHASE3<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG3 | 0C72 | TRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON3 | 0C74 | TRGDIV<3:0> | | | | — | — | — | — | — | — | TRGSTRT<5:0> | | | | | | 0000 |
| PWMCAP3 | 0C78 | PWMCAP3<15:0> | | | | | | | | | | | | | | | | 0000 |
| LEBCON3 | 0C7A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY3 | 0C7C | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON3 | 0C7E | — | — | — | — | BLANKSEL<3:0> | | | | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-16: PWM GENERATOR 4 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON4 | 0C80 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC<1:0> | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON4 | 0C82 | PENH | PENL | POLH | POLL | PMOD<1:0> | | OVRENH | OVRENL | OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC | 0000 |
| FCLCON4 | 0C84 | IFLTMOD | CLSRC<4:0> | | | | | CLPOL | CLMOD | FLTSRC<4:0> | | | | | FLTPOL | FLTMOD<1:0> | | 0000 |
| PDC4 | 0C86 | PDC4<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE4 | 0C88 | PHASE4<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR4 | 0C8A | — | — | DTR4<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR4 | 0C8C | — | — | ALTDTR4<13:0> | | | | | | | | | | | | | | 0000 |
| SDC4 | 0C8E | SDC4<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE4 | 0C90 | SPHASE4<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG4 | 0C92 | TRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON4 | 0C94 | TRGDIV<3:0> | | | | — | — | — | — | — | — | TRGSTRT<5:0> | | | | | | 0000 |
| PWMCAP4 | 0C98 | PWMCAP4<15:0> | | | | | | | | | | | | | | | | 0000 |
| LEBCON4 | 0C9A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY4 | 0C9C | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON4 | 0C9E | — | — | — | — | BLANKSEL<3:0> | | | | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-17: PWM GENERATOR 5 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON5 | 0CA0 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC<1:0> | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON5 | 0CA2 | PENH | PENL | POLH | POLL | PMOD<1:0> | | OVRENH | OVRENL | OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC | 0000 |
| FCLCON5 | 0CA4 | IFLTMOD | CLSRC<4:0> | | | | | CLPOL | CLMOD | FLTSRC<4:0> | | | | | FLTPOL | FLTMOD<1:0> | | 0000 |
| PDC5 | 0CA6 | PDC5<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE5 | 0CA8 | PHASE5<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR5 | 0CAA | — | — | DTR5<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR5 | 0CAC | — | — | ALTDTR5<13:0> | | | | | | | | | | | | | | 0000 |
| SDC5 | 0CAE | SDC5<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE5 | 0CB0 | SPHASE5<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG5 | 0CB2 | TRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON5 | 0CB4 | TRGDIV<3:0> | | | | — | — | — | — | — | — | TRGSTRT<5:0> | | | | | | 0000 |
| PWMCAP5 | 0CB8 | PWM Capture<15:0> | | | | | | | | | | | | | | | | 0000 |
| LEBCON5 | 0CBA | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY5 | 0CBC | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON5 | 0CBE | — | — | — | — | BLANKSEL<3:0> | | | | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-18: PWM GENERATOR 6 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON6 | 0CC0 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC<1:0> | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON6 | 0CC2 | PENH | PENL | POLH | POLL | PMOD<1:0> | | OVRENH | OVRENL | OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC | 0000 |
| FCLCON6 | 0CC4 | IFLTMOD | CLSRC<4:0> | | | | | CLPOL | CLMOD | FLTSRC<4:0> | | | | | FLTPOL | FLTMOD<1:0> | | 0000 |
| PDC6 | 0CC6 | PDC6<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE6 | 0CC8 | PHASE6<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR6 | 0CCA | — | — | DTR6<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR6 | 0CCC | — | — | ALTDTR6<13:0> | | | | | | | | | | | | | | 0000 |
| SDC6 | 0CCE | SDC6<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE6 | 0CD0 | SPHASE6<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG6 | 0CD2 | TRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON6 | 0CD4 | TRGDIV<3:0> | | | | — | — | — | — | — | — | TRGSTRT<5:0> | | | | | | 0000 |
| PWMCAP6 | 0CD8 | PWMCAP6<15:0> | | | | | | | | | | | | | | | | 0000 |
| LEBCON6 | 0CDA | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY6 | 0CDC | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON6 | 0CDE | — | — | — | — | BLANKSEL<3:0> | | | | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-19: PWM GENERATOR 7 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON7 | 0CE0 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC<1:0> | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON7 | 0CE2 | PENH | PENL | POLH | POLL | PMOD<1:0> | | OVRENH | OVRENL | OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC | 0000 |
| FCLCON7 | 0CE4 | IFLTMOD | CLSRC<4:0> | | | | | CLPOL | CLMOD | FLTSRC<4:0> | | | | | FLTPOL | FLTMOD<1:0> | | 0000 |
| PDC7 | 0CE6 | PDC7<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE7 | 0CE8 | PHASE7<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR7 | 0CEA | — | — | DTR7<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR7 | 0CEC | — | — | ALTDTR7<13:0> | | | | | | | | | | | | | | 0000 |
| SDC7 | 0CEE | SDC7<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE7 | 0CF0 | SPHASE7<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG7 | 0CF2 | TRGCMP<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON7 | 0CF4 | TRGDIV<3:0> | | | | — | — | — | — | — | — | TRGSTRT<5:0> | | | | | | 0000 |
| PWMCAP7 | 0CF8 | PWMCAP7<15:0> | | | | | | | | | | | | | | | | 0000 |
| LEBCON7 | 0CFA | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY7 | 0CFC | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON7 | 0CFE | — | — | — | — | BLANKSEL<3:0> | | | | — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-20: QEI1 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| QEI1CON | 01C0 | QEIEN | — | QEISIDL | PIMOD<2:0> | | | IMV<1:0> | | — | INTDIV<2:0> | | | CNTPOL | GATEN | CCM<1:0> | | 0000 |
| QEI1IOC | 01C2 | QCAPEN | FLTREN | QFDIV<2:0> | | | OUTFNC<1:0> | | SWPAB | HOMPOL | IDXPOL | QEBPOL | QEAPOL | HOME | INDEX | QEB | QEA | 000x |
| QEI1STAT | 01C4 | — | — | PCHEQIRQ | PCHEQIEN | PCLEQIRQ | PCLEQIEN | POSOVIRQ | POSOVIEN | PCIIRQ | PCIIEN | VELOVIRQ | VELOVIEN | HOMIRQ | HOMIEN | IDXIRQ | IDXIEN | 0000 |
| POS1CNTL | 01C6 | POSCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| POS1CNTH | 01C8 | POSCNT<31:16> | | | | | | | | | | | | | | | | 0000 |
| POS1HLD | 01CA | POSHLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| VEL1CNT | 01CC | VELCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| INT1TMRL | 01CE | INTTMR<15:0> | | | | | | | | | | | | | | | | 0000 |
| INT1TMRH | 01D0 | INTTMR<31:16> | | | | | | | | | | | | | | | | 0000 |
| INT1HLDL | 01D2 | INTHLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| INT1HLDH | 01D4 | INTHLD<31:16> | | | | | | | | | | | | | | | | 0000 |
| INDX1CNTL | 01D6 | INDXCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| INDX1CNTH | 01D8 | INDXCNT<31:16> | | | | | | | | | | | | | | | | 0000 |
| INDX1HLD | 01DA | INDXHLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| QEI1GECL | 01DC | QEIGEC<15:0> | | | | | | | | | | | | | | | | 0000 |
| QEI1ICL | 01DC | QEIIC<15:0> | | | | | | | | | | | | | | | | 0000 |
| QEI1GECH | 01DE | QEIGEC<31:16> | | | | | | | | | | | | | | | | 0000 |
| QEI1ICH | 01DE | QEIIC<31:16> | | | | | | | | | | | | | | | | 0000 |
| QEI1LECL | 01E0 | QEILEC<15:0> | | | | | | | | | | | | | | | | 0000 |
| QEI1LECH | 01E2 | QEILEC<31:16> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-21: QEI2 REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| QEI2CON | 05C0 | QEIEN | — | QEISIDL | PIMOD<2:0> | | | IMV<1:0> | | — | INTDIV<2:0> | | | CNTPOL | GATEN | CCM<1:0> | | 0000 |
| QEI2IOC | 05C2 | QCAPEN | FLTREN | QFDIV<2:0> | | | OUTFNC<1:0> | | SWPAB | HOMPOL | IDXPOL | QEBPOL | QEAPOL | HOME | INDEX | QEB | QEA | 000x |
| QEI2STAT | 05C4 | — | — | PCHEQIRQ | PCHEQIEN | PCLEQIRQ | PCLEQIEN | POSOVIRQ | POSOVIEN | PCIIRQ | PCIIEN | VELOVIRQ | VELOVIEN | HOMIRQ | HOMIEN | IDXIRQ | IDXIEN | 0000 |
| POS2CNTL | 05C6 | POSCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| POS2CNTH | 05C8 | POSCNT<31:16> | | | | | | | | | | | | | | | | 0000 |
| POS2HLD | 05CA | POSHLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| VEL2CNT | 05CC | VELCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| INT2TMRL | 05CE | INTTMR<15:0> | | | | | | | | | | | | | | | | 0000 |
| INT2TMRH | 05D0 | INTTMR<31:16> | | | | | | | | | | | | | | | | 0000 |
| INT2HLDL | 05D2 | INTHLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| INT2HLDH | 05D4 | INTHLD<31:16> | | | | | | | | | | | | | | | | 0000 |
| INDX2CNTL | 05D6 | INDXCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| INDX2CNTH | 05D8 | INDXCNT<31:16> | | | | | | | | | | | | | | | | 0000 |
| INDX2HLD | 05DA | INDXHLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| QEI2GECL | 05DC | QEIGEC<15:0> | | | | | | | | | | | | | | | | 0000 |
| QEI2ICL | 05DC | QEIIC<15:0> | | | | | | | | | | | | | | | | 0000 |
| QEI2GECH | 05DE | QEIGEC<31:16> | | | | | | | | | | | | | | | | 0000 |
| QEI2ICH | 05DE | QEIIC<31:16> | | | | | | | | | | | | | | | | 0000 |
| QEI2LECL | 05E0 | QEILEC<15:0> | | | | | | | | | | | | | | | | 0000 |
| QEI2LECH | 05E2 | QEILEC<31:16> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-22: I2C1 and I2C2 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| I2C1RCV | 0200 | — | — | — | — | — | — | — | — | I2Cx Receive Register | | | | | | | | 0000 |
| I2C1TRN | 0202 | — | — | — | — | — | — | — | — | I2Cx Transmit Register | | | | | | | | 00FF |
| I2C1BRG | 0204 | — | — | — | — | — | — | — | Baud Rate Generator | | | | | | | | | 0000 |
| I2C1CON | 0206 | I2CEN | — | I2CSIDL | SCLREL | IPMIEN | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| I2C1STAT | 0208 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 |
| I2C1ADD | 020A | — | — | — | — | — | — | I2Cx Address Register | | | | | | | | | | 0000 |
| I2C1MSK | 020C | — | — | — | — | — | — | I2Cx Address Mask | | | | | | | | | | 0000 |
| I2C2RCV | 0210 | — | — | — | — | — | — | — | — | I2Cx Receive Register | | | | | | | | 0000 |
| I2C2TRN | 0212 | — | — | — | — | — | — | — | — | I2Cx Transmit Register | | | | | | | | 00FF |
| I2C2BRG | 0214 | — | — | — | — | — | — | — | Baud Rate Generator | | | | | | | | | 0000 |
| I2C2CON | 0216 | I2CEN | — | I2CSIDL | SCLREL | IPMIEN | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| I2C2STAT | 0218 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 |
| I2C2ADD | 021A | — | — | — | — | — | — | I2Cx Address Register | | | | | | | | | | 0000 |
| I2C2MSK | 021C | — | — | — | — | — | — | I2Cx Address Mask | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-23: UART1, UART2, UART3 and UART4 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U1MODE | 0220 | UARTEN | — | USIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| U1STA | 0222 | UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| U1TXREG | 0224 | — | — | — | — | — | — | — | UARTx Transmit Register | | | | | | | | | xxxx |
| U1RXREG | 0226 | — | — | — | — | — | — | — | UARTxReceive Register | | | | | | | | | 0000 |
| U1BRG | 0228 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| U2MODE | 0230 | UARTEN | — | USIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| U2STA | 0232 | UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| U2TXREG | 0234 | — | — | — | — | — | — | — | UARTx Transmit Register | | | | | | | | | xxxx |
| U2RXREG | 0236 | — | — | — | — | — | — | — | UARTx Receive Register | | | | | | | | | 0000 |
| U2BRG | 0238 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| U3MODE | 0250 | UARTEN | — | USIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| U3STA | 0252 | UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| U3TXREG | 0254 | — | — | — | — | — | — | — | UARTx Transmit Register | | | | | | | | | xxxx |
| U3RXREG | 0256 | — | — | — | — | — | — | — | UARTx Receive Register | | | | | | | | | 0000 |
| U3BRG | 0258 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| U4MODE | 02B0 | UARTEN | — | USIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| U4STA | 02B2 | UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| U4TXREG | 02B4 | — | — | — | — | — | — | — | UARTx Transmit Register | | | | | | | | | xxxx |
| U4RXREG | 02B6 | — | — | — | — | — | — | — | UARTx Receive Register | | | | | | | | | 0000 |
| U4BRG | 02B8 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-24: SPI1, SPI2, SPI3 and SPI4 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SPI1STAT | 0240 | SPIEN | — | SPISIDL | — | — | SPIBEC<2:0> | | | SRMPT | SPIROV | SRXMPT | SISEL<2:0> | | | SPITBF | SPIRBF | 0000 |
| SPI1CON1 | 0242 | — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | SPRE<2:0> | | | PPRE<1:0> | | 0000 |
| SPI1CON2 | 0244 | FRMEN | SPIFSD | FRMPOL | — | — | — | — | — | — | — | — | — | — | — | FRMDLY | SPIBEN | 0000 |
| SPI1BUF | 0248 | SPIx Transmit and Receive Buffer Register | | | | | | | | | | | | | | | | 0000 |
| SPI2STAT | 0260 | SPIEN | — | SPISIDL | — | — | SPIBEC<2:0> | | | SRMPT | SPIROV | SRXMPT | SISEL<2:0> | | | SPITBF | SPIRBF | 0000 |
| SPI2CON1 | 0262 | — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | SPRE<2:0> | | | PPRE<1:0> | | 0000 |
| SPI2CON2 | 0264 | FRMEN | SPIFSD | FRMPOL | — | — | — | — | — | — | — | — | — | — | — | FRMDLY | SPIBEN | 0000 |
| SPI2BUF | 0268 | SPIx Transmit and Receive Buffer Register | | | | | | | | | | | | | | | | 0000 |
| SPI3STAT | 02A0 | SPIEN | — | SPISIDL | — | — | SPIBEC<2:0> | | | SRMPT | SPIROV | SRXMPT | SISEL<2:0> | | | SPITBF | SPIRBF | 0000 |
| SPI3CON1 | 02A2 | — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | SPRE<2:0> | | | PPRE<1:0> | | 0000 |
| SPI3CON2 | 02A4 | FRMEN | SPIFSD | FRMPOL | — | — | — | — | — | — | — | — | — | — | — | FRMDLY | SPIBEN | 0000 |
| SPI3BUF | 02A8 | SPIx Transmit and Receive Buffer Register | | | | | | | | | | | | | | | | 0000 |
| SPI4STAT | 02C0 | SPIEN | — | SPISIDL | — | — | SPIBEC<2:0> | | | SRMPT | SPIROV | SRXMPT | SISEL<2:0> | | | SPITBF | SPIRBF | 0000 |
| SPI4CON1 | 02C2 | — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | SPRE<2:0> | | | PPRE<1:0> | | 0000 |
| SPI4CON2 | 02C4 | FRMEN | SPIFSD | FRMPOL | — | — | — | — | — | — | — | — | — | — | — | FRMDLY | SPIBEN | 0000 |
| SPI4BUF | 02C8 | SPIx Transmit and Receive Buffer Register | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-25: ADC1 and ADC2 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC1BUF0 | 0300 | ADCx Data Buffer 0 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF1 | 0302 | ADCx Data Buffer 1 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF2 | 0304 | ADCx Data Buffer 2 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF3 | 0306 | ADCx Data Buffer 3 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF4 | 0308 | ADCx Data Buffer 4 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF5 | 030A | ADCx Data Buffer 5 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF6 | 030C | ADCx Data Buffer 6 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF7 | 030E | ADCx Data Buffer 7 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF8 | 0310 | ADCx Data Buffer 8 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF9 | 0312 | ADCx Data Buffer 9 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFA | 0314 | ADCx Data Buffer 10 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFB | 0316 | ADCx Data Buffer 11 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFC | 0318 | ADCx Data Buffer 12 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFD | 031A | ADCx Data Buffer 13 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFE | 031C | ADCx Data Buffer 14 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFF | 031E | ADCx Data Buffer 15 | | | | | | | | | | | | | | | | xxxx |
| AD1CON1 | 0320 | ADON | — | ADSIDL | ADDMABM | — | AD12B | FORM<1:0> | | SSRC<2:0> | | | SSRCG | SIMSAM | ASAM | SAMP | DONE | 0000 |
| AD1CON2 | 0322 | VCFG<2:0> | | | — | — | CSCNA | CHPS<1:0> | | BUFS | SMPI<4:0> | | | | | BUFM | ALTS | 0000 |
| AD1CON3 | 0324 | ADRC | — | — | SAMC<4:0> | | | | | ADCS<7:0> | | | | | | | | 0000 |
| AD1CHS123 | 0326 | — | — | — | — | — | CH123NB<1:0> | | CH123SB | — | — | — | — | — | CH123NA<1:0> | | CH123SA | 0000 |
| AD1CHS0 | 0328 | CH0NB | — | — | CH0SB<4:0> | | | | | CH0NA | — | — | CH0SA<4:0> | | | | | 0000 |
| AD1CSSH | 032E | CSS31 | CSS30 | CSS29 | CSS28 | CSS27 | CSS26 | CSS25 | CSS24 | CSS23(1) | CSS22(1) | CSS21(1) | CSS20(1) | CSS19(1) | CSS18(1) | CSS17(1) | CSS16(1) | 0000 |
| AD1CSSL | 0330 | CSS15 | CSS14 | CSS13 | CSS12 | CSS11 | CSS10 | CSS9 | CSS8 | CSS7 | CSS6 | CSS5 | CSS4 | CSS3 | CSS2 | CSS1 | CSS0 | 0000 |
| AD1CON4 | 0332 | — | — | — | — | — | — | — | ADDMAEN | — | — | — | — | — | DMABL<2:0> | | | 0000 |
| ADC2BUF0 | 0340 | ADCx Data Buffer 0 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF1 | 0342 | ADCx Data Buffer 1 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF2 | 0344 | ADCx Data Buffer 2 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF3 | 0346 | ADCx Data Buffer 3 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF4 | 0348 | ADCx Data Buffer 4 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF5 | 034A | ADCx Data Buffer 5 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF6 | 034C | ADCx Data Buffer 6 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF7 | 034E | ADCx Data Buffer 7 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF8 | 0350 | ADCx Data Buffer 8 | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** These bits are not available on dsPIC33EP256MU806 devices.

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**TABLE 4-25: ADC1 and ADC2 REGISTER MAP (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC2BUF9 | 0352 | ADCx Data Buffer 9 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUFA | 0354 | ADCx Data Buffer 10 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUFB | 0356 | ADCx Data Buffer 11 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUFC | 0358 | ADCx Data Buffer 12 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUFD | 035A | ADCx Data Buffer 13 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUFE | 035C | ADCx Data Buffer 14 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUFF | 035E | ADCx Data Buffer 15 | | | | | | | | | | | | | | | | xxxx |
| AD2CON1 | 0360 | ADON | — | ADSIDL | ADDMABM | — | — | FORM<1:0> | | SSRC<2:0> | | | SSRCG | SIMSAM | ASAM | SAMP | DONE | 0000 |
| AD2CON2 | 0362 | VCFG<2:0> | | | — | — | CSCNA | CHPS<1:0> | | BUFS | — | SMPI<3:0> | | | | BUFM | ALTS | 0000 |
| AD2CON3 | 0364 | ADRC | — | — | SAMC<4:0> | | | | | ADCS<7:0> | | | | | | | | 0000 |
| AD2CHS123 | 0366 | — | — | — | — | — | CH123NB<1:0> | | CH123SB | — | — | — | — | — | CH123NA<1:0> | | CH123SA | 0000 |
| AD2CHS0 | 0368 | CH0NB | — | — | CH0SB<4:0> | | | | | CH0NA | — | — | CH0SA<4:0> | | | | | 0000 |
| AD2CSSL | 0270 | CSS15 | CSS14 | CSS13 | CSS12 | CSS11 | CSS10 | CSS9 | CSS8 | CSS7 | CSS6 | CSS5 | CSS4 | CSS3 | CSS2 | CSS1 | CSS0 | 0000 |
| AD2CON4 | 0272 | — | — | — | — | — | — | — | ADDMAEN | — | — | — | — | — | DMABL<2:0> | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** These bits are not available on dsPIC33EP256MU806 devices.



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**TABLE 4-26: DCI REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DCICON1 | 0280 | DCIEN | — | DCISIDL | — | DLOOP | CSCKD | CSCKE | COFSD | UNFM | CSDOM | DJST | — | — | — | COFSM<1:0> | | 0000 |
| DCICON2 | 0282 | — | — | — | — | BLEN<1:0> | | — | COFSG<3:0> | | | | — | WS<3:0> | | | | 0000 |
| DCICON3 | 0284 | — | — | — | — | BCG<11:0> | | | | | | | | | | | | 0000 |
| DCISTAT | 0286 | — | — | — | — | SLOT<3:0> | | | | — | — | — | — | ROV | RFUL | TUNF | TMPTY | 0000 |
| TSCON | 0288 | TSE15 | TSE14 | TSE13 | TSE12 | TSE11 | TSE10 | TSE9 | TSE8 | TSE7 | TSE6 | TSE5 | TSE4 | TSE3 | TSE2 | TSE1 | TSE0 | 0000 |
| RSCON | 028C | RSE15 | RSE14 | RSE13 | RSE12 | RSE11 | RSE10 | RSE9 | RSE8 | RSE7 | RSE6 | RSE5 | RSE4 | RSE3 | RSE2 | RSE1 | RSE0 | 0000 |
| RXBUF0 | 0290 | DCI Receive 0 Data Register | | | | | | | | | | | | | | | | uuuu |
| RXBUF1 | 0292 | DCI Receive 1 Data Register | | | | | | | | | | | | | | | | uuuu |
| RXBUF2 | 0294 | DCI Receive 2 Data Register | | | | | | | | | | | | | | | | uuuu |
| RXBUF3 | 0296 | DCI Receive 3 Data Register | | | | | | | | | | | | | | | | uuuu |
| TXBUF0 | 0298 | DCI Transmit 0 Data Register | | | | | | | | | | | | | | | | 0000 |
| TXBUF1 | 029A | DCI Transmit 1 Data Register | | | | | | | | | | | | | | | | 0000 |
| TXBUF2 | 029C | DCI Transmit 2 Data Register | | | | | | | | | | | | | | | | 0000 |
| TXBUF3 | 029E | DCI Transmit 3 Data Register | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, u = unchanged, — = unimplemented, read as '0'. Reset values are shown in hexadecimal. Shaded locations indicate reserved space in the SFR map for future module expansion. Read reserved locations as '0's.

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**TABLE 4-27: USB OTG REGISTER MAP FOR dsPIC33EPMU806/810/814 AND PIC24EPGU806/10/814) DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U1OTGIR | 0488 | — | — | — | — | — | — | — | — | IDIF | T1MSECIF | LSTATEIF | ACTVIF | SESVDIF | SESENDIF | — | VBUSVDIF | 0000 |
| U1OTGIE | 048A | — | — | — | — | — | — | — | — | IDIE | T1MSECIE | LSTATEIE | ACTVIE | SESVDIE | SESENDIE | — | VBUSVDIE | 0000 |
| U1OTGSTAT | 048C | — | — | — | — | — | — | — | — | ID | — | LSTATE | — | SESVD | SESEND | — | VBUSVD | 0000 |
| U1OTGCON | 048E | — | — | — | — | — | — | — | — | DPPULUP | DMPULUP | DPPULDWN | DMPULDWN | VBUSON | OTGEN | VBUSCHG | VBUSDIS | 0000 |
| U1PWRC | 0490 | — | — | — | — | — | — | — | — | UACTPND(4) | — | — | USLPGRD | — | — | USUSPND | USBPWR | 0000 |
| U1IR(1) | 04C0 | — | — | — | — | — | — | — | — | STALLIF | — | RESUMEIF | IDLEIF | TRNIF | SOFIF | UERRIF | URSTIF | 0000 |
| U1IR(2) | 04C0 | — | — | — | — | — | — | — | — | STALLIF | ATTACHIF | RESUMEIF | IDLEIF | TRNIF | SOFIF | UERRIF | DETACHIF | 0000 |
| U1IE(1) | 04C2 | — | — | — | — | — | — | — | — | STALLIE | — | RESUMEIE | IDLEIE | TRNIE | SOFIE | UERRIE | URSTIE | 0000 |
| U1IE(2) | 04C2 | — | — | — | — | — | — | — | — | STALLIE | ATTACHIE | RESUMEIE | IDLEIE | TRNIE | SOFIE | UERRIE | DETACHIE | 0000 |
| U1EIR(1) | 04C4 | — | — | — | — | — | — | — | — | BTSEF | BUSACCEF | DMAEF | BTOEF | DFN8EF | CRC16EF | CRC5EF | PIDEF | 0000 |
| U1EIR(2) | 04C4 | — | — | — | — | — | — | — | — | BTSEF | BUSACCEF | DMAEF | BTOEF | DFN8EF | CRC16EF | EOFEF | PIDEF | 0000 |
| U1EIE(1) | 04C6 | — | — | — | — | — | — | — | — | BTSEE | BUSACCEE | DMAEE | BTOEE | DFN8EE | CRC16EE | CRC5EE | PIDEE | 0000 |
| U1EIE(2) | 04C6 | — | — | — | — | — | — | — | — | BTSEE | BUSACCEE | DMAEE | BTOEE | DFN8EE | CRC16EE | EOFEE | PIDEE | 0000 |
| U1STAT | 04C8 | — | — | — | — | — | — | — | — | ENDPT<3:0>(3) | | | | DIR | PPBI | — | — | 0000 |
| U1CON(1) | 04CA | — | — | — | — | — | — | — | — | — | SE0 | PKTDIS | — | HOSTEN | RESUME | PPBRST | USBEN | 0000 |
| U1CON(2) | 04CA | — | — | — | — | — | — | — | — | JSTATE | SE0 | TOKBUSY | USBRST | HOSTEN | RESUME | PPBRST | SOFEN | 0000 |
| U1ADDR | 04CC | — | — | — | — | — | — | — | — | LSPDEN(1) | USB Device Address (DEVADDR) | | | | | | | 0000 |
| U1BDTP1 | 04CE | — | — | — | — | — | — | — | — | BDTPTRL<15:9> | | | | | | | — | 0000 |
| U1FRML | 04D0 | — | — | — | — | — | — | — | — | FRML<7:0> | | | | | | | | 0000 |
| U1FRMH | 04D2 | — | — | — | — | — | — | — | — | — | — | — | — | — | FRMH<2:0> | | | 0000 |
| U1TOK(3) | 04D4 | — | — | — | — | — | — | — | — | PID<3:0> | | | | EP<3:0> | | | | 0000 |
| U1SOF(3) | 04D6 | — | — | — | — | — | — | — | — | CNT<7:0> | | | | | | | | 0000 |
| U1BDTP2 | 04D8 | — | — | — | — | — | — | — | — | BDTPTRH<23:16> | | | | | | | | 0000 |
| U1BDTP3 | 04DA | — | — | — | — | — | — | — | — | BDTPTRU<31:24> | | | | | | | | 0000 |
| U1CNFG1 | 04DC | — | — | — | — | — | — | — | — | UTEYE | UOEMON | — | USBSIDL | — | — | — | — | 0000 |
| U1CNFG2 | O4DE | — | — | — | — | — | — | — | — | — | — | UVCMPSEL | PUVBUS | EXTI2CEN | UVBUSDIS | UVCMPDIS | UTRDIS | 0000 |
| U1EP0 | 04E0 | — | — | — | — | — | — | — | — | LSPD | RETRYDIS | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP1 | 04E2 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP2 | 04E4 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP3 | 04E6 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP4 | 04E8 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This bit is available when the module is operating in Device mode.

**2:** This bit is available when the module is operating in Host mode

**3:** Device mode only. These bits are always read as '0' in Host mode.

**4:** The Reset value for this bit is undefined.



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**TABLE 4-27: USB OTG REGISTER MAP FOR dsPIC33EPMU806/810/814 AND PIC24EPGU806/10/814) DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U1EP5 | 04EA | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP6 | 04EC | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP7 | 04EE | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP8 | 04F0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP9 | 04F2 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP10 | 04F4 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP11 | 04F6 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP12 | 04F8 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP13 | 04FA | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP14 | 04FC | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1EP15 | 04FE | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| U1PWMRRS | 0580 | DC<7:0> | | | | | | | | PER<7:0> | | | | | | | | 0000 |
| U1PWMCON | 0582 | PWMEN | — | — | — | — | — | PWMPOL | CNTEN | — | — | — | — | — | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This bit is available when the module is operating in Device mode.

**2:** This bit is available when the module is operating in Host mode

**3:** Device mode only. These bits are always read as '0' in Host mode.

**4:** The Reset value for this bit is undefined.

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**TABLE 4-28: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 OR 1**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C1CTRL1 | 0400 | — | — | CSIDL | ABAT | CANCKS | REQOP<2:0> | | | OPMODE<2:0> | | | — | CANCAP | — | — | WIN | 0480 |
| C1CTRL2 | 0402 | — | — | — | — | — | — | — | — | — | — | — | DNCNT<4:0> | | | | | 0000 |
| C1VEC | 0404 | — | — | — | FILHIT<4:0> | | | | | — | ICODE<6:0> | | | | | | | 0040 |
| C1FCTRL | 0406 | DMABS<2:0> | | | — | — | — | — | — | — | — | — | FSA<4:0> | | | | | 0000 |
| C1FIFO | 0408 | — | — | FBP<5:0> | | | | | | — | — | FNRB<5:0> | | | | | | 0000 |
| C1INTF | 040A | — | — | TXBO | TXBP | RXBP | TXWAR | RXWAR | EWARN | IVRIF | WAKIF | ERRIF | — | FIFOIF | RBOVIF | RBIF | TBIF | 0000 |
| C1INTE | 040C | — | — | — | — | — | — | — | — | IVRIE | WAKIE | ERRIE | — | FIFOIE | RBOVIE | RBIE | TBIE | 0000 |
| C1EC | 040E | TERRCNT<7:0> | | | | | | | | RERRCNT<7:0> | | | | | | | | 0000 |
| C1CFG1 | 0410 | — | — | — | — | — | — | — | — | SJW<1:0> | | BRP<5:0> | | | | | | 0000 |
| C1CFG2 | 0412 | — | WAKFIL | — | — | — | SEG2PH<2:0> | | | SEG2PHTS | SAM | SEG1PH<2:0> | | | PRSEG<2:0> | | | 0000 |
| C1FEN1 | 0414 | FLTEN15 | FLTEN14 | FLTEN13 | FLTEN12 | FLTEN11 | FLTEN10 | FLTEN9 | FLTEN8 | FLTEN7 | FLTEN6 | FLTEN5 | FLTEN4 | FLTEN3 | FLTEN2 | FLTEN1 | FLTEN0 | FFFF |
| C1FMSKSEL1 | 0418 | F7MSK<1:0> | | F6MSK<1:0> | | F5MSK<1:0> | | F4MSK<1:0> | | F3MSK<1:0> | | F2MSK<1:0> | | F1MSK<1:0> | | F0MSK<1:0> | | 0000 |
| C1FMSKSEL2 | 041A | F15MSK<1:0> | | F14MSK<1:0> | | F13MSK<1:0> | | F12MSK<1:0> | | F11MSK<1:0> | | F10MSK<1:0> | | F9MSK<1:0> | | F8MSK<1:0> | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-29: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| — | 0400-041E | See Table 4-28 | | | | | | | | | | | | | | | | — |
| C1RXFUL1 | 0420 | RXFUL15 | RXFUL14 | RXFUL13 | RXFUL12 | RXFUL11 | RXFUL10 | RXFUL9 | RXFUL8 | RXFUL7 | RXFUL6 | RXFUL5 | RXFUL4 | RXFUL3 | RXFUL2 | RXFUL1 | RXFUL0 | 0000 |
| C1RXFUL2 | 0422 | RXFUL31 | RXFUL30 | RXFUL29 | RXFUL28 | RXFUL27 | RXFUL26 | RXFUL25 | RXFUL24 | RXFUL23 | RXFUL22 | RXFUL21 | RXFUL20 | RXFUL19 | RXFUL18 | RXFUL17 | RXFUL16 | 0000 |
| C1RXOVF1 | 0428 | RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF9 | RXOVF8 | RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 | 0000 |
| C1RXOVF2 | 042A | RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 | RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 | 0000 |
| C1TR01CON | 0430 | TXEN1 | TXABT1 | TXLARB1 | TXERR1 | TXREQ1 | RTREN1 | TX1PRI<1:0> | | TXEN0 | TXABAT0 | TXLARB0 | TXERR0 | TXREQ0 | RTREN0 | TX0PRI<1:0> | | 0000 |
| C1TR23CON | 0432 | TXEN3 | TXABT3 | TXLARB3 | TXERR3 | TXREQ3 | RTREN3 | TX3PRI<1:0> | | TXEN2 | TXABAT2 | TXLARB2 | TXERR2 | TXREQ2 | RTREN2 | TX2PRI<1:0> | | 0000 |
| C1TR45CON | 0434 | TXEN5 | TXABT5 | TXLARB5 | TXERR5 | TXREQ5 | RTREN5 | TX5PRI<1:0> | | TXEN4 | TXABAT4 | TXLARB4 | TXERR4 | TXREQ4 | RTREN4 | TX4PRI<1:0> | | 0000 |
| C1TR67CON | 0436 | TXEN7 | TXABT7 | TXLARB7 | TXERR7 | TXREQ7 | RTREN7 | TX7PRI<1:0> | | TXEN6 | TXABAT6 | TXLARB6 | TXERR6 | TXREQ6 | RTREN6 | TX6PRI<1:0> | | xxxx |
| C1RXD | 0440 | Received Data Word | | | | | | | | | | | | | | | | xxxx |
| C1TXD | 0442 | Transmit Data Word | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-30: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| — | 0400-041E | See Table 4-28 | | | | | | | | | | | | | | | | — |
| C1BUFPNT1 | 0420 | F3BP<3:0> | | | | F2BP<3:0> | | | | F1BP<3:0> | | | | F0BP<3:0> | | | | 0000 |
| C1BUFPNT2 | 0422 | F7BP<3:0> | | | | F6BP<3:0> | | | | F5BP<3:0> | | | | F4BP<3:0> | | | | 0000 |
| C1BUFPNT3 | 0424 | F11BP<3:0> | | | | F10BP<3:0> | | | | F9BP<3:0> | | | | F8BP<3:0> | | | | 0000 |
| C1BUFPNT4 | 0426 | F15BP<3:0> | | | | F14BP<3:0> | | | | F13BP<3:0> | | | | F12BP<3:0> | | | | 0000 |
| C1RXM0SID | 0430 | SID<10:3> | | | | | | | | SID<2:0> | | | — | MIDE | — | EID<17:16> | | xxxx |
| C1RXM0EID | 0432 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXM1SID | 0434 | SID<10:3> | | | | | | | | SID<2:0> | | | — | MIDE | — | EID<17:16> | | xxxx |
| C1RXM1EID | 0436 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXM2SID | 0438 | SID<10:3> | | | | | | | | SID<2:0> | | | — | MIDE | — | EID<17:16> | | xxxx |
| C1RXM2EID | 043A | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF0SID | 0440 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF0EID | 0442 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF1SID | 0444 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF1EID | 0446 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF2SID | 0448 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF2EID | 044A | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF3SID | 044C | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF3EID | 044E | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF4SID | 0450 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF4EID | 0452 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF5SID | 0454 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF5EID | 0456 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF6SID | 0458 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF6EID | 045A | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF7SID | 045C | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF7EID | 045E | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF8SID | 0460 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF8EID | 0462 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF9SID | 0464 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF9EID | 0466 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF10SID | 0468 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF10EID | 046A | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF11SID | 046C | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-30: ECAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 (CONTINUED)**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C1RXF11EID | 046E | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF12SID | 0470 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF12EID | 0472 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF13SID | 0474 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF13EID | 0476 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF14SID | 0478 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF14EID | 047A | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C1RXF15SID | 047C | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C1RXF15EID | 047E | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-31: ECAN2 REGISTER MAP WHEN WIN (C2CTRL<0>) = 0 OR 1**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C2CTRL1 | 0500 | — | — | CSIDL | ABAT | CANCKS | REQOP<2:0> | | | OPMODE<2:0> | | | — | CANCAP | — | — | WIN | 0480 |
| C2CTRL2 | 0502 | — | — | — | — | — | — | — | — | — | — | — | DNCNT<4:0> | | | | | 0000 |
| C2VEC | 0504 | — | — | — | FILHIT<4:0> | | | | | — | ICODE<6:0> | | | | | | | 0040 |
| C2FCTRL | 0506 | DMABS<2:0> | | | — | — | — | — | — | — | — | — | FSA<4:0> | | | | | 0000 |
| C2FIFO | 0508 | — | — | FBP<5:0> | | | | | | — | — | FNRB<5:0> | | | | | | 0000 |
| C2INTF | 050A | — | — | TXBO | TXBP | RXBP | TXWAR | RXWAR | EWARN | IVRIF | WAKIF | ERRIF | — | FIFOIF | RBOVIF | RBIF | TBIF | 0000 |
| C2INTE | 050C | — | — | — | — | — | — | — | — | IVRIE | WAKIE | ERRIE | — | FIFOIE | RBOVIE | RBIE | TBIE | 0000 |
| C2EC | 050E | TERRCNT<7:0> | | | | | | | | RERRCNT<7:0> | | | | | | | | 0000 |
| C2CFG1 | 0510 | — | — | — | — | — | — | — | — | SJW<1:0> | | BRP<5:0> | | | | | | 0000 |
| C2CFG2 | 0512 | — | WAKFIL | — | — | — | SEG2PH<2:0> | | | SEG2PHTS | SAM | SEG1PH<2:0> | | | PRSEG<2:0> | | | 0000 |
| C2FEN1 | 0514 | FLTEN15 | FLTEN14 | FLTEN13 | FLTEN12 | FLTEN11 | FLTEN10 | FLTEN9 | FLTEN8 | FLTEN7 | FLTEN6 | FLTEN5 | FLTEN4 | FLTEN3 | FLTEN2 | FLTEN1 | FLTEN0 | FFFF |
| C2FMSKSEL1 | 0518 | F7MSK<1:0> | | F6MSK<1:0> | | F5MSK<1:0> | | F4MSK<1:0> | | F3MSK<1:0> | | F2MSK<1:0> | | F1MSK<1:0> | | F0MSK<1:0> | | 0000 |
| C2FMSKSEL2 | 051A | F15MSK<1:0> | | F14MSK<1:0> | | F13MSK<1:0> | | F12MSK<1:0> | | F11MSK<1:0> | | F10MSK<1:0> | | F9MSK<1:0> | | F8MSK<1:0> | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-32: ECAN2 REGISTER MAP WHEN WIN (C2CTRL<0>) = 0**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| — | 0500-051E | See Table 4-31 | | | | | | | | | | | | | | | | — |
| C2RXFUL1 | 0520 | RXFUL15 | RXFUL14 | RXFUL13 | RXFUL12 | RXFUL11 | RXFUL10 | RXFUL9 | RXFUL8 | RXFUL7 | RXFUL6 | RXFUL5 | RXFUL4 | RXFUL3 | RXFUL2 | RXFUL1 | RXFUL0 | 0000 |
| C2RXFUL2 | 0522 | RXFUL31 | RXFUL30 | RXFUL29 | RXFUL28 | RXFUL27 | RXFUL26 | RXFUL25 | RXFUL24 | RXFUL23 | RXFUL22 | RXFUL21 | RXFUL20 | RXFUL19 | RXFUL18 | RXFUL17 | RXFUL16 | 0000 |
| C2RXOVF1 | 0528 | RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF09 | RXOVF08 | RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 | 0000 |
| C2RXOVF2 | 052A | RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 | RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 | 0000 |
| C2TR01CON | 0530 | TXEN1 | TXABAT1 | TXLARB1 | TXERR1 | TXREQ1 | RTREN1 | TX1PRI<1:0> | | TXEN0 | TXABAT0 | TXLARB0 | TXERR0 | TXREQ0 | RTREN0 | TX0PRI<1:0> | | 0000 |
| C2TR23CON | 0532 | TXEN3 | TXABAT3 | TXLARB3 | TXERR3 | TXREQ3 | RTREN3 | TX3PRI<1:0> | | TXEN2 | TXABAT2 | TXLARB2 | TXERR2 | TXREQ2 | RTREN2 | TX2PRI<1:0> | | 0000 |
| C2TR45CON | 0534 | TXEN5 | TXABAT5 | TXLARB5 | TXERR5 | TXREQ5 | RTREN5 | TX5PRI<1:0> | | TXEN4 | TXABAT4 | TXLARB4 | TXERR4 | TXREQ4 | RTREN4 | TX4PRI<1:0> | | 0000 |
| C2TR67CON | 0536 | TXEN7 | TXABAT7 | TXLARB7 | TXERR7 | TXREQ7 | RTREN7 | TX7PRI<1:0> | | TXEN6 | TXABAT6 | TXLARB6 | TXERR6 | TXREQ6 | RTREN6 | TX6PRI<1:0> | | xxxx |
| C2RXD | 0540 | ECAN2 Received Data Word | | | | | | | | | | | | | | | | xxxx |
| C2TXD | 0542 | ECAN2 Transmit Data Word | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-33: ECAN2 REGISTER MAP WHEN WIN (C2CTRL<0>) = 1**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| — | 0500-051E | See Table 4-31 | | | | | | | | | | | | | | | | — |
| C2BUFPNT1 | 0520 | F3BP<3:0> | | | | F2BP<3:0> | | | | F1BP<3:0> | | | | F0BP<3:0> | | | | 0000 |
| C2BUFPNT2 | 0522 | F7BP<3:0> | | | | F6BP<3:0> | | | | F5BP<3:0> | | | | F4BP<3:0> | | | | 0000 |
| C2BUFPNT3 | 0524 | F11BP<3:0> | | | | F10BP<3:0> | | | | F9BP<3:0> | | | | F8BP<3:0> | | | | 0000 |
| C2BUFPNT4 | 0526 | F15BP<3:0> | | | | F14BP<3:0> | | | | F13BP<3:0> | | | | F12BP<3:0> | | | | 0000 |
| C2RXM0SID | 0530 | SID<10:3> | | | | | | | | SID<2:0> | | | — | MIDE | — | EID<17:16> | | xxxx |
| C2RXM0EID | 0532 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXM1SID | 0534 | SID<10:3> | | | | | | | | SID<2:0> | | | — | MIDE | — | EID<17:16> | | xxxx |
| C2RXM1EID | 0536 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXM2SID | 0538 | SID<10:3> | | | | | | | | SID<2:0> | | | — | MIDE | — | EID<17:16> | | xxxx |
| C2RXM2EID | 053A | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF0SID | 0540 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF0EID | 0542 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF1SID | 0544 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF1EID | 0546 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF2SID | 0548 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF2EID | 054A | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF3SID | 054C | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF3EID | 054E | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF4SID | 0550 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF4EID | 0552 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF5SID | 0554 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF5EID | 0556 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF6SID | 0558 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF6EID | 055A | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF7SID | 055C | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF7EID | 055E | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF8SID | 0560 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF8EID | 0562 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF9SID | 0564 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF9EID | 0566 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF10SID | 0568 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF10EID | 056A | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF11SID | 056C | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-33: ECAN2 REGISTER MAP WHEN WIN (C2CTRL<0>) = 1 (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C2RXF11EID | 056E | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF12SID | 0570 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF12EID | 0572 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF13SID | 0574 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF13EID | 0576 | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF14SID | 0578 | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF14EID | 057A | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |
| C2RXF15SID | 057C | SID<10:3> | | | | | | | | SID<2:0> | | | — | EXIDE | — | EID<17:16> | | xxxx |
| C2RXF15EID | 057E | EID<15:8> | | | | | | | | EID<7:0> | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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## TABLE 4-34: PARALLEL MASTER/SLAVE PORT REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMCON | 0600 | PMPEN | — | PSIDL | ADRMUX<1:0> | | PTBEEN | PTWREN | PTRDEN | CSF<1:0> | | ALP | CS2P | CS1P | BEP | WRSP | RDSP | 0000 |
| PMMODE | 0602 | BUSY | IRQM<1:0> | | INCM<1:0> | | MODE16 | MODE<1:0> | | WAITB<1:0> | | WAITM<3:0> | | | | WAITE<1:0> | | 0000 |
| PMADDR(1) | 0604 | CS2 | CS1 | Parallel Port Address (ADDR<13:0>) | | | | | | | | | | | | | | 0000 |
| PMDOUT1(1) | 0604 | Parallel Port Data Out Register 1 (Buffers Level 0 and 1) | | | | | | | | | | | | | | | | 0000 |
| PMDOUT2 | 0606 | Parallel Port Data Out Register 2 (Buffers Level 2 and 3) | | | | | | | | | | | | | | | | 0000 |
| PMDIN1 | 0608 | Parallel Port Data In Register 1 (Buffers Level 0 and 1) | | | | | | | | | | | | | | | | 0000 |
| PMDIN2 | 060A | Parallel Port Data In Register 2 (Buffers Level 2 and 3) | | | | | | | | | | | | | | | | 0000 |
| PMAEN | 060C | PTEN15 | PTEN14 | PTEN13 | PTEN12 | PTEN11 | PTEN10 | PTEN9 | PTEN8 | PTEN7 | PTEN6 | PTEN5 | PTEN4 | PTEN3 | PTEN2 | PTEN1 | PTEN0 | 0000 |
| PMSTAT | 060E | IBF | IBOV | — | — | IB3F | IB2F | IB1F | IB0F | OBE | OBUF | — | — | OB3E | OB2E | OB1E | OB0E | 008F |

**Legend:** — = unimplemented, read as '0'. Shaded bits are not used in the operation of the PMP module.

**Note 1:** PMADDR and PMDOUT1 are the same physical register, but are defined differently depending on the module's operating mode.

## TABLE 4-35: CRC REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CRCCON1 | 0640 | CRCEN | — | CSIDL | VWORD<4:0> | | | | | CRCFUL | CRCMPT | CRCISEL | CRCGO | LENDIAN | — | — | — | 0000 |
| CRCCON2 | 0642 | — | — | — | DWIDTH<4:0> | | | | | — | — | — | PLEN<4:0> | | | | | 0000 |
| CRCXORL | 0644 | X<15:1> | | | | | | | | | | | | | | | — | 0000 |
| CRCXORH | 0646 | X<31:16> | | | | | | | | | | | | | | | | 0000 |
| CRCDATL | 0648 | CRC Data Input Low Word | | | | | | | | | | | | | | | | 0000 |
| CRCDATH | 064A | CRC Data Input High Word | | | | | | | | | | | | | | | | 0000 |
| CRCWDATL | 064C | CRC Result Low Word | | | | | | | | | | | | | | | | 0000 |
| CRCWDATH | 064E | CRC Result High Word | | | | | | | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

## TABLE 4-36: REAL-TIME CLOCK AND CALENDAR REGISTER MAP

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ALRMVAL | 0620 | Alarm Value Register Window based on ALRMPTR<1:0> | | | | | | | | | | | | | | | | xxxx |
| ALCFGRPT | 0622 | ALRMEN | CHIME | AMASK<3:0> | | | | ALRMPTR<1:0> | | ARPT<7:0> | | | | | | | | 0000 |
| RTCVAL | 0624 | RTCC Value Register Window based on RTCPTR<1:0> | | | | | | | | | | | | | | | | xxxx |
| RCFGCAL | 0626 | RTCEN | — | RTCWREN | RTCSYNC | HALFSEC | RTCOE | RTCPTR<1:0> | | CAL<7:0> | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-37: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPOR0 | 0680 | — | — | RP65R<5:0> | | | | | | — | — | RP64R<5:0> | | | | | | 0000 |
| RPOR1 | 0682 | — | — | RP67R<5:0> | | | | | | — | — | RP66R<5:0> | | | | | | 0000 |
| RPOR2 | 0684 | — | — | RP69R<5:0> | | | | | | — | — | RP68R<5:0> | | | | | | 0000 |
| RPOR3 | 0686 | — | — | RP71R<5:0> | | | | | | — | — | RP70R<5:0> | | | | | | 0000 |
| RPOR4 | 0688 | — | — | RP80R<5:0> | | | | | | — | — | RP79R<5:0> | | | | | | 0000 |
| RPOR5 | 068A | — | — | RP84R<5:0> | | | | | | — | — | RP82R<5:0> | | | | | | 0000 |
| RPOR6 | 068C | — | — | RP87R<5:0> | | | | | | — | — | RP85R<5:0> | | | | | | 0000 |
| RPOR7 | 068E | — | — | RP97R<5:0> | | | | | | — | — | RP96R<5:0> | | | | | | 0000 |
| RPOR8 | 0690 | — | — | RP99R<5:0> | | | | | | — | — | RP98R<5:0> | | | | | | 0000 |
| RPOR9 | 0692 | — | — | RP101R<5:0> | | | | | | — | — | RP100R<5:0> | | | | | | 0000 |
| RPOR11 | 0696 | — | — | RP108R<5:0> | | | | | | — | — | RP104R<5:0> | | | | | | 0000 |
| RPOR12 | 0698 | — | — | RP112R<5:0> | | | | | | — | — | RP109R<5:0> | | | | | | 0000 |
| RPOR13 | 069A | — | — | RP118R<5:0> | | | | | | — | — | RP113R<5:0> | | | | | | 0000 |
| RPOR14 | 069C | — | — | RP125R<5:0> | | | | | | — | — | RP120R<5:0> | | | | | | 0000 |
| RPOR15 | 069E | — | — | RP127R<5:0> | | | | | | — | — | RP126R<5:0> | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-38: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPOR0 | 0680 | — | — | RP65R<5:0> | | | | | | — | — | RP64R<5:0> | | | | | | 0000 |
| RPOR1 | 0682 | — | — | RP67R<5:0> | | | | | | — | — | RP66R<5:0> | | | | | | 0000 |
| RPOR2 | 0684 | — | — | RP69R<5:0> | | | | | | — | — | RP68R<5:0> | | | | | | 0000 |
| RPOR3 | 0686 | — | — | RP71R<5:0> | | | | | | — | — | RP70R<5:0> | | | | | | 0000 |
| RPOR4 | 0688 | — | — | RP80R<5:0> | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPOR5 | 068A | — | — | RP84R<5:0> | | | | | | — | — | RP82R<5:0> | | | | | | 0000 |
| RPOR6 | 068C | — | — | RP87R<5:0> | | | | | | — | — | RP85R<5:0> | | | | | | 0000 |
| RPOR7 | 068E | — | — | RP97R<5:0> | | | | | | — | — | RP96R<5:0> | | | | | | 0000 |
| RPOR8 | 0690 | — | — | RP99R<5:0> | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPOR9 | 0692 | — | — | RP101R<5:0> | | | | | | — | — | RP100R<5:0> | | | | | | 0000 |
| RPOR13 | 069A | — | — | RP118R<5:0> | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPOR14 | 069C | — | — | — | — | — | — | — | — | — | — | RP120R<5:0> | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-39: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPOR0 | 0680 | — | — | RP65R<5:0> | | | | | | — | — | RP64R<5:0> | | | | | | 0000 |
| RPOR1 | 0682 | — | — | RP67R<5:0> | | | | | | — | — | RP66R<5:0> | | | | | | 0000 |
| RPOR2 | 0684 | — | — | RP69R<5:0> | | | | | | — | — | RP68R<5:0> | | | | | | 0000 |
| RPOR3 | 0686 | — | — | RP71R<5:0> | | | | | | — | — | RP70R<5:0> | | | | | | 0000 |
| RPOR4 | 0688 | — | — | RP80R<5:0> | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPOR5 | 068A | — | — | RP84R<5:0> | | | | | | — | — | RP82R<5:0> | | | | | | 0000 |
| RPOR6 | 068C | — | — | RP87R<5:0> | | | | | | — | — | RP85R<5:0> | | | | | | 0000 |
| RPOR7 | 068E | — | — | RP97R<5:0> | | | | | | — | — | RP96R<5:0> | | | | | | 0000 |
| RPOR8 | 0690 | — | — | RP99R<5:0> | | | | | | — | — | RP98R<5:0> | | | | | | 0000 |
| RPOR9 | 0692 | — | — | RP101R<5:0> | | | | | | — | — | RP100R<5:0> | | | | | | 0000 |
| RPOR10 | 0694 | — | — | — | — | — | — | — | — | — | — | RP102R<5:0> | | | | | | 0000 |
| RPOR13 | 069A | — | — | RP118R<5:0> | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPOR14 | 069C | — | — | — | — | — | — | — | — | — | — | RP120R<5:0> | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-40: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMU814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | INT3R<6:0> | | | | | | | — | INT2R<6:0> | | | | | | | 0000 |
| RPINR2 | 06A4 | — | — | — | — | — | — | — | — | — | INT4R<6:0> | | | | | | | 0000 |
| RPINR3 | 06A6 | — | T3CKR<6:0> | | | | | | | — | T2CKR<6:0> | | | | | | | 0000 |
| RPINR4 | 06A8 | — | T5CKR<6:0> | | | | | | | — | T4CKR<6:0> | | | | | | | 0000 |
| RPINR5 | 06AA | — | T7CKR<6:0> | | | | | | | — | T6CKR<6:0> | | | | | | | 0000 |
| RPINR6 | 06AC | — | T9CKR<6:0> | | | | | | | — | T8CKR<6:0> | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | — | IC1R<6:0> | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | — | IC3R<6:0> | | | | | | | 0000 |
| RPINR9 | 06B2 | — | IC6R<6:0> | | | | | | | — | IC5R<6:0> | | | | | | | 0000 |
| RPINR10 | 06B4 | — | IC8R<6:0> | | | | | | | — | IC7R<6:0> | | | | | | | 0000 |
| RPINR11 | 06B6 | — | OCFBR<6:0> | | | | | | | — | OCFAR<6:0> | | | | | | | 0000 |
| RPINR12 | 06B8 | — | FLT2R<6:0> | | | | | | | — | FLT1R<6:0> | | | | | | | 0000 |
| RPINR13 | 06BA | — | FLT4R<6:0> | | | | | | | — | FLT3R<6:0> | | | | | | | 0000 |
| RPINR14 | 06BC | — | QEB1R<6:0> | | | | | | | — | QEA1R<6:0> | | | | | | | 0000 |
| RPINR15 | 06BE | — | HOME1R<6:0> | | | | | | | — | INDX1R<6:0> | | | | | | | 0000 |
| RPINR16 | 06C0 | — | QEB2R<6:0> | | | | | | | — | QEA2R<6:0> | | | | | | | 0000 |
| RPINR17 | 06C2 | — | HOME2R<6:0> | | | | | | | — | INDX2R<6:0> | | | | | | | 0000 |
| RPINR18 | 06C4 | — | U1CTSR<6:0> | | | | | | | — | U1RXR<6:0> | | | | | | | 0000 |
| RPINR19 | 06C6 | — | U2CTSR<6:0> | | | | | | | — | U2RXR<6:0> | | | | | | | 0000 |
| RPINR20 | 06C8 | — | SCK1R<6:0> | | | | | | | — | SDI1R<6:0> | | | | | | | 0000 |
| RPINR21 | 06CA | — | — | — | — | — | — | — | — | — | SS1R<6:0> | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | 0000 |
| RPINR24 | 06D0 | — | CSCKR<6:0> | | | | | | | — | CSDIR<6:0> | | | | | | | 0000 |
| RPINR25 | 06D2 | — | — | — | — | — | — | — | — | — | COFSR<6:0> | | | | | | | 0000 |
| RPINR26 | 06D4 | — | C2RXR<6:0> | | | | | | | — | C1RXR<6:0> | | | | | | | 0000 |
| RPINR27 | 06D6 | — | U3CTSR<6:0> | | | | | | | — | U3RXR<6:0> | | | | | | | 0000 |
| RPINR28 | 06D8 | — | U4CTSR<6:0> | | | | | | | — | U4RXR<6:0> | | | | | | | 0000 |
| RPINR29 | 06DA | — | SCK3R<6:0> | | | | | | | — | SDI3R<6:0> | | | | | | | 0000 |
| RPINR30 | 06DC | — | — | — | — | — | — | — | — | — | SS3R<6:0> | | | | | | | 0000 |
| RPINR31 | 06DE | — | SCK4R<6:0> | | | | | | | — | SDI4R<6:0> | | | | | | | 0000 |
| RPINR32 | 06E0 | — | — | — | — | — | — | — | — | — | SS4R<6:0> | | | | | | | 0000 |
| RPINR33 | 06E2 | — | IC10R<6:0> | | | | | | | — | IC9R<6:0> | | | | | | | 0000 |
| RPINR34 | 06E4 | — | IC12R<6:0> | | | | | | | — | IC11R<6:0> | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-40: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMU814 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR35 | 06E6 | — | IC14R<6:0> | | | | | | | — | IC13R<6:0> | | | | | | | 0000 |
| RPINR36 | 06E8 | — | IC16R<6:0> | | | | | | | — | IC15R<6:0> | | | | | | | 0000 |
| RPINR37 | 06EA | — | SYNCI1R<6:0> | | | | | | | — | OCFCR<6:0> | | | | | | | 0000 |
| RPINR38 | 06EC | — | DTCMP1R<6:0> | | | | | | | — | SYNCI2R<6:0> | | | | | | | 0000 |
| RPINR39 | 06EE | — | DTCMP3R<6:0> | | | | | | | — | DTCMP2R<6:0> | | | | | | | 0000 |
| RPINR40 | 06F0 | — | DTCMP5R<6:0> | | | | | | | — | DTCMP4R<6:0> | | | | | | | 0000 |
| RPINR41 | 06F2 | — | DTCMP7R<6:0> | | | | | | | — | DTCMP6R<6:0> | | | | | | | 0000 |
| RPINR42 | 06F4 | — | FLT6R<6:0> | | | | | | | — | FLT5R<6:0> | | | | | | | 0000 |
| RPINR43 | 06F6 | — | — | — | — | — | — | — | — | — | FLT7R<6:0> | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-41: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMU810 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | INT3R<6:0> | | | | | | | — | INT2R<6:0> | | | | | | | 0000 |
| RPINR2 | 06A4 | — | — | — | — | — | — | — | — | — | INT4R<6:0> | | | | | | | 0000 |
| RPINR3 | 06A6 | — | T3CKR<6:0> | | | | | | | — | T2CKR<6:0> | | | | | | | 0000 |
| RPINR4 | 06A8 | — | T5CKR<6:0> | | | | | | | — | T4CKR<6:0> | | | | | | | 0000 |
| RPINR5 | 06AA | — | T7CKR<6:0> | | | | | | | — | T6CKR<6:0> | | | | | | | 0000 |
| RPINR6 | 06AC | — | T9CKR<6:0> | | | | | | | — | T8CKR<6:0> | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | — | IC1R<6:0> | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | — | IC3R<6:0> | | | | | | | 0000 |
| RPINR9 | 06B2 | — | IC6R<6:0> | | | | | | | — | IC5R<6:0> | | | | | | | 0000 |
| RPINR10 | 06B4 | — | IC8R<6:0> | | | | | | | — | IC7R<6:0> | | | | | | | 0000 |
| RPINR11 | 06B6 | — | OCFBR<6:0> | | | | | | | — | OCFAR<6:0> | | | | | | | 0000 |
| RPINR12 | 06B8 | — | FLT2R<6:0> | | | | | | | — | FLT1R<6:0> | | | | | | | 0000 |
| RPINR13 | 06BA | — | FLT4R<6:0> | | | | | | | — | FLT3R<6:0> | | | | | | | 0000 |
| RPINR14 | 06BC | — | QEB1R<6:0> | | | | | | | — | QEA1R<6:0> | | | | | | | 0000 |
| RPINR15 | 06BE | — | HOME1R<6:0> | | | | | | | — | INDX1R<6:0> | | | | | | | 0000 |
| RPINR16 | 06C0 | — | QEB2R<6:0> | | | | | | | — | QEA2R<6:0> | | | | | | | 0000 |
| RPINR17 | 06C2 | — | HOME2R<6:0> | | | | | | | — | INDX2R<6:0> | | | | | | | 0000 |
| RPINR18 | 06C4 | — | U1CTSR<6:0> | | | | | | | — | U1RXR<6:0> | | | | | | | 0000 |
| RPINR19 | 06C6 | — | U2CTSR<6:0> | | | | | | | — | U2RXR<6:0> | | | | | | | 0000 |
| RPINR20 | 06C8 | — | SCK1R<6:0> | | | | | | | — | SDI1R<6:0> | | | | | | | 0000 |
| RPINR21 | 06CA | — | — | — | — | — | — | — | — | — | SS1R<6:0> | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | 0000 |
| RPINR24 | 06D0 | — | CSCKR<6:0> | | | | | | | — | CSDIR<6:0> | | | | | | | 0000 |
| RPINR25 | 06D2 | — | — | — | — | — | — | — | — | — | COFSINR<6:0> | | | | | | | 0000 |
| RPINR26 | 06D4 | — | C2RXR<6:0> | | | | | | | — | C1RXR<6:0> | | | | | | | 0000 |
| RPINR27 | 06D6 | — | U3CTSR<6:0> | | | | | | | — | U3RXR<6:0> | | | | | | | 0000 |
| RPINR28 | 06D8 | — | U4CTSR<6:0> | | | | | | | — | U4RXR<6:0> | | | | | | | 0000 |
| RPINR29 | 06DA | — | SCK3R<6:0> | | | | | | | — | SDI3R<6:0> | | | | | | | 0000 |
| RPINR30 | 06DC | — | — | — | — | — | — | — | — | — | SS3R<6:0> | | | | | | | 0000 |
| RPINR31 | 06DE | — | SCK4R<6:0> | | | | | | | — | SDI4R<6:0> | | | | | | | 0000 |
| RPINR32 | 06E0 | — | — | — | — | — | — | — | — | — | SS4R<6:0> | | | | | | | 0000 |
| RPINR33 | 06E2 | — | IC10R<6:0> | | | | | | | — | IC9R<6:0> | | | | | | | 0000 |
| RPINR34 | 06E4 | — | IC12R<6:0> | | | | | | | — | IC11R<6:0> | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-41: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMU810 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR35 | 06E6 | — | IC14R<6:0> | | | | | | | — | IC13R<6:0> | | | | | | | 0000 |
| RPINR36 | 06E8 | — | IC16R<6:0> | | | | | | | — | IC15R<6:0> | | | | | | | 0000 |
| RPINR37 | 06EA | — | SYNCI1R<6:0> | | | | | | | — | OCFCR<6:0> | | | | | | | 0000 |
| RPINR38 | 06EC | — | DTCMP1R<6:0> | | | | | | | — | SYNCI2R<6:0> | | | | | | | 0000 |
| RPINR39 | 06EE | — | DTCMP3R<6:0> | | | | | | | — | DTCMP2R<6:0> | | | | | | | 0000 |
| RPINR40 | 06F0 | — | DTCMP5R<6:0> | | | | | | | — | DTCMP4R<6:0> | | | | | | | 0000 |
| RPINR41 | 06F2 | — | — | — | — | — | — | — | — | — | DTCMP6R<6:0> | | | | | | | 0000 |
| RPINR42 | 06F4 | — | FLT6R<6:0> | | | | | | | — | FLT5R<6:0> | | | | | | | 0000 |
| RPINR43 | 06F6 | — | — | — | — | — | — | — | — | — | FLT7R<6:0> | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-42: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | INT3R<6:0> | | | | | | | — | INT2R<6:0> | | | | | | | 0000 |
| RPINR2 | 06A4 | — | — | — | — | — | — | — | — | — | INT4R<6:0> | | | | | | | 0000 |
| RPINR3 | 06A6 | — | T3CKR<6:0> | | | | | | | — | T2CKR<6:0> | | | | | | | 0000 |
| RPINR4 | 06A8 | — | T5CKR<6:0> | | | | | | | — | T4CKR<6:0> | | | | | | | 0000 |
| RPINR5 | 06AA | — | T7CKR<6:0> | | | | | | | — | T6CKR<6:0> | | | | | | | 0000 |
| RPINR6 | 06AC | — | T9CKR<6:0> | | | | | | | — | T8CKR<6:0> | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | — | IC1R<6:0> | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | — | IC3R<6:0> | | | | | | | 0000 |
| RPINR9 | 06B2 | — | IC6R<6:0> | | | | | | | — | IC5R<6:0> | | | | | | | 0000 |
| RPINR10 | 06B4 | — | IC8R<6:0> | | | | | | | — | IC7R<6:0> | | | | | | | 0000 |
| RPINR11 | 06B6 | — | OCFBR<6:0> | | | | | | | — | OCFAR<6:0> | | | | | | | 0000 |
| RPINR12 | 06B8 | — | FLT2R<6:0> | | | | | | | — | FLT1R<6:0> | | | | | | | 0000 |
| RPINR13 | 06BA | — | FLT4R<6:0> | | | | | | | — | FLT3R<6:0> | | | | | | | 0000 |
| RPINR14 | 06BC | — | QEB1R<6:0> | | | | | | | — | QEA1R<6:0> | | | | | | | 0000 |
| RPINR15 | 06BE | — | HOME1R<6:0> | | | | | | | — | INDX1R<6:0> | | | | | | | 0000 |
| RPINR16 | 06C0 | — | QEB2R<6:0> | | | | | | | — | QEA2R<6:0> | | | | | | | 0000 |
| RPINR17 | 06C2 | — | HOME2R<6:0> | | | | | | | — | INDX2R<6:0> | | | | | | | 0000 |
| RPINR18 | 06C4 | — | U1CTSR<6:0> | | | | | | | — | U1RXR<6:0> | | | | | | | 0000 |
| RPINR19 | 06C6 | — | U2CTSR<6:0> | | | | | | | — | U2RXR<6:0> | | | | | | | 0000 |
| RPINR20 | 06C8 | — | SCK1R<6:0> | | | | | | | — | SDI1R<6:0> | | | | | | | 0000 |
| RPINR21 | 06CA | — | — | — | — | — | — | — | — | — | SS1R<6:0> | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | 0000 |
| RPINR24 | 06D0 | — | CSCKR<6:0> | | | | | | | — | CSDIR<6:0> | | | | | | | 0000 |
| RPINR25 | 06D2 | — | — | — | — | — | — | — | — | — | COFSINR<6:0> | | | | | | | 0000 |
| RPINR26 | 06D4 | — | C2RXR<6:0> | | | | | | | — | C1RXR<6:0> | | | | | | | 0000 |
| RPINR27 | 06D6 | — | U3CTSR<6:0> | | | | | | | — | U3RXR<6:0> | | | | | | | 0000 |
| RPINR28 | 06D8 | — | U4CTSR<6:0> | | | | | | | — | U4RXR<6:0> | | | | | | | 0000 |
| RPINR29 | 06DA | — | SCK3R<6:0> | | | | | | | — | SDI3R<6:0> | | | | | | | 0000 |
| RPINR30 | 06DC | — | — | — | — | — | — | — | — | — | SS3R<6:0> | | | | | | | 0000 |
| RPINR31 | 06DE | — | SCK4R<6:0> | | | | | | | — | SDI4R<6:0> | | | | | | | 0000 |
| RPINR32 | 06E0 | — | — | — | — | — | — | — | — | — | SS4R<6:0> | | | | | | | 0000 |
| RPINR33 | 06E2 | — | IC10R<6:0> | | | | | | | — | IC9R<6:0> | | | | | | | 0000 |
| RPINR34 | 06E4 | — | IC12R<6:0> | | | | | | | — | IC11R<6:0> | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-42: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXX(MC/MU)806 DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR35 | 06E6 | — | IC14R<6:0> | | | | | | | — | IC13R<6:0> | | | | | | | 0000 |
| RPINR36 | 06E8 | — | IC16R<6:0> | | | | | | | — | IC15R<6:0> | | | | | | | 0000 |
| RPINR37 | 06EA | — | SYNCI1R<6:0> | | | | | | | — | OCFCR<6:0> | | | | | | | 0000 |
| RPINR38 | 06EC | — | DTCMP1R<6:0> | | | | | | | — | SYNCI2R<6:0> | | | | | | | 0000 |
| RPINR39 | 06EE | — | DTCMP3R<6:0> | | | | | | | — | DTCMP2R<6:0> | | | | | | | 0000 |
| RPINR40 | 06F0 | — | — | — | — | — | — | — | — | — | DTCMP4R<6:0> | | | | | | | 0000 |
| RPINR42 | 06F4 | — | FLT6R<6:0> | | | | | | | — | FLT5R<6:0> | | | | | | | 0000 |
| RPINR43 | 06F6 | — | — | — | — | — | — | — | — | — | FLT7R<6:0> | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-43: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | INT3R<6:0> | | | | | | | — | INT2R<6:0> | | | | | | | 0000 |
| RPINR2 | 06A4 | — | — | — | — | — | — | — | — | — | INT4R<6:0> | | | | | | | 0000 |
| RPINR3 | 06A6 | — | T3CKR<6:0> | | | | | | | — | T2CKR<6:0> | | | | | | | 0000 |
| RPINR4 | 06A8 | — | T5CKR<6:0> | | | | | | | — | T4CKR<6:0> | | | | | | | 0000 |
| RPINR5 | 06AA | — | T7CKR<6:0> | | | | | | | — | T6CKR<6:0> | | | | | | | 0000 |
| RPINR6 | 06AC | — | T9CKR<6:0> | | | | | | | — | T8CKR<6:0> | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | — | IC1R<6:0> | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | — | IC3R<6:0> | | | | | | | 0000 |
| RPINR9 | 06B2 | — | IC6R<6:0> | | | | | | | — | IC5R<6:0> | | | | | | | 0000 |
| RPINR10 | 06B4 | — | IC8R<6:0> | | | | | | | — | IC7R<6:0> | | | | | | | 0000 |
| RPINR11 | 06B6 | — | OCFBR<6:0> | | | | | | | — | OCFAR<6:0> | | | | | | | 0000 |
| RPINR18 | 06C4 | — | U1CTSR<6:0> | | | | | | | — | U1RXR<6:0> | | | | | | | 0000 |
| RPINR19 | 06C6 | — | U2CTSR<6:0> | | | | | | | — | U2RXR<6:0> | | | | | | | 0000 |
| RPINR20 | 06C8 | — | SCK1R<6:0> | | | | | | | — | SDI1R<6:0> | | | | | | | 0000 |
| RPINR21 | 06CA | — | — | — | — | — | — | — | — | — | SS1R<6:0> | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | 0000 |
| RPINR26 | 06D4 | — | C2RXR<6:0> | | | | | | | — | C1RXR<6:0> | | | | | | | 0000 |
| RPINR27 | 06D6 | — | U3CTSR<6:0> | | | | | | | — | U3RXR<6:0> | | | | | | | 0000 |
| RPINR28 | 06D8 | — | U4CTSR<6:0> | | | | | | | — | U4RXR<6:0> | | | | | | | 0000 |
| RPINR29 | 06DA | — | SCK3R<6:0> | | | | | | | — | SDI3R<6:0> | | | | | | | 0000 |
| RPINR30 | 06DC | — | — | — | — | — | — | — | — | — | SS3R<6:0> | | | | | | | 0000 |
| RPINR31 | 06DE | — | SCK4R<6:0> | | | | | | | — | SDI4R<6:0> | | | | | | | 0000 |
| RPINR32 | 06E0 | — | — | — | — | — | — | — | — | — | SS4R<6:0> | | | | | | | 0000 |
| RPINR33 | 06E2 | — | IC10R<6:0> | | | | | | | — | IC9R<6:0> | | | | | | | 0000 |
| RPINR34 | 06E4 | — | IC12R<6:0> | | | | | | | — | IC11R<6:0> | | | | | | | 0000 |
| RPINR35 | 06E6 | — | IC14R<6:0> | | | | | | | — | IC13R<6:0> | | | | | | | 0000 |
| RPINR36 | 06E8 | — | IC16R<6:0> | | | | | | | — | IC15R<6:0> | | | | | | | 0000 |
| RPINR37 | 06EA | — | — | — | — | — | — | — | — | — | OCFCR<6:0> | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-44: REFERENCE CLOCK REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REFOCON | 074E | ROON | — | ROSSLP | ROSEL | RODIV<3:0> | | | | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-45: NVM REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NVMCON | 0728 | WR | WREN | WRERR | NVMSIDL | — | — | — | — | — | — | — | — | NVMOP<3:0> | | | | 0000 |
| NVMADR | 072A | NVMADR<15:0> | | | | | | | | | | | | | | | | 0000 |
| NVMADRU | 072C | — | — | — | — | — | — | — | — | NVMADR<23:16> | | | | | | | | 0000 |
| NVMKEY | 072E | — | — | — | — | — | — | — | — | NVMKEY<7:0> | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-46: SYSTEM CONTROL REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RCON | 0740 | TRAPR | IOPUWR | — | — | VREGSF | — | CM | VREGS | EXTR | SWR | SWDTEN | WDTO | SLEEP | IDLE | BOR | POR | Note 1 |
| OSCCON | 0742 | — | COSC<2:0> | | | — | NOSC<2:0> | | | CLKLOCK | IOLOCK | LOCK | — | CF | — | LPOSCEN | OSWEN | Note 2 |
| CLKDIV | 0744 | ROI | DOZE<2:0> | | | DOZEN | FRCDIV<2:0> | | | PLLPOST<1:0> | | — | PLLPRE<4:0> | | | | | 3040 |
| PLLFBD | 0746 | — | — | — | — | — | — | — | PLLDIV<8:0> | | | | | | | | | 0030 |
| OSCTUN | 0748 | — | — | — | — | — | — | — | — | — | — | TUN<5:0> | | | | | | 0000 |
| ACLKCON3 | 0758 | ENAPLL | — | SELACLK | AOSCMD<1:0> | | ASRCSEL | FRCSEL | — | APLLPOST2<2:0> | | | — | — | APLLPRE<2:0> | | | 0000 |
| ACLKDIV3 | 075A | — | — | — | — | — | — | — | — | — | — | — | — | — | APLLDIV<2:0> | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
**Note 1:** RCON register Reset values are dependent on the type of Reset.
**2:** OSCCON register Reset values are dependent on the Configuration Fuses and by the type of Reset.


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**TABLE 4-47: PMD REGISTER MAP FOR dsPIC33EPXXXMU814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | QEI1MD | PWMMD | DCIMD | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | C2MD | C1MD | AD1MD | 0000 |
| PMD2 | 0762 | IC8MD | IC7MD | IC6MD | IC5MD | IC4MD | IC3MD | IC2MD | IC1MD | OC8MD | OC7MD | OC6MD | OC5MD | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | T9MD | T8MD | T7MD | T6MD | — | CMPMD | RTCCMD | PMPMD | CRCMD | — | QEI2MD | — | U3MD | — | I2C2MD | AD2MD | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | U4MD | — | REFOMD | — | — | USB1MD | 0000 |
| PMD5 | 0768 | IC16MD | IC15MD | IC14MD | IC13MD | IC12MD | IC11MD | IC10MD | IC9MD | OC16MD | OC15MD | OC14MD | OC13MD | OC12MD | OC11MD | OC10MD | OC9MD | 0000 |
| PMD6 | 076A | — | PWM7MD | PWM6MD | PWM5MD | PWM4MD | PWM3MD | PWM2MD | PWM1MD | — | — | — | — | — | — | SPI4MD | SPI3MD | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | DMA12MD | DMA8MD | DMA4MD | DMA0MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | DMA13MD | DMA9MD | DMA5MD | DMA1MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | DMA14MD | DMA10MD | DMA6MD | DMA2MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | — | DMA11MD | DMA7MD | DMA3MD | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-48: PMD REGISTER MAP FOR dsPIC33EPXXXMU810 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | QEI1MD | PWMMD | DCIMD | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | C2MD | C1MD | AD1MD | 0000 |
| PMD2 | 0762 | IC8MD | IC7MD | IC6MD | IC5MD | IC4MD | IC3MD | IC2MD | IC1MD | OC8MD | OC7MD | OC6MD | OC5MD | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | T9MD | T8MD | T7MD | T6MD | — | CMPMD | RTCCMD | PMPMD | CRCMD | — | QEI2MD | — | U3MD | — | I2C2MD | AD2MD | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | U4MD | — | REFOMD | — | — | USB1MD | 0000 |
| PMD5 | 0768 | IC16MD | IC15MD | IC14MD | IC13MD | IC12MD | IC11MD | IC10MD | IC9MD | OC16MD | OC15MD | OC14MD | OC13MD | OC12MD | OC11MD | OC10MD | OC9MD | 0000 |
| PMD6 | 076A | — | — | PWM6MD | PWM5MD | PWM4MD | PWM3MD | PWM2MD | PWM1MD | — | — | — | — | — | — | SPI4MD | SPI3MD | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | DMA12MD | DMA8MD | DMA4MD | DMA0MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | DMA13MD | DMA9MD | DMA5MD | DMA1MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | DMA14MD | DMA10MD | DMA6MD | DMA2MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | — | DMA11MD | DMA7MD | DMA3MD | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-49: PMD REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | QEI1MD | PWMMD | DCIMD | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | C2MD | C1MD | AD1MD | 0000 |
| PMD2 | 0762 | IC8MD | IC7MD | IC6MD | IC5MD | IC4MD | IC3MD | IC2MD | IC1MD | OC8MD | OC7MD | OC6MD | OC5MD | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | T9MD | T8MD | T7MD | T6MD | — | CMPMD | RTCCMD | PMPMD | CRCMD | — | QEI2MD | — | U3MD | — | I2C2MD | AD2MD | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | U4MD | — | REFOMD | — | — | USB1MD | 0000 |
| PMD5 | 0768 | IC16MD | IC15MD | IC14MD | IC13MD | IC12MD | IC11MD | IC10MD | IC9MD | OC16MD | OC15MD | OC14MD | OC13MD | OC12MD | OC11MD | OC10MD | OC9MD | 0000 |
| PMD6 | 076A | — | — | — | — | PWM4MD | PWM3MD | PWM2MD | PWM1MD | — | — | — | — | — | — | SPI4MD | SPI3MD | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | DMA12MD | DMA8MD | DMA4MD | DMA0MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | DMA13MD | DMA9MD | DMA5MD | DMA1MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | DMA14MD | DMA10MD | DMA6MD | DMA2MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | — | DMA11MD | DMA7MD | DMA3MD | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-50: PMD REGISTER MAP FOR dsPIC33EPXXXMC806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | QEI1MD | PWMMD | DCIMD | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | C2MD | C1MD | AD1MD | 0000 |
| PMD2 | 0762 | IC8MD | IC7MD | IC6MD | IC5MD | IC4MD | IC3MD | IC2MD | IC1MD | OC8MD | OC7MD | OC6MD | OC5MD | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | T9MD | T8MD | T7MD | T6MD | — | CMPMD | RTCCMD | PMPMD | CRCMD | — | QEI2MD | — | U3MD | — | I2C2MD | AD2MD | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | U4MD | — | REFOMD | — | — | — | 0000 |
| PMD5 | 0768 | IC16MD | IC15MD | IC14MD | IC13MD | IC12MD | IC11MD | IC10MD | IC9MD | OC16MD | OC15MD | OC14MD | OC13MD | OC12MD | OC11MD | OC10MD | OC9MD | 0000 |
| PMD6 | 076A | — | — | — | — | PWM4MD | PWM3MD | PWM2MD | PWM1MD | — | — | — | — | — | — | SPI4MD | SPI3MD | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | DMA12MD | DMA8MD | DMA4MD | DMA0MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | DMA13MD | DMA9MD | DMA5MD | DMA1MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | DMA14MD | DMA10MD | DMA6MD | DMA2MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | — | DMA11MD | DMA7MD | DMA3MD | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-51: PMD REGISTER MAP FOR dsPIC33EPXXXGP8XX AND PIC24EPXXXGP8XX DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | — | — | DCIMD | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | C2MD | C1MD | AD1MD | 0000 |
| PMD2 | 0762 | IC8MD | IC7MD | IC6MD | IC5MD | IC4MD | IC3MD | IC2MD | IC1MD | OC8MD | OC7MD | OC6MD | OC5MD | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | T9MD | T8MD | T7MD | T6MD | — | CMPMD | RTCCMD | PMPMD | CRCMD | — | — | — | U3MD | — | I2C2MD | AD2MD | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | U4MD | — | REFOMD | — | — | — | 0000 |
| PMD5 | 0768 | IC16MD | IC15MD | IC14MD | IC13MD | IC12MD | IC11MD | IC10MD | IC9MD | OC16MD | OC15MD | OC14MD | OC13MD | OC12MD | OC11MD | OC10MD | OC9MD | 0000 |
| PMD6 | 076A | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SPI4MD | SPI3MD | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | DMA12MD | DMA8MD | DMA4MD | DMA0MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | DMA13MD | DMA9MD | DMA5MD | DMA1MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | DMA14MD | DMA10MD | DMA6MD | DMA2MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | — | DMA11MD | DMA7MD | DMA3MD | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-52: PMD REGISTER MAP FOR PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | — | — | DCIMD | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | C2MD | C1MD | AD1MD | 0000 |
| PMD2 | 0762 | IC8MD | IC7MD | IC6MD | IC5MD | IC4MD | IC3MD | IC2MD | IC1MD | OC8MD | OC7MD | OC6MD | OC5MD | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | T9MD | T8MD | T7MD | T6MD | — | CMPMD | RTCCMD | PMPMD | CRCMD | — | — | — | U3MD | — | I2C2MD | AD2MD | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | U4MD | — | REFOMD | — | — | USB1MD | 0000 |
| PMD5 | 0768 | IC16MD | IC15MD | IC14MD | IC13MD | IC12MD | IC11MD | IC10MD | IC9MD | OC16MD | OC15MD | OC14MD | OC13MD | OC12MD | OC11MD | OC10MD | OC9MD | 0000 |
| PMD6 | 076A | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SPI4MD | SPI3MD | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | DMA12MD | DMA8MD | DMA4MD | DMA0MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | DMA13MD | DMA9MD | DMA5MD | DMA1MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | DMA14MD | DMA10MD | DMA6MD | DMA2MD | — | — | — | — | 0000 |
| | | — | — | — | — | — | — | — | — | — | DMA11MD | DMA7MD | DMA3MD | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-53: COMPARATOR REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CMSTAT | 0A80 | CMSIDL | — | — | — | — | C3EVT | C2EVT | C1EVT | — | — | — | — | — | C3OUT | C2OUT | C1OUT | 0000 |
| CVRCON | 0A82 | — | — | — | — | — | VREFSEL | BGSEL<1:0> | | CVREN | CVROE | CVRR | CVRSS | CVR<3:0> | | | | 0000 |
| CM1CON | 0A84 | CON | COE | CPOL | — | — | — | CEVT | COUT | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | | 0000 |
| CM1MSKSRC | 0A86 | — | — | — | — | SELSRCC<3:0> | | | | SELSRCB<3:0> | | | | SELSRCA<3:0> | | | | 0000 |
| CM1MSKCON | 0A88 | HLMS | — | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN | NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN | 0000 |
| CM1FLTR | 0A8A | — | — | — | — | — | — | — | — | — | CFSEL<2:0> | | | CFLTREN | CFDIV<2:0> | | | 0000 |
| CM2CON | 0A8C | CON | COE | CPOL | — | — | — | CEVT | COUT | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | | 0000 |
| CM2MSKSRC | 0A8E | — | — | — | — | SELSRCC<3:0> | | | | SELSRCB<3:0> | | | | SELSRCA<3:0> | | | | 0000 |
| CM2MSKCON | 0A90 | HLMS | — | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN | NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN | 0000 |
| CM2FLTR | 0A92 | — | — | — | — | — | — | — | — | — | CFSEL<2:0> | | | CFLTREN | CFDIV<2:0> | | | 0000 |
| CM3CON | 0A94 | CON | COE | CPOL | — | — | — | CEVT | COUT | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | | 0000 |
| CM3MSKSRC | 0A96 | — | — | — | — | SELSRCC<3:0> | | | | SELSRCB<3:0> | | | | SELSRCA<3:0> | | | | 0000 |
| CM3MSKCON | 0A98 | HLMS | — | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN | NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN | 0000 |
| CM3FLTR | 0A9A | — | — | — | — | — | — | — | — | — | CFSEL<2:0> | | | CFLTREN | CFDIV<2:0> | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-54: DMAC REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DMA0CON | 0B00 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA0REQ | 0B02 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA0STAL | 0B04 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA0STAH | 0B06 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA0STBL | 0B08 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA0STBH | 0B0A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA0PAD | 0B0C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA0CNT | 0B0E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA1CON | 0B10 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA1REQ | 0B12 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA1STAL | 0B14 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA1STAH | 0B16 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA1STBL | 0B18 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA1STBH | 0B1A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA1PAD | 0B1C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA1CNT | 0B1E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA2CON | 0B20 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA2REQ | 0B22 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA2STAL | 0B24 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA2STAH | 0B26 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA2STBL | 0B28 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA2STBH | 0B2A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA2PAD | 0B2C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA2CNT | 0B2E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA2CON | 0B30 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA3REQ | 0B32 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA3STAL | 0B34 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA3STAH | 0B36 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA3STBL | 0B38 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA3STBH | 0B3A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA3PAD | 0B3C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA3CNT | 0B3E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA4CON | 0B40 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA4REQ | 0B42 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-54: DMAC REGISTER MAP (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DMA4STAL | 0B44 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA4STAH | 0B46 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA4STBL | 0B48 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA4STBH | 0B4A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA4PAD | 0B4C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA4CNT | 0B4E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA5CON | 0B50 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA5REQ | 0B52 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA5STAL | 0B54 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA5STAH | 0B56 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA5STBL | 0B58 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA5STBH | 0B5A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA5PAD | 0B5C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA5CNT | 0B5E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA6CON | 0B60 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA6REQ | 0B62 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA6STAL | 0B64 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA6STAH | 0B66 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA6STBL | 0B68 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA6STBH | 0B6A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA6PAD | 0B6C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA6CNT | 0B6E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA7CON | 0B70 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA7REQ | 0B72 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA7STAL | 0B74 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA7STAH | 0B76 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA7STBL | 0B78 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA7STBH | 0B7A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA7PAD | 0B7C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA7CNT | 0B7E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA8CON | 0B80 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA8REQ | 0B82 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA8STAL | 0B84 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA8STAH | 0B86 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA8STBL | 0B88 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-54: DMAC REGISTER MAP (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DMA8STBH | 0B8A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA8PAD | 0B8C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA8CNT | 0B8E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA9CON | 0B90 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA9REQ | 0B92 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA9STAL | 0B94 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA9STAH | 0B96 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA9STBL | 0B98 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA9STBH | 0B9A | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA9PAD | 0B9C | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA9CNT | 0B9E | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA10CON | 0BA0 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA10REQ | 0BA2 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA10STAL | 0BA4 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA10STAH | 0BA6 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA10STBL | 0BA8 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA10STBH | 0BAA | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA10PAD | 0BAC | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA10CNT | 0BAE | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA11CON | 0BB0 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DM11AREQ | 0BB2 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA11STAL | 0BB4 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA11STAH | 0BB6 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA11STBL | 0BB8 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA11STBH | 0BBA | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA11PAD | 0BBC | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA11CNT | 0BBE | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA12CON | 0BC0 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA12REQ | 0BC2 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA12STAL | 0BC4 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA12STAH | 0BC6 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA12STBL | 0BC8 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA12STBH | 0BCA | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA12PAD | 0BCC | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA12CNT | 0BCE | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-54: DMAC REGISTER MAP (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DMA13CON | 0BD0 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA13REQ | 0BD2 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA13STAL | 0BD4 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA13STAH | 0BD6 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA13STBL | 0BD8 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA13STBH | 0BDA | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA13PAD | 0BDC | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA13CNT | 0BDE | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMA14CON | 0BE0 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE<1:0> | | — | — | MODE<1:0> | | 0000 |
| DMA14REQ | 0BE2 | FORCE | — | — | — | — | — | — | — | IRQSEL<7:0> | | | | | | | | 00FF |
| DMA14STAL | 0BE4 | STA<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA14STAH | 0BE6 | — | — | — | — | — | — | — | — | STA<23:16> | | | | | | | | 0000 |
| DMA14STBL | 0BE8 | STB<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA14STBH | 0BEA | — | — | — | — | — | — | — | — | STB<23:16> | | | | | | | | 0000 |
| DMA14PAD | 0BEC | PAD<15:0> | | | | | | | | | | | | | | | | 0000 |
| DMA14CNT | 0BEE | — | — | CNT<13:0> | | | | | | | | | | | | | | 0000 |
| DMAPWC | 0BF0 | — | PWCOL14 | PWCOL13 | PWCOL12 | PWCOL11 | PWCOL10 | PWCOL9 | PWCOL8 | PWCOL7 | PWCOL6 | PWCOL5 | PWCOL4 | PWCOL3 | PWCOL2 | PWCOL1 | PWCOL0 | 0000 |
| DMARQC | 0BF2 | — | RQCOL14 | RQCOL13 | RQCOL12 | RQCOL11 | RQCOL10 | RQCOL9 | RQCOL8 | RQCOL7 | RQCOL6 | RQCOL5 | RQCOL4 | RQCOL3 | RQCOL2 | RQCOL1 | RQCOL0 | 0000 |
| DMAPPS | 0BF4 | — | PPST14 | PPST13 | PPST12 | PPST11 | PPST10 | PPST9 | PPST8 | PPST7 | PPST6 | PPST5 | PPST4 | PPST3 | PPST2 | PPST1 | PPST0 | 0000 |
| DMALCA | 0BF6 | — | — | — | — | — | — | — | — | — | — | — | — | LSTCH<3:0> | | | | 000F |
| DSADRL | 0BF8 | DSADR<15:0> | | | | | | | | | | | | | | | | 0000 |
| DSADRH | 0BFA | — | — | — | — | — | — | — | — | DSADR<23:16> | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-55: PORTA REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 0E00 | TRISA15 | TRISA14 | — | — | — | TRISA10 | TRISA9 | — | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | C6FF |
| PORTA | 0E02 | RA15 | RA14 | — | — | — | RA10 | RA9 | — | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | xxxx |
| LATA | 0E04 | LATA15 | LATA14 | — | — | — | LATA10 | LATA9 | — | LATA7 | LATA6 | LATA5 | LATA4 | LATA3 | LATA2 | LATA1 | LATA0 | xxxx |
| ODCA | 0E06 | ODCA15 | ODCA14 | — | — | — | — | — | — | — | — | ODCA5 | ODCA4 | ODCA3 | ODCA2 | ODCA1 | ODCA0 | 0000 |
| CNENA | 0E08 | CNIEA15 | CNIEA14 | — | — | — | CNIEA10 | CNIEA9 | — | CNIEA7 | CNIEA6 | CNIEA5 | CNIEA4 | CNIEA3 | CNIEA2 | CNIEA1 | CNIEA0 | 0000 |
| CNPUA | 0E0A | CNPUA15 | CNPUA14 | — | — | — | CNPUA10 | CNPUA9 | — | CNPUA7 | CNPUA6 | CNPUA5 | CNPUA4 | CNPUA3 | CNPUA2 | CNPUA1 | CNPUA0 | 0000 |
| CNPDA | 0E0C | CNPDA15 | CNPDA14 | — | — | — | CNPDA10 | CNPDA9 | — | CNPDA7 | CNPDA6 | CNPDA5 | CNPDA4 | CNPDA3 | CNPDA2 | CNPDA1 | CNPDA0 | 0000 |
| ANSELA | 0E0E | — | — | — | — | — | ANSA10 | ANSA9 | — | ANSA7 | ANSA6 | — | — | — | — | — | — | 06C0 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-56: PORTB REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 0E10 | TRISB15 | TRISB14 | TRISB13 | TRISB12 | TRISB11 | TRISB10 | TRISB9 | TRISB8 | TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 | FFFF |
| PORTB | 0E12 | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx |
| LATB | 0E14 | LATB15 | LATB14 | LATB13 | LATB12 | LATB11 | LATB10 | LATB9 | LATB8 | LATB7 | LATB6 | LATB5 | LATB4 | LATB3 | LATB2 | LATB1 | LATB0 | xxxx |
| ODCB | 0E16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNENB | 0E18 | CNIEB15 | CNIEB14 | CNIEB13 | CNIEB12 | CNIEB11 | CNIEB10 | CNIEB9 | CNIEB8 | CNIEB7 | CNIEB6 | CNIEB5 | CNIEB4 | CNIEB3 | CNIEB2 | CNIEB1 | CNIEB0 | 0000 |
| CNPUB | 0E1A | CNPUB15 | CNPUB14 | CNPUB13 | CNPUB12 | CNPUB11 | CNPUB10 | CNPUB9 | CNPUB8 | CNPUB7 | CNPUB6 | CNPUB5 | CNPUB4 | CNPUB3 | CNPUB2 | CNPUB1 | CNPUB0 | 0000 |
| CNPDB | 0E1C | CNPDB15 | CNPDB14 | CNPDB13 | CNPDB12 | CNPDB11 | CNPDB10 | CNPDB9 | CNPDB8 | CNPDB7 | CNPDB6 | CNPDB5 | CNPDB4 | CNPDB3 | CNPDB2 | CNPDB1 | CNPDB0 | 0000 |
| ANSELB | 0E1E | ANSB15 | ANSB14 | ANSB13 | ANSB12 | ANSB11 | ANSB10 | ANSB9 | ANSB8 | ANSB7 | ANSB6 | ANSB5 | ANSB4 | ANSB3 | ANSB2 | ANSB1 | ANSB0 | FFFF |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-57: PORTC REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISC | 0E20 | TRISC15 | TRISC14 | TRISC13 | TRISC12 | — | — | — | — | — | — | — | TRISC4 | TRISC3 | TRISC2 | TRISC1 | — | F01E |
| PORTC | 0E22 | RC15 | RC14 | RC13 | RC12 | — | — | — | — | — | — | — | RC4 | RC3 | RC2 | RC1 | — | xxxx |
| LATC | 0E24 | LATC15 | LATC14 | LATC13 | LATC12 | — | — | — | — | — | — | — | LATC4 | LATC3 | LATC2 | LATC1 | — | xxxx |
| ODCC | 0E26 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNENC | 0E28 | CNIEC15 | CNIEC14 | CNIEC13 | CNIEC12 | — | — | — | — | — | — | — | CNIEC4 | CNIEC3 | CNIEC2 | CNIEC1 | — | 0000 |
| CNPUC | 0E2A | CNPUC15 | CNPUC14 | CNPUC13 | CNPUC12 | — | — | — | — | — | — | — | CNPUC4 | CNPUC3 | CNPUC2 | CNPUC1 | — | 0000 |
| CNPDC | 0E2C | CNPDC15 | CNPDC14 | CNPDC13 | CNPDC12 | — | — | — | — | — | — | — | CNPDC4 | CNPDC3 | CNPDC2 | CNPDC1 | — | 0000 |
| ANSELC | 0E2E | — | ANSC14 | ANSC13 | — | — | — | — | — | — | — | — | ANSC4 | ANSC3 | ANSC2 | ANSC1 | — | 601E |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-58: PORTC REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY**

| File Name | Addr, | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISC | 0E20 | TRISC15 | TRISC14 | TRISC13 | TRISC12 | — | — | — | — | — | — | — | — | — | — | — | — | F000 |
| PORTC | 0E22 | RC15 | RC14 | RC13 | RC12 | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| LATC | 0E24 | LATC15 | LATC14 | LATC13 | LATC12 | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| ODCC | 0E26 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNENC | 0E28 | CNIEC15 | CNIEC14 | CNIEC13 | CNIEC12 | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNPUC | 0E2A | CNPUC15 | CNPUC14 | CNPUC13 | CNPUC12 | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNPDC | 0E2C | CNPDC15 | CNPDC14 | CNPDC13 | CNPDC12 | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| ANSELC | 0E2E | — | ANSC14 | ANSC13 | — | — | — | — | — | — | — | — | — | — | — | — | — | 6000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-59: PORTD REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISD | 0E30 | TRISD15 | TRISD14 | TRISD13 | TRISD12 | TRISD11 | TRISD10 | TRISD9 | TRISD8 | TRISD7 | TRISD6 | TRISD5 | TRISD4 | TRISD3 | TRISD2 | TRISD1 | TRISD0 | FFFF |
| PORTD | 0E32 | RD15 | RD14 | RD13 | RD12 | RD11 | RD10 | RD9 | RD8 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 | xxxx |
| LATD | 0E34 | LATD15 | LATD14 | LATD13 | LATD12 | LATD11 | LATD10 | LATD9 | LATD8 | LATD7 | LATD6 | LATD5 | LATD4 | LATD3 | LATD2 | LATD1 | LATD0 | xxxx |
| ODCD | 0E36 | ODCD15 | ODCD14 | ODCD13 | ODCD12 | ODCD11 | ODCD10 | ODCD9 | ODCD8 | — | — | ODCD5 | ODCD4 | ODCD3 | ODCD2 | ODCD1 | ODCD0 | 0000 |
| CNEND | 0E38 | CNIED15 | CNIED14 | CNIED13 | CNIED12 | CNIED11 | CNIED10 | CNIED9 | CNIED8 | CNIED7 | CNIED6 | CNIED5 | CNIED4 | CNIED3 | CNIED2 | CNIED1 | CNIED0 | 0000 |
| CNPUD | 0E3A | CNPUD15 | CNPUD14 | CNPUD13 | CNPUD12 | CNPUD11 | CNPUD10 | CNPUD9 | CNPUD8 | CNPUD7 | CNPUD6 | CNPUD5 | CNPUD4 | CNPUD3 | CNPUD2 | CNPUD1 | CNPUD0 | 0000 |
| CNPDD | 0E3C | CNPDD15 | CNPDD14 | CNPDD13 | CNPDD12 | CNPDD11 | CNPDD10 | CNPDD9 | CNPDD8 | CNPDD7 | CNPDD6 | CNPDD5 | CNPDD4 | CNPDD3 | CNPDD2 | CNPDD1 | CNPDD0 | 0000 |
| ANSELD | 0E3E | — | — | — | — | — | — | — | — | ANSD7 | ANSD6 | — | — | — | — | — | — | 00C0 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-60: PORTD REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISD | 0E30 | — | — | — | — | TRISD11 | TRISD10 | TRISD9 | TRISD8 | TRISD7 | TRISD6 | TRISD5 | TRISD4 | TRISD3 | TRISD2 | TRISD1 | TRISD0 | 0FFF |
| PORTD | 0E32 | — | — | — | — | RD11 | RD10 | RD9 | RD8 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 | xxxx |
| LATD | 0E34 | — | — | — | — | LATD11 | LATD10 | LATD9 | LATD8 | LATD7 | LATD6 | LATD5 | LATD4 | LATD3 | LATD2 | LATD1 | LATD0 | xxxx |
| ODCD | 0E36 | — | — | — | — | ODCD11 | ODCD10 | ODCD9 | ODCD8 | — | — | ODCD5 | ODCD4 | ODCD3 | ODCD2 | ODCD1 | ODCD0 | 0000 |
| CNEND | 0E38 | — | — | — | — | CNIED11 | CNIED10 | CNIED9 | CNIED8 | CNIED7 | CNIED6 | CNIED5 | CNIED4 | CNIED3 | CNIED2 | CNIED1 | CNIED0 | 0000 |
| CNPUD | 0E3A | — | — | — | — | CNPUD11 | CNPUD10 | CNPUD9 | CNPUD8 | CNPUD7 | CNPUD6 | CNPUD5 | CNPUD4 | CNPUD3 | CNPUD2 | CNPUD1 | CNPUD0 | 0000 |
| CNPDD | 0E3C | — | — | — | — | CNPDD11 | CNPDD10 | CNPDD9 | CNPDD8 | CNPDD7 | CNPDD6 | CNPDD5 | CNPDD4 | CNPDD3 | CNPDD2 | CNPDD1 | CNPDD0 | 0000 |
| ANSELD | 0E3E | — | — | — | — | — | — | — | — | ANSD7 | ANSD6 | — | — | — | — | — | — | 00C0 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-61: PORTE REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISE | 0E40 | — | — | — | — | — | — | TRISE9 | TRISE8 | TRISE7 | TRISE6 | TRISE5 | TRISE4 | TRISE3 | TRISE2 | TRISE1 | TRISE0 | 03FF |
| PORTE | 0E42 | — | — | — | — | — | — | RE9 | RE8 | RE7 | RE6 | RE5 | RE4 | RE3 | RE2 | RE1 | RE0 | xxxx |
| LATE | 0E44 | — | — | — | — | — | — | LATE9 | LATE8 | LATE7 | LATE6 | LATE5 | LATE4 | LATE3 | LATE2 | LATE1 | LATE0 | xxxx |
| ODCE | 0E46 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNENE | 0E48 | — | — | — | — | — | — | CNIEE9 | CNIEE8 | CNIEE7 | CNIEE6 | CNIEE5 | CNIEE4 | CNIEE3 | CNIEE2 | CNIEE1 | CNIEE0 | 0000 |
| CNPUE | 0E4A | — | — | — | — | — | — | CNPUE9 | CNPUE8 | CNPUE7 | CNPUE6 | CNPUE5 | CNPUE4 | CNPUE3 | CNPUE2 | CNPUE1 | CNPUE0 | 0000 |
| CNPDE | 0E4C | — | — | — | — | — | — | CNPDE9 | CNPDE8 | CNPDE7 | CNPDE6 | CNPDE5 | CNPDE4 | CNPDE3 | CNPDE2 | CNPDE1 | CNPDE0 | 0000 |
| ANSELE | 0E4E | — | — | — | — | — | — | ANSE9 | ANSE8 | ANSE7 | ANSE6 | ANSE5 | ANSE4 | ANSE3 | ANSE2 | ANSE1 | ANSE0 | 03FF |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-62: PORTE REGISTER MAP FOR dsPIC33EPXXX(GP/MC/MU)806 AND PIC24EPXXXGP806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISE | 0E40 | — | — | — | — | — | — | — | — | TRISE7 | TRISE6 | TRISE5 | TRISE4 | TRISE3 | TRISE2 | TRISE1 | TRISE0 | 00FF |
| PORTE | 0E42 | — | — | — | — | — | — | — | — | RE7 | RE6 | RE5 | RE4 | RE3 | RE2 | RE1 | RE0 | xxxx |
| LATE | 0E44 | — | — | — | — | — | — | — | — | LATE7 | LATE6 | LATE5 | LATE4 | LATE3 | LATE2 | LATE1 | LATE0 | xxxx |
| ODCE | 0E46 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNENE | 0E48 | — | — | — | — | — | — | — | — | CNIEE7 | CNIEE6 | CNIEE5 | CNIEE4 | CNIEE3 | CNIEE2 | CNIEE1 | CNIEE0 | 0000 |
| CNPUE | 0E4A | — | — | — | — | — | — | — | — | CNPUE7 | CNPUE6 | CNPUE5 | CNPUE4 | CNPUE3 | CNPUE2 | CNPUE1 | CNPUE0 | 0000 |
| CNPDE | 0E4C | — | — | — | — | — | — | — | — | CNPDE7 | CNPDE6 | CNPDE5 | CNPDE4 | CNPDE3 | CNPDE2 | CNPDE1 | CNPDE0 | 0000 |
| ANSELE | 0E4E | — | — | — | — | — | — | — | — | ANSE7 | ANSE6 | ANSE5 | ANSE4 | ANSE3 | ANSE2 | ANSE1 | ANSE0 | 00FF |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-63: PORTF REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISF | 0E50 | — | — | TRISF13 | TRISF12 | — | — | — | TRISF8 | — | — | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | 313F |
| PORTF | 0E52 | — | — | RF13 | RF12 | — | — | — | RF8 | — | — | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx |
| LATF | 0E54 | — | — | LATF13 | LATF12 | — | — | — | LATF8 | — | — | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx |
| ODCF | 0E56 | — | — | ODCF13 | ODCF12 | — | — | — | ODCF8 | — | — | ODCF5 | ODCF4 | ODCF3 | ODCF2 | ODCF1 | ODCF0 | 0000 |
| CNENF | 0E58 | — | — | CNIEF13 | CNIEF12 | — | — | — | CNIEF8 | — | — | CNIEF5 | CNIEF4 | CNIEF3 | CNIEF2 | CNIEF1 | CNIEF0 | 0000 |
| CNPUF | 0E5A | — | — | CNPUF13 | CNPUF12 | — | — | — | CNPUF8 | — | — | CNPUF5 | CNPUF4 | CNPUF3 | CNPUF2 | CNPUF1 | CNPUF0 | 0000 |
| CNPDF | 0E5C | — | — | CNPDF13 | CNPDF12 | — | — | — | CNPDF8 | — | — | CNPDF5 | CNPDF4 | CNPDF3 | CNPDF2 | CNPDF1 | CNPDF0 | 0000 |
| ANSELF | 0E5E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-64: PORTF REGISTER MAP FOR dsPIC33EPXXX(GP/MC)806 AND PIC24EPXXXGP806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISF | 0E50 | — | — | — | — | — | — | — | — | — | TRISG6 | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | 003B |
| PORTF | 0E52 | — | — | — | — | — | — | — | — | — | RG6 | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx |
| LATF | 0E54 | — | — | — | — | — | — | — | — | — | LATG6 | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx |
| ODCF | 0E56 | — | — | — | — | — | — | — | — | — | ODCF6 | ODCF5 | ODCF4 | ODCF3 | ODCF2 | ODCF1 | ODCF0 | 0000 |
| CNENF | 0E58 | — | — | — | — | — | — | — | — | — | CNIEG6 | CNIEF5 | CNIEF4 | CNIEF3 | CNIEF2 | CNIEF1 | CNIEF0 | 0000 |
| CNPUF | 0E5A | — | — | — | — | — | — | — | — | — | CNPUG6 | CNPUF5 | CNPUF4 | CNPUF3 | CNPUF2 | CNPUF1 | CNPUF0 | 0000 |
| CNPDF | 0E5C | — | — | — | — | — | — | — | — | — | CNPDG6 | CNPDF5 | CNPDF4 | CNPDF3 | CNPDF2 | CNPDF1 | CNPDF0 | 0000 |
| ANSELF | 0E5E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-65: PORTF REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISF | 0E50 | — | — | — | — | — | — | — | — | — | — | TRISF5 | TRISF4 | TRISF3 | — | TRISF1 | TRISF0 | 003B |
| PORTF | 0E52 | — | — | — | — | — | — | — | — | — | — | RF5 | RF4 | RF3 | — | RF1 | RF0 | xxxx |
| LATF | 0E54 | — | — | — | — | — | — | — | — | — | — | LATF5 | LATF4 | LATF3 | — | LATF1 | LATF0 | xxxx |
| ODCF | 0E56 | — | — | — | — | — | — | — | — | — | — | ODCF5 | ODCF4 | ODCF3 | — | ODCF1 | ODCF0 | 0000 |
| CNENF | 0E58 | — | — | — | — | — | — | — | — | — | — | CNIEF5 | CNIEF4 | CNIEF3 | — | CNIEF1 | CNIEF0 | 0000 |
| CNPUF | 0E5A | — | — | — | — | — | — | — | — | — | — | CNPUF5 | CNPUF4 | CNPUF3 | — | CNPUF1 | CNPUF0 | 0000 |
| CNPDF | 0E5C | — | — | — | — | — | — | — | — | — | — | CNPDF5 | CNPDF4 | CNPDF3 | — | CNPDF1 | CNPDF0 | 0000 |
| ANSELF | 0E5E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-66: PORTG REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISG | 0E60 | TRISG15 | TRISG14 | TRISG13 | TRISG12 | — | — | TRISG9 | TRISG8 | TRISG7 | TRISG6 | — | — | — | — | TRISG1 | TRISG0 | F3C3 |
| PORTG | 0E62 | RG15 | RG14 | RG13 | RG12 | — | — | RG9 | RG8 | RG7 | RG6 | — | — | RG3(1) | RG2(1) | RG1 | RG0 | xxxx |
| LATG | 0E64 | LATG15 | LATG14 | LATG13 | LATG12 | — | — | LATG9 | LATG8 | LATG7 | LATG6 | — | — | — | — | LATG1 | LATG0 | xxxx |
| ODCG | 0E66 | ODCG15 | ODCG14 | ODCG13 | ODCG12 | — | — | — | — | — | — | — | — | — | — | ODCG1 | ODCG0 | 0000 |
| CNENG | 0E68 | CNIEG15 | CNIEG14 | CNIEG13 | CNIEG12 | — | — | CNIEG9 | CNIEG8 | CNIEG7 | CNIEG6 | — | — | CNIEG3(1) | CNIEG2(1) | CNIEG1 | CNIEG0 | 0000 |
| CNPUG | 0E6A | CNPUG15 | CNPUG14 | CNPUG13 | CNPUG12 | — | — | CNPUG9 | CNPUG8 | CNPUG7 | CNPUG6 | — | — | — | — | CNPUG1 | CNPUG0 | 0000 |
| CNPDG | 0E6C | CNPDG15 | CNPDG14 | CNPDG13 | CNPDG12 | — | — | CNPDG9 | CNPDG8 | CNPDG7 | CNPDG6 | — | — | — | — | CNPDG1 | CNPDG0 | 0000 |
| ANSELG | 0E6E | — | — | — | — | — | — | ANSG9 | ANSG8 | ANSG7 | ANSG6 | — | — | — | — | — | — | 03C0 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** If RG2 and RG3 are used as general purpose inputs, the $V_{USB3V3}$ pin must be connected to $V_{DD}$.



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**TABLE 4-67: PORTG REGISTER MAP FOR dsPIC33EPXXX(GP/MC)806 AND PIC24EPXXXGP806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISG | 0E60 | — | — | — | — | — | — | TRISG9 | TRISG8 | TRISG7 | TRISG6 | — | — | TRISG3 | TRISG2 | — | — | 03C0 |
| PORTG | 0E62 | — | — | — | — | — | — | RG9 | RG8 | RG7 | RG6 | — | — | RG3(1) | RG2(1) | — | — | xxxx |
| LATG | 0E64 | — | — | — | — | — | — | LATG9 | LATG8 | LATG7 | LATG6 | — | — | LATG3 | LATG2 | — | — | xxxx |
| ODCG | 0E66 | — | — | — | — | — | — | — | — | — | — | — | — | ODCG3 | ODCG2 | — | — | 0000 |
| CNENG | 0E68 | — | — | — | — | — | — | CNIEG9 | CNIEG8 | CNIEG7 | CNIEG6 | — | — | CNIEG3(1) | CNIEG2(1) | — | — | 0000 |
| CNPUG | 0E6A | — | — | — | — | — | — | CNPUG9 | CNPUG8 | CNPUG7 | CNPUG6 | — | — | CNPUG3 | CNPUG2 | — | — | 0000 |
| CNPDG | 0E6C | — | — | — | — | — | — | CNPDG9 | CNPDG8 | CNPDG7 | CNPDG6 | — | — | CNPDG3 | CNPDG2 | — | — | 0000 |
| ANSELG | 0E6E | — | — | — | — | — | — | ANSG9 | ANSG8 | ANSG7 | ANSG6 | — | — | — | — | — | — | 03C0 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
**Note 1:** If RG2 and RG3 are used as general purpose inputs, the $V_{USB3V3}$ pin must be connected to $V_{DD}$.

**TABLE 4-68: PORTG REGISTER MAP FOR dsPIC33EPXXXMU806 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISG | 0E60 | — | — | — | — | — | — | TRISG9 | TRISG8 | TRISG7 | TRISG6 | — | — | — | — | — | — | 03C0 |
| PORTG | 0E62 | — | — | — | — | — | — | RG9 | RG8 | RG7 | RG6 | — | — | RG3(1) | RG2(1) | — | — | xxxx |
| LATG | 0E64 | — | — | — | — | — | — | LATG9 | LATG8 | LATG7 | LATG6 | — | — | — | — | — | — | xxxx |
| ODCG | 0E66 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNENG | 0E68 | — | — | — | — | — | — | CNIEG9 | CNIEG8 | CNIEG7 | CNIEG6 | — | — | CNIEG3(1) | CNIEG2(1) | — | — | 0000 |
| CNPUG | 0E6A | — | — | — | — | — | — | CNPUG9 | CNPUG8 | CNPUG7 | CNPUG6 | — | — | — | — | — | — | 0000 |
| CNPDG | 0E6C | — | — | — | — | — | — | CNPDG9 | CNPDG8 | CNPDG7 | CNPDG6 | — | — | — | — | — | — | 0000 |
| ANSELG | 0E6E | — | — | — | — | — | — | ANSG9 | ANSG8 | ANSG7 | ANSG6 | — | — | — | — | — | — | 03C0 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
**Note 1:** If RG2 and RG3 are used as general purpose inputs, the $V_{USB3V3}$ pin must be connected to $V_{DD}$.

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**TABLE 4-69: PORTH REGISTER MAP FOR dsPIC33EPXXXMU814 AND PIC24EPXXXGU814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISH | 0E70 | TRISH15 | TRISH14 | TRISH13 | TRISH12 | TRISH11 | TRISH10 | TRISH9 | TRISH8 | TRISH7 | TRISH6 | TRISH5 | TRISH4 | TRISH3 | TRISH2 | TRISH1 | TRISH0 | FFFF |
| PORTH | 0E72 | RH15 | RH14 | RH13 | RH12 | RH11 | RH10 | RH9 | RH8 | RH7 | RH6 | RH5 | RH4 | RH3 | RH2 | RH1 | RH0 | xxxx |
| LATH | 0E74 | LATH15 | LATH14 | LATH13 | LATH12 | LATH11 | LATH10 | LATH9 | LATH8 | LATH7 | LATH6 | LATH5 | LATH4 | LATH3 | LATH2 | LATH1 | LATH0 | xxxx |
| ODCH | 0E76 | ODCH15 | ODCH14 | ODCH13 | ODCH12 | ODCH11 | ODCH10 | ODCH9 | ODCH8 | ODCH7 | ODCH6 | ODCH5 | ODCH4 | ODCH3 | ODCH2 | ODCH1 | ODCH0 | 0000 |
| CNENH | 0E78 | CNIEH15 | CNIEH14 | CNIEH13 | CNIEH12 | CNIEH11 | CNIEH10 | CNIEH9 | CNIEH8 | CNIEH7 | CNIEH6 | CNIEH5 | CNIEH4 | CNIEH3 | CNIEH2 | CNIEH1 | CNIEH0 | 0000 |
| CNPUH | 0E7A | CNPUH15 | CNPUH14 | CNPUH13 | CNPUH12 | CNPUH11 | CNPUH10 | CNPUH9 | CNPUH8 | CNPUH7 | CNPUH6 | CNPUH5 | CNPUH4 | CNPUH3 | CNPUH2 | CNPUH1 | CNPUH0 | 0000 |
| CNPDH | 0E7C | CNPDH15 | CNPDH14 | CNPDH13 | CNPDH12 | CNPDH11 | CNPDH10 | CNPDH9 | CNPDH8 | CNPDH7 | CNPDH6 | CNPDH5 | CNPDH4 | CNPDH3 | CNPDH2 | CNPDH1 | CNPDH0 | 0000 |
| ANSELH | 0E7E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-70: PORTJ REGISTER MAP FOR dsPIC33EPXXXMU814 AND PIC24EPXXXGU814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISJ | 0E80 | TRISJ15 | TRISJ14 | TRISJ13 | TRISJ12 | TRISJ11 | TRISJ10 | TRISJ9 | TRISJ8 | TRISJ7 | TRISJ6 | TRISJ5 | TRISJ4 | TRISJ3 | TRISJ2 | TRISJ1 | TRISJ0 | FFFF |
| PORTJ | 0E82 | RJ15 | RJ14 | RJ13 | RJ12 | RJ12 | RJ10 | RJ9 | RJ8 | RJ7 | RJ6 | RJ5 | RJ4 | RJ3 | RJ2 | RJ1 | RJ0 | xxxx |
| LATJ | 0E84 | LATJ15 | LATJ14 | LATJ13 | LATJ12 | LATJ11 | LATJ10 | LATJ9 | LATJ8 | LATJ7 | LATJ6 | LATJ5 | LATJ4 | LATJ3 | LATJ2 | LATJ1 | LATJ0 | xxxx |
| ODCJ | 0E86 | ODCJ15 | ODCJ14 | ODCJ13 | ODCJ12 | ODCJ11 | ODCJ10 | ODCJ9 | ODCJ8 | ODCJ7 | ODCJ6 | ODCJ5 | ODCJ4 | ODCJ3 | ODCJ2 | ODCJ1 | ODCJ0 | 0000 |
| CNENJ | 0E88 | CNIEJ15 | CNIEJ14 | CNIEJ13 | CNIEJ12 | CNIEJ11 | CNIEJ10 | CNIEJ9 | CNIEJ8 | CNIEJ7 | CNIEJ6 | CNIEJ5 | CNIEJ4 | CNIEJ3 | CNIEJ2 | CNIEJ1 | CNIEJ0 | 0000 |
| CNPUJ | 0E8A | CNPUJ15 | CNPUJ14 | CNPUJ13 | CNPUJ12 | CNPUJ11 | CNPUJ10 | CNPUJ9 | CNPUJ8 | CNPUJ7 | CNPUJ6 | CNPUJ5 | CNPUJ4 | CNPUJ3 | CNPUJ2 | CNPUJ1 | CNPUJ0 | 0000 |
| CNPDJ | 0E8C | CNPDJ15 | CNPDJ14 | CNPDJ13 | CNPDJ12 | CNPDJ11 | CNPDJ10 | CNPDJ9 | CNPDJ8 | CNPDJ7 | CNPDJ6 | CNPDJ5 | CNPDJ4 | CNPDJ3 | CNPDJ2 | CNPDJ1 | CNPDJ0 | 0000 |
| ANSELJ | 0E8E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-71: PORTK REGISTER MAP FOR dsPIC33EPXXXMU814 AND PIC24EPXXXGU814 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISK | 0E90 | TRISK15 | TRISK14 | TRISK13 | TRISK12 | TRISK11 | — | — | — | — | — | — | — | — | — | TRISK1 | TRISK0 | F803 |
| PORTK | 0E92 | RK15 | RK14 | RK13 | RK12 | RK11 | — | — | — | — | — | — | — | — | — | RK1 | RK0 | xxxx |
| LATK | 0E94 | LATK15 | LATK14 | LATK13 | LATK12 | LATK11 | — | — | — | — | — | — | — | — | — | LATK1 | LATK0 | xxxx |
| ODCK | 0E96 | ODCK15 | ODCK14 | ODCK13 | ODCK12 | ODCK11 | — | — | — | — | — | — | — | — | — | ODCK1 | ODCK0 | 0000 |
| CNENK | 0E98 | CNIEK15 | CNIEK14 | CNIEK13 | CNIEK12 | CNIEK11 | — | — | — | — | — | — | — | — | — | CNIEK1 | CNIEK0 | 0000 |
| CNPUK | 0E9A | CNPUK15 | CNPUK14 | CNPUK13 | CNPUK12 | CNPUK11 | — | — | — | — | — | — | — | — | — | CNPUK1 | CNPUK0 | 0000 |
| CNPDK | 0E9C | CNPDK15 | CNPDK14 | CNPDK13 | CNPDK12 | CNPDK11 | — | — | — | — | — | — | — | — | — | CNPDK1 | CNPDK0 | 0000 |
| ANSELK | 0E9E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-72: PAD CONFIGURATION REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PADCFG1 | 0EFE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RTSECSEL | PMPTTL | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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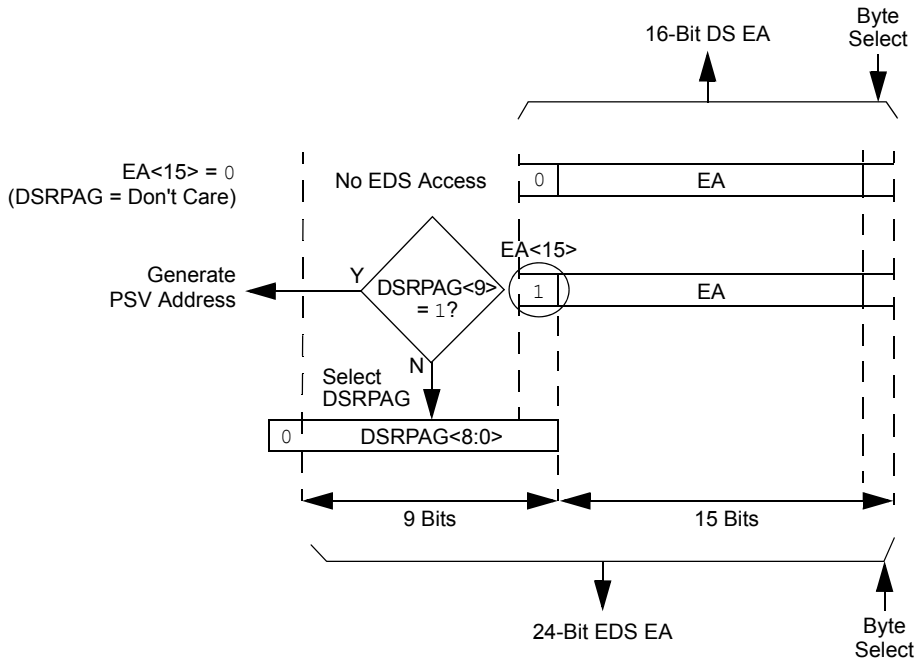
### 4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 architecture extends the available data space through a paging scheme, which allows the available data space to be accessed using MOV instructions in a linear fashion for pre- and post-modified Effective Addresses (EA). The upper half of Base Data Space address is used in conjunction with the Data Space Page registers, the 10-Bit Read Page register (DSRPAG) or the 9-Bit Write Page register (DSWPAG), to form an Extended Data Space (EDS) address or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

Construction of the EDS address is shown in Figure 4-1. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, DSRPAG<8:0> is concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when the base address bit, EA<15> = 1, DSWPAG<8:0> is concatenated onto EA<14:0> to form the 24-bit EDS write address.

**EXAMPLE 4-1: EXTENDED DATA SPACE (EDS) READ ADDRESS GENERATION**




**Note:** DS read access when DSRPAG = 0x000 will force an address error trap.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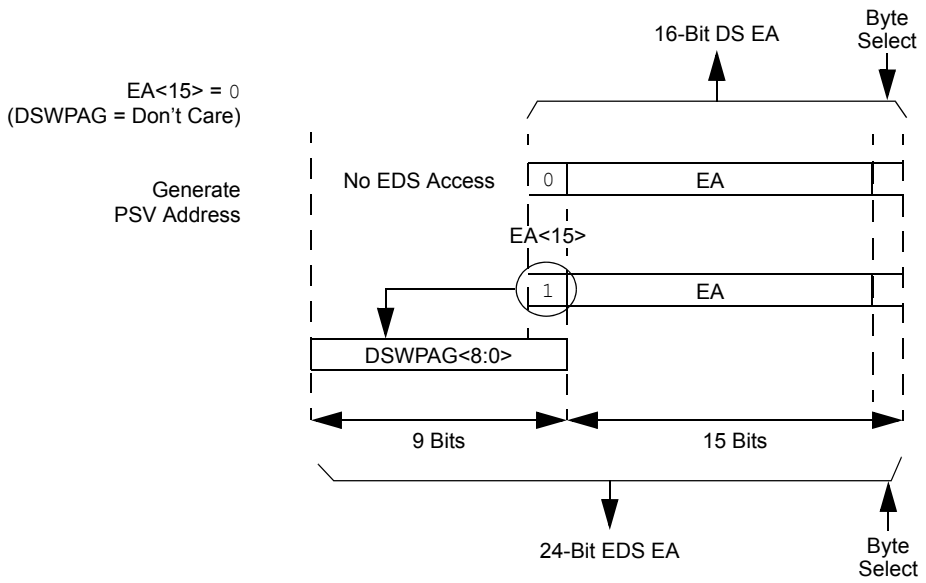
**EXAMPLE 4-2: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION**

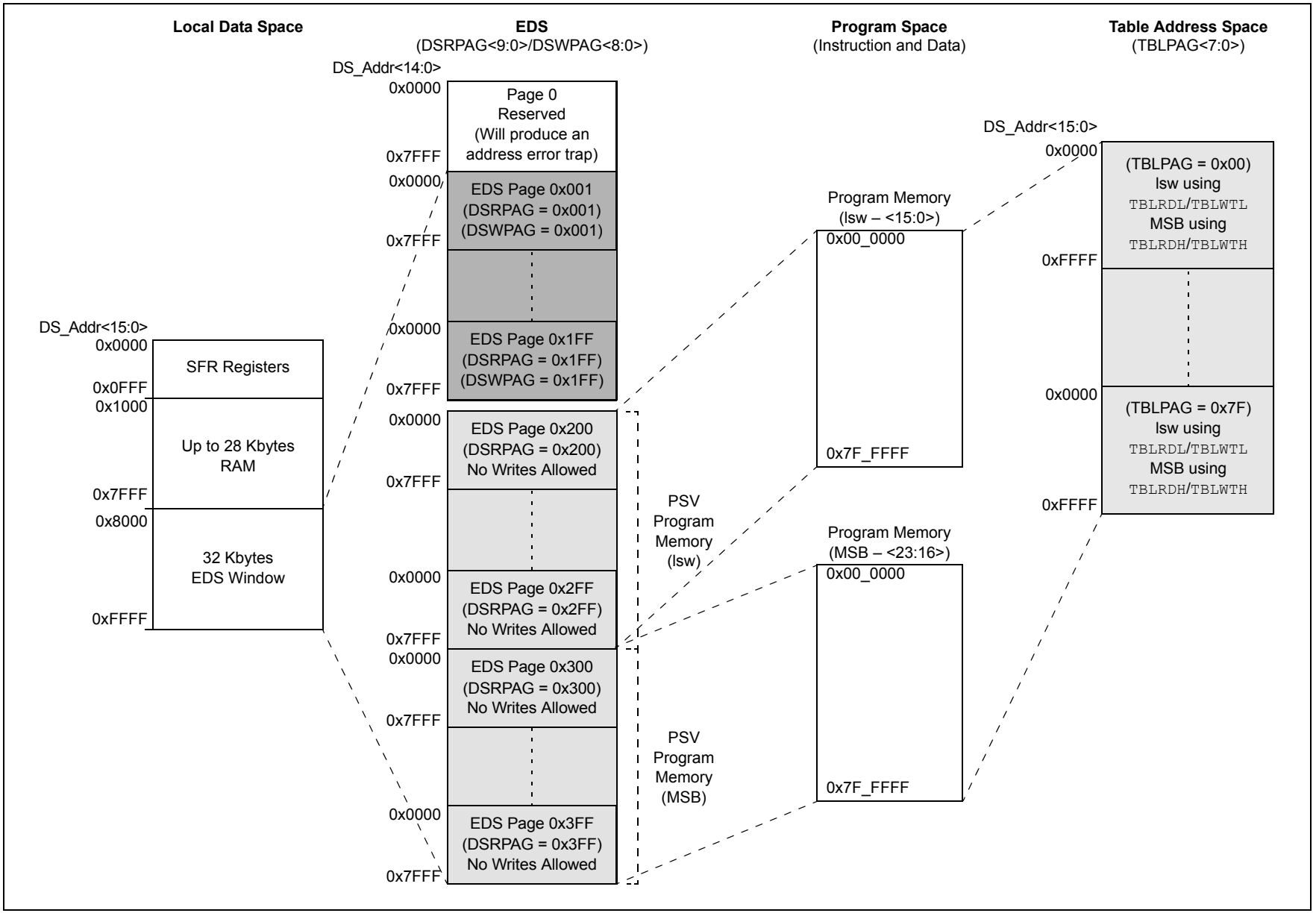



**Note:** DS read access when DSRPAG = 0x000 will force an address error trap.

The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers DSxPAG, in combination with the upper half of data space address can provide up to 16 Mbytes of additional address space in the EDS and 12 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The Program Space (PS) can be accessed with DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS, only. The data space and EDS can be read from and written to using DSRPAG and DSWPAG, respectively.

**EXAMPLE 4-3: PAGED DATA MEMORY SPACE**



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Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read and configuring the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages, by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address, prior to modification, addresses an EDS or PSV page.
- The EA calculation uses Pre- or Post-Modified Register Indirect Addressing. However, this does not include Register Offset Addressing.

In general, when an overflow is detected, the DSxPAG register is incremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-73 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

**TABLE 4-73: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS and PSV SPACE BOUNDARIES(2,3,4)**

| O/U, R/W | Operation | Before | | | After | | |
|---|---|---|---|---|---|---|---|
| | | DSxPAG | DS EA<15> | Page Description | DSxPAG | DS EA<15> | Page Description |
| O, Read | [++Wn] or [Wn++] | DSRPAG = 0x1FF | 1 | EDS: Last page | DSRPAG = 0x1FF | 0 | See **Note 1** |
| O, Read | | DSRPAG = 0x2FF | 1 | PSV: Last lsw page | DSRPAG = 0x300 | 1 | PSV: First MSB page |
| O, Read | | DSRPAG = 0x3FF | 1 | PSV: Last MSB page | DSRPAG = 0x3FF | 0 | See **Note 1** |
| O, Write | | DSWPAG = 0x1FF | 1 | EDS: Last page | DSWPAG = 0x1FF | 0 | See **Note 1** |
| U, Read | [--Wn] or [Wn--] | DSRPAG = 0x001 | 1 | EDS page | DSRPAG = 0x001 | 0 | See **Note 1** |
| U, Read | | DSRPAG = 0x200 | 1 | PSV: First lsw page | DSRPAG = 0x200 | 0 | See **Note 1** |
| U, Read | | DSRPAG = 0x300 | 1 | PSV: First MSB page | DSRPAG = 0x2FF | 1 | PSV: Last lsw page |

**Legend:** O = Overflow, U = Underflow, R = Read, W = Write

**Note 1:** Register Indirect Addressing now addresses a location in the Base Data Space (0x0000-0x8000).

**2:** An EDS access with DSxPAG = 0x000 will generate an address error trap.

**3:** Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.

**4:** Pseudo-Linear Addressing is not supported for large offsets.

### 4.4.2 EXTENDED X DATA SPACE

The lower half of the base address space range, between 0x0000 and 0x7FFF, is always accessible regardless of the contents of the Data Space Page registers. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes (0x8000 to 0xFFFF) of Base Data Space, in combination with DSRPAG = 0x00 or DSWPAG = 0x00. Consequently, DSRPAG and DSWPAG are initialized to 0x001 at Reset.

**Note 1:** DSxPAG should not be used to access Page 0. An EDS access with DSxPAG set to 0x000 will generate an address error trap.

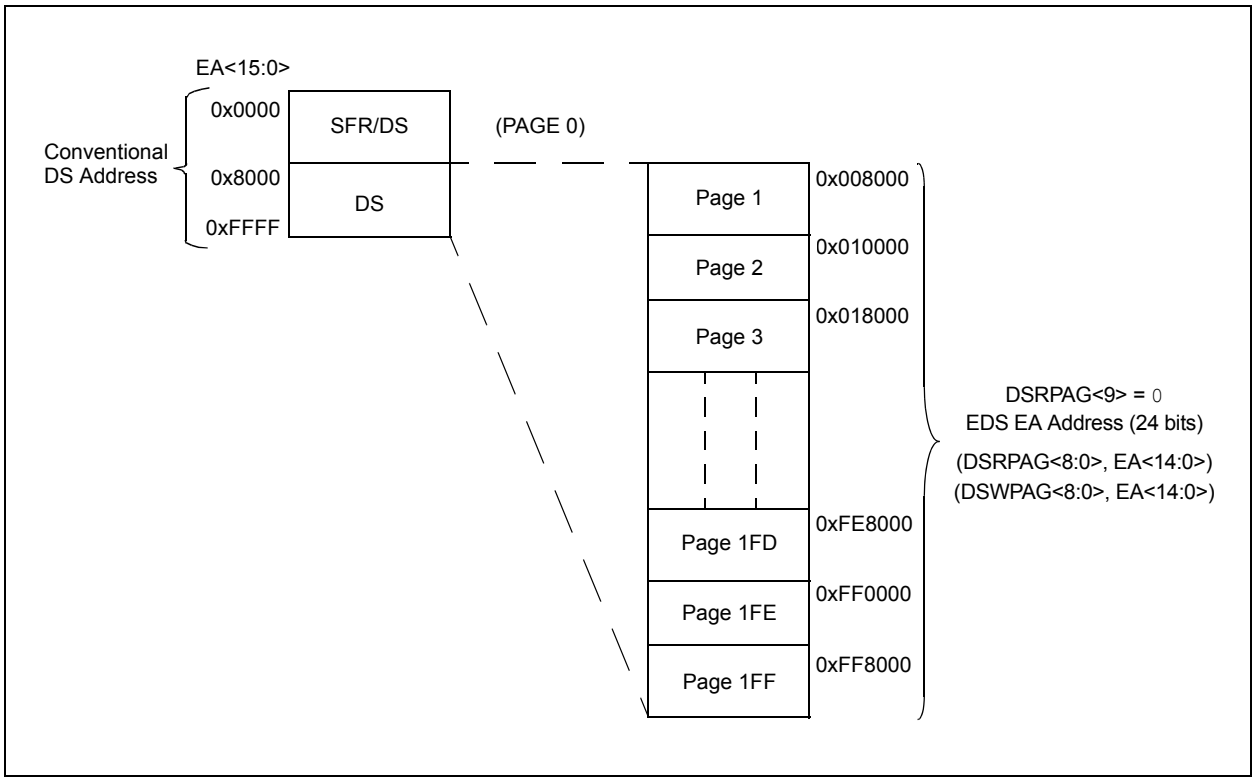
**2:** Clearing DSxPAG in software has no effect.

The remaining pages including both EDS and PSV pages are only accessible using the DSRPAG or DSWPAG registers in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA<15> = 1.

For example, when DSRPAG = 0x01 or DSWPAG = 0x01, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF, of the data space will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x02 or DSWPAG = 0x02, accesses to the upper 32 Kbytes of the data space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-7.

For more information of the PSV page access using Data Space Page registers refer to **Section 4.5 "Program Space Visibility from Data Space"** in **Section 4. "Program Memory"** (DS70613) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

**FIGURE 4-7: EDS MEMORY MAP**





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### 4.4.3 EDS ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA, the USB module and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus masters (USB and DMA Controllers) are allocated to M2 and M3, respectively (M1 is reserved and cannot be used). The user application may raise or lower the priority of the masters to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-74.

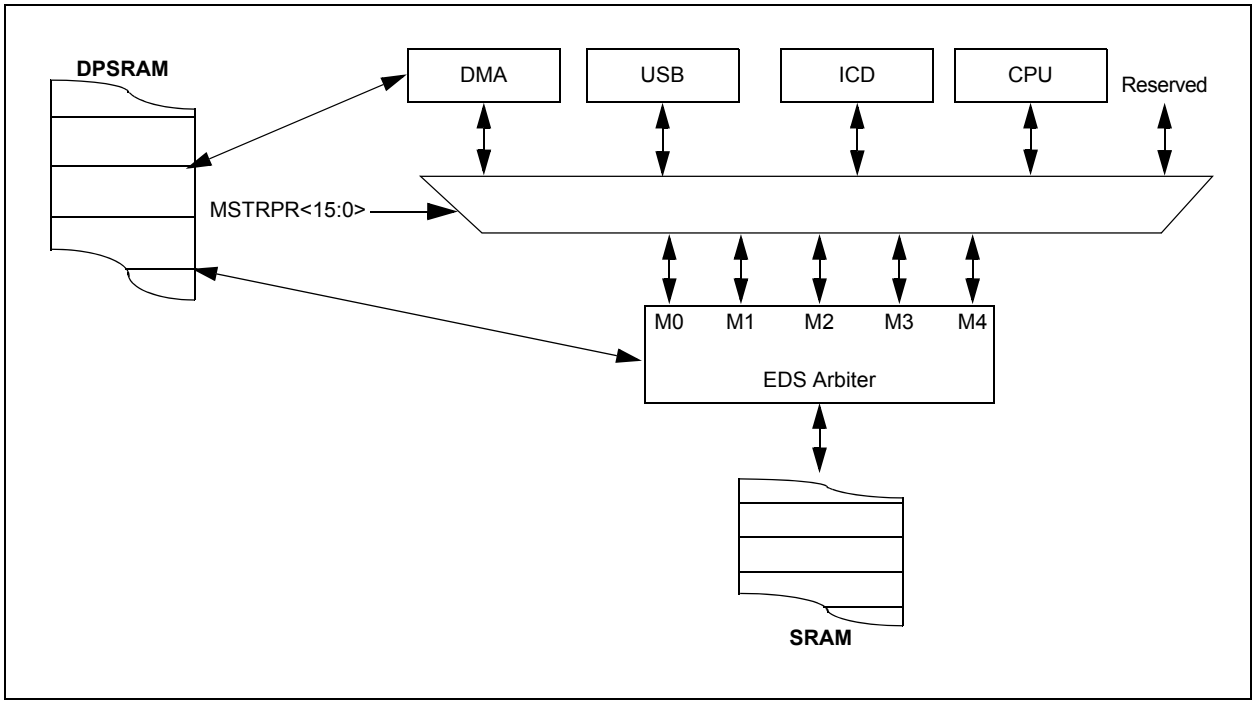
This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization, or dynamically in response to real-time events.

**TABLE 4-74: EDS BUS ARBITER PRIORITY**

| Priority | MSTRPR<15:0> Bit Setting(1) | | | |
|---|---|---|---|---|
| | 0x0000 | 0x0008 | 0x0020 | 0x0028 |
| M0 (highest) | CPU | USB | DMA | USB |
| M1 | Reserved | CPU | CPU | DMA |
| M2 | USB | Reserved | Reserved | CPU |
| M3 | DMA | DMA | USB | Reserved |
| M4 (lowest) | ICD | ICD | ICD | ICD |

**Note 1:** All other values of MSTRPR<15:0> are reserved.

**FIGURE 4-8: EDS ARBITER ARCHITECTURE**



### 4.4.4 SOFTWARE STACK

The W15 register serves as a dedicated software Stack Pointer (SP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating of the Stack Pointer (for example, creating stack frames).

| | |
|---|---|
| **Note:** | To protect against misaligned stack accesses, W15<0> is fixed to '0' by the hardware. |

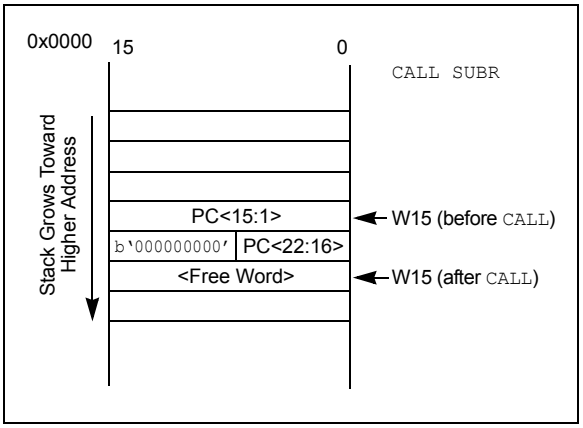
W15 is initialized to 0x1000 during all Resets. This address ensures that the SP points to valid RAM in all dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices and permits stack availability for non-maskable trap exceptions. These can occur before the SP is initialized by the user software. You can reprogram the SP during initialization to any location within data space.

The Stack Pointer always points to the first available free word and fills the software stack working from lower toward higher addresses. Figure 4-9 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> is pushed onto the first available stack word, then PC<22:16> is pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-9. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

| | |
|---|---|
| **Note 1:** | For main system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging and is therefore, restricted to the address range of 0x0000 to 0xFFFF. The same applies to W14 when used as a Stack Frame Pointer (SFA = 1). |
| **2:** | As the stack can be placed in and across X, Y and DMA RAM spaces, care must be exercised regarding its use, particularly with regard to local automatic variables in a C development environment. |

**FIGURE 4-9: CALL STACK FRAME**




## 4.5 Instruction Addressing Modes

The addressing modes, shown in Table 4-75, form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

### 4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire data space.

### 4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register, fetched from data memory, or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-bit or 10-bit Literal

| | |
|---|---|
| **Note:** | Not all instructions support all of the addressing modes given above. Individual instructions can support different subsets of these addressing modes. |


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**TABLE 4-75: FUNDAMENTAL ADDRESSING MODES SUPPORTED**

| Addressing Mode | Description |
|---|---|
| File Register Direct | The address of the file register is specified explicitly. |
| Register Direct | The contents of a register are accessed directly. |
| Register Indirect | The contents of Wn forms the Effective Address (EA). |
| Register Indirect Post-Modified | The contents of Wn forms the EA. Wn is post-modified (incremented or decremented) by a constant value. |
| Register Indirect Pre-Modified | Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA. |
| Register Indirect with Register Offset (Register Indexed) | The sum of Wn and Wb forms the EA. |
| Register Indirect with Literal Offset | The sum of Wn and a literal forms the EA. |

### 4.5.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions (dsPIC33EPXXXMU806/810/814 and PIC24EPXXXGU810/814) and the DSP accumulator class of instructions (dsPIC33EPXXXMU806/810/814 only) provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

**Note:** For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

**Note:** Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

### 4.5.4 MAC INSTRUCTIONS (dsPIC33EPXXXMU806/810/814 DEVICES ONLY)

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must, therefore, be valid addresses within X data space for W8 and W9 and Y data space for W10 and W11.

**Note:** Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

### 4.5.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as NOP, do not have any operands.

## 4.6 Modulo Addressing (dsPIC33EPXXXMU806/810/814 Devices Only)

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y data spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction as there are certain restrictions on the buffer start address (for incrementing buffers), or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

### 4.6.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

| **Note:** | Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear). |
|---|---|

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

### 4.6.2 W ADDRESS REGISTER SELECTION

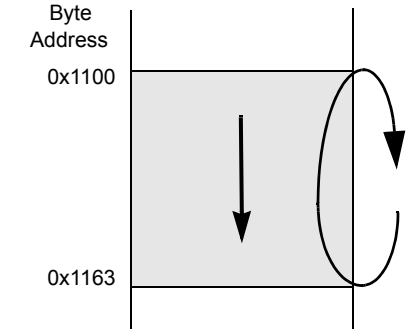
The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = `1111`, X RAGU and X WAGU Modulo Addressing is disabled.
- If YWM = `1111`, Y AGU Modulo Addressing is disabled.

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X data space when XWM is set to any value other than '`1111`' and the XMODEN bit is set at MODCON<15>.

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y data space when YWM is set to any value other than '`1111`' and the YMODEN bit is set at MODCON<14>.

**FIGURE 4-10: MODULO ADDRESSING OPERATION EXAMPLE**




```
MOV     #0x1100, W0
MOV     W0, XMODSRT     ;set modulo start address
MOV     #0x1163, W0
MOV     W0, MODEND      ;set modulo end address
MOV     #0x8001, W0
MOV     W0, MODCON      ;enable W1, X AGU for modulo

MOV     #0x0000, W0     ;W0 holds buffer fill value

MOV     #0x1110, W1     ;point W1 to buffer

DO      AGAIN, #0x31    ;fill the 50 buffer locations
MOV     W0, [W1++]      ;fill the next location
AGAIN:  INC W0, W0      ;increment the fill value
```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### 4.6.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

| | |
|---|---|
| **Note:** | The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed but the contents of the register remain unchanged. |

## 4.7 Bit-Reversed Addressing (dsPIC33EPXXXMU806/810/814 Devices Only)

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

### 4.7.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled in any of these situations:

- BWMx bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is $M = 2^N$ bytes, the last 'N' bits of the data buffer start address must be zeros.

XB<14:0> is the Bit-Reversed Address modifier, or 'pivot point,' which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

| | |
|---|---|
| **Note:** | All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses. |

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

| | |
|---|---|
| **Note:** | Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled. |

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

**FIGURE 4-11: BIT-REVERSED ADDRESS EXAMPLE**

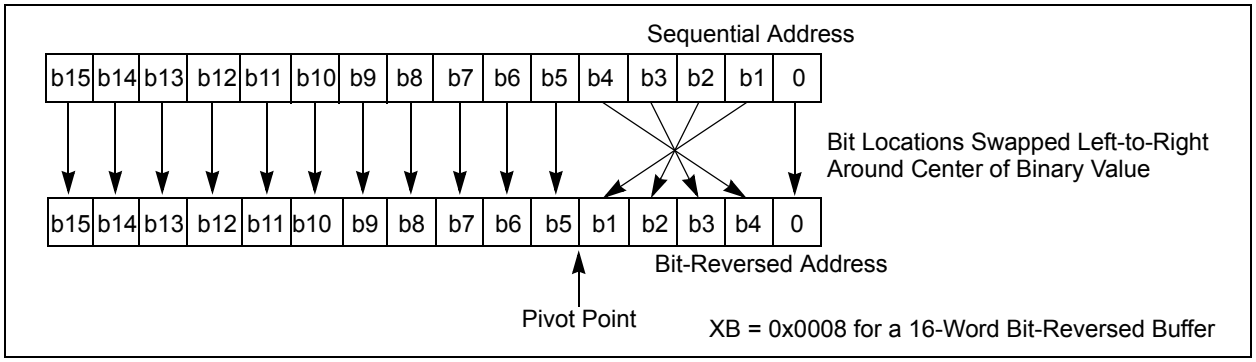


**TABLE 4-76: BIT-REVERSED ADDRESS SEQUENCE (16-ENTRY)**

| Normal Address | | | | | Bit-Reversed Address | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **A3** | **A2** | **A1** | **A0** | **Decimal** | **A3** | **A2** | **A1** | **A0** | **Decimal** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 8 |
| 0 | 0 | 1 | 0 | 2 | 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 1 | 1 | 3 | 1 | 1 | 0 | 0 | 12 |
| 0 | 1 | 0 | 0 | 4 | 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | 0 | 10 |
| 0 | 1 | 1 | 0 | 6 | 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 | 1 | 1 | 1 | 0 | 14 |
| 1 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 9 | 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 | 0 | 1 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 11 | 1 | 1 | 0 | 1 | 13 |
| 1 | 1 | 0 | 0 | 12 | 0 | 0 | 1 | 1 | 3 |
| 1 | 1 | 0 | 1 | 13 | 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 1 | 0 | 14 | 0 | 1 | 1 | 1 | 7 |
| 1 | 1 | 1 | 1 | 15 | 1 | 1 | 1 | 1 | 15 |


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## 4.8 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 architecture uses a 24-bit wide Program Space and a 16-bit wide data space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 architecture provides two methods by which Program Space can be accessed during operation:

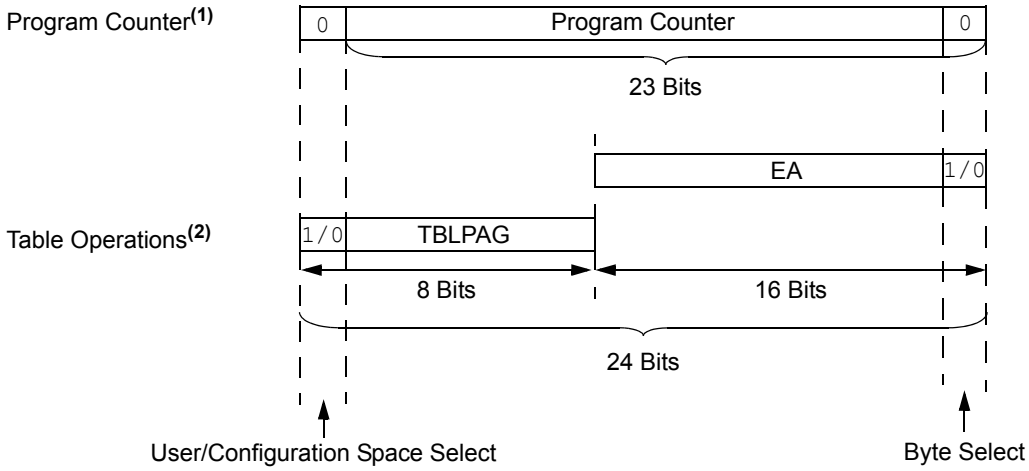
- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the data space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

**TABLE 4-77: PROGRAM SPACE ADDRESS CONSTRUCTION**

| Access Type | Access Space | Program Space Address | | | | |
|---|---|---|---|---|---|---|
| | | <23> | <22:16> | <15> | <14:1> | <0> |
| Instruction Access (Code Execution) | User | 0 | PC<22:1> | | | 0 |
| | | 0xx xxxx xxxx xxxx xxxx xxx0 | | | | |
| TBLRD/TBLWT (Byte/Word Read/Write) | User | TBLPAG<7:0> | | Data EA<15:0> | | |
| | | 0xxx xxxx | | xxxx xxxx xxxx xxxx | | |
| | Configuration | TBLPAG<7:0> | | Data EA<15:0> | | |
| | | 1xxx xxxx | | xxxx xxxx xxxx xxxx | | |

**FIGURE 4-12: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION**




**Note 1:** The Least Significant bit (LSb) of Program Space addresses is always fixed as '0' to maintain word alignment of data in the program and data spaces.

**2:** Table operations are not required to be word-aligned. Table read operations are permitted in the configuration memory space.

### 4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through data space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

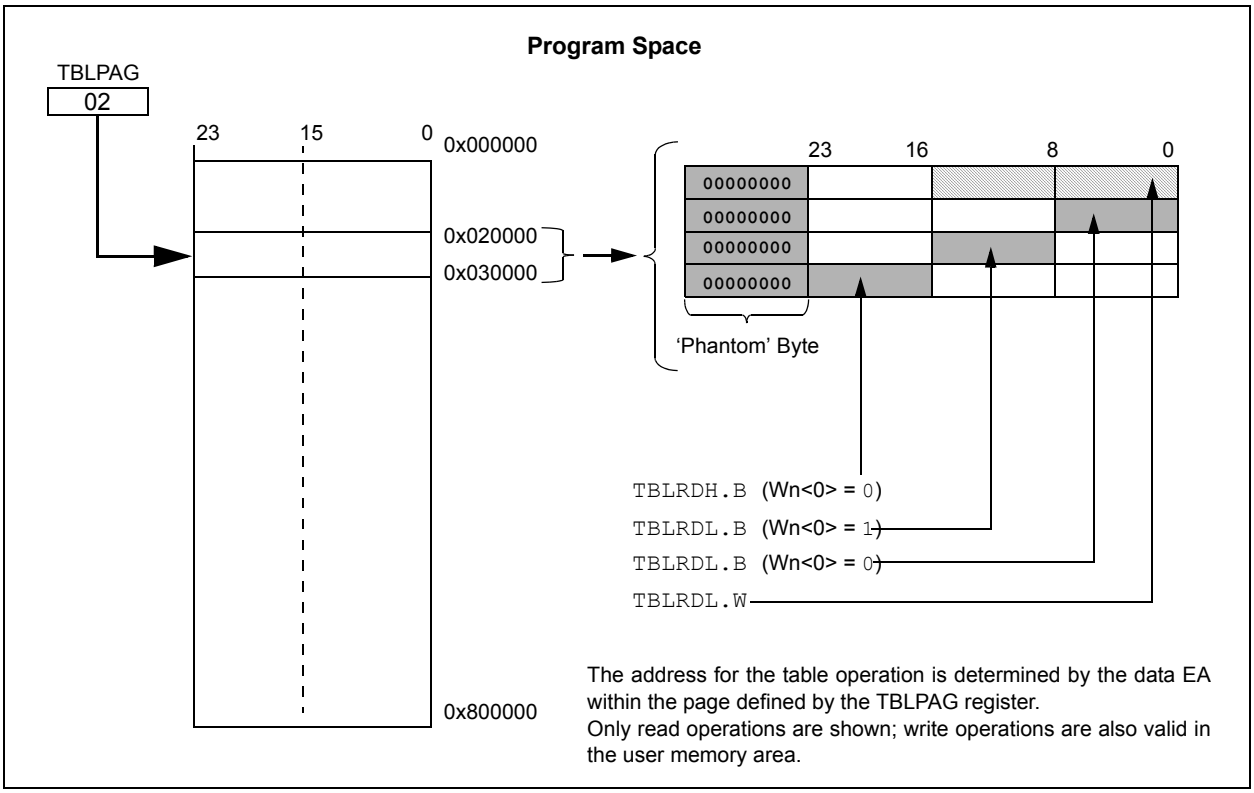
Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
  - In Word mode, this instruction maps the lower word of the Program Space location (P<15:0>) to a data address (D<15:0>).
  - In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.
- TBLRDH (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. The 'phantom' byte (D<15:8>), is always '0'.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to D<7:0> of the data address, in the TBLRDL instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

**FIGURE 4-13: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS**




The address for the table operation is determined by the data EA within the page defined by the TBLPAG register.
Only read operations are shown; write operations are also valid in the user memory area.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# 5.0 FLASH PROGRAM MEMORY

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Programming"** (DS70609) of the *"dsPIC33E/PIC24E Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows a dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (VSS) and Master Clear ($\overline{MCLR}$). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (table read) and TBLWT (table write) instructions. With RTSP, the user application can write program memory data either in blocks or 'rows' of 128 instructions (384 bytes) at a time or a single program memory word, and erase program memory in blocks or 'pages' of 1024 instructions (3072 bytes) at a time.

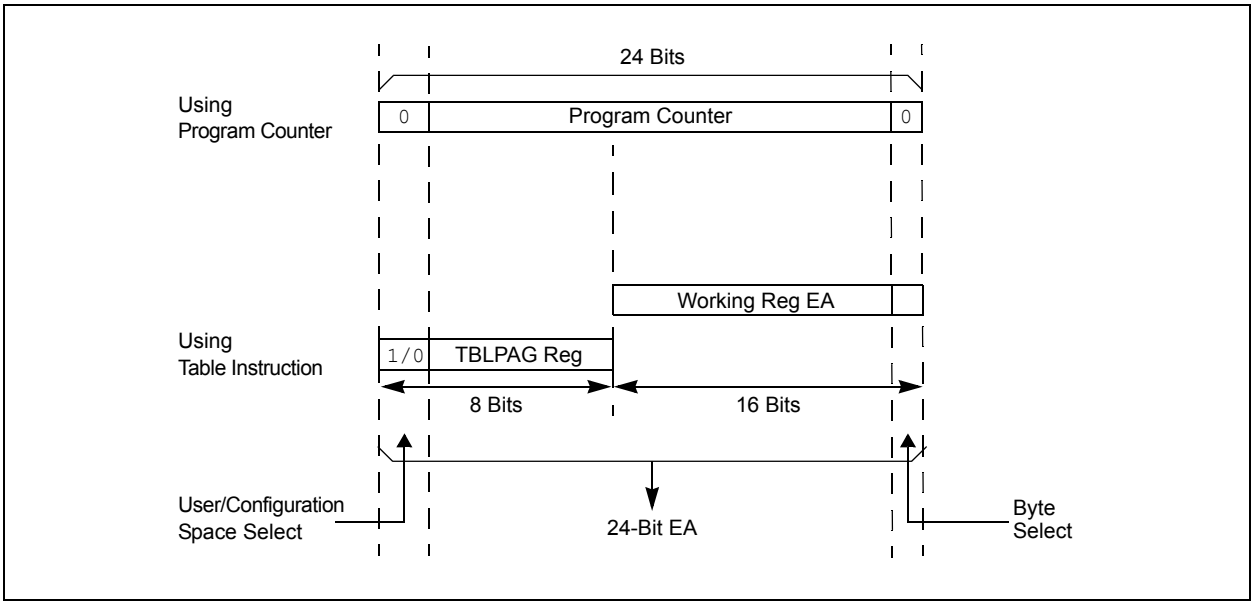
## 5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the table read and table write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

**FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS**



## 5.2 RTSP Operation

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 Flash program memory array is organized into rows of 128 instructions or 384 bytes. RTSP allows the user application to erase a page of memory, which consists of eight rows (1024 instructions) at a time, and to program one row or one word at a time. Table 32-12 lists typical erase and programming times. The 8-row erase pages and single row write rows are edge-aligned from the beginning of program memory, on boundaries of 3072 bytes and 384 bytes, respectively.

The program memory implements holding buffers, which are located in the write latch area, that can contain 128 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the buffers sequentially. The instruction words loaded must always be from a group of 64 boundary.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of `TBLWT` instructions to load the buffers. Programming is performed by setting the control bits in the NVMCON register. A total of 128 `TBLWTL` and `TBLWTH` instructions are required to load the instructions.

All of the table write operations are single-word writes (two instruction cycles) because only the buffers are written. A programming cycle is required for programming each row. For more information on erasing and programming Flash memory, refer to **Section 5. "Flash Programming"** (DS70609) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

## 5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

The programming time depends on the FRC accuracy (see Table 32-19) and the value of the FRC Oscillator Tuning register (see Register 9-4). Use the following formula to calculate the minimum and maximum values for the Row Write Time, Page Erase Time and Word Write Cycle Time parameters (see Table 32-12).

**EQUATION 5-1: PROGRAMMING TIME**

$$\frac{T}{7.37\ MHz \times (FRC\ Accuracy)\% \times (FRC\ Tuning)\%}$$

For example, if the device is operating at +125°C, the FRC accuracy will be ±5%. If the TUN<5:0> bits (see Register 9-4) are set to `'b111111`, the minimum row write time is equal to Equation 5-2.

**EQUATION 5-2: MINIMUM ROW WRITE TIME**

$$T_{RW} = \frac{11064\ Cycles}{7.37\ MHz \times (1 + 0.05) \times (1 - 0.00375)} = 1.435 ms$$

The maximum row write time is equal to Equation 5-3.

**EQUATION 5-3: MAXIMUM ROW WRITE TIME**

$$T_{RW} = \frac{11064\ Cycles}{7.37\ MHz \times (1 - 0.05) \times (1 - 0.00375)} = 1.586 ms$$

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.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## 5.4 Flash Program Memory Resources

Many useful resources related to Flash program memory are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 5.4.1 KEY RESOURCES

- **Section 5. "Flash Programming"** (DS70609) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 5.5 Control Registers

Four SFRs are used to read and write the program Flash memory: NVMCON, NVMKEY, NVMADRU and NVMADR.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected row or word for programming operations, or the selected page for erase operations.

The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

**REGISTER 5-1: NVMCON: NON-VOLATILE MEMORY (NVM) CONTROL REGISTER**

| R/SO-0(1) | R/W-0(1) | R/W-0(1) | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| WR | WREN | WRERR | NVMSIDL(2) | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R/W-0(1) | R/W-0(1) | R/W-0(1) | R/W-0(1) |
|---|---|---|---|---|---|---|---|
| — | — | — | — | NVMOP<3:0>(3,4) | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | SO = Settable Only bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **WR:** Write Control bit(1)
- 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once operation is complete
- 0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit(1)
- 1 = Enables Flash program/erase operations
- 0 = Inhibits Flash program/erase operations

bit 13 **WRERR:** Write Sequence Error Flag bit(1)
- 1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
- 0 = The program or erase operation completed normally

bit 12 **NVMSIDL:** NVM Stop-in-Idle Control bit(2)
- 1 = Flash voltage regulator goes into Stand-by mode during Idle mode
- 0 = Flash voltage regulator is active during Idle mode

bit 11-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation Select bits(1,3,4)
- 1111 = Reserved
- 1110 = Reserved
- 1101 = Bulk erase primary program Flash memory
- 1100 = Reserved
- 1011 = Reserved
- 1010 = Bulk erase auxiliary program Flash memory
- 0011 = Memory page erase operation
- 0010 = Memory row program operation
- 0001 = Memory word program operation(5)
- 0000 = Program a single Configuration register byte

**Note 1:** These bits can only be reset on a POR.

**2:** If this bit is set, upon exiting Idle mode, there is a delay (TVREG) before Flash memory becomes operational.

**3:** All other combinations of NVMOP<3:0> are unimplemented.

**4:** Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.

**5:** Two adjacent words are programmed during execution of this operation.


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**REGISTER 5-2: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADRU<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **NVMADRU<7:0>:** Nonvolatile Memory Upper Write Address bits

Selects the upper 8 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

**REGISTER 5-3: NVMADR: NONVOLATILE MEMORY ADDRESS REGISTER**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Write Address bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

**REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
|---|---|---|---|---|---|---|---|
| NVMKEY<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **NVMKEY<7:0>:** Key Register (write-only) bits

**NOTES:**


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## 6.0 RESETS

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Reset"** (DS70602) of the *"dsPIC33E/PIC24E Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{SYSRST}$. The following is a list of device Reset sources:

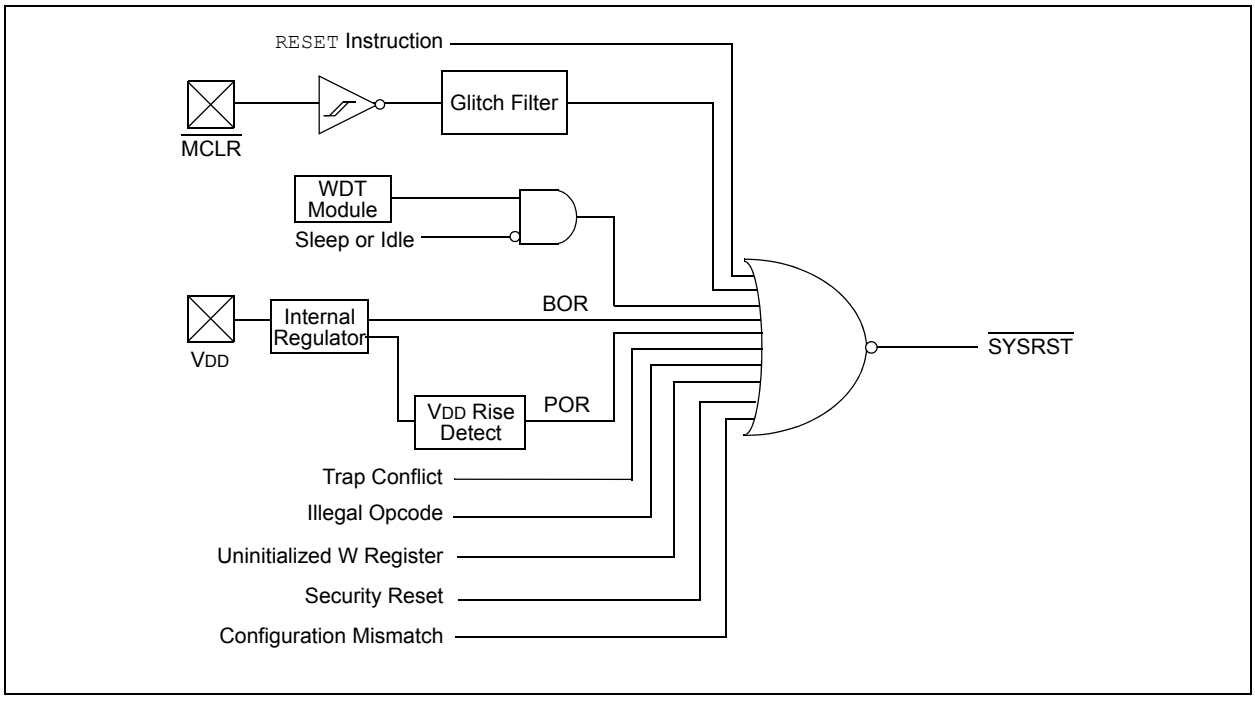
- POR: Power-on Reset
- BOR: Brown-out Reset
- $\overline{MCLR}$: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
  - Illegal Opcode Reset
  - Uninitialized W Register Reset
  - Security Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the $\overline{SYSRST}$ signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

**Note:** Refer to the specific peripheral section or **Section 4.0 "Memory Organization"** of this manual for register Reset states.

**FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM**



## 6.1 Resets Resources

Many useful resources related to Resets are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 6.1.1 KEY RESOURCES

- **Section 8. "Reset"** (DS70602) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 6.2 RCON Control Register

All types of device Resets set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits, except for the POR and BOR bits (RCON<1:0>), that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

| | |
|---|---|
| **Note:** | The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful. |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**REGISTER 6-1: RCON: RESET CONTROL REGISTER(1)**

| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TRAPR | IOPUWR | — | — | VREGSF | — | CM | VREGS |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| EXTR | SWR | SWDTEN(2) | WDTO | SLEEP | IDLE | BOR | POR |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or uninitialized W Reset has not occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **VREGSF:** Flash Voltage Regulator Standby During Sleep bit
1 = Flash voltage regulator is active during Sleep
0 = Flash voltage regulator goes into Standby mode during Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Mismatch Flag bit
1 = A Configuration Mismatch Reset has occurred.
0 = A Configuration Mismatch Reset has NOT occurred

bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(2)
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

**Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

**REGISTER 6-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)**

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

**Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.


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# 7.0 INTERRUPT CONTROLLER

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. "Interrupts"** (DS70600) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Fixed interrupt entry and return latencies

## 7.1 Interrupt Vector Table

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 Interrupt Vector Table (IVT), shown in Figure 7-1, resides in the General Segment of program memory, starting at location, 0x000004, and is used when executing code from the General Segment. The IVT contains seven non-maskable trap vectors and up to 114 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with vector 0 takes priority over interrupts at any other vector address.

**Note:** Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a `RESET` instruction.

## 7.2 Auxiliary Interrupt Vector

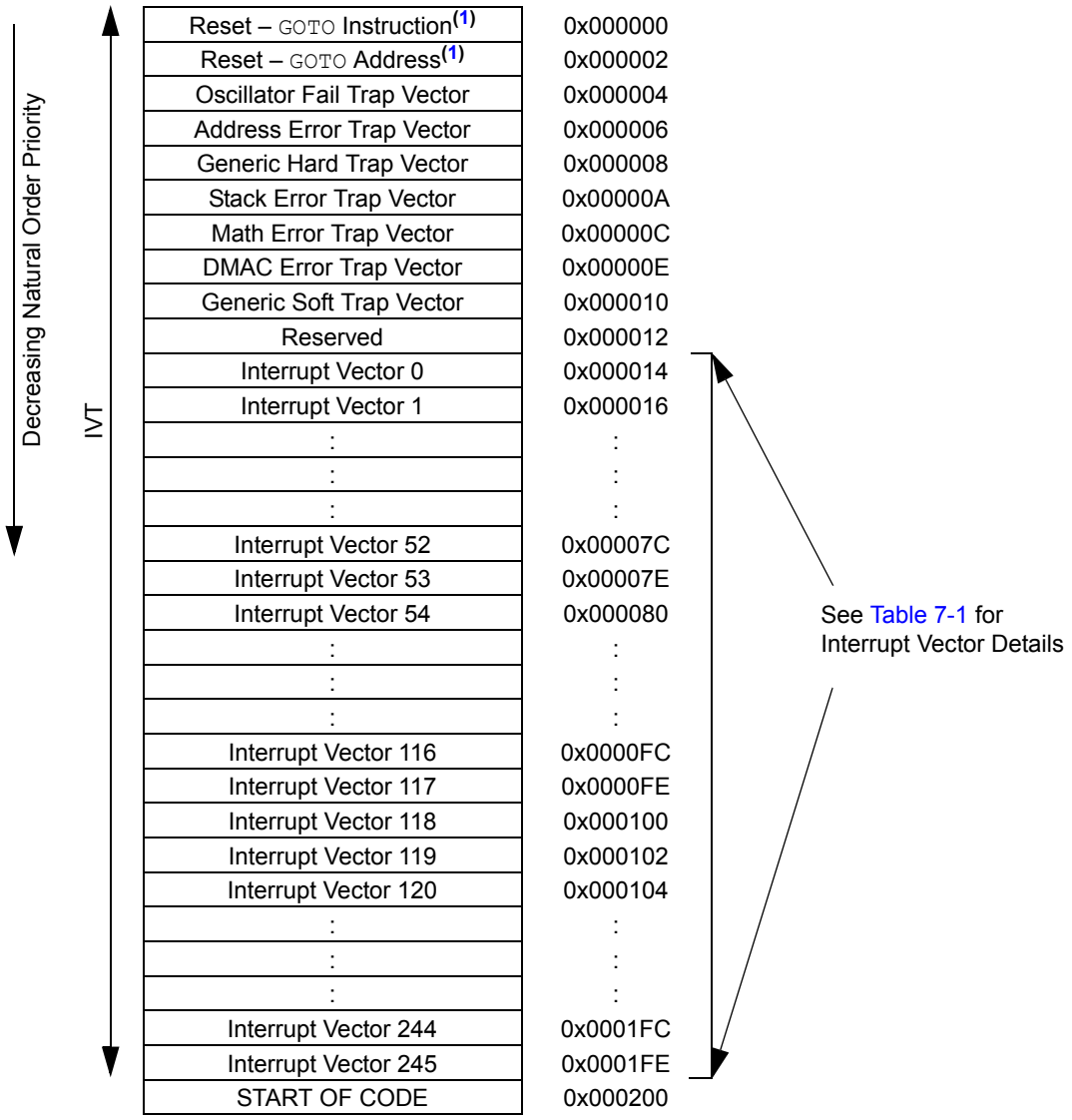
When code is being executed in the Auxiliary Segment, a special single interrupt vector, located at address, 0x7FFFFA, is used for all interrupt sources and traps. Once vectored to this single routine, the VECNUM<7:0> bits (INTTREG<7:0>, Register 7-7) can be examined to determine the source of the interrupt or trap so that it can be properly processed.

## 7.3 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices clear their registers in response to a Reset, which forces the PC to zero. The digital signal controller then begins program execution at location, 0x000000. A `GOTO` instruction at the Reset address can redirect program execution to the appropriate start-up routine.

**Note:** Reset locations are also located in the Auxiliary Segment at the addresses 0x7FFFFC and 0x7FFFFE. The Reset Target Vector Select bit, RSTPRI (FICD<2>) controls whether the primary (General Segment) or Auxiliary Segment Reset location is used.

**FIGURE 7-1: dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 INTERRUPT VECTOR TABLE**




**Note 1:** Reset locations are also located in the Auxiliary Segment at the addresses 0x7FFFFC and 0x7FFFFE. The Reset Target Vector Select bit, RSTPRI (FICD<2>) controls whether the primary (General Segment) or Auxiliary Segment Reset location is used.


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**TABLE 7-1: INTERRUPT VECTOR DETAILS**

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| Highest Natural Order Priority | | | | | | |
| INT0 – External Interrupt 0 | 8 | 0 | 0x000014 | IFS0<0> | IEC0<0> | IPC0<2:0> |
| IC1 – Input Capture 1 | 9 | 1 | 0x000016 | IFS0<1> | IEC0<1> | IPC0<6:4> |
| OC1 – Output Compare 1 | 10 | 2 | 0x000018 | IFS0<2> | IEC0<2> | IPC0<10:8> |
| T1 – Timer1 | 11 | 3 | 0x00001A | IFS0<3> | IEC0<3> | IPC0<14:12> |
| DMA0 – DMA Channel 0 | 12 | 4 | 0x00001C | IFS0<4> | IEC0<4> | IPC1<2:0> |
| IC2 – Input Capture 2 | 13 | 5 | 0x00001E | IFS0<5> | IEC0<5> | IPC1<6:4> |
| OC2 – Output Compare 2 | 14 | 6 | 0x000020 | IFS0<6> | IEC0<6> | IPC1<10:8> |
| T2 – Timer2 | 15 | 7 | 0x000022 | IFS0<7> | IEC0<7> | IPC1<14:12> |
| T3 – Timer3 | 16 | 8 | 0x000024 | IFS0<8> | IEC0<8> | IPC2<2:0> |
| SPI1E – SPI1 Error | 17 | 9 | 0x000026 | IFS0<9> | IEC0<9> | IPC2<6:4> |
| SPI1 – SPI1 Transfer Done | 18 | 10 | 0x000028 | IFS0<10> | IEC0<10> | IPC2<10:8> |
| U1RX – UART1 Receiver | 19 | 11 | 0x00002A | IFS0<11> | IEC0<11> | IPC2<14:12> |
| U1TX – UART1 Transmitter | 20 | 12 | 0x00002C | IFS0<12> | IEC0<12> | IPC3<2:0> |
| AD1 – ADC1 Convert Done | 21 | 13 | 0x00002E | IFS0<13> | IEC0<13> | IPC3<6:4> |
| DMA1 – DMA Channel 1 | 22 | 14 | 0x000030 | IFS0<14> | IEC0<14> | IPC3<10:8> |
| NVM – NVM Write Complete | 23 | 15 | 0x000032 | IFS0<15> | IEC0<15> | IPC3<14:12> |
| SI2C1 – I2C1 Slave Event | 24 | 16 | 0x000034 | IFS1<0> | IEC1<0> | IPC4<2:0> |
| MI2C1 – I2C1 Master Event | 25 | 17 | 0x000036 | IFS1<1> | IEC1<1> | IPC4<6:4> |
| CM – Comparator Combined Event | 26 | 18 | 0x000038 | IFS1<2> | IEC1<2> | IPC4<10:8> |
| CN – Input Change Interrupt | 27 | 19 | 0x00003A | IFS1<3> | IEC1<3> | IPC4<14:12> |
| INT1 – External Interrupt 1 | 28 | 20 | 0x00003C | IFS1<4> | IEC1<4> | IPC5<2:0> |
| AD2 – ADC2 Convert Done | 29 | 21 | 0x00003E | IFS1<5> | IEC1<5> | IPC5<6:4> |
| IC7 – Input Capture 7 | 30 | 22 | 0x000040 | IFS1<6> | IEC1<6> | IPC5<10:8> |
| IC8 – Input Capture 8 | 31 | 23 | 0x000042 | IFS1<7> | IEC1<7> | IPC5<14:12> |
| DMA2 – DMA Channel 2 | 32 | 24 | 0x000044 | IFS1<8> | IEC1<8> | IPC6<2:0> |
| OC3 – Output Compare 3 | 33 | 25 | 0x000046 | IFS1<9> | IEC1<9> | IPC6<6:4> |
| OC4 – Output Compare 4 | 34 | 26 | 0x000048 | IFS1<10> | IEC1<10> | IPC6<10:8> |
| T4 – Timer4 | 35 | 27 | 0x00004A | IFS1<11> | IEC1<11> | IPC6<14:12> |
| T5 – Timer5 | 36 | 28 | 0x00004C | IFS1<12> | IEC1<12> | IPC7<2:0> |
| INT2 – External Interrupt 2 | 37 | 29 | 0x00004E | IFS1<13> | IEC1<13> | IPC7<6:4> |
| U2RX – UART2 Receiver | 38 | 30 | 0x000050 | IFS1<14> | IEC1<14> | IPC7<10:8> |
| U2TX – UART2 Transmitter | 39 | 31 | 0x000052 | IFS1<15> | IEC1<15> | IPC7<14:12> |
| SPI2E – SPI2 Error | 40 | 32 | 0x000054 | IFS2<0> | IEC2<0> | IPC8<2:0> |
| SPI2 – SPI2 Transfer Done | 41 | 33 | 0x000056 | IFS2<1> | IEC2<1> | IPC8<6:4> |
| C1RX – CAN1 RX Data Ready | 42 | 34 | 0x000058 | IFS2<2> | IEC2<2> | IPC8<10:8> |
| C1 – CAN1 Event | 43 | 35 | 0x00005A | IFS2<3> | IEC2<3> | IPC8<14:12> |
| DMA3 – DMA Channel 3 | 44 | 36 | 0x00005C | IFS2<4> | IEC2<4> | IPC9<2:0> |
| IC3 – Input Capture 3 | 45 | 37 | 0x00005E | IFS2<5> | IEC2<5> | IPC9<6:4> |
| IC4 – Input Capture 4 | 46 | 38 | 0x000060 | IFS2<6> | IEC2<6> | IPC9<10:8> |
| IC5 – Input Capture 5 | 47 | 39 | 0x000062 | IFS2<7> | IEC2<7> | IPC9<14:12> |
| IC6 – Input Capture 6 | 48 | 40 | 0x000064 | IFS2<8> | IEC2<8> | IPC10<2:0> |

**Note 1:** This interrupt source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**2:** This interrupt source is available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices only.

**TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)**

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| OC5 – Output Compare 5 | 49 | 41 | 0x000066 | IFS2<9> | IEC2<9> | IPC10<6:4> |
| OC6 – Output Compare 6 | 50 | 42 | 0x000068 | IFS2<10> | IEC2<10> | IPC10<10:8> |
| OC7 – Output Compare 7 | 51 | 43 | 0x00006A | IFS2<11> | IEC2<11> | IPC10<14:12> |
| OC8 – Output Compare 8 | 52 | 44 | 0x00006C | IFS2<12> | IEC2<12> | IPC11<2:0> |
| PMP – Parallel Master Port | 53 | 45 | 0x00006E | IFS2<13> | IEC2<13> | IPC11<6:4> |
| DMA4 – DMA Channel 4 | 54 | 46 | 0x000070 | IFS2<14> | IEC2<14> | IPC11<10:8> |
| T6 – Timer6 | 55 | 47 | 0x000072 | IFS2<15> | IEC2<15> | IPC11<14:12> |
| T7 – Timer7 | 56 | 48 | 0x000074 | IFS3<0> | IEC3<0> | IPC12<2:0> |
| SI2C2 – I2C2 Slave Event | 57 | 49 | 0x000076 | IFS3<1> | IEC3<1> | IPC12<6:4> |
| MI2C2 – I2C2 Master Event | 58 | 50 | 0x000078 | IFS3<2> | IEC3<2> | IPC12<10:8> |
| T8 – Timer8 | 59 | 51 | 0x00007A | IFS3<3> | IEC3<3> | IPC12<14:12> |
| T9 – Timer9 | 60 | 52 | 0x00007C | IFS3<4> | IEC3<4> | IPC13<2:0> |
| INT3 – External Interrupt 3 | 61 | 53 | 0x00007E | IFS3<5> | IEC3<5> | IPC13<6:4> |
| INT4 – External Interrupt 4 | 62 | 54 | 0x000080 | IFS3<6> | IEC3<6> | IPC13<10:8> |
| C2RX – CAN2 RX Data Ready | 63 | 55 | 0x000082 | IFS3<7> | IEC3<7> | IPC13<14:12> |
| C2 – CAN2 Event | 64 | 56 | 0x000084 | IFS3<8> | IEC3<8> | IPC14<2:0> |
| PSEM – PWM Special Event Match(1) | 65 | 57 | 0x000086 | IFS3<9> | IEC3<9> | IPC14<6:4> |
| QEI1 – QEI1 Position Counter Compare(1) | 66 | 58 | 0x000088 | IFS3<10> | IEC3<10> | IPC14<10:8> |
| DCIE – DCI Fault Interrupt | 67 | 59 | 0x00008A | IFS3<11> | IEC3<11> | IPC14<14:12> |
| DCI – DCI Transfer Done | 68 | 60 | 0x00008C | IFS3<12> | IEC3<12> | IPC15<2:0> |
| DMA5 – DMA Channel 5 | 69 | 61 | 0x00008E | IFS3<13> | IEC3<13> | IPC15<6:4> |
| RTC – Real-Time Clock and Calendar | 70 | 62 | 0x000090 | IFS3<14> | IEC3<14> | IPC15<10:8> |
| Reserved | 71-72 | 63-64 | 0x000092-0x000094 | — | — | — |
| U1E – UART1 Error Interrupt | 73 | 65 | 0x000096 | IFS4<1> | IEC4<1> | IPC16<6:4> |
| U2E – UART2 Error Interrupt | 74 | 66 | 0x000098 | IFS4<2> | IEC4<2> | IPC16<10:8> |
| CRC – CRC Generator Interrupt | 75 | 67 | 0x00009A | IFS4<3> | IEC4<3> | IPC16<14:12> |
| DMA6 – DMA Channel 6 | 76 | 68 | 0x00009C | IFS4<4> | IEC4<4> | IPC17<2:0> |
| DMA7 – DMA Channel 7 | 77 | 69 | 0x00009E | IFS4<5> | IEC4<5> | IPC17<6:4> |
| C1TX – CAN1 TX Data Request | 78 | 70 | 0x0000A0 | IFS4<6> | IEC4<6> | IPC17<10:8> |
| C2TX – CAN2 TX Data Request | 79 | 71 | 0x0000A2 | IFS4<7> | IEC4<7> | IPC17<14:12> |
| Reserved | 80 | 72 | 0x0000A4 | — | — | — |
| PSESM – PWM Secondary Special Event Match(1) | 81 | 73 | 0x0000A6 | IFS4<9> | IEC4<9> | IPC18<6:4> |
| Reserved | 82 | 74 | 0x0000A8 | — | — | — |
| QEI2 – QEI2 Position Counter Compare(1) | 83 | 75 | 0x0000AA | IFS4<11> | IEC4<11> | IPC18<14:12> |
| Reserved | 84-88 | 76-80 | 0x0000AC-0x0000B4 | — | — | — |
| U3E – UART3 Error Interrupt | 89 | 81 | 0x0000B6 | IFS5<1> | IEC5<1> | IPC20<6:4> |
| U3RX – UART3 Receiver | 90 | 82 | 0x0000B8 | IFS5<2> | IEC5<2> | IPC20<10:8> |
| U3TX – UART3 Transmitter | 91 | 83 | 0x0000BA | IFS5<3> | IEC5<3> | IPC20<14:12> |
| Reserved | 9293 | 84-85 | 0x0000BC-0x0000BE | — | — | — |

**Note 1:** This interrupt source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**2:** This interrupt source is available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices only.


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**TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)**

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| USB1 – USB OTG Interrupt(2) | 94 | 86 | 0x0000C0 | IFS5<6> | IEC5<6> | IPC21<10:8> |
| U4E – UART4 Error Interrupt | 95 | 87 | 0x0000C2 | IFS5<7> | IEC5<7> | IPC21<14:12> |
| U4RX – UART4 Receiver | 96 | 88 | 0x0000C4 | IFS5<8> | IEC5<8> | IPC22<2:0> |
| U4TX – UART4 Transmitter | 97 | 89 | 0x0000C6 | IFS5<9> | IEC5<9> | IPC22<6:4> |
| SPI3E – SPI3 Error | 98 | 90 | 0x0000C8 | IFS5<10> | IEC5<10> | IPC22<10:8> |
| SPI3 – SPI3 Transfer Done | 99 | 91 | 0x0000CA | IFS5<11> | IEC5<11> | IPC22<14:12> |
| OC9 – Output Compare 9 | 100 | 92 | 0x0000CC | IFS5<12> | IEC5<12> | IPC23<2:0> |
| IC9 – Input Capture 9 | 101 | 93 | 0x0000CE | IFS5<13> | IEC5<13> | IPC23<6:4> |
| PWM1 – PWM Generator 1(1) | 102 | 94 | 0x0000D0 | IFS5<14> | IEC5<14> | IPC23<10:8> |
| PWM2 – PWM Generator 2(1) | 103 | 95 | 0x0000D2 | IFS5<15> | IEC5<15> | IPC23<14:12> |
| PWM3 – PWM Generator 3(1) | 104 | 96 | 0x0000D4 | IFS6<0> | IEC6<0> | IPC24<2:0> |
| PWM4 – PWM Generator 4(1) | 105 | 97 | 0x0000D6 | IFS6<1> | IEC6<1> | IPC24<6:4> |
| PWM5 – PWM Generator 5(1) | 106 | 98 | 0x0000D8 | IFS6<2> | IEC6<2> | IPC24<10:8> |
| PWM6 – PWM Generator 6(1) | 107 | 99 | 0x0000DA | IFS6<3> | IEC6<3> | IPC24<14:12> |
| PWM7 – PWM Generator 7(1) | 108 | 100 | 0x0000DC | IFS6<4> | IEC6<4> | IPC25<2:0> |
| Reserved | 109-125 | 101-117 | 0x0000DE-0x0000FC | — | — | — |
| DMA8 – DMA Channel 8 | 126 | 118 | 0x000100 | IFS7<6> | IEC7<6> | IPC29<10:8> |
| DMA9 – DMA Channel 9 | 127 | 119 | 0x000102 | IFS7<7> | IEC7<7> | IPC29<14:12> |
| DMA10 – DMA Channel 10 | 128 | 120 | 0x000104 | IFS7<8> | IEC7<8> | IPC30<2:0> |
| DMA11 – DMA Channel 11 | 129 | 121 | 0x000106 | IFS7<9> | IEC7<9> | IPC30<6:4> |
| SPI4E – SPI4 Error | 130 | 122 | 0x000108 | IFS7<10> | IEC7<10> | IPC30<10:8> |
| SPI4 – SPI4 Transfer Done | 131 | 123 | 0x00010A | IFS7<11> | IEC7<11> | IPC30<14:12> |
| OC10 – Output Compare 10 | 132 | 124 | 0x00010C | IFS7<12> | IEC7<12> | IPC31<2:0> |
| IC10 – Input Capture 10 | 133 | 125 | 0x00010E | IFS7<13> | IEC7<13> | IPC31<6:4> |
| OC11 – Output Compare11 | 134 | 126 | 0x000110 | IFS7<14> | IEC7<14> | IPC31<10:8> |
| IC11 – Input Capture 11 | 135 | 127 | 0x000112 | IFS7<15> | IEC7<15> | IPC31<14:12> |
| OC12 – Output Compare 12 | 136 | 128 | 0x000114 | IFS8<0> | IEC8<0> | IPC32<2:0> |
| IC12 – Input Capture 12 | 137 | 129 | 0x000116 | IFS8<1> | IEC8<1> | IPC32<6:4> |
| DMA12 – DMA Channel 12 | 138 | 130 | 0x000118 | IFS8<2> | IEC8<2> | IPC32<10:8> |
| DMA13– DMA Channel 13 | 139 | 131 | 0x00011A | IFS8<3> | IEC8<3> | IPC32<14:12> |
| DMA14 – DMA Channel 14 | 140 | 132 | 0x00011C | IFS8<4> | IEC8<4> | IPC33<2:0> |
| Reserved | 141 | 133 | 0x00011E | — | — | — |
| OC13 – Output Compare 13 | 142 | 134 | 0x000120 | IFS8<6> | IEC8<6> | IPC33<10:8> |
| IC13 – Input Capture 13 | 143 | 135 | 0x000122 | IFS8<7> | IEC8<7> | IPC33<14:12> |
| OC14 – Output Compare14 | 144 | 136 | 0x000124 | IFS8<8> | IEC8<8> | IPC34<2:0> |
| IC14 – Input Capture 14 | 145 | 137 | 0x000126 | IFS8<9> | IEC8<9> | IPC34<6:4> |
| OC15 – Output Compare 15 | 146 | 138 | 0x000128 | IFS8<10> | IEC8<10> | IPC34<10:8> |
| IC15 – Input Capture 15 | 147 | 139 | 0x00012A | IFS8<11> | IEC8<11> | IPC34<14:12> |
| OC16 – Output Compare 16 | 148 | 140 | 0x00012C | IFS8<12> | IEC8<12> | IPC35<2:0> |
| IC16 – Input Capture 16 | 149 | 141 | 0x00012E | IFS8<13> | IEC8<13> | IPC35<6:4> |
| ICD – ICD Application | 150 | 142 | 0x000130 | IFS8<14> | IEC8<14> | IPC35<10:8> |
| Reserved | 151-245 | 142-237 | 0x000130-0x0001FE | — | — | — |
| Lowest Natural Order Priority | | | | | | |

**Note 1:** This interrupt source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**2:** This interrupt source is available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices only.

## 7.4 Interrupt Resources

Many useful resources related to Interrupts are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

### 7.4.1 KEY RESOURCES

- **Section 6. "Interrupts"** (DS70600) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 7.5 Interrupt Control and Status Registers

dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices implement the following registers for the interrupt controller:

- INTCON1-INTCON4
- INTTREG

### 7.5.1 INTCON1 THROUGH INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS) as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior and software trap enable. This register also contains the Global Interrupt Enable bit (GIE).

INTCON3 contains the status flags for the USB, DMA and DO stack overflow status trap sources.

The INTCON4 register contains the software generated Hard Trap Status bit (SGHT).

### 7.5.2 IFSx

The IFS registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

### 7.5.3 IECx

The IEC registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

### 7.5.4 IPCx

The IPC registers are used to set the Interrupt Priority Level for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

### 7.5.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the vector number (VECNUM<7:0>) and Interrupt level bit (ILR<3:0>) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0<0>, the INT0IE bit in IEC0<0> and the INT0IP bits in the first position of IPC0 (IPC0<2:0>).

### 7.5.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers refer to **Section 2. "CPU"** (DS70359) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

- The CPU STATUS register, SR, contains the IPL<2:0> bits (SR<7:5>). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU priority level by writing to the IPL bits.
- The CORCON register contains the IPL3 bit which, together with IPL<2:0>, also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-3 through Register 7-7 in the following pages.


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**REGISTER 7-1: SR: CPU STATUS REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/C-0 | R/C-0 | R-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OA | OB | SA | SB | OAB | SAB | DA | DC |
| bit 15 | | | | | | | bit 8 |

| R/W-0(3) | R/W-0(3) | R/W-0(3) | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IPL<2:0>(2) | | | RA | N | OV | Z | C |
| bit 7 | | | | | | | bit 0 |

| Legend: | C = Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(2,3)

111 = CPU Interrupt Priority Level is 7 (15, user interrupts are disabled)
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

**Note 1:** For complete register details, see **Register 3-1: "SR: CPU Status Register"**.

**2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1.

**3:** The IPL<2:0> Status bits are read-only when NSTDIS (INTCON1<15>) = 1.

**REGISTER 7-2: CORCON: CORE CONTROL REGISTER(1)**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| **VAR** | — | US<1:0> | | EDT | DL<2:0> | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SATA | SATB | SATDW | ACCSAT | **IPL3(2)** | SFA | RND | IF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing is enabled
0 = Fixed exception processing is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

**Note 1:** For complete register details, see **Register 3-2: "CORCON: Core Control Register"**.
**2:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.


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**REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| NSTDIS | OVAERR(1) | OVBERR(1) | COVAERR(1) | COVBERR(1) | OVATE(1) | OVBTE(1) | COVTE(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| SFTACERR(1) | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit(1)
1 = Trap was caused by overflow of Accumulator A
0 = Trap was not caused by overflow of Accumulator A

bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit(1)
1 = Trap was caused by overflow of Accumulator B
0 = Trap was not caused by overflow of Accumulator B

bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit(1)
1 = Trap was caused by catastrophic overflow of Accumulator A
0 = Trap was not caused by catastrophic overflow of Accumulator A

bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit(1)
1 = Trap was caused by catastrophic overflow of Accumulator B
0 = Trap was not caused by catastrophic overflow of Accumulator B

bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit(1)
1 = Trap overflow of Accumulator A
0 = Trap is disabled

bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit(1)
1 = Trap overflow of Accumulator B
0 = Trap is disabled

bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit(1)
1 = Trap on catastrophic overflow of Accumulator A or B is enabled
0 = Trap is disabled

bit 7 **SFTACERR:** Shift Accumulator Error Status bit(1)
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift

bit 6 **DIV0ERR:** Divide-by-Zero Error Status bit
1 = Math error trap was caused by a divide-by-zero
0 = Math error trap was not caused by a divide-by-zero

bit 5 **DMACERR:** DMAC Trap Flag bit
1 = DMAC trap has occurred
0 = DMAC trap has not occurred

**Note 1:** This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

**REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)**

bit 4 **MATHERR:** Math Error Status bit
1 = Math error trap has occurred
0 = Math error trap has not occurred

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as '0'

**Note 1:** This bit is available on dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.


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**REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2**

| R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| GIE | DISI | SWTRAP | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **GIE:** Global Interrupt Enable bit
1 = Interrupts and associated IE bits are enabled
0 = Interrupts are disabled, but traps are still enabled

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13 **SWTRAP:** Software Trap Status bit
1 = Software trap is enabled
0 = Software trap is disabled

bit 12-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 3 **INT3EP:** External Interrupt 3 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

**REGISTER 7-5: INTCON3: INTERRUPT CONTROL REGISTER 3**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | UAE | DAE | DOOVR | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **UAE:** USB Address Error Soft Trap Status bit
1 = USB address error (soft) trap has occurred
0 = USB address error (soft) trap has not occurred

bit 5 **DAE:** DMA Address Error Soft Trap Status bit
1 = DMA address error soft trap has occurred
0 = DMA address error soft trap has not occurred

bit 4 **DOOVR:** Do Stack Overflow Soft Trap Status bit
1 = Do stack overflow soft trap has occurred
0 = Do stack overflow soft trap has not occurred

bit 3-0 **Unimplemented:** Read as '0'

**REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | SGHT |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-1 **Unimplemented:** Read as '0'

bit 0 **SGHT:** Software Generated Hard Trap Status bit
1 = Software generated hard trap has occurred
0 = Software generated hard trap has not occurred


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**REGISTER 7-7: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | ILR<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VECNUM<7:0>(1) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **ILR<3:0>:** New CPU Interrupt Priority Level bits
1111 = CPU Interrupt Priority Level is 15
•
•
•
0001 = CPU Interrupt Priority Level is 1
0000 = CPU Interrupt Priority Level is 0

bit 7-0 **VECNUM<7:0>:** Vector Number of Pending Interrupt bits(1)
11111111 = 255, Reserved
•
•
•
00001001 = 9, IC1 – Input Capture 1
00001000 = 8, INT0 – External Interrupt 0
00000111 = 7, Reserved
00000110 = 6, Generic soft error trap
00000101 = 5, DMAC error trap
00000100 = 4, Math error trap
00000011 = 3, Stack error trap
00000010 = 2, Generic hard trap
00000001 = 1, Address error trap
00000000 = 0, Oscillator fail trap

**Note 1:** See Table 7-1 for the complete list of interrupt vector numbers.

**NOTES:**


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## 8.0 DIRECT MEMORY ACCESS (DMA)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 22. "Direct Memory Access (DMA)"** (DS70348) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The DMA controller transfers data between peripheral data registers and data space SRAM. The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 DMA subsystem uses dual-ported SRAM memory (DPSRAM) and register structures that allow the DMA to operate across its own, independent address and data buses with no impact on CPU operation. This architecture eliminates the need for cycle stealing, which halts the CPU when a higher priority DMA transfer is requested. Both the CPU and DMA controller can write and read to/from addresses within data space without interference, such as CPU stalls, resulting in maximized, real-time performance. Alternatively, DMA operation and data transfer to/from the memory and peripherals are not impacted by CPU processing. For example, when a Run-Time Self-Programming (RTSP) operation is performed, the CPU does not execute any instructions until RTSP is finished. This condition, however, does not impact data transfer to/from memory and the peripherals.

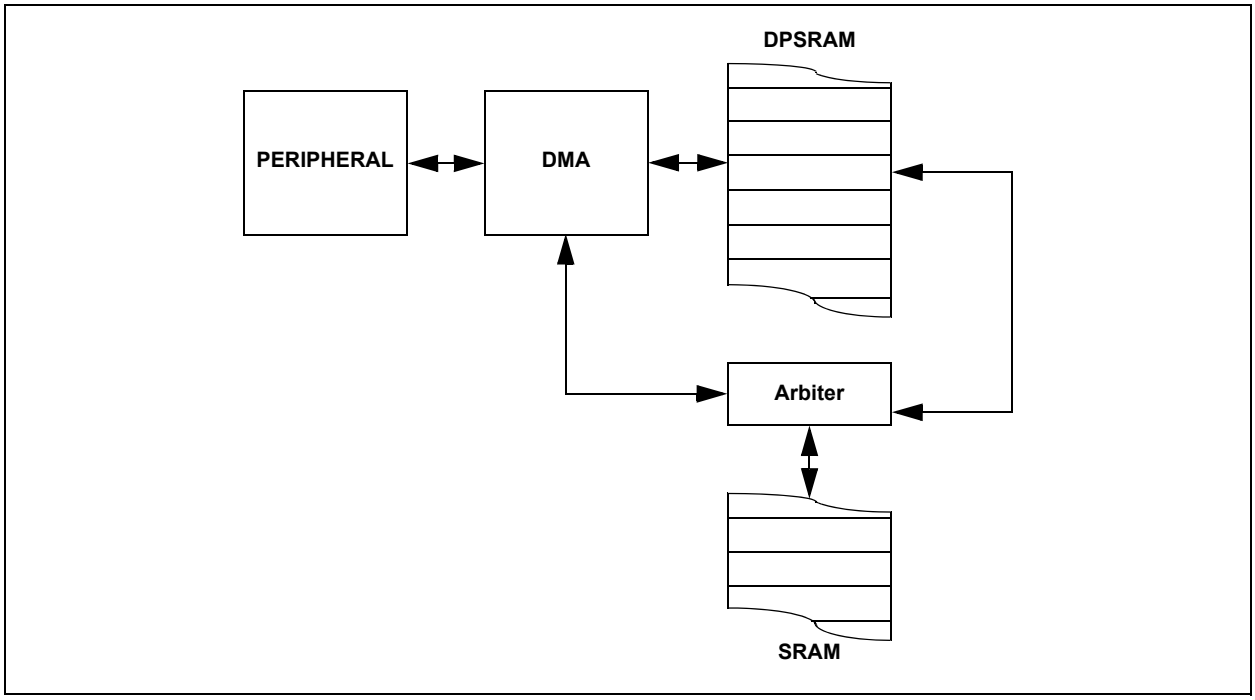
In addition, DMA can access entire data memory space (SRAM and DPSRAM). The Data Memory Bus Arbiter is utilized when either the CPU or DMA attempts to access non-dual ported SRAM, resulting in potential DMA or CPU stalls.

The DMA controller supports up to 15 independent channels. Each channel can be configured for transfers to or from selected peripherals. Some of the peripherals supported by the DMA controller include:

- ECAN™
- Data Converter Interface (DCI)
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI)
- UART
- Input Capture
- Output Compare
- Parallel Master Port (PMP)

Refer to Table 8-1 for a complete list of supported peripherals.

**FIGURE 8-1: DMA CONTROLLER**



In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receive a request to transfer data, a simple fixed priority scheme, based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA controller provides these functional capabilities:

- Up to 15 DMA Channels
- Register Indirect With Post-Increment Addressing mode
- Register Indirect Without Post-Increment Addressing mode
- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU Interrupt after Half or Full Block Transfer Complete
- Byte or Word Transfers
- Fixed Priority Channel Arbitration
- Manual (software) or Automatic (peripheral DMA requests) Transfer Initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two DPSRAM start addresses after each block transfer complete)
- DMA Request for Each Channel can be Selected from Any Supported Interrupt Source
- Debug Support Features

The peripherals that can utilize DMA are listed in Table 8-1.

**TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS**

| Peripheral to DMA Association | DMAxREQ Register IRQSEL<7:0> Bits | DMAxPAD Register (Values to Read from Peripheral) | DMAxPAD Register (Values to Write to Peripheral) |
|---|---|---|---|
| INT0 – External Interrupt 0 | 00000000 | — | — |
| IC1 – Input Capture 1 | 00000001 | 0x0144 (IC1BUF) | — |
| IC2 – Input Capture 2 | 00000101 | 0x014C (IC2BUF) | — |
| IC3 – Input Capture 3 | 00100101 | 0x0154 (IC3BUF) | — |
| IC4 – Input Capture 4 | 00100110 | 0x015C (IC4BUF) | — |
| OC1 – Output Compare 1 | 00000010 | — | 0x0906 (OC1R)<br>0x0904 (OC1RS) |
| OC2 – Output Compare 2 | 00000110 | — | 0x0910 (OC2R)<br>0x090E (OC2RS) |
| OC3 – Output Compare 3 | 00011001 | — | 0x091A (OC3R)<br>0x0918 (OC3RS) |
| OC4 – Output Compare 4 | 00011010 | — | 0x0924 (OC4R)<br>0x0922 (OC4RS) |
| TMR2 – Timer2 | 00000111 | — | — |
| TMR3 – Timer3 | 00001000 | — | — |
| TMR4 – Timer4 | 00011011 | — | — |
| TMR5 – Timer5 | 00011100 | — | — |
| SPI1 Transfer Done | 00001010 | 0x0248 (SPI1BUF) | 0x0248 (SPI1BUF) |
| SPI2 Transfer Done | 00100001 | 0x0268 (SPI2BUF) | 0x0268 (SPI2BUF) |
| SPI3 Transfer Done | 01011011 | 0x02A8 (SPI3BUF) | 0x02A8 (SPI3BUF) |
| SPI4 Transfer Done | 01111011 | 0x02C8 (SPI4BUF) | 0x02C8 (SPI4BUF) |
| UART1RX – UART1 Receiver | 00001011 | 0x0226 (U1RXREG) | — |
| UART1TX – UART1 Transmitter | 00001100 | — | 0x0224 (U1TXREG) |
| UART2RX – UART2 Receiver | 00011110 | 0x0236 (U2RXREG) | — |
| UART2TX – UART2 Transmitter | 00011111 | — | 0x0234 (U2TXREG) |
| UART3RX – UART3 Receiver | 01010010 | 0x0256 (U3RXREG) | — |
| UART3TX – UART3 Transmitter | 01010011 | — | 0x0254 (U3TXREG) |


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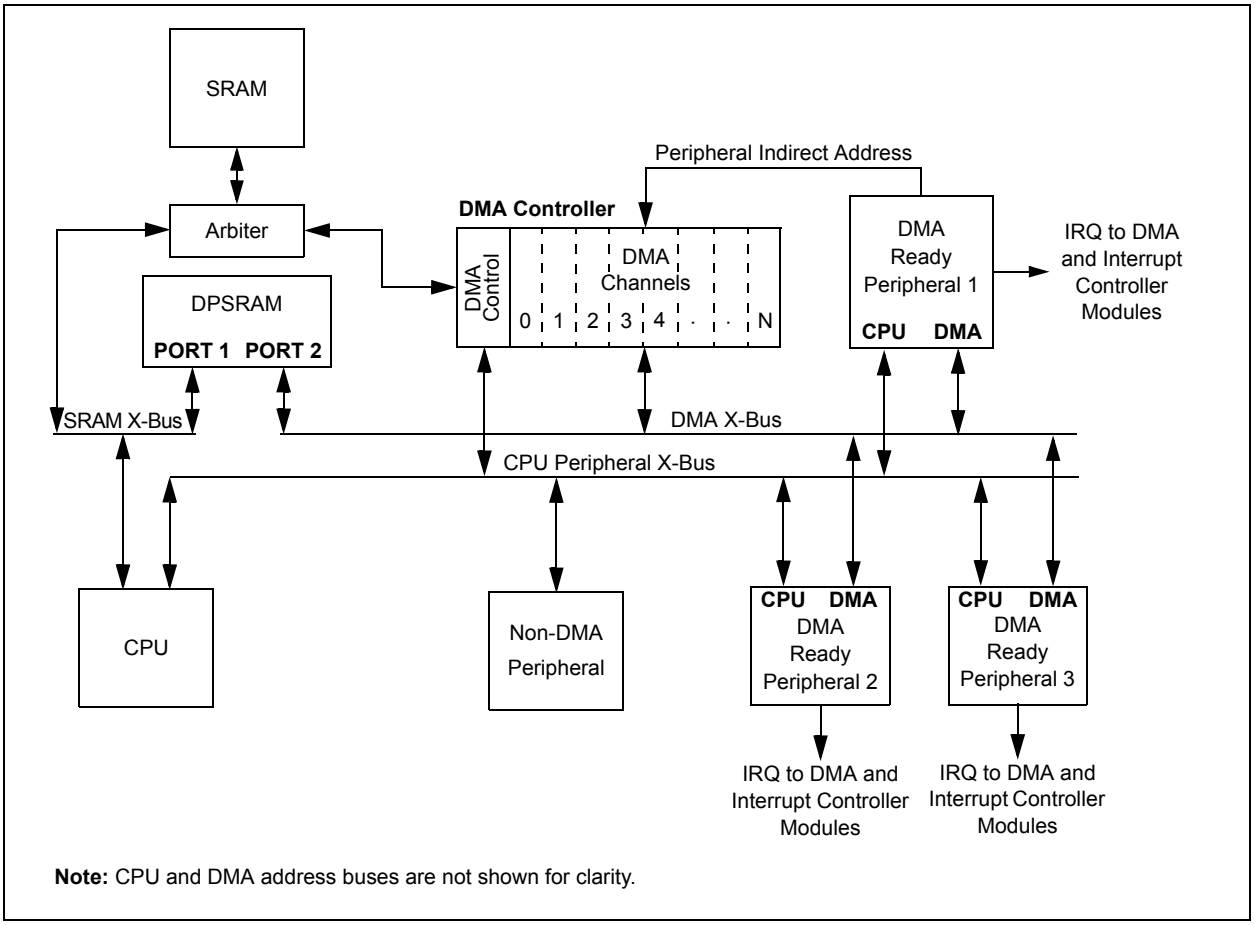
**TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS (CONTINUED)**

| Peripheral to DMA Association | DMAxREQ Register IRQSEL<7:0> Bits | DMAxPAD Register (Values to Read from Peripheral) | DMAxPAD Register (Values to Write to Peripheral) |
|---|---|---|---|
| UART4RX – UART4 Receiver | 01011000 | 0x02B6 (U4RXREG) | — |
| UART4TX – UART4 Transmitter | 01011001 | — | 0x02B4 (U4TXREG) |
| ECAN1 – RX Data Ready | 00100010 | 0x0440 (C1RXD) | — |
| ECAN1 – TX Data Request | 01000110 | — | 0x0442 (C1TXD) |
| ECAN2 – RX Data Ready | 00110111 | 0x0540 (C2RXD) | — |
| ECAN2 – TX Data Request | 01000111 | — | 0x0542 (C2TXD) |
| DCI – DCI Transfer Done | 00111100 | 0x0290 (RXBUF0) | 0x0298 (TXBUF0) |
| ADC1 – ADC1 Convert Done | 00001101 | 0x0300 (ADC1BUF0) | — |
| ADC2 – ADC2 Convert Done | 00010101 | 0x0340 (ADC2BUF0) | — |
| PMP – PMP Data Move | 00101101 | 0x0608 (PMDIN1) | 0x0608 (PMDIN1) |

**FIGURE 8-2: DMA CONTROLLER TO PERIPHERAL ASSOCIATIONS BLOCK DIAGRAM**




**Note:** CPU and DMA address buses are not shown for clarity.

## 8.1 DMA Resources

Many useful resources related to DMA are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

### 8.1.1 KEY RESOURCES

- **Section 22. "Direct Memory Access (DMA)"** (DS70348) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 8.2 DMA Control Registers

Each DMAC Channel x (where x = 0 through 14) contains the following registers:

- 16-Bit DMA Channel Control register (DMAxCON)
- 16-Bit DMA Channel IRQ Select register (DMAxREQ)
- 32-Bit DMA RAM Primary Start Address register (DMAxSTA)
- 32-Bit DMA RAM Secondary Start Address register (DMAxSTB)
- 16-Bit DMA Peripheral Address register (DMAxPAD)
- 14-Bit DMA Transfer Count register (DMAxCNT)

Additional status registers (DMAPWC, DMARQC, DMAPPS, DMALCA and DSADR) are common to all DMAC channels. These status registers provide information on write and request collisions, as well as on last address and channel access information.

The DMA Interrupt Flags (DMAxIF) are located in an IFSx register in the interrupt controller. The corresponding interrupt enable control bits (DMAxIE) are located in an IECx register in the interrupt controller, and the corresponding interrupt priority control bits (DMAxIP) are located in an IPCx register in the interrupt controller.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**REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CHEN | SIZE | DIR | HALF | NULLW | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | AMODE<1:0> | | — | — | MODE<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CHEN:** Channel Enable bit
1 = Channel is enabled
0 = Channel is disabled

bit 14 **SIZE:** Data Transfer Size bit
1 = Byte
0 = Word

bit 13 **DIR**: Transfer Direction bit (source/destination bus select)
1 = Reads from DPSRAM (or RAM) address, writes to peripheral address
0 = Reads from peripheral address, writes to DPSRAM (or RAM) address

bit 12 **HALF:** Block Transfer Interrupt Select bit
1 = Initiates interrupt when half of the data has been moved
0 = Initiates interrupt when all of the data has been moved

bit 11 **NULLW:** Null Data Peripheral Write Mode Select bit
1 = Null data write to peripheral in addition to DPSRAM (or RAM) write (DIR bit must also be clear)
0 = Normal operation

bit 10-6 **Unimplemented:** Read as '0'

bit 5-4 **AMODE<1:0>:** DMA Channel Addressing Mode Select bits
11 = Reserved
10 = Peripheral Indirect Addressing mode
01 = Register Indirect without Post-Increment mode
00 = Register Indirect with Post-Increment mode

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **MODE<1:0>:** DMA Channel Operating Mode Select bits
11 = One-Shot, Ping-Pong modes are enabled (one block transfer from/to each DMA buffer)
10 = Continuous, Ping-Pong modes are enabled
01 = One-Shot, Ping-Pong modes are disabled
00 = Continuous, Ping-Pong modes are disabled

**REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER**

| R/S-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| FORCE(1) | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IRQSEL<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | S = Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FORCE:** Force DMA Transfer bit(1)
1 = Forces a single DMA transfer (Manual mode)
0 = Automatic DMA transfer initiation by DMA request

bit 14-8 **Unimplemented:** Read as '0'

bit 7-0 **IRQSEL<7:0>:** DMA Peripheral IRQ Number Select bits
00000000 = INT0 – External Interrupt 0
00000001 = IC1 – Input Capture 1
00000010 = OC1 – Output Compare 1
00000101 = IC2 – Input Capture 2
00000110 = OC2 – Output Compare 2
00000111 = TMR2 – Timer2
00001000 = TMR3 – Timer3
00001010 = SPI1 – Transfer done
00001011 = UART1RX – UART1 Receiver
00001100 = UART1TX – UART1 Transmitter
00001101 = ADC1 – ADC1 convert done
00010101 = ADC2 – ADC2 convert done
00011001 = OC3 – Output Compare 3
00011010 = OC4 – Output Compare 4
00011011 = TMR4 – Timer4
00011100 = TMR5 – Timer5
00011110 = UART2RX – UART2 Receiver
00011111 = UART2TX – UART2 Transmitter
00100001 = SPI2 – Transfer done
00100010 = ECAN1 – RX data ready
00100101 = IC3 – Input Capture 3
00100110 = IC4 – Input Capture 4
00101101 = PMP Data mode
00110111 = ECAN2 – RX data ready
00111100 = DCI – DCI transfer done
01000110 = ECAN1 – TX data request
01000111 = ECAN2 – TX data request
01010010 = UART3RX – UART3 Receiver
01010011 = UART3TX – UART3 Transmitter
01011000 = UART4RX – UART4 Receiver
01011001 = UART4TX – UART4 Transmitter
01011011 = SPI3 – Transfer done
01111011 = SPI4 – Transfer done

**Note 1:** The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).


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**REGISTER 8-3: DMAxSTAH: DMA CHANNEL x START ADDRESS REGISTER A (HIGH)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STA<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STA<23:16>:** Primary Start Address bits (source or destination)

**REGISTER 8-4: DMAxSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STA<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STA<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **STA<15:0>:** Primary Start Address bits (source or destination)

**REGISTER 8-5: DMAxSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STB<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STB<23:16>:** Secondary Start Address bits (source or destination)

**REGISTER 8-6: DMAxSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STB<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STB<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **STB<15:0>:** Secondary Start Address bits (source or destination)


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**REGISTER 8-7: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PAD<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PAD<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PAD<15:0>:** Peripheral Address Register bits

**Note 1:** If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

**REGISTER 8-8: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER(1)**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | CNT<13:8>(2) | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CNT<7:0>(2) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **CNT<13:0>:** DMA Transfer Count Register bits(2)

**Note 1:** If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

**2:** The number of DMA transfers = CNT<13:0> + 1.

**REGISTER 8-9: DSADRH: MOST RECENT DMA DATA SPACE HIGH ADDRESS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| DSADR<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **DSADR<23:16>:** Most Recent DMA Address Accessed by DMA bits

**REGISTER 8-10: DSADRL: MOST RECENT DMA DATA SPACE LOW ADDRESS REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| DSADR<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| DSADR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **DSADR<15:0>:** Most Recent DMA Address Accessed by DMA bits


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**REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER**

| U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | PWCOL14 | PWCOL13 | PWCOL12 | PWCOL11 | PWCOL10 | PWCOL9 | PWCOL8 |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PWCOL7 | PWCOL6 | PWCOL5 | PWCOL4 | PWCOL3 | PWCOL2 | PWCOL1 | PWCOL0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14 **PWCOL14:** Channel 14 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 13 **PWCOL13:** Channel 13 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 12 **PWCOL12:** Channel 12 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 11 **PWCOL11:** Channel 11 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 10 **PWCOL10:** Channel 10 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 9 **PWCOL9:** Channel 9 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 8 **PWCOL8:** Channel 8 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 7 **PWCOL7:** Channel 7 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 6 **PWCOL6:** Channel 6 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 5 **PWCOL5:** Channel 5 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 4 **PWCOL4:** Channel 4 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 3 **PWCOL3:** Channel 3 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

**REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER (CONTINUED)**

bit 2 **PWCOL2:** Channel 2 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 1 **PWCOL1:** Channel 1 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected

bit 0 **PWCOL0:** Channel 0 Peripheral Write Collision Flag bit
1 = Write collision detected
0 = No write collision detected


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**REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER**

| U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | RQCOL14 | RQCOL13 | RQCOL12 | RQCOL11 | RQCOL10 | RQCOL9 | RQCOL8 |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| RQCOL7 | RQCOL6 | RQCOL5 | RQCOL4 | RQCOL3 | RQCOL2 | RQCOL1 | RQCOL0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14 **RQCOL14:** Channel 14 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 13 **RQCOL13:** Channel 13 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 12 **RQCOL12:** Channel 12 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 11 **RQCOL11:** Channel 11 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 10 **RQCOL10:** Channel 10 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 9 **RQCOL9:** Channel 9 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 8 **RQCOL8:** Channel 8 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 7 **RQCOL7:** Channel 7 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 6 **RQCOL6:** Channel 6 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 5 **RQCOL5:** Channel 5 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 4 **RQCOL4:** Channel 4 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 3 **RQCOL3:** Channel 3 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

**REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER (CONTINUED)**

bit 2 **RQCOL2:** Channel 2 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 1 **RQCOL1:** Channel 1 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected

bit 0 **RQCOL0:** Channel 0 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision detected
0 = No request collision detected


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**REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R-1 | R-1 | R-1 | R-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | LSTCH<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-4 **Unimplemented:** Read as '0'

bit 3-0 **LSTCH<3:0>:** Last DMAC Channel Active Status bits

1111 = No DMA transfer has occurred since system Reset
1110 = Last data transfer was handled by Channel 14
1101 = Last data transfer was handled by Channel 13
1100 = Last data transfer was handled by Channel 12
1011 = Last data transfer was handled by Channel 11
1010 = Last data transfer was handled by Channel 10
1001 = Last data transfer was handled by Channel 9
1000 = Last data transfer was handled by Channel 8
0111 = Last data transfer was handled by Channel 7
0110 = Last data transfer was handled by Channel 6
0101 = Last data transfer was handled by Channel 5
0100 = Last data transfer was handled by Channel 4
0011 = Last data transfer was handled by Channel 3
0010 = Last data transfer was handled by Channel 2
0001 = Last data transfer was handled by Channel 1
0000 = Last data transfer was handled by Channel 0

**REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER**

| U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | PPST14 | PPST13 | PPST12 | PPST11 | PPST10 | PPST9 | PPST8 |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PPST7 | PPST6 | PPST5 | PPST4 | PPST3 | PPST2 | PPST1 | PPST0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14 **PPST14:** Channel 14 Ping-Pong Mode Status Flag bit
1 = DMASTB14 register selected
0 = DMASTA14 register selected

bit 13 **PPST13:** Channel 13 Ping-Pong Mode Status Flag bit
1 = DMASTB13 register selected
0 = DMASTA13 register selected

bit 12 **PPST12:** Channel 12 Ping-Pong Mode Status Flag bit
1 = DMASTB12 register selected
0 = DMASTA12 register selected

bit 11 **PPST11:** Channel 11 Ping-Pong Mode Status Flag bit
1 = DMASTB11 register selected
0 = DMASTA11 register selected

bit 10 **PPST10:** Channel 10 Ping-Pong Mode Status Flag bit
1 = DMASTB10 register selected
0 = DMASTA10 register selected

bit 9 **PPST9:** Channel 9 Ping-Pong Mode Status Flag bit
1 = DMASTB9 register selected
0 = DMASTA9 register selected

bit 8 **PPST8:** Channel 8 Ping-Pong Mode Status Flag bit
1 = DMASTB8 register selected
0 = DMASTA8 register selected

bit 7 **PPST7:** Channel 7 Ping-Pong Mode Status Flag bit
1 = DMASTB7 register selected
0 = DMASTA7 register selected

bit 6 **PPST6:** Channel 6 Ping-Pong Mode Status Flag bit
1 = DMASTB6 register selected
0 = DMASTA6 register selected

bit 5 **PPST5:** Channel 5 Ping-Pong Mode Status Flag bit
1 = DMASTB5 register selected
0 = DMASTA5 register selected

bit 4 **PPST4:** Channel 4 Ping-Pong Mode Status Flag bit
1 = DMASTB4 register selected
0 = DMASTA4 register selected

bit 3 **PPST3:** Channel 3 Ping-Pong Mode Status Flag bit
1 = DMASTB3 register selected
0 = DMASTA3 register selected


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**REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER (CONTINUED)**

bit 2 **PPST2:** Channel 2 Ping-Pong Mode Status Flag bit
1 = DMASTB2 register selected
0 = DMASTA2 register selected

bit 1 **PPST1:** Channel 1 Ping-Pong Mode Status Flag bit
1 = DMASTB1 register selected
0 = DMASTA1 register selected

bit 0 **PPST0:** Channel 0 Ping-Pong Mode Status Flag bit
1 = DMASTB0 register selected
0 = DMASTA0 register selected

**NOTES:**


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# 9.0 OSCILLATOR CONFIGURATION

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Oscillator"** (DS70580) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

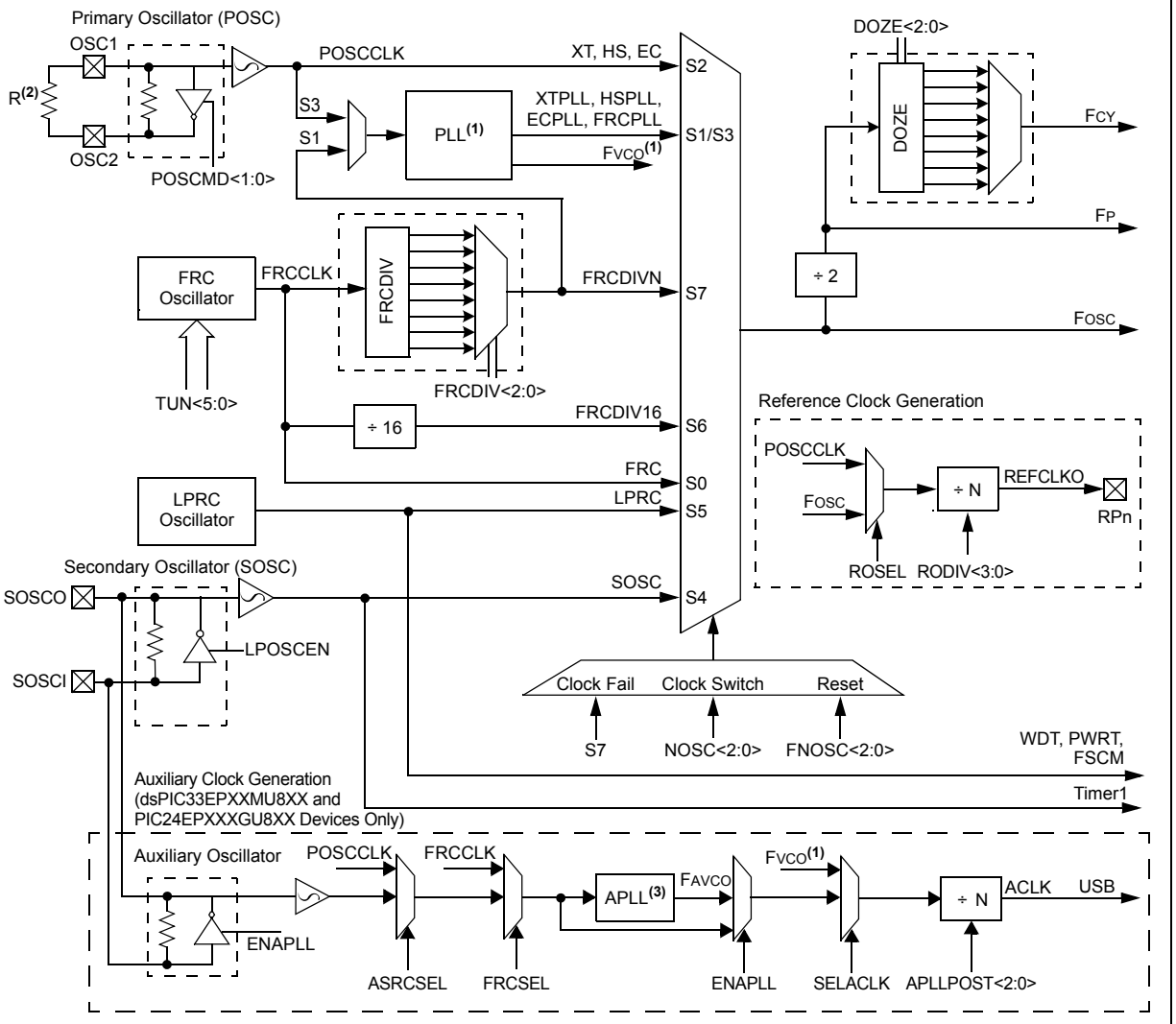
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The oscillator system provides:

- Four external and internal oscillator options
- Auxiliary oscillator that provides clock source to the USB module (if available)
- On-chip Phase-Locked Loop (PLL) to boost internal operating frequency on select internal and external oscillator sources
- On-the-fly clock switching between various clock sources
- Doze mode for system power savings
- Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Nonvolatile Configuration bits for clock source selection

A simplified diagram of the oscillator system is shown in Figure 9-1.

**FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM**




**Note 1:** See Figure 9-2 for PLL and FVCO details.
**2:** If the oscillator is used with XT or HS modes, an external parallel resistor with the value of 1 MΩ must be connected.
**3:** See Figure 9-3 for APLL details.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## 9.1 CPU Clocking System

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 family of devices provides seven system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase-Locked Loop (PLL)
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Secondary (LP) Oscillator
- Low-Power RC (LPRC) Oscillator
- FRC Oscillator with postscaler

Instruction execution speed or device operating frequency, FCY, is given by Equation 9-1.

**EQUATION 9-1: DEVICE OPERATING FREQUENCY**

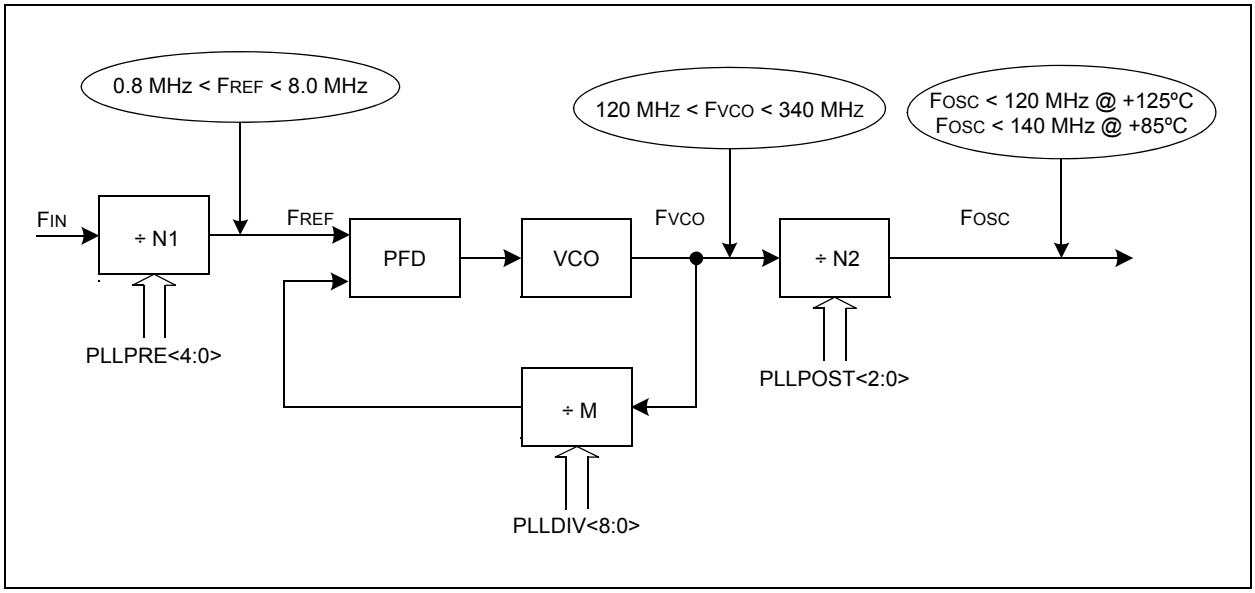
$$FCY = FOSC/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relation between input frequency (FIN) and output frequency (FOSC).

Equation 9-3 provides the relation between input frequency (FIN) and VCO frequency (FVCO).

**FIGURE 9-2: PLL BLOCK DIAGRAM**




**EQUATION 9-2: FOSC CALCULATION**

$$FOSC = FIN \times \left(\frac{M}{N1 \times N2}\right) = FIN \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)}\right)$$

Where,

$N1 = PLLPRE + 2$

$N2 = 2 \times (PLLPOST + 1)$

$M = PLLDIV + 2$

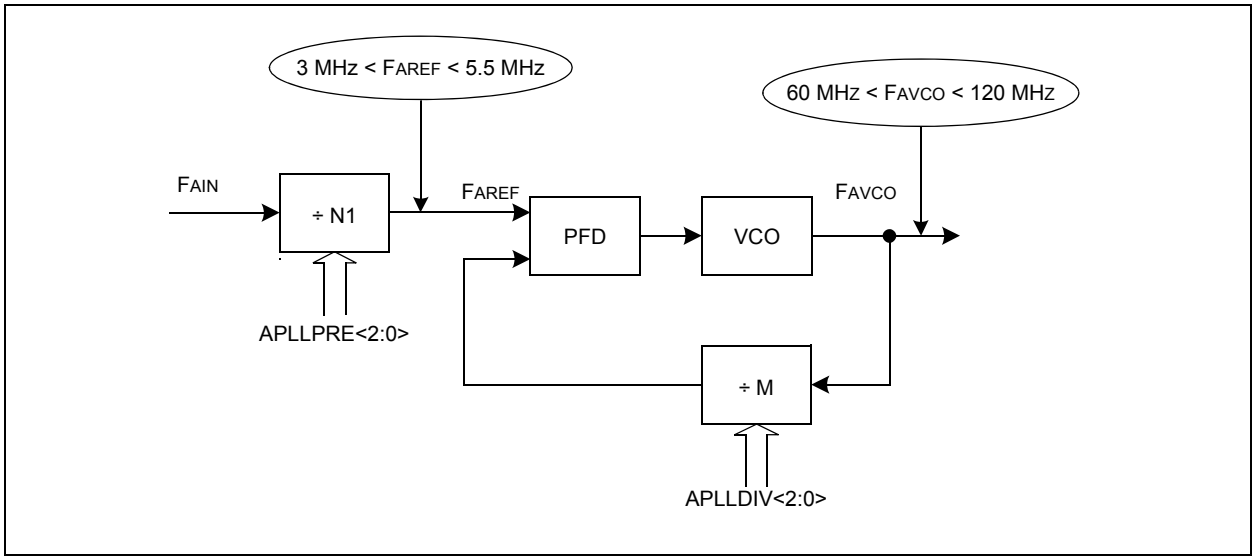
**EQUATION 9-3: FVCO CALCULATION**

$$FVCO = FIN \times \left(\frac{M}{N1}\right) = FIN \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)}\right)$$

Figure 9-3 illustrates a block diagram of the auxiliary PLL module.

| **Note:** | The auxiliary PLL module is only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices. |
|---|---|

**FIGURE 9-3: APLL BLOCK DIAGRAM**




Equation 9-4 shows the relationship between the auxiliary PLL input clock frequency (FAIN) and the AVCO frequency (FAVCO).

**EQUATION 9-4: FAVCO CALCULATION**

$$F_{AVCO} = F_{AIN} \times \left(\frac{M}{N1}\right)$$


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**TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION**

| Oscillator Mode | Oscillator Source | POSCMD<1:0> | FNOSC<2:0> | See Notes |
|---|---|---|---|---|
| Fast RC Oscillator with Divide-by-N (FRCDIVN) | Internal | xx | 111 | 1, 2 |
| Fast RC Oscillator with Divide-by-16 (FRCDIV16) | Internal | xx | 110 | 1 |
| Low-Power RC Oscillator (LPRC) | Internal | xx | 101 | 1 |
| Secondary (Timer1) Oscillator (SOSC) | Secondary | xx | 100 | 1 |
| Primary Oscillator (HS) with PLL (HSPLL) | Primary | 10 | 011 | — |
| Primary Oscillator (XT) with PLL (XTPLL) | Primary | 01 | 011 | — |
| Primary Oscillator (EC) with PLL (ECPLL) | Primary | 00 | 011 | 1 |
| Primary Oscillator (HS) | Primary | 10 | 010 | — |
| Primary Oscillator (XT) | Primary | 01 | 010 | — |
| Primary Oscillator (EC) | Primary | 00 | 010 | 1 |
| Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL) | Internal | xx | 001 | 1 |
| Fast RC Oscillator (FRC) | Internal | xx | 000 | 1 |

**Note 1:** OSC2 pin function is determined by the OSCIOFNC Configuration bit.

**2:** This is the default oscillator mode for an unprogrammed (erased) device.

## 9.2 Oscillator Resources

Many useful resources related to the Oscillator are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

### 9.2.1 KEY RESOURCES

- **Section 7. "Oscillator"** (DS70580) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 9.3 Oscillator Control Registers

**REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1,3)**

| U-0 | R-0 | R-0 | R-0 | U-0 | R/W-y | R/W-y | R/W-y |
|---|---|---|---|---|---|---|---|
| — | COSC<2:0> | | | — | NOSC<2:0>(2) | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R-0 | U-0 | R/C-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CLKLOCK | IOLOCK | LOCK | — | CF | — | LPOSCEN | OSWEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | y = Value Set from Configuration bits on POR | | C = Clearable bit |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits (read-only)
111 = Fast RC Oscillator (FRC) with Divide-by-N
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL
000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits(2)
111 = Fast RC Oscillator (FRC) with Divide-by-N
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL
000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit
1 = If (FCKSM0 = 1), then clock and PLL configurations are locked
If (FCKSM0 = 0), then clock and PLL configurations may be modified
0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 **IOLOCK:** I/O Lock Enable bit
1 = I/O lock is active
0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit (read-only)
1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

bit 4 **Unimplemented:** Read as '0'

**Note 1:** Writes to this register require an unlock sequence. Refer to **Section 7. "Oscillator"** (DS70580) in the *"dsPIC33E/PIC24E Family Reference Manual"* (available from the Microchip web site) for details.

**2:** Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

**3:** This register resets only on a Power-on Reset (POR).


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**REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1,3) (CONTINUED)**

bit 3 **CF:** Clock Fail Detect bit (read/clear by application)
1 = FSCM has detected clock failure
0 = FSCM has not detected clock failure

bit 2 **Unimplemented:** Read as '0'

bit 1 **LPOSCEN:** Secondary (LP) Oscillator Enable bit
1 = Enables Secondary Oscillator
0 = Disables Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Requests oscillator switch to selection specified by NOSC<2:0> bits
0 = Oscillator switch is complete

**Note 1:** Writes to this register require an unlock sequence. Refer to **Section 7. "Oscillator"** (DS70580) in the *"dsPIC33E/PIC24E Family Reference Manual"* (available from the Microchip web site) for details.

**2:** Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

**3:** This register resets only on a Power-on Reset (POR).

**REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER(2)**

| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ROI | DOZE<2:0>(3) | | | DOZEN(1,4) | FRCDIV<2:0> | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-1 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PLLPOST<1:0> | | — | PLLPRE<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | y = Value set from Configuration bits on POR | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts will clear the DOZEN bit and the processor clock and peripheral clock ratio is set to 1:1
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** Processor Clock Reduction Select bits(3)
111 = FCY divided by 128
110 = FCY divided by 64
101 = FCY divided by 32
100 = FCY divided by 16
011 = FCY divided by 8 (default)
010 = FCY divided by 4
001 = FCY divided by 2
000 = FCY divided by 1

bit 11 **DOZEN:** Doze Mode Enable bit(1,4)
1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks
0 = Processor clock and peripheral clock ratio forced to 1:1

bit 10-8 **FRCDIV<2:0>:** Internal Fast RC Oscillator Postscaler bits
111 = FRC divided by 256
110 = FRC divided by 64
101 = FRC divided by 32
100 = FRC divided by 16
011 = FRC divided by 8
010 = FRC divided by 4
001 = FRC divided by 2
000 = FRC divided by 1 (default)

bit 7-6 **PLLPOST<1:0>:** PLL VCO Output Divider Select bits (also denoted as 'N2', PLL postscaler)
11 = Output divided by 8
10 = Reserved
01 = Output divided by 4 (default)
00 = Output divided by 2

bit 5 **Unimplemented:** Read as '0'

**Note 1:** This bit is cleared when the ROI bit is set and an interrupt occurs.
**2:** This register resets only on a Power-on Reset (POR).
**3:** DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
**4:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.


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**REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER(2) (CONTINUED)**

bit 4-0 **PLLPRE<4:0>:** PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)
11111 = Input divided by 33
•
•
•
00001 = Input divided by 3
00000 = Input divided by 2 (default)

**Note 1:** This bit is cleared when the ROI bit is set and an interrupt occurs.

**2:** This register resets only on a Power-on Reset (POR).

**3:** DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.

**4:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

**REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | PLLDIV<8> |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PLLDIV<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

111111111 = 513
•
•
•
000110000 = 50 (default)
•
•
•
000000010 = 4
000000001 = 3
000000000 = 2

**Note 1:** This register is reset only on a Power-on Reset (POR).


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**REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | TUN<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits

011111 = Center frequency + 11.625% (8.23 MHz)
011110 = Center frequency + 11.25% (8.20 MHz)
•
•
•
000001 = Center frequency + 0.375% (7.40 MHz)
000000 = Center frequency (7.37 MHz nominal)
111111 = Center frequency – 0.375% (7.345 MHz)
•
•
•
100001 = Center frequency – 11.625% (6.52 MHz)
100000 = Center frequency – 12% (6.49 MHz)

**Note 1:** This register resets only on a Power-on Reset (POR).

**REGISTER 9-5: ACLKCON3: AUXILIARY CLOCK CONTROL REGISTER 3(1,2)**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| ENAPLL | — | SELACLK | AOSCMD<1:0> | | ASRCSEL | FRCSEL | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| APLLPOST<2:0> | | | — | — | APLLPRE<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ENAPLL:** Enable Auxiliary PLL (APLL) and Select APLL as USB Clock Source bit
1 = APLL is enabled, the USB clock source is the APLL output
0 = APLL is disabled, the USB clock source is the input clock to the APLL

bit 14 **Unimplemented:** Read as '0'

bit 13 **SELACLK:** Select Auxiliary Clock Source for Auxiliary Clock Divider bit
1 = Auxiliary PLL or oscillator provides the source clock for auxiliary clock divider
0 = Primary PLL provides the source clock for auxiliary clock divider

bit 12-11 **AOSCMD<1:0>:** Auxiliary Oscillator Mode bits
11 = EC (External Clock) Oscillator mode select
10 = XT (Crystal) Oscillator mode select
01 = HS (High-Speed) Oscillator mode select
00 = Auxiliary Oscillator disabled (default)

bit 10 **ASRCSEL:** Select Reference Clock Source for APLL bit
1 = Primary Oscillator is the clock source for APLL
0 = Auxiliary Oscillator is the clock source for APLL

bit 9 **FRCSEL:** Select FRC as Reference Clock Source for APLL bit
1 = FRC is the clock source for APLL
0 = Auxiliary Oscillator or Primary Oscillator is the clock source for APLL (determined by ASRCSEL bit)

bit 8 **Unimplemented:** Read as '0'

bit 7-5 **APLLPOST<2:0>:** Select PLL VCO Output Divider bits
111 = Divided by 1
110 = Divided by 2
101 = Divided by 4
100 = Divided by 8
011 = Divided by 16
010 = Divided by 32
001 = Divided by 64
000 = Divided by 256 (default)

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **APLLPRE<2:0>:** PLL Phase Detector Input Divider bits
111 = Divided by 12
110 = Divided by 10
101 = Divided by 6
100 = Divided by 5
011 = Divided by 4
010 = Divided by 3
001 = Divided by 2
000 = Divided by 1 (default)

**Note 1:** This register resets only on a Power-on Reset (POR).
**2:** This register is only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.


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**REGISTER 9-6: ACLKDIV3: AUXILIARY CLOCK DIVISOR REGISTER 3(1,2)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | APLLDIV<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **APLLDIV<2:0>:** PLL Feedback Divisor bits (PLL Multiplier Ratio)

111 = 24
110 = 21
101 = 20
100 = 19
011 = 18
010 = 17
001 = 16
000 = 15 (default)

**Note 1:** This register resets only on a Power-on Reset (POR).

**2:** This register is only available on dsPIC33EPXXXMU8XX and PIC24EPXXXGU8XX devices.

**REGISTER 9-7: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ROON | — | ROSSLP | ROSEL | RODIV<3:0>(1) | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ROON:** Reference Oscillator Output Enable bit
1 = Reference oscillator output is enabled on REFCLK pin(2)
0 = Reference oscillator output is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Run in Sleep bit
1 = Reference oscillator output continues to run in Sleep
0 = Reference oscillator output is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Oscillator crystal used as the reference clock
0 = System clock used as the reference clock

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divider bits(1)
1111 = Reference clock divided by 32,768
1110 = Reference clock divided by 16,384
1101 = Reference clock divided by 8,192
1100 = Reference clock divided by 4,096
1011 = Reference clock divided by 2,048
1010 = Reference clock divided by 1,024
1001 = Reference clock divided by 512
1000 = Reference clock divided by 256
0111 = Reference clock divided by 128
0110 = Reference clock divided by 64
0101 = Reference clock divided by 32
0100 = Reference clock divided by 16
0011 = Reference clock divided by 8
0010 = Reference clock divided by 4
0001 = Reference clock divided by 2
0000 = Reference clock

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
**2:** This pin is remappable. See **Section 11.4 "Peripheral Pin Select"** for more information.


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# 10.0 POWER-SAVING FEATURES

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70615) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power.

dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices can manage power consumption in four ways:

- Clock frequency
- Instruction-based Sleep and Idle modes
- Software-controlled Doze mode
- Selective peripheral control in software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

## 10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

## 10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices have two special power-saving modes that are entered through the execution of a special `PWRSAV` instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the `PWRSAV` instruction is shown in Example 10-1.

**Note:** `SLEEP_MODE` and `IDLE_MODE` are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to wake up.

### 10.2.1 SLEEP MODE

The following occur in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the input change notification on the I/O ports, or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of the these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

**EXAMPLE 10-1: `PWRSAV` INSTRUCTION SYNTAX**

```
PWRSAV  #SLEEP_MODE    ; Put the device into SLEEP mode
PWRSAV  #IDLE_MODE     ; Put the device into IDLE mode
```

### 10.2.2 IDLE MODE

The following occur in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.4 "Peripheral Module Disable"**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the `PWRSAV` instruction, or the first instruction in the ISR.

### 10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a `PWRSAV` instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

## 10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN module has been configured for 500 kbps based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

## 10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

| | |
|---|---|
| **Note:** | If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation). |


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## 10.5 Power-Saving Resources

Many useful resources related to Power-Saving features are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 10.5.1 KEY RESOURCES

- **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70615) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 10.6 Special Function Registers

Seven registers, PMD1: Peripheral Module Disable Control Register 1 through PMD7: Peripheral Module Disable Control Register 7, are provided for peripheral module control.

**REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| T5MD | T4MD | T3MD | T2MD | T1MD | QEI1MD(1) | PWMMD(1) | DCIMD |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | C2MD | C1MD | AD1MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **T5MD:** Timer5 Module Disable bit
1 = Timer5 module is disabled
0 = Timer5 module is enabled

bit 14 **T4MD:** Timer4 Module Disable bit
1 = Timer4 module is disabled
0 = Timer4 module is enabled

bit 13 **T3MD:** Timer3 Module Disable bit
1 = Timer3 module is disabled
0 = Timer3 module is enabled

bit 12 **T2MD:** Timer2 Module Disable bit
1 = Timer2 module is disabled
0 = Timer2 module is enabled

bit 11 **T1MD:** Timer1 Module Disable bit
1 = Timer1 module is disabled
0 = Timer1 module is enabled

bit 10 **QEI1MD:** QEI1 Module Disable bit(1)
1 = QEI1 module is disabled
0 = QEI1 module is enabled

bit 9 **PWMMD:** PWM Module Disable bit(1)
1 = PWM module is disabled
0 = PWM module is enabled

bit 8 **DCIMD:** DCI Module Disable bit
1 = DCI module is disabled
0 = DCI module is enabled

bit 7 **I2C1MD:** I2C1 Module Disable bit
1 = I2C1 module is disabled
0 = I2C1 module is enabled

bit 6 **U2MD:** UART2 Module Disable bit
1 = UART2 module is disabled
0 = UART2 module is enabled

bit 5 **U1MD:** UART1 Module Disable bit
1 = UART1 module is disabled
0 = UART1 module is enabled

bit 4 **SPI2MD:** SPI2 Module Disable bit
1 = SPI2 module is disabled
0 = SPI2 module is enabled

**Note 1:** This bit is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.


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**REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)**

bit 3 **SPI1MD:** SPI1 Module Disable bit
1 = SPI1 module is disabled
0 = SPI1 module is enabled

bit 2 **C2MD:** ECAN2 Module Disable bit
1 = ECAN2 module is disabled
0 = ECAN2 module is enabled

bit 1 **C1MD:** ECAN1 Module Disable bit
1 = ECAN1 module is disabled
0 = ECAN1 module is enabled

bit 0 **AD1MD:** ADC1 Module Disable bit
1 = ADC1 module is disabled
0 = ADC1 module is enabled

**Note 1:** This bit is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IC8MD | IC7MD | IC6MD | IC5MD | IC4MD | IC3MD | IC2MD | IC1MD |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OC8MD | OC7MD | OC6MD | OC5MD | OC4MD | OC3MD | OC2MD | OC1MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **IC8MD:** Input Capture 8 Module Disable bit
1 = Input Capture 8 module is disabled
0 = Input Capture 8 module is enabled

bit 14 **IC7MD:** Input Capture 2 Module Disable bit
1 = Input Capture 7 module is disabled
0 = Input Capture 7 module is enabled

bit 13 **IC6MD:** Input Capture 6 Module Disable bit
1 = Input Capture 6 module is disabled
0 = Input Capture 6 module is enabled

bit 12 **IC5MD:** Input Capture 5 Module Disable bit
1 = Input Capture 5 module is disabled
0 = Input Capture 5 module is enabled

bit 11 **IC4MD:** Input Capture 4 Module Disable bit
1 = Input Capture 4 module is disabled
0 = Input Capture 4 module is enabled

bit 10 **IC3MD:** Input Capture 3 Module Disable bit
1 = Input Capture 3 module is disabled
0 = Input Capture 3 module is enabled

bit 9 **IC2MD:** Input Capture 2 Module Disable bit
1 = Input Capture 2 module is disabled
0 = Input Capture 2 module is enabled

bit 8 **IC1MD:** Input Capture 1 Module Disable bit
1 = Input Capture 1 module is disabled
0 = Input Capture 1 module is enabled

bit 7 **OC8MD:** Output Compare 8 Module Disable bit
1 = Output Compare 8 module is disabled
0 = Output Compare 8 module is enabled

bit 6 **OC7MD:** Output Compare 7 Module Disable bit
1 = Output Compare 7 module is disabled
0 = Output Compare 7 module is enabled

bit 5 **OC6MD:** Output Compare 6 Module Disable bit
1 = Output Compare 6 module is disabled
0 = Output Compare 6 module is enabled

bit 4 **OC5MD:** Output Compare 5 Module Disable bit
1 = Output Compare 5 module is disabled
0 = Output Compare 5 module is enabled


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**REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2 (CONTINUED)**

bit 3 **OC4MD:** Output Compare 4 Module Disable bit
1 = Output Compare 4 module is disabled
0 = Output Compare 4 module is enabled

bit 2 **OC3MD:** Output Compare 3 Module Disable bit
1 = Output Compare 3 module is disabled
0 = Output Compare 3 module is enabled

bit 1 **OC2MD:** Output Compare 2 Module Disable bit
1 = Output Compare 2 module is disabled
0 = Output Compare 2 module is enabled

bit 0 **OC1MD:** Output Compare 1 Module Disable bit
1 = Output Compare 1 module is disabled
0 = Output Compare 1 module is enabled

**REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| T9MD | T8MD | T7MD | T6MD | — | CMPMD | RTCCMD | PMPMD |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CRCMD | — | QEI2MD(1) | — | U3MD | — | I2C2MD | AD2MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **T9MD:** Timer9 Module Disable bit
1 = Timer9 module is disabled
0 = Timer9 module is enabled

bit 14 **T8MD:** Timer8 Module Disable bit
1 = Timer8 module is disabled
0 = Timer8 module is enabled

bit 13 **T7MD:** Timer7 Module Disable bit
1 = Timer7 module is disabled
0 = Timer7 module is enabled

bit 12 **T6MD:** Timer6 Module Disable bit
1 = Timer6 module is disabled
0 = Timer6 module is enabled

bit 11 **Unimplemented:** Read as '0'

bit 10 **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled

bit 9 **RTCCMD:** RTCC Module Disable bit
1 = RTCC module is disabled
0 = RTCC module is enabled

bit 8 **PMPMD:** PMP Module Disable bit
1 = PMP module is disabled
0 = PMP module is enabled

bit 7 **CRCMD:** CRC Module Disable bit
1 = CRC module is disabled
0 = CRC module is enabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **QEI2MD:** QEI2 Module Disable bit(1)
1 = QEI2 module is disabled
0 = QEI2 module is enabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **U3MD:** UART3 Module Disable bit
1 = UART3 module is disabled
0 = UART3 module is enabled

bit 2 **Unimplemented:** Read as '0'

**Note 1:** This bit is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.


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bit 1 **I2C2MD:** I2C2 Module Disable bit
1 = I2C2 module is disabled
0 = I2C2 module is enabled

bit 0 **AD2MD:** ADC2 Module Disable bit
1 = ADC2 module is disabled
0 = ADC2 module is enabled

**Note 1:** This bit is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**REGISTER 10-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | U4MD | — | REFOMD | — | — | USB1MD(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **U4MD:** UART4 Module Disable bit
1 = UART4 module is disabled
0 = UART4 module is enabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **REFOMD:** Reference Clock Module Disable bit
1 = Reference clock module is disabled
0 = Reference clock module is enabled

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **USB1MD:** USB Module Disable bit(1)
1 = USB module is disabled
0 = USB module is enabled

**Note 1:** This bit is only available on dsPIC33EPXXXMU8XXX and PIC24EPXXXGU8XX devices.


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**REGISTER 10-5: PMD5: PERIPHERAL MODULE DISABLE CONTROL REGISTER 5**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IC16MD | IC15MD | IC14MD | IC13MD | IC12MD | IC11MD | IC10MD | IC9MD |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OC16MD | OC15MD | OC14MD | OC13MD | OC12MD | OC11MD | OC10MD | OC9MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **IC16MD:** IC16 Module Disable bit
1 = IC16 module is disabled
0 = IC16 module is enabled

bit 14 **IC15MD:** IC15 Module Disable bit
1 = IC15 module is disabled
0 = IC15 module is enabled

bit 13 **IC14MD:** IC14 Module Disable bit
1 = IC14 module is disabled
0 = IC14 module is enabled

bit 12 **IC13MD:** IC13 Module Disable bit
1 = IC13 module is disabled
0 = IC13 module is enabled

bit 11 **IC12MD:** IC12 Module Disable bit
1 = IC12 module is disabled
0 = IC12 module is enabled

bit 10 **IC11MD:** IC11 Module Disable bit
1 = IC11 module is disabled
0 = IC11 module is enabled

bit 9 **IC10MD:** IC10 Module Disable bit
1 = IC10 module is disabled
0 = IC10 module is enabled

bit 8 **IC9MD:** IC9 Module Disable bit
1 = IC9 module is disabled
0 = IC9 module is enabled

bit 7 **OC16MD:** OC16 Module Disable bit
1 = OC16 module is disabled
0 = OC16 module is enabled

bit 6 **OC15MD:** OC15 Module Disable bit
1 = OC15 module is disabled
0 = OC15 module is enabled

bit 5 **OC14MD:** OC14 Module Disable bit
1 = OC14 module is disabled
0 = OC14 module is enabled

bit 4 **OC13MD:** OC13 Module Disable bit
1 = OC13 module is disabled
0 = OC13 module is enabled

**REGISTER 10-5: PMD5: PERIPHERAL MODULE DISABLE CONTROL REGISTER 5 (CONTINUED)**

bit 3 **OC12MD:** OC12 Module Disable bit
1 = OC12 module is disabled
0 = OC12 module is enabled

bit 2 **OC11MD:** OC11 Module Disable bit
1 = OC11 module is disabled
0 = OC11 module is enabled

bit 1 **OC10MD:** OC10 Module Disable bit
1 = OC10 module is disabled
0 = OC10 module is enabled

bit 0 **OC9MD:** OC9 Module Disable bit
1 = OC9 module is disabled
0 = OC9 module is enabled


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**REGISTER 10-6: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | PWM7MD(1) | PWM6MD(1) | PWM5MD(1) | PWM4MD(1) | PWM3MD(1) | PWM2MD(1) | PWM1MD(1) |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | SPI4MD | SPI3MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14 **PWM7MD:** PWM7 Module Disable bit(1)
1 = PWM7 module is disabled
0 = PWM7 module is enabled

bit 13 **PWM6MD:** PWM6 Module Disable bit(1)
1 = PWM6 module is disabled
0 = PWM6 module is enabled

bit 12 **PWM5MD:** PWM5 Module Disable bit(1)
1 = PWM5 module is disabled
0 = PWM5 module is enabled

bit 11 **PWM4MD:** PWM4 Module Disable bit(1)
1 = PWM4 module is disabled
0 = PWM4 module is enabled

bit 10 **PWM3MD:** PWM3 Module Disable bit(1)
1 = PWM3 module is disabled
0 = PWM3 module is enabled

bit 9 **PWM2MD:** PWM2 Module Disable bit(1)
1 = PWM2 module is disabled
0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit(1)
1 = PWM1 module is disabled
0 = PWM1 module is enabled

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **SPI4MD:** SPI4 Module Disable bit
1 = SPI4 module is disabled
0 = SPI4 module is enabled

bit 0 **SPI3MD:** SPI3 Module Disable bit
1 = SPI3 module is disabled
0 = SPI3 module is enabled

**Note 1:** This bit is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**REGISTER 10-7: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| DMA12MD | DMA8MD | DMA4MD | DMA0MD | — | — | — | — |
| DMA13MD | DMA9MD | DMA5MD | DMA1MD | | | | |
| DMA14MD | DMA10MD | DMA6MD | DMA2MD | | | | |
| — | DMA11MD | DMA7MD | DMA3MD | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **DMA12MD:** DMA12 Module Disable bit
1 = DMA12 module is disabled
0 = DMA12 module is enabled

**DMA13MD:** DMA13 Module Disable bit
1 = DMA13 module is disabled
0 = DMA13 module is enabled

**DMA14MD:** DMA14 Module Disable bit
1 = DMA14 module is disabled
0 = DMA14 module is enabled

bit 6 **DMA8MD:** DMA3 Module Disable bit
1 = DMA8 module is disabled
0 = DMA8 module is enabled

**DMA9MD:** DMA2 Module Disable bit
1 = DMA9 module is disabled
0 = DMA9 module is enabled

**DMA10MD:** DMA10 Module Disable bit
1 = DMA10 module is disabled
0 = DMA10 module is enabled

**DMA11MD:** DMA11 Module Disable bit
1 = DMA11 module is disabled
0 = DMA11 module is enabled

bit 5 **DMA4MD:** DMA4 Module Disable bit
1 = DMA4 module is disabled
0 = DMA4 module is enabled

**DMA5MD:** DMA5 Module Disable bit
1 = DMA5 module is disabled
0 = DMA5 module is enabled

**DMA6MD:** DMA6 Module Disable bit
1 = DMA6 module is disabled
0 = DMA6 module is enabled

**DMA7MD:** DMA7 Module Disable bit
1 = DMA7 module is disabled
0 = DMA7 module is enabled


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**REGISTER 10-7: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7 (CONTINUED)**

bit 4 **DMA0MD:** DMA0 Module Disable bit
1 = DMA0 module is disabled
0 = DMA0 module is enabled

**DMA1MD:** DMA1 Module Disable bit
1 = DMA1 module is disabled
0 = DMA1 module is enabled

**DMA2MD:** DMA2 Module Disable bit
1 = DMA2 module is disabled
0 = DMA2 module is enabled

**DMA3MD:** DMA3 Module Disable bit
1 = DMA3 module is disabled
0 = DMA3 module is enabled

bit 3-0 **Unimplemented:** Read as '0'

**NOTES:**


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## 11.0 I/O PORTS

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "I/O Ports"** (DS70598) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

All of the device pins (except VDD, VSS, MCLR and OSC1/CLKI) are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

### 11.1 Parallel I/O (PIO) Ports

Generally, a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through," in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

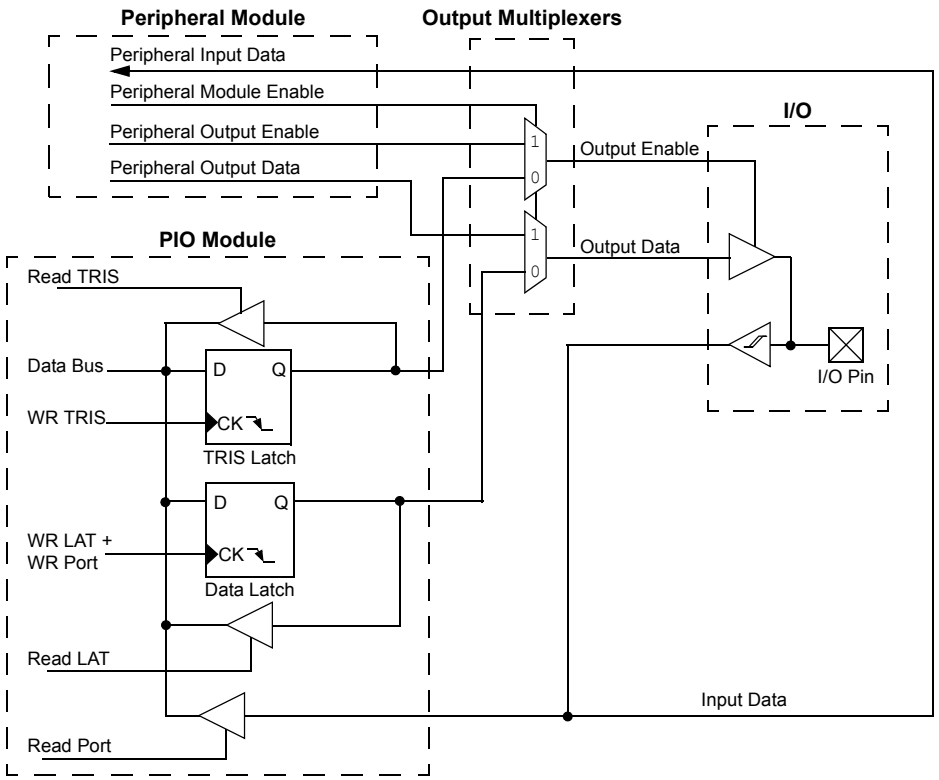
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have eight registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device is disabled. This means the corresponding LATx and TRISx registers and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

**FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE**





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### 11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V on a 5V tolerant pin) by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification for that pin.

See the **"Pin Diagrams"** section for the available pins and their functionality.

## 11.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default. Refer to the Pinout I/O Descriptions (Table 1-1 in **Section 1.0 "Device Overview"**) for the complete list of analog pins.

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the pins defined as Analog in Table 1-1 in **Section 1.0 "Device Overview"**) can cause the input buffer to consume current that exceeds the device specifications.

### 11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be an NOP, as shown in Example 11-1.

## 11.3 Input Change Notification

The input change notification function of the I/O ports allows the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the CN functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

| **Note:** | Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output. |
|---|---|

**EXAMPLE 11-1: PORT WRITE/READ EXAMPLE**

```
MOV    0xFF00, W0    ; Configure PORTB<15:8>
                     ; as inputs
MOV    W0, TRISB     ; and PORTB<7:0>
                     ; as outputs
NOP                  ; Delay 1 cycle
BTSS   PORTB, #13    ; Next Instruction
```

## 11.4 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Peripheral Pin Select is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

### 11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the designation “RPn” or “RPIn” in their full pin designation, where “RP” designates a remappable function for input or output and “RPI” designates a remappable functions for input only, and “n” is the remappable pin number.

### 11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include $I^2C$ and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

### 11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

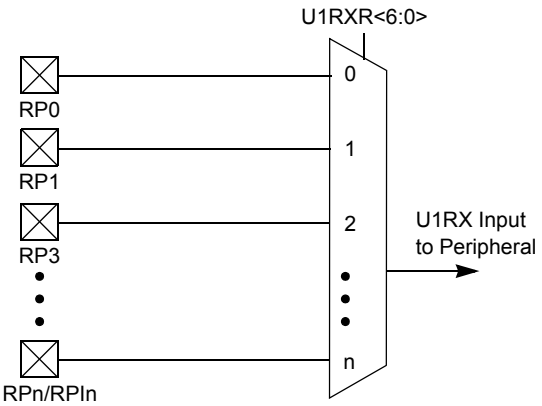
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

### 11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-22). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals (see Table 11-1). Programming a given peripheral’s bit field with an appropriate 7-bit value maps the RPn/RPIn pin with the corresponding value to that peripheral (see Table 11-2). For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

**FIGURE 11-2: U1RX REMAPPABLE INPUT**




**Note:** For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring RPn/RPIn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to ‘1’).


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**TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)**

| Input Name(1) | Function Name | Register | Configuration Bits |
|---|---|---|---|
| External Interrupt 1 | INT1 | RPINR0 | INT1R<6:0> |
| External Interrupt 2 | INT2 | RPINR1 | INT2R<6:0> |
| External Interrupt 3 | INT3 | RPINR1 | INT3R<6:0> |
| External Interrupt 4 | INT4 | RPINR2 | INT4R<6:0> |
| Timer2 External Clock | T2CK | RPINR3 | T2CKR<6:0> |
| Timer3 External Clock | T3CK | RPINR3 | T3CKR<6:0> |
| Timer4 External Clock | T4CK | RPINR4 | T4CKR<6:0> |
| Timer5 External Clock | T5CK | RPINR4 | T5CKR<6:0> |
| Timer6 External Clock | T6CK | RPINR5 | T6CKR<6:0> |
| Timer7 External Clock | T7CK | RPINR5 | T7CKR<6:0> |
| Timer8 External Clock | T8CK | RPINR6 | T8CKR<6:0> |
| Timer9 External Clock | T9CK | RPINR6 | T9CKR<6:0> |
| Input Capture 1 | IC1 | RPINR7 | IC1R<6:0> |
| Input Capture 2 | IC2 | RPINR7 | IC2R<6:0> |
| Input Capture 3 | IC3 | RPINR8 | IC3R<6:0> |
| Input Capture 4 | IC4 | RPINR8 | IC4R<6:0> |
| Input Capture 5 | IC5 | RPINR9 | IC5R<6:0> |
| Input Capture 6 | IC6 | RPINR9 | IC6R<6:0> |
| Input Capture 7 | IC7 | RPINR10 | IC7R<6:0> |
| Input Capture 8 | IC8 | RPINR10 | IC8R<6:0> |
| Output Compare Fault A | OCFA | RPINR11 | OCFAR<6:0> |
| Output Compare Fault B | OCFB | RPINR11 | OCFBR<6:0> |
| PMW Fault 1(2) | FLT1 | RPINR12 | FLT1R<6:0> |
| PMW Fault 2(2) | FLT2 | RPINR12 | FLT2R<6:0> |
| PMW Fault 3(2) | FLT3 | RPINR13 | FLT3R<6:0> |
| PMW Fault 4(2) | FLT4 | RPINR13 | FLT4R<6:0> |
| QEI1 Phase A(2) | QEA1 | RPINR14 | QEA1R<6:0> |
| QEI1 Phase A(2) | QEB1 | RPINR14 | QEB1R<6:0> |
| QEI1 Index(2) | INDX1 | RPINR15 | INDX1R<6:0> |
| QEI1 Home(2) | HOME1 | RPINR15 | HOM1R<6:0> |
| QEI2 Phase A(2) | QEA2 | RPINR16 | QEA2R<6:0> |
| QEI2 Phase A(2) | QEB2 | RPINR16 | QEB2R<6:0> |
| QEI2 Index(2) | INDX2 | RPINR17 | INDX2R<6:0> |
| QEI2 Home(2) | HOME2 | RPINR17 | HOM2R<6:0> |
| UART1 Receive | U1RX | RPINR18 | U1RXR<6:0> |
| UART1 Clear-to-Send | $\overline{\text{U1CTS}}$ | RPINR18 | U1CTSR<6:0> |
| UART2 Receive | U2RX | RPINR19 | U2RXR<6:0> |
| UART2 Clear-to-Send | $\overline{\text{U2CTS}}$ | RPINR19 | U2CTSR<6:0> |
| SPI1 Data Input | SDI1 | RPINR20 | SDI1R<6:0> |
| SPI1 Clock Input | SCK1 | RPINR20 | SCK1R<6:0> |
| SPI1 Slave Select | $\overline{\text{SS1}}$ | RPINR21 | SS1R<6:0> |
| SPI2 Slave Select | $\overline{\text{SS2}}$ | RPINR23 | SS2R<6:0> |

**Note 1:** Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

**2:** This input source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION) (CONTINUED)**

| Input Name(1) | Function Name | Register | Configuration Bits |
|---|---|---|---|
| DCI Data Input | CSDI | RPINR24 | CSDIR<6:0> |
| DCI Clock Input | CSCKIN | RPINR24 | CSCKR<6:0> |
| DCI FSYNC Input | COFSIN | RPINR25 | COFSR<6:0> |
| CAN1 Receive | C1RX | RPINR26 | C1RXR<6:0> |
| CAN2 Receive | C2RX | RPINR26 | C2RXR<6:0> |
| UART3 Receive | U3RX | RPINR27 | U3RXR<6:0> |
| UART3 Clear-to-Send | $\overline{\text{U3CTS}}$ | RPINR27 | U3CTSR<6:0> |
| UART4 Receive | U4RX | RPINR28 | U4RXR<6:0> |
| UART4 Clear-to-Send | $\overline{\text{U4CTS}}$ | RPINR28 | U4CTSR<6:0> |
| SPI3 Data Input | SDI3 | RPINR29 | SDI3R<6:0> |
| SPI3 Clock Input | SCK3 | RPINR29 | SCK3R<6:0> |
| SPI3 Slave Select | $\overline{\text{SS3}}$ | RPINR30 | SS3R<6:0> |
| SPI4 Data Input | SDI4 | RPINR31 | SDI4R<6:0> |
| SPI4 Clock Input | SCK4 | RPINR31 | SCK4R<6:0> |
| SPI4 Slave Select | $\overline{\text{SS4}}$ | RPINR32 | SS4R<6:0> |
| Input Capture 9 | IC9 | RPINR33 | IC9R<6:0> |
| Input Capture 10 | IC10 | RPINR33 | IC10R<6:0> |
| Input Capture 11 | IC11 | RPINR34 | IC11R<6:0> |
| Input Capture 12 | IC12 | RPINR34 | IC12R<6:0> |
| Input Capture 13 | IC13 | RPINR35 | IC13R<6:0> |
| Input Capture 14 | IC14 | RPINR35 | IC14R<6:0> |
| Input Capture 15 | IC15 | RPINR36 | IC15R<6:0> |
| Input Capture 16 | IC16 | RPINR36 | IC16R<6:0> |
| Output Compare Fault C | OCFC | RPINR37 | OCFCR<6:0> |
| PWM Fault 5(2) | FLT5 | RPINR42 | FLT5R<6:0> |
| PWM Fault 6(2) | FLT6 | RPINR42 | FLT6R<6:0> |
| PWM Fault 7(2) | FLT7 | RPINR43 | FLT7R<6:0> |
| PWM Dead-Time Compensation 1(2) | DTCMP1 | RPINR38 | DTCMP1R<6:0> |
| PWM Dead-Time Compensation 2(2) | DTCMP2 | RPINR39 | DTCMP2R<6:0> |
| PWM Dead-Time Compensation 3(2) | DTCMP3 | RPINR39 | DTCMP3R<6:0> |
| PWM Dead-Time Compensation 4(2) | DTCMP4 | RPINR40 | DTCMP4R<6:0> |
| PWM Dead-Time Compensation 5(2) | DTCMP5 | RPINR40 | DTCMP5R<6:0> |
| PWM Dead-Time Compensation 6(2) | DTCMP6 | RPINR41 | DTCMP6R<6:0> |
| PWM Dead-Time Compensation 7(2) | DTCMP7 | RPINR41 | DTCMP7R<6:0> |
| PWM Synch Input 1(2) | SYNCI1 | RPINR37 | SYNCI1R<6:0> |
| PWM Synch Input 2(2) | SYNCI2 | RPINR38 | SYNCI2R<6:0> |

**Note 1:** Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

**2:** This input source is available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.


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**TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES**

| Peripheral Pin Select Input Register Value | Input/ Output | Pin Assignment |
|---|---|---|
| 000 0000 | I | Vss |
| 000 0001 | I | C1OUT(1) |
| 000 0010 | I | C2OUT(1) |
| 000 0011 | I | C3OUT(1) |
| 000 0100 | — | Reserved |
| 000 0101 | — | Reserved |
| 000 0110 | — | Reserved |
| 000 0111 | — | Reserved |
| 000 1000 | I | FINDX1(1) |
| 000 1001 | I | FHOME1(1) |
| 000 1010 | I | FINDX2(1) |
| 000 1011 | I | FHOME2(1) |
| 000 1100 | — | Reserved |
| 000 1101 | — | Reserved |
| 000 1110 | — | Reserved |
| 000 1111 | — | Reserved |
| 001 0000 | I | RPI16 |
| 001 0001 | I | RPI17 |
| 001 0010 | I | RPI18 |
| 001 0011 | I | RPI19 |
| 001 0100 | I | RPI20 |
| 001 0101 | I | RPI21 |
| 001 0110 | I | RPI22 |
| 001 0111 | I | RPI23 |
| 001 1000 | — | Reserved |
| 001 1001 | — | Reserved |
| 001 1010 | — | Reserved |
| 001 1011 | — | Reserved |
| 001 1100 | — | Reserved |
| 001 1101 | — | Reserved |
| 001 1110 | I | RPI30 |
| 001 1111 | I | RPI31 |
| 010 0000 | I | RPI32 |
| 010 0001 | I | RPI33 |
| 010 0010 | I | RPI34 |
| 010 0011 | I | RPI35 |
| 010 0100 | I | RPI36 |
| 010 0101 | I | RPI37 |
| 010 0110 | I | RPI38 |
| 010 0111 | I | RPI39 |
| 010 1000 | I | RPI40 |
| 010 1001 | I | RPI41 |
| 010 1010 | I | RPI42 |
| 010 1101 | I | RPI45 |
| 010 1110 | I | RPI46 |
| 010 1111 | I | RPI47 |
| 011 0000 | — | Reserved |
| 011 0001 | I | RPI49 |
| 011 0010 | I | RPI50 |
| 011 0011 | I | RPI51 |
| 011 0100 | I | RPI52 |
| 011 0101 | — | Reserved |
| 011 0110 | — | Reserved |
| 011 0111 | — | Reserved |
| 011 1000 | — | Reserved |
| 011 1001 | — | Reserved |
| 011 1010 | — | Reserved |
| 011 1011 | — | Reserved |
| 011 1100 | I | RPI60 |
| 011 1101 | I | RPI61 |
| 011 1110 | I | RPI62 |
| 011 1111 | — | Reserved |
| 100 0000 | I/O | RP64 |
| 100 0001 | I/O | RP65 |
| 100 0010 | I/O | RP66 |
| 100 0011 | I/O | RP67 |
| 100 0100 | I/O | RP68 |
| 100 0101 | I/O | RP69 |
| 100 0110 | I/O | RP70 |
| 100 0111 | I/O | RP71 |
| 100 1000 | I | RPI72 |
| 100 1001 | I | RPI73 |
| 100 1010 | I | RPI74 |
| 100 1011 | I | RPI75 |
| 100 1100 | I | RPI76 |
| 100 1101 | I | RPI77 |
| 100 1110 | I | RPI78 |
| 100 1111 | I/O | RP79 |
| 101 0000 | I/O | RP80 |
| 101 0001 | I | RPI81 |
| 101 0010 | I/O | RP82 |
| 101 0011 | I | RPI83 |
| 101 0100 | I/O | RP84 |
| 101 0101 | I/O | RP85 |
| 101 0110 | I | RPI86 |
| 101 0111 | I/O | RP87 |

**Note 1:** See **Section 11.4.4.2 "Virtual Connections"** for more information on selecting this pin assignment.

**TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES (CONTINUED)**

| Peripheral Pin Select Input Register Value | Input/ Output | Pin Assignment |
|---|---|---|
| 010 1011 | I | RPI43 |
| 010 1100 | I | RPI44 |
| 101 1010 | — | Reserved |
| 101 1011 | — | Reserved |
| 101 1100 | — | Reserved |
| 101 1101 | — | Reserved |
| 101 1110 | — | Reserved |
| 101 1111 | — | Reserved |
| 110 0000 | I/O | RP96 |
| 110 0001 | I/O | RP97 |
| 110 0010 | I/O | RP98 |
| 110 0011 | I/O | RP99 |
| 110 0100 | I/O | RP100 |
| 110 0101 | I/O | RP101 |
| 110 0110 | I/O | RP102 |
| 110 0111 | — | Reserved |
| 110 1000 | I/O | RP104 |
| 110 1001 | — | Reserved |
| 110 1010 | — | Reserved |
| 110 1011 | — | Reserved |
| 110 1100 | I/O | RP108 |

| Peripheral Pin Select Input Register Value | Input/ Output | Pin Assignment |
|---|---|---|
| 101 1000 | I | RPI88 |
| 101 1001 | I | RPI89 |
| 110 1101 | I/O | RP109 |
| 110 1110 | — | Reserved |
| 110 1111 | — | Reserved |
| 111 0000 | I/O | RP112 |
| 111 0001 | I/O | RP113 |
| 111 0010 | — | Reserved |
| 111 0011 | — | Reserved |
| 111 0100 | — | Reserved |
| 111 0101 | — | Reserved |
| 111 0110 | I/O | RP118 |
| 111 0111 | I | RPI119 |
| 111 1000 | I/O | RP120 |
| 111 1001 | I | RPI121 |
| 111 1010 | — | Reserved |
| 111 1011 | — | Reserved |
| 111 1100 | I | RPI124 |
| 111 1101 | I/O | RP125 |
| 111 1110 | I/O | RP126 |
| 111 1111 | I/O | RP127 |

**Note 1:** See **Section 11.4.4.2 “Virtual Connections”** for more information on selecting this pin assignment.


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#### 11.4.4.1 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6 bit fields, with each set associated with one RPn pin (see Register 11-44 through Register 11-51). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the Output Register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

**FIGURE 11-3: MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPn**

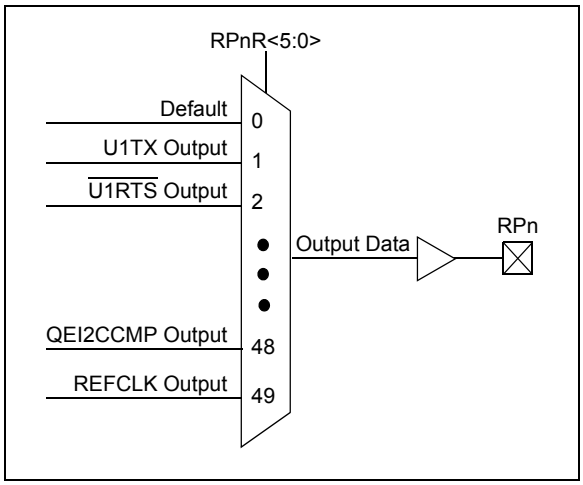


**TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)**

| Function | RPnR<5:0> | Output Name |
|---|---|---|
| DEFAULT PORT | 000000 | RPn tied to Default Pin |
| U1TX | 000001 | RPn tied to UART1 Transmit |
| $\overline{\text{U1RTS}}$ | 000010 | RPn tied to UART1 Ready-to-Send |
| U2TX | 000011 | RPn tied to UART2 Transmit |
| $\overline{\text{U2RTS}}$ | 000100 | RPn tied to UART2 Ready-to-Send |
| SDO1 | 000101 | RPn tied to SPI1 Data Output |
| SCK1 | 000110 | RPn tied to SPI1 Clock Output |
| $\overline{\text{SS1}}$ | 000111 | RPn tied to SPI1 Slave Select |
| $\overline{\text{SS2}}$ | 001010 | RPn tied to SPI2 Slave Select |
| CSDO | 001011 | RPn tied to DCI Data Output |
| CSCK | 001100 | RPn tied to DCI Clock Output |
| COFS | 001101 | RPn tied to DCI FSYNC Output |
| C1TX | 001110 | RPn tied to CAN1 Transmit |
| C2TX | 001111 | RPn tied to CAN2 Transmit |
| OC1 | 010000 | RPn tied to Output Compare 1 Output |
| OC2 | 010001 | RPn tied to Output Compare 2 Output |
| OC3 | 010010 | RPn tied to Output Compare 3 Output |
| OC4 | 010011 | RPn tied to Output Compare 4 Output |
| OC5 | 010100 | RPn tied to Output Compare 5 Output |
| OC6 | 010101 | RPn tied to Output Compare 6 Output |
| OC7 | 010110 | RPn tied to Output Compare 7 Output |
| OC8 | 010111 | RPn tied to Output Compare 8 Output |
| C1OUT | 011000 | RPn tied to Comparator Output 1 |
| C2OUT | 011001 | RPn tied to Comparator Output 2 |
| C3OUT | 011010 | RPn tied to Comparator Output 3 |
| U3TX | 011011 | RPn tied to UART3 Transmit |
| $\overline{\text{U3RTS}}$ | 011100 | RPn tied to UART3 Ready-to-Send |

**Note 1:** This function is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn) (CONTINUED)**

| Function | RPnR<5:0> | Output Name |
|---|---|---|
| U4TX | 011101 | RPn tied to UART4 Transmit |
| $\overline{\text{U4RTS}}$ | 011110 | RPn tied to UART4 Ready-to-Send |
| SDO3 | 011111 | RPn tied to SPI3 Data Output |
| SCK3 | 100000 | RPn tied to SPI3 Clock Output |
| $\overline{\text{SS3}}$ | 100001 | RPn tied to SPI3 Slave Select |
| SDO4 | 100010 | RPn tied to SPI4 Data Output |
| SCK4 | 100011 | RPn tied to SPI4 Clock Output |
| $\overline{\text{SS4}}$ | 100100 | RPn tied to SPI4 Slave Select |
| OC9 | 100101 | RPn tied to Output Compare 9 Output |
| OC10 | 100110 | RPn tied to Output Compare 10 Output |
| OC11 | 100111 | RPn tied to Output Compare 11 Output |
| OC12 | 101000 | RPn tied to Output Compare 12 Output |
| OC13 | 101001 | RPn tied to Output Compare 13 Output |
| OC14 | 101010 | RPn tied to Output Compare 14 Output |
| OC15 | 101011 | RPn tied to Output Compare 15 Output |
| OC16 | 101100 | RPn tied to Output Compare 16 Output |
| SYNCO1(1) | 101101 | RPn tied to PWM Primary Time Base Sync Output |
| SYNCO2(1) | 101110 | RPn tied to PWM Secondary Time Base Sync Output |
| QEI1CCMP(1) | 101111 | RPn tied to QEI 1 Counter Comparator Output |
| QEI2CCMP(1) | 110000 | RPn tied to QEI 2 Counter Comparator Output |
| REFCLK | 110001 | RPn tied to Reference Clock Output |

**Note 1:** This function is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.


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#### 11.4.4.2 Virtual Connections

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices support virtual (internal) connections to the output of the comparator modules, CMP1OUT, CMP2OUT and CMP3OUT (see Figure 25-1 in **Section 25.0 "Comparator Module"**). In addition, dsPIC33EPXXXMU806/810/814 devices support virtual connections to the filtered QEI module inputs, FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in **Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXX(MC/MU)8XX Devices Only)"**.

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of 'b0000001, the output of the analog comparator, CMP1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEI module allows peripherals to be connected to the QEI digital filter input. To utilize this filter, the QEI module must be enabled, and its inputs must be connected to a physical RPn/RPIn pin. Example 11-2 illustrates how the input capture module can be connected to the QEI digital filter.

#### 11.4.4.3 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn/RPIn pins is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

**EXAMPLE 11-2: CONNECTING IC1 TO HOME1 DIGITAL FILTER INPUT ON PIN 3 OF THE dsPIC33EP512MU810 DEVICE**

```
RPINR15 = 0x5600;      /* Connect the QEI1 HOME1 input to RP86 (pin 3) */
RPINR7 = 0x009;        /* Connect the IC1 input to the digital filter on the FHOME1 input */

QEI1IOC = 0x4000;      /* Enable the QEI digital filter */
QEI1CON = 0x8000;      /* Enable the QEI module */
```

## 11.5 I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 32-9 in **Section 32.0 "Electrical Characteristics"** under "Injection Current", have internal protection diodes to VDD and VSS; the term "Injection Current" is also referred to as "Clamp Current". On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin, (i.e., ANx, see Table 1-1 in **Section 1.0 "Device Overview"**), are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin, automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared analog pin (see Table 1-1 in **Section 1.0 "Device Overview"**), the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.

| **Note:** | Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver. |
|---|---|

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in the data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left to right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1; this indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin. Dedicated peripheral functions are always higher priority than remappable functions. I/O pins are always the lowest priority.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD-0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of the data sheet. For example:

   VOH = 2.4v @ IOH = -8 mA and VDD = 3.3V

   The maximum output current sourced by any 8 mA I/O pin = 12 mA.

   LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in **Section 32.0 "Electrical Characteristics"** for additional information.
6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
   a) Only one "output" function can be active on a given pin at any time regardless if it is a dedicated or remappable function (one pin, one output).
   b) It is possible to assign a "remappable output" function to multiple pins and externally short or tie them together for increased current drive.
   c) If any "dedicated output" function is enabled on a pin, it will take precedence over any remappable "output" function.
   d) If any "dedicated digital" (input or output) function is enabled on a pin, any number of "input" remappable functions can be mapped to the same pin.
   e) If any "dedicated analog" function(s) are enabled on a given pin, "digital input(s)" of any kind will all be disabled, although a single "digital output", at the user's cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input, provided there is no external analog input, such as for a built-in self test.
   f) Any number of "input" remappable functions can be mapped to the same pin(s) at the same time, including any pin with a single output from either a dedicated or remappable "output".


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g) The TRIS registers control *only* the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRIS setting. The TRIS register *does not* control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRIS settings, which means that the TRIS bit must be set to input for pins with only remappable input function(s) assigned.

h) All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin is disabled. Only the Analog Pin Select registers control the digital input buffer, *not* the TRIS register. The user must disable the analog function on a pin using the Analog Pin Select registers in order to use any “digital input(s)” on a corresponding pin, no exceptions.

## 11.6 I/O Resources

Many useful resources related to I/O are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554301

### 11.6.1 KEY RESOURCES

- **Section 10. “I/O Ports”** (DS70598) in the *“dsPIC33E/PIC24E Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *“dsPIC33E/PIC24E Family Reference Manual”* Sections
- Development Tools

## 11.7 Peripheral Pin Select Control Registers

**REGISTER 11-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | INT1R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **INT1R<6:0>:** Assign External Interrupt 1 (INT1) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'


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**REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | INT3R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | INT2R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **INT3R<6:0>:** Assign External Interrupt 3 (INT3) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **INT2R<6:0>:** Assign External Interrupt 2 (INT2) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-3: RPINR2: PERIPHERAL PIN SELECT INPUT REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | INT4R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **INT4R<6:0>:** Assign External Interrupt 4 (INT4) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-4: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T3CKR<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T2CKR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **T3CKR<6:0>:** Assign Timer3 External Clock (T3CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **T2CKR<6:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-5: RPINR4: PERIPHERAL PIN SELECT INPUT REGISTER 4**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T5CKR<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T4CKR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **T5CKR<6:0>:** Assign Timer5 External Clock (T5CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **T4CKR<6:0>:** Assign Timer4 External Clock (T4CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-6: RPINR5: PERIPHERAL PIN SELECT INPUT REGISTER 5**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T7CKR<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T6CKR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **T7CKR<6:0>:** Assign Timer7 External Clock (T7CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **T6CKR<6:0>:** Assign Timer6 External Clock (T6CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-7: RPINR6: PERIPHERAL PIN SELECT INPUT REGISTER 6**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T9CKR<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T8CKR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **T9CKR<6:0>:** Assign Timer9 External Clock (T9CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **T8CKR<6:0>:** Assign Timer8 External Clock (T8CK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-8: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC2R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC1R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC2R<6:0>:** Assign Input Capture 2 (IC2) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC1R<6:0>:** Assign Input Capture 1 (IC1) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-9: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC4R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC3R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC4R<6:0>:** Assign Input Capture 4 (IC4) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC3R<6:0>:** Assign Input Capture 3 (IC3) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-10: RPINR9: PERIPHERAL PIN SELECT INPUT REGISTER 9**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC6R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC5R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC6R<6:0>:** Assign Input Capture 6 (IC6) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC5R<6:0>:** Assign Input Capture 5 (IC5) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-11: RPINR10: PERIPHERAL PIN SELECT INPUT REGISTER 10**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC8R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC7R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC8R<6:0>:** Assign Input Capture 8 (IC8) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC7R<6:0>:** Assign Input Capture 7 (IC7) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-12: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | OCFBR<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | OCFAR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **OCFBR<6:0>:** Assign Output Compare Fault B (OCFB) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **OCFAR<6:0>:** Assign Output Compare Fault A (OCFA) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-13: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12 (dsPIC33EPXXXMU806/810/814 DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | FLT2R<6:0>(1) | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | FLT1R<6:0>(1) | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **FLT2R<6:0>:** Assign PWM Fault 2 ($\overline{FLT2}$) to the Corresponding RPn/RPIn Pin bits(1)
(see Table 11-2 for input pin selection numbers)
1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **FLT1R<6:0>:** Assign PWM Fault 1 ($\overline{FLT1}$) to the Corresponding RPn/RPIn Pin bits(1)
(see Table 11-2 for input pin selection numbers)
1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**Note 1:** These pins are available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.


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**REGISTER 11-14: RPINR13: PERIPHERAL PIN SELECT INPUT REGISTER 13 (dsPIC33EPXXXMU806/810/814 DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | FLT4R<6:0>(1) | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | FLT3R<6:0>(1) | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **FLT4R<6:0>:** Assign PWM Fault 4 ($\overline{FLT4}$) to the Corresponding RPn/RPIn Pin bits(1) (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **FLT3R<4:0>:** Assign PWM Fault 3 ($\overline{FLT3}$) to the Corresponding RPn/RPIn Pin bits(1) (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**Note 1:** These pins are available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**REGISTER 11-15: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14 (dsPIC33EPXXXMU806/810/814 DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | QEB1R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | QEA1R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **QEB1R<6:0>:** Assign B (QEB) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **QEA1R<6:0>:** Assign A (QEA) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-16: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15 (dsPIC33EPXXXMU806/810/814 DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | HOME1R<6:0>(1) | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | INDX1R<6:0>(1) | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **HOME1R<6:0>:** Assign QEI1 HOME1 (HOME1) to the Corresponding RPn/RPIn Pin bits(1) (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IND1XR<6:0>:** Assign QEI1 INDEX1 (INDX1) to the Corresponding RPn/RPIn Pin bits(1) (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**Note 1:** These bits are available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**REGISTER 11-17: RPINR16: PERIPHERAL PIN SELECT INPUT REGISTER 16 (dsPIC33EPXXXMU806/810/814 DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | QEB2R<6:0>(1) | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | QEA2R<6:0>(1) | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **QEB2R<6:0>:** Assign B (QEI2) to the Corresponding RPn/RPIn Pin bits(1)
(see Table 11-2 for input pin selection numbers)
1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **QEA2R<6:0>:** Assign A (QEI2) to the Corresponding RPn/RPIn Pin bits(1)
(see Table 11-2 for input pin selection numbers)
1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**Note 1:** These bits are available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.


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**REGISTER 11-18: RPINR17: PERIPHERAL PIN SELECT INPUT REGISTER 17 (dsPIC33EPXXXMU806/810/814 DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | HOME2R<6:0>(1) | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | INDX2R<6:0>(1) | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **HOME2R<6:0>:** Assign QEI2 HOME2 (HOME2) to the Corresponding RPn/RPIn Pin bits(1) (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **INDX2R<6:0>:** Assign QEI2 INDEX2 (INDX2) to the Corresponding RPn/RPIn Pin bits(1) (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**Note 1:** These bits are available on dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**REGISTER 11-19: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | U1CTSR<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | U1RXR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **U1CTSR<6:0>:** Assign UART1 Clear-to-Send ($\overline{\text{U1CTS}}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **U1RXR<6:0>:** Assign UART1 Receive (U1RX) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-20: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | U2CTSR<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | U2RXR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **U2CTSR<6:0>:** Assign UART2 Clear-to-Send ($\overline{\text{U2CTS}}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **U2RXR<6:0>:** Assign UART2 Receive (U2RX) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-21: RPINR20: PERIPHERAL PIN SELECT INPUT REGISTER 20**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SCK1R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SDI1R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **SCK1R<6:0>:** Assign SPI1 Clock Input (SCK1) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **SDI1R<6:0>:** Assign SPI1 Data Input (SDI1) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-22: RPINR21: PERIPHERAL PIN SELECT INPUT REGISTER 21**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SS1R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **SS1R<6:0>:** Assign SPI1 Slave Select Input ($\overline{SS1}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-23: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SS2R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **SS2R<6:0>:** Assign SPI2 Slave Select Input ($\overline{SS2}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-24: RPINR24: PERIPHERAL PIN SELECT INPUT REGISTER 24**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | CSCKR<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | CSDIR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **CSCKR<6:0>:** Assign DCI Clock Input (CSCK) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **CSDIR<6:0>:** Assign DCI Data Input (CSDI) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-25: RPINR25: PERIPHERAL PIN SELECT INPUT REGISTER 25**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | COFSR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **COFSR<6:0>:** Assign DCI FSYNC Input (COFS) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-26: RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | C2RXR<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | C1RXR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **C2RXR<6:0>:** Assign CAN2 RX Input (CRX2) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **C1RXR<6:0>:** Assign CAN1 RX Input (CRX1) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-27: RPINR27: PERIPHERAL PIN SELECT INPUT REGISTER 27**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | U3CTSR<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | U3RXR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **U3CTSR<6:0>:** Assign UART3 Clear-to-Send ($\overline{U3CTS}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **U3RXR<6:0>:** Assign UART3 Receive (U3RX) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-28: RPINR28: PERIPHERAL PIN SELECT INPUT REGISTER 28**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | U4CTSR<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | U4RXR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **U4CTSR<6:0>:** Assign UART4 Clear-to-Send ($\overline{\text{U4CTS}}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **U4RXR<6:0>:** Assign UART4 Receive (U4RX) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-29: RPINR29: PERIPHERAL PIN SELECT INPUT REGISTER 29**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SCK3R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SDI3R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **SCK3R<6:0>:** Assign SPI3 Clock Input (SCK3) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **SDI3R<6:0>:** Assign SPI3 Data Input (SDI3) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-30: RPINR30: PERIPHERAL PIN SELECT INPUT REGISTER 30**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SS3R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **SS3R<6:0>:** Assign SPI3 Slave Select Input ($\overline{SS3}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-31: RPINR31: PERIPHERAL PIN SELECT INPUT REGISTER 31**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SCK4R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SDI4R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **SCK4R<6:0>:** Assign SPI4 Clock Input (SCK4) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **SDI4R<6:0>:** Assign SPI4 Data Input (SDI4) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-32: RPINR32: PERIPHERAL PIN SELECT INPUT REGISTER 32**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SS4R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **SS4R<6:0>:** Assign SPI4 Slave Select Input ($\overline{SS4}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-33: RPINR33: PERIPHERAL PIN SELECT INPUT REGISTER 33**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC10R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC9R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC10R<6:0>:** Assign Input Capture 10 (IC10) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC9R<6:0>:** Assign Input Capture 9 (IC9) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-34: RPINR34: PERIPHERAL PIN SELECT INPUT REGISTER 34**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC12R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC11R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC12R<6:0>:** Assign Input Capture 12 (IC12) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC11R<6:0>:** Assign Input Capture 11 (IC11) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-35: RPINR35: PERIPHERAL PIN SELECT INPUT REGISTER 35**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC14R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC13R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC14R<6:0>:** Assign Input Capture 14 (IC14) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC13R<6:0>:** Assign Input Capture 13 (IC13) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-36: RPINR36: PERIPHERAL PIN SELECT INPUT REGISTER 36**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC16R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC15R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC16R<6:0>:** Assign Input Capture 16 (IC16) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC15R<6:0>:** Assign Input Capture 15 (IC15) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-37: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SYNCI1R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | OCFCR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **SYNCI1R<6:0>:** Assign PWM Synchronization Input 1 to the Corresponding RPn/RPIn Pin bits. (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **OCFCR<6:0>:** Assign Output Fault C (OCFC) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-38: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP1R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SYNCI2R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP1R<6:0>:** Assign PWM Dead-Time Compensation Input 1 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **SYNCI2R<6:0>:** Assign PWM Synchronization Input 2 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-39: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP3R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP2R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP3R<6:0>:** Assign PWM Dead-Time Compensation Input 3 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **DTCMP2R<6:0>:** Assign PWM Dead-Time Compensation Input 2 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-40: RPINR40: PERIPHERAL PIN SELECT INPUT REGISTER 40**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP5R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP4R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP5R<6:0>:** Assign PWM Dead-Time Compensation Input 5 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **DTCMP4R<6:0>:** Assign PWM Dead-Time Compensation Input 4 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-41: RPINR41: PERIPHERAL PIN SELECT INPUT REGISTER 41**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP7R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP6R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP7R<6:0>:** Assign PWM Dead-Time Compensation Input 7 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **DTCMP6R<6:0>:** Assign PWM Dead-Time Compensation Input 6 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-42: RPINR42: PERIPHERAL PIN SELECT INPUT REGISTER 42**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | FLT6R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | FLT5R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **FLT6R<6:0>:** Assign PWM Fault 6 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **FLT5R<6:0>:** Assign PWM Fault 5 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-43: RPINR43: PERIPHERAL PIN SELECT INPUT REGISTER 43**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | FLT7R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **FLT7R<6:0>:** Assign PWM Fault 7 to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP127
.
.
.
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-44: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP65R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP64R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP65R<5:0>:** Peripheral Output Function is Assigned to RP65 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP64R<5:0>:** Peripheral Output Function is Assigned to RP64 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-45: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP67R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP66R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP67R<5:0>:** Peripheral Output Function is Assigned to RP67 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP66R<5:0>:** Peripheral Output Function is Assigned to RP66 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-46: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP69R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP68R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP69R<5:0>:** Peripheral Output Function is Assigned to RP69 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP68R<5:0>:** Peripheral Output Function is Assigned to RP68 Output Pin bits (see Table 11-3 for peripheral function numbers)


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**REGISTER 11-47: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP71R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP70R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP71R<5:0>:** Peripheral Output Function is Assigned to RP71 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP70R<5:0>:** Peripheral Output Function is Assigned to RP70 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-48: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP80R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP79R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP80R<5:0>:** Peripheral Output Function is Assigned to RP80 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP79R<5:0>:** Peripheral Output Function is Assigned to RP79 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-49: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP84R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP82R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP84R<5:0>:** Peripheral Output Function is Assigned to RP84 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP82R<5:0>:** Peripheral Output Function is Assigned to RP82 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-50: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP87R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP85R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP87R<5:0>:** Peripheral Output Function is Assigned to RP87 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP85R<5:0>:** Peripheral Output Function is Assigned to RP85 Output Pin bits (see Table 11-3 for peripheral function numbers)


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**REGISTER 11-51: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP97R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP96R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP97R<5:0>:** Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP96R<5:0>:** Peripheral Output Function is Assigned to RP96 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-52: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP99R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP98R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP99R<5:0>:** Peripheral Output Function is Assigned to RP99 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP98R<5:0>:** Peripheral Output Function is Assigned to RP98 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-53: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP101R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP100R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP101R<5:0>:** Peripheral Output Function is Assigned to RP101Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP100R<5:0>:** Peripheral Output Function is Assigned to RP100 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-54: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP102R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **RP102R<5:0>:** Peripheral Output Function is Assigned to RP102 Output Pin bits (see Table 11-3 for peripheral function numbers)


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**REGISTER 11-55: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP108R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP104R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP108R<5:0>:** Peripheral Output Function is Assigned to RP108 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP104R<5:0>:** Peripheral Output Function is Assigned to RP104 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-56: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP112R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP109R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP112R<5:0>:** Peripheral Output Function is Assigned to RP112 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP109R<5:0>:** Peripheral Output Function is Assigned to RP109 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-57: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP118R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP113R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP118R<5:0>:** Peripheral Output Function is Assigned to RP118 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP113R<5:0>:** Peripheral Output Function is Assigned to RP113 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-58: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP125R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP120R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP125R<5:0>:** Peripheral Output Function is Assigned to RP125 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP120R<5:0>:** Peripheral Output Function is Assigned to RP120 Output Pin bits (see Table 11-3 for peripheral function numbers)


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**REGISTER 11-59: RPOR15: PERIPHERAL PIN SELECT OUTPUT REGISTER 15**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP127R<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP126R<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP127R<5:0>:** Peripheral Output Function is Assigned to RP127 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP126R<5:0>:** Peripheral Output Function is Assigned to RP126 Output Pin bits (see Table 11-3 for peripheral function numbers)

**NOTES:**


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## 12.0 TIMER1

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 11. "Timers"** (DS70362) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer, which can serve as the time counter for the real-time clock, or operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated from the low-power 32 kHz crystal oscillator available on the device.
- Can be operated in Asynchronous Counter mode from an external clock source.
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and clock synchronization is performed after the prescaler.

The unique features of Timer1 allow it to be used for Real-Time Clock (RTC) applications. A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

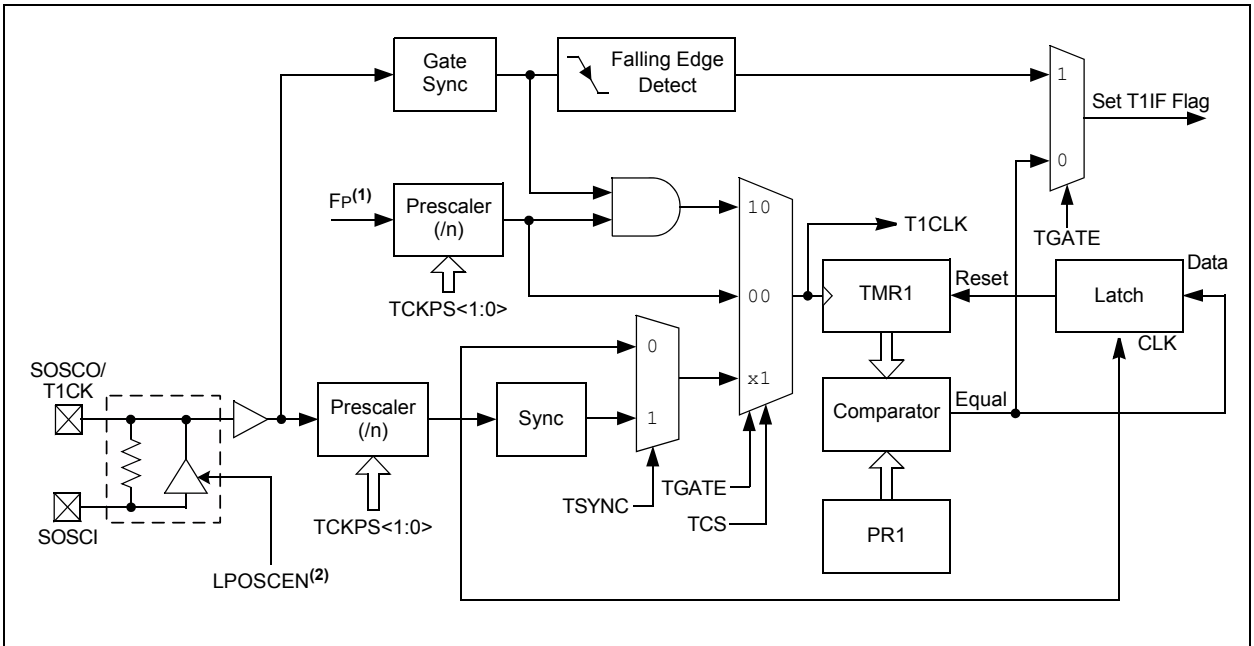
- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit setting for different operating modes are given in the Table 12-1.

**TABLE 12-1: TIMER MODE SETTINGS**

| Mode | TCS | TGATE | TSYNC |
|---|---|---|---|
| Timer | 0 | 0 | x |
| Gated Timer | 0 | 1 | x |
| Synchronous Counter | 1 | x | 1 |
| Asynchronous Counter | 1 | x | 0 |

**FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM**




**Note 1:** FP is the peripheral clock.

**2:** See **Section 9.0 "Oscillator Configuration"** for information on enabling the Secondary Oscillator (SOSC).

## 12.1 Timer Resources

Many useful resources related to Timers are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 12.1.1 KEY RESOURCES

- **Section 11. "Timers"** (DS70362) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools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## 12.2 Timer1 Control Register

**REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON(1) | — | TSIDL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE | TCKPS<1:0> | | — | TSYNC(1) | TCS(1) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timer1 On bit(1)
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit(1)
When TCS = 1:
1 = Synchronizes external clock input
0 = Does not synchronize external clock input
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit(1)
1 = External clock from T1CK pin (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.

**NOTES:**


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## 13.0 TIMER2/3, TIMER4/5, TIMER6/7 AND TIMER8/9

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 11. "Timers"** (DS70362) of the *"dsPIC33E/PIC24E Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3, Timer4/5, Timer6/7 and Timer8/9 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3, Timer4/5, Timer6/7 and Timer8/9 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (Timer2/3 only)
- ADC2 Event Trigger (Timer4/5 only)

Individually, all eight of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed above, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON, T5CON, T6CON, T7CON, T8CON and T9CON registers. T2CON, T4CON, T6CON and T8CON are shown in generic form in Register 13-1. T3CON, T5CON, T7CON and T9CON are shown in Register 13-2.

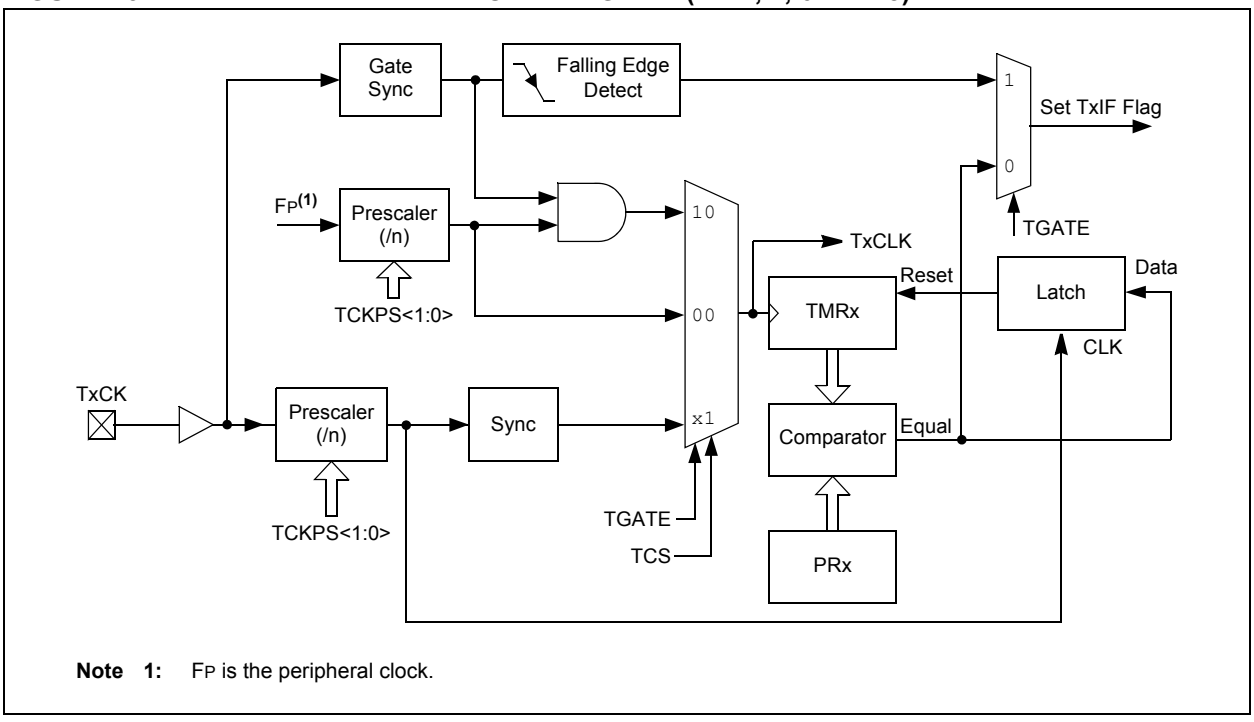
For 32-bit timer/counter operation, Timer2, Timer4, Timer6 or Timer8 is the least significant word; Timer3, Timer5, Timer7 or Timer9 is the most significant word of the 32-bit timers.

**Note:** For 32-bit operation, T3CON, T5CON, T7CON and T9CON control bits are ignored. Only T2CON, T4CON, T6CON and T8CON control bits are used for setup and control. Timer2, Timer4, Timer6 and Timer8 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3, Timer5, Ttimer7 and Timer9 interrupt flags.

A block diagram for an example 32-bit timer pair is shown Figure 13-3.

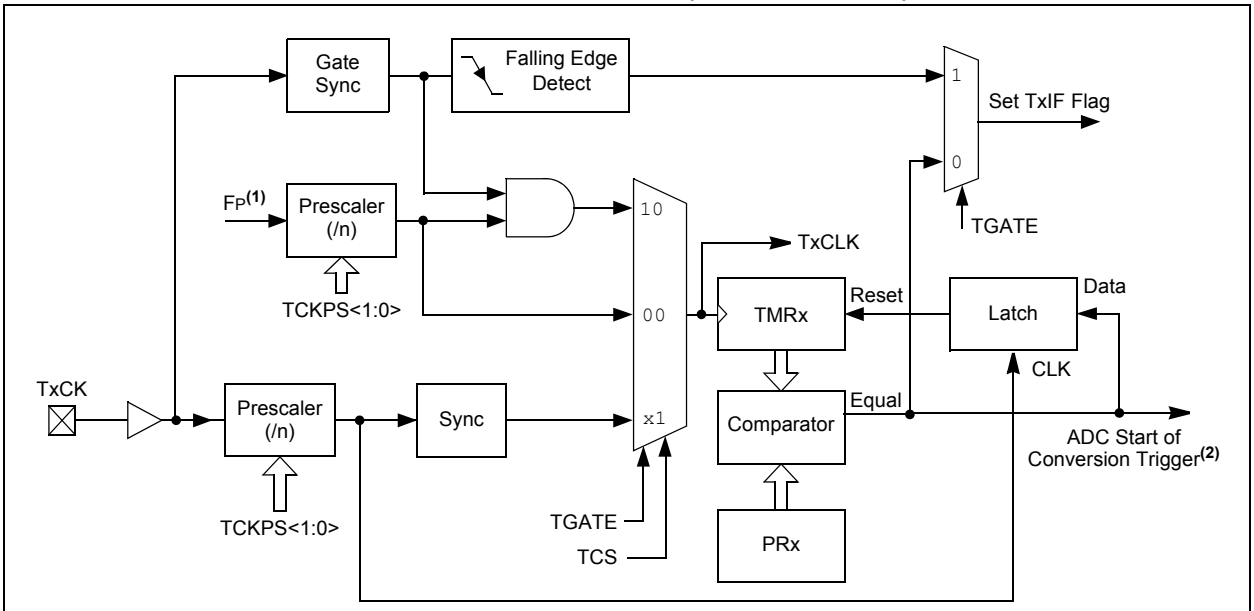
**Note:** Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

**FIGURE 13-1: TYPE B TIMERx BLOCK DIAGRAM (x = 2, 4, 6 AND 8)**




**Note 1:** FP is the peripheral clock.

**FIGURE 13-2: TYPE C TIMERx BLOCK DIAGRAM (x = 3, 5, 7 AND 9)**




**Note 1:** FP is the peripheral clock.
**2:** The ADC trigger is available on TMR3 and TMR5 only.


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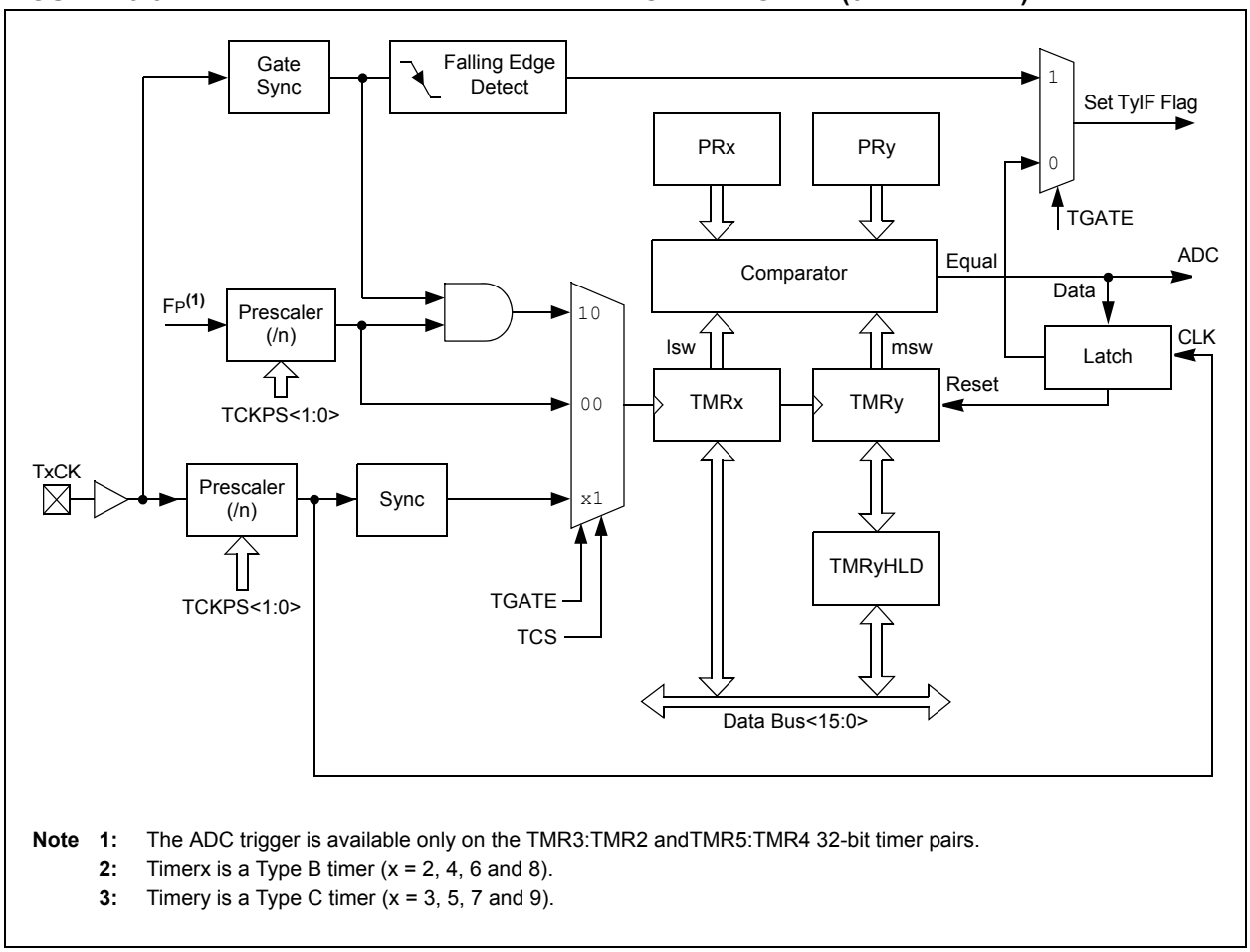
**FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)**




**Note 1:** The ADC trigger is available only on the TMR3:TMR2 andTMR5:TMR4 32-bit timer pairs.
**2:** Timerx is a Type B timer (x = 2, 4, 6 and 8).
**3:** Timery is a Type C timer (x = 3, 5, 7 and 9).

## 13.1 Timer Resources

Many useful resources related to timers are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |
|---|---|

### 13.1.1 KEY RESOURCES

- **Section 11. "Timers"** (DS70362) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 13.2 Timerx/y Control Registers

**REGISTER 13-1: TxCON: (T2CON, T4CON, T6CON OR T8CON) CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON | — | TSIDL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE | TCKPS<1:0> | | T32 | — | TCS(1) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timerx On bit
When T32 = 1:
1 = Starts 32-bit Timerx/y
0 = Stops 32-bit Timerx/y
When T32 = 0:
1 = Starts 16-bit Timerx
0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timerx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **T32:** 32-Bit Timer Mode Select bit
1 = Timerx and Timery form a single 32-bit timer
0 = Timerx and Timery act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit(1)
1 = External clock from TxCK pin (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

**Note 1:** The TxCK pin is not available on all timers. Refer to the **"Pin Diagrams"** section for the available pins.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**REGISTER 13-2: TyCON: (T3CON, T5CON, T7CON OR T9CON) CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON(1) | — | TSIDL(2) | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE(1) | TCKPS<1:0>(1) | | — | — | TCS(1,3) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timery On bit(1)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timery Stop in Idle Mode bit(2)
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(1,3)
1 = External clock from TyCK pin (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through TxCON.

**2:** When 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

**3:** The TyCK pin is not available on all timers. Refer to the **"Pin Diagrams"** section for the available pins.

**NOTES:**


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## 14.0 INPUT CAPTURE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "Input Capture"** (DS70352) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

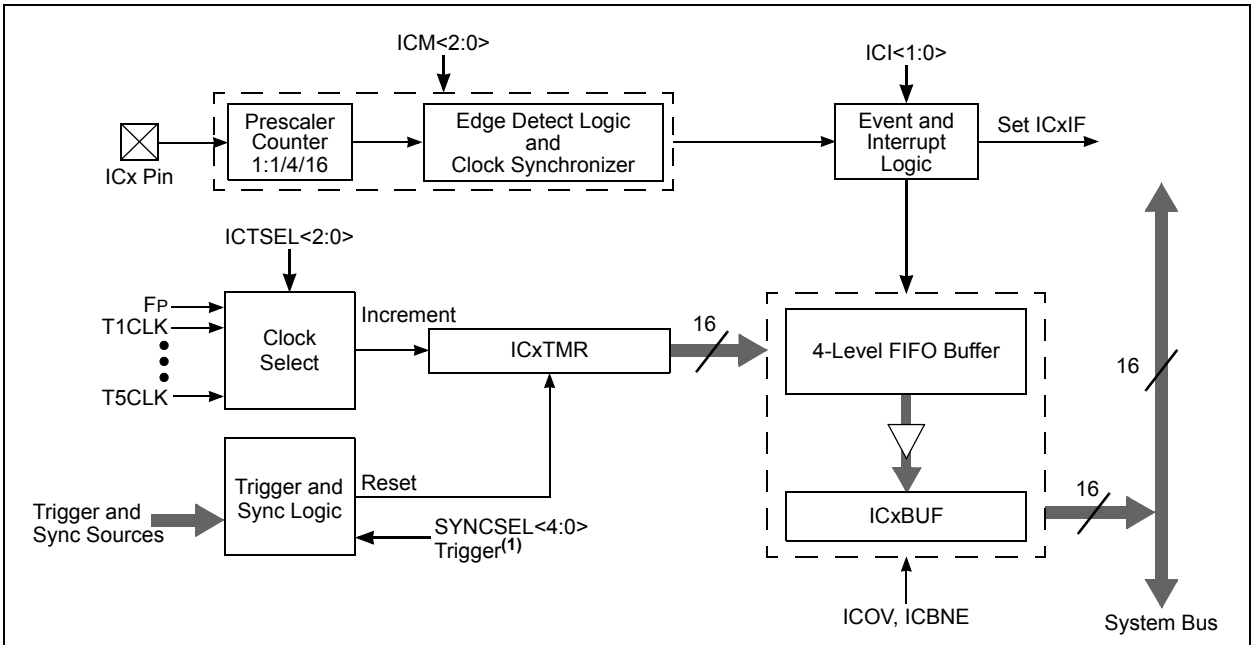
The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices support up to 16 input capture channels.

Key features of the input capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 30 user-selectable Trigger/Sync sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- Configurable interrupt generation
- Up to six clock sources available for each module, driving a separate internal 16-bit counter

**Note:** Only IC1, IC2, IC3 and IC4 can trigger a DMA data transfer. If DMA data transfers are required, the FIFO buffer size must be set to '1' (ICI<1:0> = 00).

**FIGURE 14-1: INPUT CAPTURE MODULE BLOCK DIAGRAM**




**Note 1:** The Trigger/Sync source is enabled by default and is set to Timer3 as a source. This timer must be enabled for proper ICx module operation or the Trigger/Sync source must be changed to another source option.

## 14.1 Input Capture Resources

Many useful resources related to input capture are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 14.1.1 KEY RESOURCES

- **Section 12. "Input Capture"** (DS70352) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools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## 14.2 Input Capture Control Registers

**REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | ICSIDL | ICTSEL<2:0> | | | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/HC/HS-0 | R/HC/HS-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | HC = Hardware Clearable bit | HS = Hardware Settable bit | '0' = Bit is cleared |
| -n = Value at POR | W = Writable bit | U = Unimplemented bit, read as '0' | |

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Stop in Idle Control bit
- 1 = Input capture will Halt in CPU Idle mode
- 0 = Input capture will continue to operate in CPU Idle mode

bit 12-10 **ICTSEL<12:10>:** Input Capture Timer Select bits
- 111 = Peripheral clock (FP) is the clock source of the ICx
- 110 = Reserved
- 101 = Reserved
- 100 = Clock source of T1CLK is the clock source of the ICx (only the synchronous clock is supported)
- 011 = Clock source of T5CLK is the clock source of the ICx
- 010 = Clock source of T4CLK is the clock source of the ICx
- 001 = Clock source of T2CLK is the clock source of the ICx
- 000 = Clock source of T3CLK is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI<1:0>:** Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture buffer overflow occurred
- 0 = No input capture buffer overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty, at least one more capture value can be read
- 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
- 111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
- 110 = Unused (module disabled)
- 101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
- 100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
- 011 = Capture mode, every rising edge (Simple Capture mode)
- 010 = Capture mode, every falling edge (Simple Capture mode)
- 001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
- 000 = Input capture module is turned off

**REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | IC32 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W/HS-0 | U-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-1 |
|---|---|---|---|---|---|---|---|
| ICTRIG(2) | TRIGSTAT(3) | — | SYNCSEL<4:0>(4) | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | HS = Set by Hardware | ‘0’ = Bit is cleared |
| -n = Value at POR | W = Writable bit | U = Unimplemented bit, read as ‘0’ |

bit 15-9 **Unimplemented:** Read as ‘0’

bit 8 **IC32:** 32-Bit Timer Mode Select bit (Cascade mode)
1 = ODD IC and EVEN IC form a single 32-bit input capture module(1)
0 = Cascade module operation is disabled

bit 7 **ICTRIG:** Trigger Operation Select bit(2)
1 = Input source is used to trigger the input capture timer (Trigger mode)
0 = Input source is used to synchronize the input capture timer to a timer of another module (Synchronization mode)

bit 6 **TRIGSTAT:** Timer Trigger Status bit(3)
1 = ICxTMR has been triggered and is running
0 = ICxTMR has not been triggered and is being held clear

bit 5 **Unimplemented:** Read as ‘0’

**Note 1:** The IC32 bit in both the ODD and EVEN IC must be set to enable Cascade mode.
**2:** The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
**3:** This bit is set by the selected input source (selected by the SYNCSEL<4:0> bits); it can be read, set and cleared in software.
**4:** Do not use the ICx module as its own Sync or Trigger source.
**5:** This option should only be selected as a trigger source and not as a synchronization source.


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**REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)**

bit 4-0 **SYNCSEL<4:0>:** Input Source Select for Synchronization and Trigger Operation bits(4)

11111 = No Sync or Trigger source for ICx
11110 = No Sync or Trigger source for ICx
11101 = No Sync or Trigger source for ICx
11100 = Reserved
11011 = ADC1 module synchronizes or triggers ICx(5)
11010 = CMP3 module synchronizes or triggers ICx(5)
11001 = CMP2 module synchronizes or triggers ICx(5)
11000 = CMP1 module synchronizes or triggers ICx(5)
10111 = IC8 module synchronizes or triggers ICx
10110 = IC7 module synchronizes or triggers ICx
10101 = IC6 module synchronizes or triggers ICx
10100 = IC5 module synchronizes or triggers ICx
10011 = IC4 module synchronizes or triggers ICx
10010 = IC3 module synchronizes or triggers ICx
10001 = IC2 module synchronizes or triggers ICx
10000 = IC1 module synchronizes or triggers ICx
01111 = Timer5 synchronizes or triggers ICx
01110 = Timer4 synchronizes or triggers ICx
01101 = Timer3 synchronizes or triggers ICx **(default)**
01100 = Timer2 synchronizes or triggers ICx
01011 = Timer1 synchronizes or triggers ICx
01010 = No Sync or Trigger source for ICx
01001 = OC9 module synchronizes or triggers ICx
01000 = OC8 module synchronizes or triggers ICx
00111 = OC7 module synchronizes or triggers ICx
00110 = OC6 module synchronizes or triggers ICx
00101 = OC5 module synchronizes or triggers ICx
00100 = OC4 module synchronizes or triggers ICx
00011 = OC3 module synchronizes or triggers ICx
00010 = OC2 module synchronizes or triggers ICx
00001 = OC1 module synchronizes or triggers ICx
00000 = No Sync or Trigger source for ICx

**Note 1:** The IC32 bit in both the ODD and EVEN IC must be set to enable Cascade mode.
**2:** The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
**3:** This bit is set by the selected input source (selected by the SYNCSEL<4:0> bits); it can be read, set and cleared in software.
**4:** Do not use the ICx module as its own Sync or Trigger source.
**5:** This option should only be selected as a trigger source and not as a synchronization source.

**NOTES:**


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## 15.0 OUTPUT COMPARE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. "Output Compare"** (DS70358) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

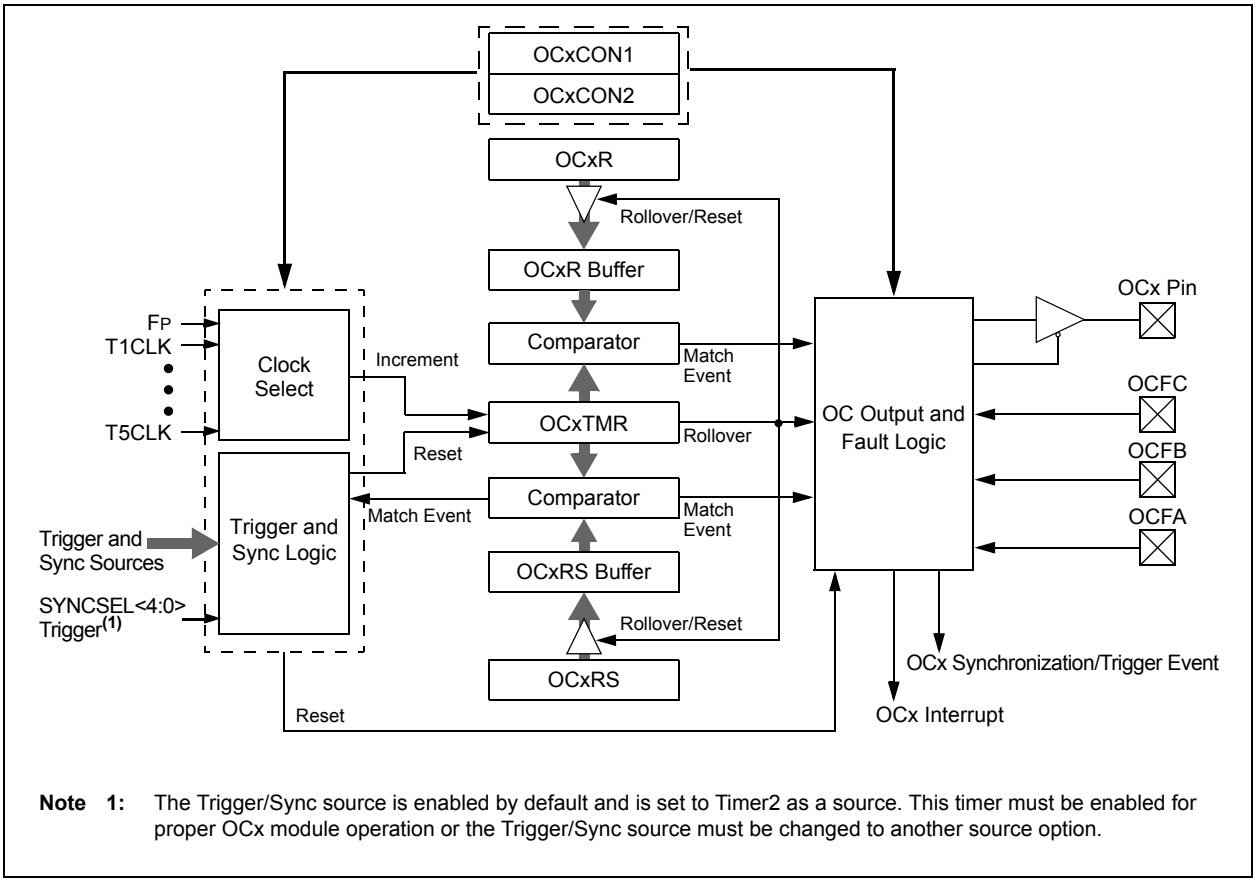
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The output compare module can select one of eight available clock sources for its time base. The module compares the value of the timer with the value of one or two Compare registers, depending on the operating mode selected. The state of the output pin changes when the timer value matches the Compare register value. The output compare module generates either a single output pulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events.

**Note 1:** Only OC1, OC2, OC3 and OC4 can trigger a DMA data transfer.

**2:** See **Section 13. "Output Compare"** (DS70358) in the *"dsPIC33E/PIC24E Family Reference Manual"* for OCxR and OCxRS register restrictions.

**FIGURE 15-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM**




**Note 1:** The Trigger/Sync source is enabled by default and is set to Timer2 as a source. This timer must be enabled for proper OCx module operation or the Trigger/Sync source must be changed to another source option.

## 15.1 Output Compare Resources

Many useful resources related to output compare are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 15.1.1 KEY RESOURCES

- **Section 13. "Output Compare"** (DS70358) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools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## 15.2 Output Compare Control Registers

**REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | OCSIDL | OCTSEL<2:0> | | | ENFLTC | ENFLTB |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0, HSC | R/W-0, HSC | R/W-0, HSC | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ENFLTA | OCFLTC | OCFLTB | OCFLTA | TRIGMODE | OCM<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HCS = Hardware Settable/Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **OCSIDL:** Stop Output Compare x in Idle Mode Control bit
1 = Output Compare x Halts in CPU Idle mode
0 = Output Compare x continues to operate in CPU Idle mode

bit 12-10 **OCTSEL<2:0>:** Output Compare x Clock Select bits
111 = Peripheral clock (FP)
110 = Reserved
101 = Reserved
100 = Clock source of T1CLK is the clock source of OCx (only the synchronous clock is supported)
011 = Clock source of T5CLK is the clock source of OCx
010 = Clock source of T4CLK is the clock source of OCx
001 = Clock source of T3CLK is the clock source of OCx
000 = Clock source of T2CLK is the clock source of OCx

bit 9 **ENFLTC:** Fault C Input Enable bit
1 = Output Compare Fault C input (OCFC) is enabled
0 = Output Compare Fault C input (OCFC) is disabled

bit 8 **ENFLTB:** Fault B Input Enable bit
1 = Output Compare Fault B input (OCFB) is enabled
0 = Output Compare Fault B input (OCFB) is disabled

bit 7 **ENFLTA:** Fault A Input Enable bit
1 = Output Compare Fault A input (OCFA) is enabled
0 = Output Compare Fault A input (OCFA) is disabled

bit 6 **OCFLTC:** PWM Fault C Condition Status bit
1 = PWM Fault C condition on OCFC pin has occurred
0 = No PWM Fault C condition on OCFC pin has occurred

bit 5 **OCFLTB:** PWM Fault B Condition Status bit
1 = PWM Fault B condition on OCFB pin has occurred
0 = No PWM Fault B condition on OCFB pin has occurred

bit 4 **OCFLTA:** PWM Fault A Condition Status bit
1 = PWM Fault A condition on OCFA pin has occurred
0 = No PWM Fault A condition on OCFA pin has occurred

bit 3 **TRIGMODE:** Trigger Status Mode Select bit
1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
0 = TRIGSTAT is cleared only by software

**Note 1:** OCxR and OCxRS are double-buffered in PWM mode only.

**REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)**

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits

111 = Center-Aligned PWM mode: Output set high when OCxTMR = OCxR and set low when OCxTMR = OCxRS(1)

110 = Edge-Aligned PWM mode: Output set high when OCxTMR = 0 and set low when OCxTMR = OCxR(1)

101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS

100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle

011 = Single Compare mode: Compares events with OCxR, continuously toggles OCx pin

010 = Single Compare Single-Shot mode: Initializes OCx pin high, compares event with OCxR, forces OCx pin low

001 = Single Compare Single-Shot mode: Initializes OCx pin low, compares event with OCxR, forces OCx pin high

000 = Output compare channel is disabled

**Note 1:** OCxR and OCxRS are double-buffered in PWM mode only.


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**REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 HS | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FLTMD:** Fault Mode Select bit
- 1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts
- 0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 **FLTOUT:** Fault Out bit
- 1 = PWM output is driven high on a Fault
- 0 = PWM output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit
- 1 = OCx pin is tri-stated on Fault condition
- 0 = OCx pin I/O state defined by FLTOUT bit on Fault condition

bit 12 **OCINV:** OCMP Invert bit
- 1 = OCx output is inverted
- 0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)
- 1 = Cascade module operation is enabled
- 0 = Cascade module operation is disabled

bit 7 **OCTRIG:** OCx Trigger/Sync Select bit
- 1 = Triggers OCx from source designated by SYNCSELx bits
- 0 = Synchronizes OCx with source designated by SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit
- 1 = Timer source has been triggered and is running
- 0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** OCx Output Pin Direction Select bit
- 1 = OCx is tri-stated
- 0 = Output compare module drives the OCx pin

**Note 1:** Do not use the OCx module as its own Sync or Trigger source.

**2:** When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

**REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)**

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits

11111 = No Sync or Trigger source for OCx
11110 = INT2 pin synchronizes or triggers OCx
11101 = INT1 pin synchronizes or triggers OCx
11100 = Reserved
11011 = ADC1 module synchronizes or triggers OCx
11010 = CMP3 module synchronizes or triggers OCx
11001 = CMP2 module synchronizes or triggers OCx
11000 = CMP1 module synchronizes or triggers OCx
10111 = IC8 module synchronizes or triggers OCx
10110 = IC7 module synchronizes or triggers OCx
10101 = IC6 module synchronizes or triggers OCx
10100 = IC5 module synchronizes or triggers OCx
10011 = IC4 module synchronizes or triggers OCx
10010 = IC3 module synchronizes or triggers OCx
10001 = IC2 module synchronizes or triggers OCx
10000 = IC1 module synchronizes or triggers OCx
01111 = Timer5 synchronizes or triggers OCx
01110 = Timer4 synchronizes or triggers OCx
01101 = Timer3 synchronizes or triggers OCx
01100 = Timer2 synchronizes or triggers OCx (default)
01011 = Timer1 synchronizes or triggers OCx
01010 = No Sync or Trigger source for OCx
01001 = OC9 module synchronizes or triggers OCx(1,2)
01000 = OC8 module synchronizes or triggers OCx(1,2)
00111 = OC7 module synchronizes or triggers OCx(1,2)
00110 = OC6 module synchronizes or triggers OCx(1,2)
00101 = OC5 module synchronizes or triggers OCx(1,2)
00100 = OC4 module synchronizes or triggers OCx(1,2)
00011 = OC3 module synchronizes or triggers OCx(1,2)
00010 = OC2 module synchronizes or triggers OCx(1,2)
00001 = OC1 module synchronizes or triggers OCx(1,2)
00000 = No Sync or Trigger source for OCx

**Note 1:** Do not use the OCx module as its own Sync or Trigger source.

**2:** When the OCy module is turned OFF, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.


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# 16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXX(MC/MU)8XX DEVICES ONLY)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "High-Speed PWM"** (DS70645) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(MC/MU)806/810/814 devices support a dedicated Pulse-Width Modulation (PWM) module with up to 14 outputs.

The high-speed PWM module consists of the following major features:

- Two master time base modules with Special Event Triggers
- PWM module input clock prescaler
- Two synchronization inputs
- Two synchronization outputs
- Up to seven PWM generators
- Two PWM outputs per generator (PWMxH and PWMxL)
- Individual period, duty cycle and phase shift for each PWM output
- Period, duty cycle, phase shift and dead-time resolution of 8.32 ns
- Immediate update mode for PWM period, duty cycle and phase shift
- Independent Fault and current-limited inputs for each PWM
- Cycle-by-Cycle and Latched Fault modes
- PWM time-base capture upon current limit
- Seven Fault inputs and three comparator outputs available for Faults and current limits
- Programmable ADC trigger with interrupt for each PWM pair
- Complementary PWM outputs
- Push-Pull PWM outputs
- Redundant PWM outputs
- Edge-Aligned PWM mode
- Center-Aligned PWM mode
- Variable Phase PWM mode
- Multi-Phase PWM mode
- Fixed Off Time PWM mode
- Current-Limit PWM mode
- Current Reset PWM mode
- PWMxH and PWMxL output override control
- PWMxH and PWMxL output pin swapping
- Chopping mode (also known as Gated mode)
- Dead-time insertion
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB)
- 8 mA PWM pin output drive

**Note:** Duty cycle, dead time, phase shift and frequency resolution is 16.64 ns in Center-Aligned PWM mode.

The high-speed PWM module contains up to seven PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. Two master time base generators provide a synchronous signal as a common time base to synchronize the various PWM outputs. Each generator can operate independently or in synchronization with either of the two master time bases. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limited signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWM can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWM module also generates two Special Event Triggers to the ADC module based on the two master time bases.

The high-speed PWM module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 and SYNCI2 pins are the input pins, which can synchronize the high-speed PWM module with an external signal. The SYNCO1 and SYNCO2 pins are output pins that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWM module and its interconnection with the CPU and other peripherals.

**FIGURE 16-1: HIGH-SPEED PWM MODULE ARCHITECTURAL OVERVIEW**

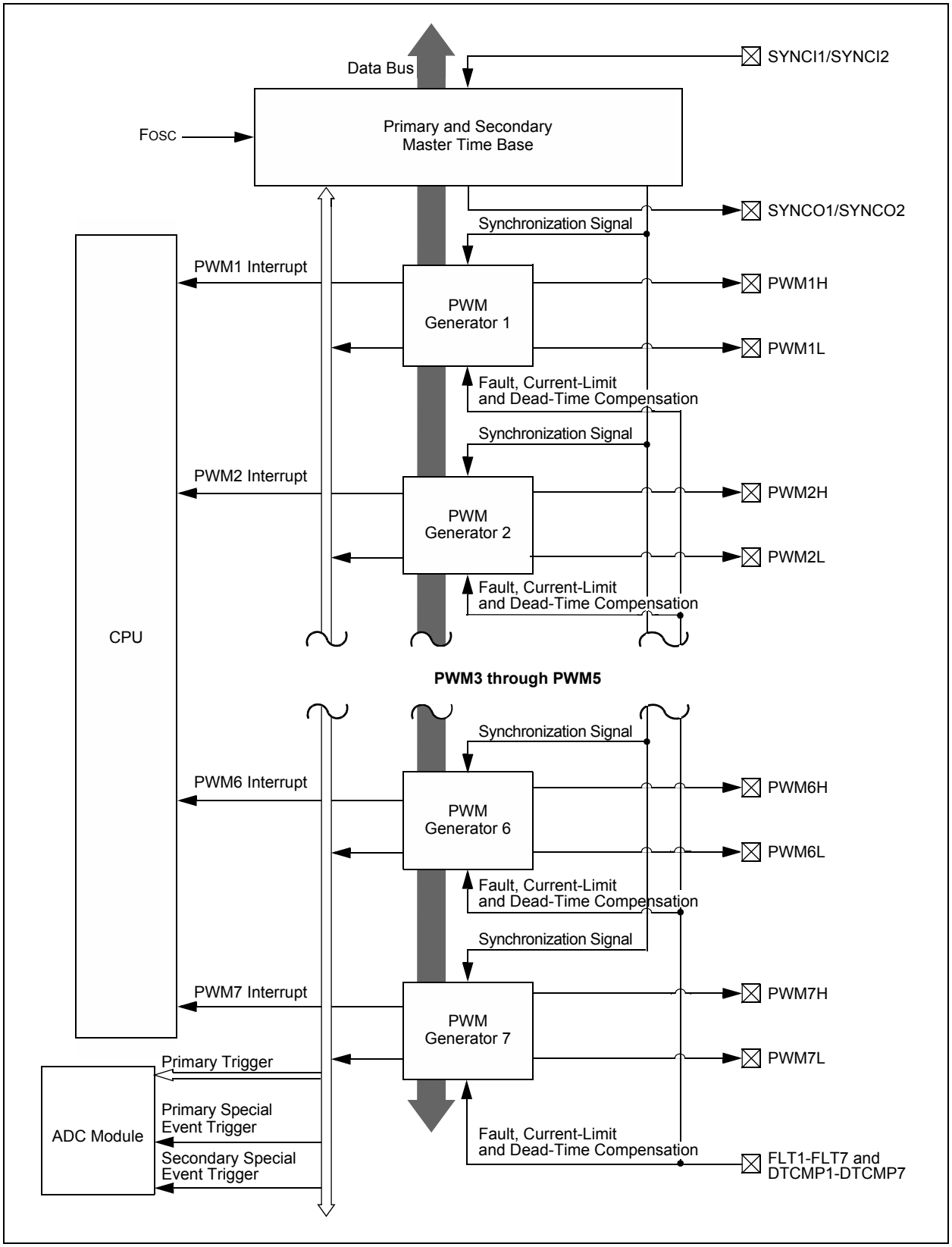



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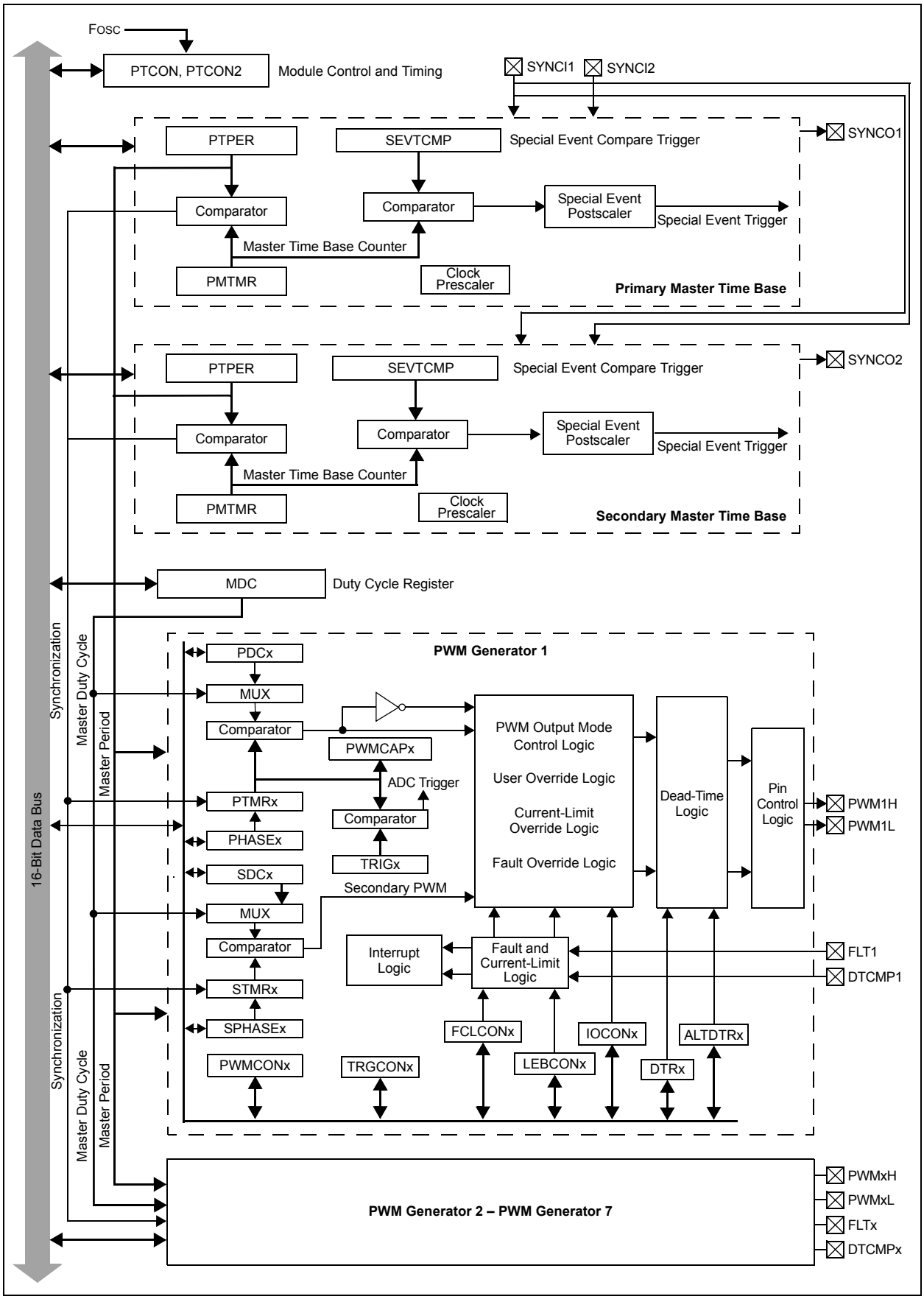
**FIGURE 16-2: HIGH-SPEED PWM MODULE REGISTER INTERCONNECTION DIAGRAM**



## 16.1 PWM Resources

Many useful resources related to the high-speed PWM are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 16.1.1 KEY RESOURCES

- **Section 11. "High-Speed PWM"** (DS70645) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools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## 16.2 PWM Control Registers

**REGISTER 16-1: PTCON: PWM TIME BASE CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | HSC-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTEN | — | PTSIDL | SESTAT | SEIEN | EIPU(1) | SYNCPOL(1) | SYNCOEN(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SYNCEN(1) | SYNCSRC<2:0>(1) | | | SEVTPS<3:0>(1) | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HSC = Hardware Settable/Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PTEN:** PWM Module Enable bit
1 = PWM module is enabled
0 = PWM module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTSIDL:** PWM Time Base Stop in Idle Mode bit
1 = PWM time base halts in CPU Idle mode
0 = PWM time base runs in CPU Idle mode

bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled

bit 10 **EIPU:** Enable Immediate Period Updates bit(1)
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWM cycle boundaries

bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit(1)
1 = SYNCIx/SYNCO polarity is inverted (active-low)
0 = SYNCIx/SYNCO is active-high

bit 8 **SYNCOEN:** Primary Time Base Sync Enable bit(1)
1 = SYNCO output is enabled
0 = SYNCO output is disabled

bit 7 **SYNCEN:** External Time Base Synchronization Enable bit(1)
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

**Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCIx feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

**REGISTER 16-1: PTCON: PWM TIME BASE CONTROL REGISTER (CONTINUED)**

bit 6-4 **SYNCSRC<2:0>:** Synchronous Source Selection bits(1)

111 = Reserved
•
•
•
010 = Reserved
001 = SYNCI2
000 = SYNCI1

bit 3-0 **SEVTPS<3:0>:** PWM Special Event Trigger Output Postscaler Select bits(1)

1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event
•
•
•
0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event
0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

**Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCIx feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.


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**REGISTER 16-2: PTCON2: PWM PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | PCLKDIV<2:0>(1) | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **PCLKDIV<2:0>:** PWM Input Clock Prescaler (Divider) Select bits(1)

111 = Reserved
110 = Divide-by-64
101 = Divide-by-32
100 = Divide-by-16
011 = Divide-by-8
010 = Divide-by-4
001 = Divide-by-2
000 = Divide-by-1, maximum PWM timing resolution (power-on default)

**Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

**REGISTER 16-3: PTPER: PRIMARY MASTER TIME BASE PERIOD REGISTER**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| PTPER<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTPER<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **PTPER<15:0>:** Primary Master Time Base (PMTMR) Period Value bits

**REGISTER 16-4: SEVTCMP: PWM PRIMARY SPECIAL EVENT COMPARE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SEVTCMP<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SEVTCMP<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **SEVTCMP<15:0>:** Special Event Compare Count Value bits


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**REGISTER 16-5: STCON: PWM SECONDARY MASTER TIME BASE CONTROL REGISTER**

| U-0 | U-0 | U-0 | HSC-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | SESTAT | SEIEN | EIPU(1) | SYNCPOL | SYNCOEN |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SYNCEN | SYNCSRC<2:0> | | | SEVTPS<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HSC = Set or Cleared in Hardware | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Secondary special event interrupt is pending
0 = Secondary special event interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Secondary special event interrupt is enabled
0 = Secondary special event interrupt is disabled

bit 10 **EIPU:** Enable Immediate Period Updates bit(1)
1 = Active Secondary Period register is updated immediately
0 = Active Secondary Period register updates occur on PWM cycle boundaries

bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit
1 = The falling edge of SYNCIN resets the SMTMR; SYNCO2 output is active-low
0 = The rising edge of SYNCIN resets the SMTMR; SYNCO2 output is active-high

bit 8 **SYNCOEN:** Secondary Master Time Base Synchronization Enable bit
1 = SYNCO2 output is enabled
0 = SYNCO2 output is disabled

bit 7 **SYNCEN:** External Secondary Master Time Base Synchronization Enable bit
1 = External synchronization of secondary time base is enabled
0 = External synchronization of secondary time base is disabled

bit 6-4 **SYNCSRC<2:0>:** Secondary Time Base Synchronization Source Selection bits
111 = Reserved
•
•
•
010 = Reserved
001 = SYNCI2
000 = SYNCI1

bit 3-0 **SEVTPS<3:0>:** PWM Secondary Special Event Trigger Output Postscaler Select bits
1111 = 1:16 Postcale
•
•
•
0001 = 1:2 Postcale
0000 = 1:1 Postscale

**Note 1:** This bit only applies to the secondary master time base period.

**REGISTER 16-6: STCON2: PWM SECONDARY CLOCK DIVIDER SELECT REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | PCLKDIV<2:0>(1) | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **PCLKDIV<2:0>:** PWM Input Clock Prescaler (Divider) Select bits(1)

111 = Reserved
110 = Divide-by-64
101 = Divide-by-32
100 = Divide-by-16
011 = Divide-by-8
010 = Divide-by-4
001 = Divide-by-2
000 = Divide-by-1, maximum PWM timing resolution (power-on default)

**Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

**REGISTER 16-7: STPER: SECONDARY MASTER TIME BASE PERIOD REGISTER(1)**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| STPER<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STPER<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **STPER<15:0>:** Secondary Master Time Base (PMTMR) Period Value bits


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**REGISTER 16-8: SSEVTCMP: PWM SECONDARY SPECIAL EVENT COMPARE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SSEVTCMP<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SSEVTCMP<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **SSEVTCMP<15:0>:** Special Event Compare Count Value bits

**REGISTER 16-9: CHOP: PWM CHOP CLOCK GENERATOR REGISTER**

| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CHPCLKEN | — | — | — | — | — | CHOPCLK<9:8> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CHOPCLK<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CHPCLKEN:** Enable Chop Clock Generator bit
1 = Chop clock generator is enabled
0 = Chop clock generator is disabled

bit 14-10 **Unimplemented:** Read as '0'

bit 9-0 **CHOPCLK<9:0>:** Chop Clock Divider bits
The frequency of the chop clock signal is given by the following expression:
Chop Frequency = FPWM/(CHOP<9:0> + 1)
Where, FPWM is FP divided by the value based on the PCLKDIV settings.

**REGISTER 16-10: MDC: PWM MASTER DUTY CYCLE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| MDC<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| MDC<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **MDC<15:0>:** Master PWM Duty Cycle Value bits


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**REGISTER 16-11: PWMCONx: PWMx CONTROL REGISTER**

| HSC-0 | HSC-0 | HSC-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTSTAT(1) | CLSTAT(1) | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB(2) | MDCS(2) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DTC<1:0> | | DTCP(3) | — | MTBS | CAM(2,4) | XPRES(5) | IUE(2) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HSC = Set or Cleared in Hardware | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
1 = Fault interrupt is pending
0 = No Fault interrupt is pending
This bit is cleared by setting FLTIEN = 0.

bit 14 **CLSTAT:** Current-Limit Interrupt Status bit(1)
1 = Current-limit interrupt is pending
0 = No current-limit interrupt is pending
This bit is cleared by setting CLIEN = 0.

bit 13 **TRGSTAT:** Trigger Interrupt Status bit
1 = Trigger interrupt is pending
0 = No trigger interrupt is pending
This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit
1 = Fault interrupt is enabled
0 = Fault interrupt is disabled and FLTSTAT bit is cleared

bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
1 = Current-limit interrupt is enabled
0 = Current-limit interrupt is disabled and CLSTAT bit is cleared

bit 10 **TRGIEN:** Trigger Interrupt Enable bit
1 = A trigger event generates an interrupt request
0 = Trigger event interrupts are disabled and TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit(2)
1 = PHASEx/SPHASEx registers provide time base period for this PWM generator
0 = PTPER register provides timing for this PWM generator

bit 8 **MDCS:** Master Duty Cycle Register Select bit(2)
1 = MDC register provides duty cycle information for this PWM generator
0 = PDCx and SDCx registers provide duty cycle information for this PWM generator

**Note 1:** Software must clear the interrupt status here and in the corresponding IFS bit in the interrupt controller.
**2:** These bits should not be changed after the PWM is enabled (PTEN = 1).
**3:** DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
**4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
**5:** To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

**REGISTER 16-11: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)**

bit 7-6 **DTC<1:0>:** Dead-Time Control bits
11 = Dead-Time Compensation mode
10 = Dead-time function is disabled
01 = Negative dead time actively applied for Complementary Output mode
00 = Positive dead time actively applied for all output modes

bit 5 **DTCP:** Dead-Time Compensation Polarity bit(3)
When set to '1':
If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened.
If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened.
When set to '0':
If DTCMPx = 0, PWMxH is shortened and PWMxL is lengthened.
If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.

bit 4 **Unimplemented:** Read as '0'

bit 3 **MTBS:** Master Time Base Select bit
1 = PWM generator uses the secondary master time base for synchronization and as the clock source for the PWM generation logic (if secondary time base is available)
0 = PWM generator uses the primary master time base for synchronization and as the clock source for the PWM generation logic

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,4)
1 = Center-Aligned mode is enabled
0 = Edge-Aligned mode is enabled

bit 1 **XPRES:** External PWM Reset Control bit(5)
1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
0 = External pins do not affect PWM time base

bit 0 **IUE:** Immediate Update Enable bit(2)
1 = Updates to the active MDC/PDCx/SDCx registers are immediate
0 = Updates to the active PDCx registers are synchronized to the PWM time base

**Note 1:** Software must clear the interrupt status here and in the corresponding IFS bit in the interrupt controller.
**2:** These bits should not be changed after the PWM is enabled (PTEN = 1).
**3:** DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
**4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
**5:** To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.


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**REGISTER 16-12: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PDCx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PDCx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PDCx<15:0>:** PWM Generator # Duty Cycle Value bits

**Note 1:** In Independent PWM mode, the PDCx register controls the PWMxH duty cycle only. In the Complementary, Redundant and Push-Pull PWM modes, the PDCx register controls the duty cycle of both the PWMxH and PWMxL.

**REGISTER 16-13: SDCx: PWMx SECONDARY DUTY CYCLE REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SDCx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SDCx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **SDCx<15:0>:** Secondary Duty Cycle bits for PWMxL Output Pin bits

**Note 1:** The SDCx register is used in Independent PWM mode only. When used in Independent PWM mode, the SDCx register controls the PWMxL duty cycle.

**REGISTER 16-14: PHASEx: PWMx PRIMARY PHASE SHIFT REGISTER(1,2)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PHASEx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PHASEx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PHASEx<15:0>:** PWM Phase Shift Value or Independent Time Base Period for the PWM Generator bits

**Note 1:** If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase shift value for PWMxH and PWMxL outputs.
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11), PHASEx<15:0> = Phase shift value for PWMxH only.

**2:** If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL.
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11), PHASEx<15:0> = Independent time base period value for PWMxH only.


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**REGISTER 16-15: SPHASEx: PWMx SECONDARY PHASE SHIFT REGISTER(1,2)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SPHASEx<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SPHASEx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **SPHASEx<15:0>:** Secondary Phase Offset bits for PWMxL Output Pin (used in Independent PWM mode only)

**Note 1:** If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), SPHASEx<15:0> = Not used.
- True Independent Output mode (PMOD<1:0> (IOCON<11:10>) = 11), SPHASEx<15:0> = Phase shift value for PWMxL only.

**2:** If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCON<11:10>) = 00, 01 or 10), SPHASEx<15:0> = Not used.
- True Independent Output mode (PMOD<1:0> (IOCON<11:10>) = 11), SPHASEx<15:0> = Independent time base period value for PWMxL only.

**REGISTER 16-16: DTRx: PWMx DEAD-TIME REGISTER**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | DTRx<13:8> | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DTRx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **DTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

**REGISTER 16-17: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | ALTDTRx<13:8> | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ALTDTRx<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **ALTDTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits


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**REGISTER 16-18: TRGCONx: PWMx TRIGGER CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TRGDIV<3:0> | | | | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | TRGSTRT<5:0>(1) | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **TRGDIV<3:0>:** Trigger # Output Divider bits

1111 = Trigger output for every 16th trigger event
1110 = Trigger output for every 15th trigger event
1101 = Trigger output for every 14th trigger event
1100 = Trigger output for every 13th trigger event
1011 = Trigger output for every 12th trigger event
1010 = Trigger output for every 11th trigger event
1001 = Trigger output for every 10th trigger event
1000 = Trigger output for every 9th trigger event
0111 = Trigger output for every 8th trigger event
0110 = Trigger output for every 7th trigger event
0101 = Trigger output for every 6th trigger event
0100 = Trigger output for every 5th trigger event
0011 = Trigger output for every 4th trigger event
0010 = Trigger output for every 3rd trigger event
0001 = Trigger output for every 2nd trigger event
0000 = Trigger output for every trigger event

bit 11-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TRGSTRT<5:0>:** Trigger Postscaler Start Enable Select bits(1)

111111 = Wait 63 PWM cycles before generating the first trigger event after the module is enabled
•
•
•
000010 = Wait 2 PWM cycles before generating the first trigger event after the module is enabled
000001 = Wait 1 PWM cycle before generating the first trigger event after the module is enabled
000000 = Wait 0 PWM cycles before generating the first trigger event after the module is enabled

**Note 1:** The secondary PWM generator cannot generate PWM trigger interrupts.

**REGISTER 16-19: IOCONx: PWMx I/O CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PENH | PENL | POLH | POLL | PMOD<1:0>(1) | | OVRENH | OVRENL |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OVRDAT<1:0> | | FLTDAT<1:0> | | CLDAT<1:0> | | SWAP | OSYNC |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PENH:** PWMxH Output Pin Ownership bit
1 = PWM module controls PWMxH pin
0 = GPIO module controls PWMxH pin

bit 14 **PENL:** PWMxL Output Pin Ownership bit
1 = PWM module controls PWMxL pin
0 = GPIO module controls PWMxL pin

bit 13 **POLH:** PWMxH Output Pin Polarity bit
1 = PWMxH pin is active-low
0 = PWMxH pin is active-high

bit 12 **POLL:** PWMxL Output Pin Polarity bit
1 = PWMxL pin is active-low
0 = PWMxL pin is active-high

bit 11-10 **PMOD<1:0>:** PWM # I/O Pin Mode bits(1)
11 = PWM I/O pin pair is in the True Independent Output mode
10 = PWM I/O pin pair is in the Push-Pull Output mode
01 = PWM I/O pin pair is in the Redundant Output mode
00 = PWM I/O pin pair is in the Complementary Output mode

bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
1 = OVRDAT<1> controls output on PWMxH pin
0 = PWM generator controls PWMxH pin

bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
1 = OVRDAT<0> controls output on PWMxL pin
0 = PWM generator controls PWMxL pin

bit 7-6 **OVRDAT<1:0>:** Data for PWMxH, PWMxL Pins if Override is Enabled bits
If OVERENH = 1, PWMxH is driven to the state specified by OVRDAT<1>.
If OVERENL = 1, PWMxL is driven to the state specified by OVRDAT<0>.

bit 5-4 **FLTDAT<1:0>:** Data for PWMxH and PWMxL Pins if FLTMOD is Enabled bits
IFLTMOD (FCLCONx<15>) = 0: Normal Fault mode:
If Fault is active, PWMxH is driven to the state specified by FLTDAT<1>.
If Fault is active, PWMxL is driven to the state specified by FLTDAT<0>.

IFLTMOD (FCLCONx<15>) = 1: Independent Fault mode:
If current limit is active, PWMxH is driven to the state specified by FLTDAT<1>.
If Fault is active, PWMxL is driven to the state specified by FLTDAT<0>.

**Note 1:** These bits should not be changed after the PWM module is enabled (PTEN = 1).


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**REGISTER 16-19: IOCONx: PWMx I/O CONTROL REGISTER (CONTINUED)**

bit 3-2 **CLDAT<1:0>:** Data for PWMxH and PWMxL Pins if CLMOD is Enabled bits

IFLTMOD (FCLCONx<15>) = 0: Normal Fault mode:
If current limit is active, PWMxH is driven to the state specified by CLDAT<1>.
If current limit is active, PWMxL is driven to the state specified by CLDAT<0>.

IFLTMOD (FCLCONx<15>) = 1: Independent Fault mode:
The CLDAT<1:0> bits are ignored.

bit 1 **SWAP:** Swap PWMxH and PWMxL Pins bit

1 = PWMxH output signal is connected to PWMxL pins; PWMxL output signal is connected to PWMxH pins
0 = PWMxH and PWMxL pins are mapped to their respective pins

bit 0 **OSYNC:** Output Override Synchronization bit

1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWM time base
0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary

**Note 1:** These bits should not be changed after the PWM module is enabled (PTEN = 1).

**REGISTER 16-20: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TRGCMP<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TRGCMP<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **TRGCMP<15:0>:** PWM Primary Trigger Control Value bits

When the primary PWM functions in local time base, this register contains the compare values that can trigger the ADC module.


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**REGISTER 16-21: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IFLTMOD | CLSRC<4:0>(2,3) | | | | | CLPOL(1) | CLMOD |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTSRC<4:0>(2,3) | | | | | FLTPOL(1) | FLTMOD<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **IFLTMOD:** Independent Fault Mode Enable bit
- 1 = Independent Fault mode: Current-limit input maps FLTDAT<1> to PWMxH output and Fault input maps FLTDAT<0> to PWMxL output; the CLDAT<1:0> bits are not used for override functions
- 0 = Normal Fault mode: Current-Limit mode maps CLDAT<1:0> bits to the PWMxH and PWMxL outputs; the PWM Fault mode maps FLTDAT<1:0> to the PWMxH and PWMxL outputs.

bit 14-10 **CLSRC<4:0>:** Current-Limit Control Signal Source Select for PWM Generator # bits(2,3)
- 11111 = Reserved
- •
- •
- •
- 01001 = Reserved
- 01010 = Comparator 3
- 01001 = Comparator 2
- 01000 = Comparator 1
- 00111 = Reserved
- 00110 = Fault 7
- 00101 = Fault 6
- 00100 = Fault 5
- 00011 = Fault 4
- 00010 = Fault 3
- 00001 = Fault 2
- 00000 = Fault 1

bit 9 **CLPOL:** Current-Limit Polarity bit for PWM Generator #(1)
- 1 = The selected current-limit source is active-low
- 0 = The selected current-limit source is active-high

bit 8 **CLMOD:** Current-Limit Mode Enable bit for PWM Generator #
- 1 = Current-Limit mode is enabled
- 0 = Current-Limit mode is disabled

**Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

**2:** When Independent Fault mode is enabled (IFLTMOD = 1) and Fault 1 is used for Fault mode (FLTSRC<4:0> = 01000), the Current-Limit Control Source Select bits (CLSRC<4:0>) should be set to an unused current-limit source to prevent the current-limit source from disabling both the PWMxH and PWMxL outputs.

**3:** When Independent Fault mode is enabled (IFLTMOD = 1) and Fault 1 is used for Current-Limit mode (CLSRC<4:0> = 01000), the Fault Control Source Select bits (FLTSRC<4:0>) should be set to an unused Fault source to prevent Fault 1 from disabling both the PWMxL and PWMxH outputs.

**REGISTER 16-21: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER (CONTINUED)**

bit 7-3 **FLTSRC<4:0>:** Fault Control Signal Source Select bits for PWM Generator #(2,3)
11111 = Reserved
•
•
•
01011 = Reserved
01010 = Comparator 3
01001 = Comparator 2
01000 = Comparator 1
00111 = Reserved
00110 = Fault 7
00101 = Fault 6
00100 = Fault 5
00011 = Fault 4
00010 = Fault 3
00001 = Fault 2
00000 = Fault 1

bit 2 **FLTPOL:** Fault Polarity bit for PWM Generator #(1)
1 = The selected Fault source is active-low
0 = The selected Fault source is active-high

bit 1-0 **FLTMOD<1:0>:** Fault Mode bits for PWM Generator #
11 = Fault input is disabled
10 = Reserved
01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (cycle)
00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDAT values (latched condition)

**Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

**2:** When Independent Fault mode is enabled (IFLTMOD = 1) and Fault 1 is used for Fault mode (FLTSRC<4:0> = 01000), the Current-Limit Control Source Select bits (CLSRC<4:0>) should be set to an unused current-limit source to prevent the current-limit source from disabling both the PWMxH and PWMxL outputs.

**3:** When Independent Fault mode is enabled (IFLTMOD = 1) and Fault 1 is used for Current-Limit mode (CLSRC<4:0> = 01000), the Fault Control Source Select bits (FLTSRC<4:0>) should be set to an unused Fault source to prevent Fault 1 from disabling both the PWMxL and PWMxH outputs.


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**REGISTER 16-22: LEBCONx: LEADING-EDGE BLANKING CONTROL REGISTER x**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | BCH(1) | BCL(1) | BPHH | BPHL | BPLH | BPLL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
1 = Rising edge of PWMxH will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores rising edge of PWMxH

bit 14 **PHF:** PWMxH Falling Edge Trigger Enable bit
1 = Falling edge of PWMxH will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores falling edge of PWMxH

bit 13 **PLR:** PWMxL Rising Edge Trigger Enable bit
1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores rising edge of PWMxL

bit 12 **PLF:** PWMxL Falling Edge Trigger Enable bit
1 = Falling edge of PWMxL will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores falling edge of PWMxL

bit 11 **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to selected Fault input
0 = Leading-Edge Blanking is not applied to selected Fault input

bit 10 **CLLEBEN:** Current-Limit Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to selected current-limit input
0 = Leading-Edge Blanking is not applied to selected current-limit input

bit 9-6 **Unimplemented:** Read as '0'

bit 5 **BCH:** Blanking in Selected Blanking Signal High Enable bit(1)
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high
0 = No blanking when selected blanking signal is high

bit 4 **BCL:** Blanking in Selected Blanking Signal Low Enable bit(1)
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low
0 = No blanking when selected blanking signal is low

bit 3 **BPHH:** Blanking in PWMxH High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high
0 = No blanking when PWMxH output is high

bit 2 **BPHL:** Blanking in PWMxH Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low
0 = No blanking when PWMxH output is low

bit 1 **BPLH:** Blanking in PWMxL High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high
0 = No blanking when PWMxL output is high

bit 0 **BPLL:** Blanking in PWMxL Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low
0 = No blanking when PWMxL output is low

**Note 1:** The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

**REGISTER 16-23: LEBDLYx: LEADING-EDGE BLANKING DELAY REGISTER x**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | LEB<11:8> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| LEB<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **LEB<11:0>:** Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits


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**REGISTER 16-24: AUXCONx: PWM AUXILIARY CONTROL REGISTER x**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | BLANKSEL<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | CHOPSEL<3:0> | | | | CHOPHEN | CHOPLEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **BLANKSEL<3:0>:** PWM State Blank Source Select bits

The selected state blank signal will block the current-limit and/or Fault input signals (if enabled via the BCH and BCL bits in the LEBCONx register).

1001 = Reserved
1000 = Reserved
0111 = PWM7H selected as state blank source
0110 = PWM6H selected as state blank source
0101 = PWM5H selected as state blank source
0100 = PWM4H selected as state blank source
0011 = PWM3H selected as state blank source
0010 = PWM2H selected as state blank source
0001 = PWM1H selected as state blank source
0000 = No state blanking

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHOPSEL<3:0>:** PWM Chop Clock Source Select bits

The selected signal will enable and disable (CHOP) the selected PWM outputs.

1001 = Reserved
1000 = Reserved
0111 = PWM7H selected as CHOP clock source
0110 = PWM6H selected as CHOP clock source
0101 = PWM5H selected as CHOP clock source
0100 = PWM4H selected as CHOP clock source
0011 = PWM3H selected as CHOP clock source
0010 = PWM2H selected as CHOP clock source
0001 = PWM1H selected as CHOP clock source
0000 = Chop clock generator selected as CHOP clock source

bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit

1 = PWMxH chopping function is enabled
0 = PWMxH chopping function is disabled

bit 0 **CHOPLEN:** PWMxL Output Chopping Enable bit

1 = PWMxL chopping function is enabled
0 = PWMxL chopping function is disabled

**REGISTER 16-25: PWMCAPx: PRIMARY PWMx TIME BASE CAPTURE REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PWMCAP<15:8>(1,2) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PWMCAP<7:0>(1,2) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PWMCAP<15:0>:** Captured PWM Time Base Value bits(1,2)

The value in this register represents the captured PWM time base value when a leading edge is detected on the current-limit input.

**Note 1:** The capture feature is only available on primary output (PWMxH).

**2:** This feature is active only after LEB processing on the current-limit input signal is complete.


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# 17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXX(MC/MU)8XX DEVICES ONLY)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Quadrature Encoder Interface (QEI)"** (DS70601) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

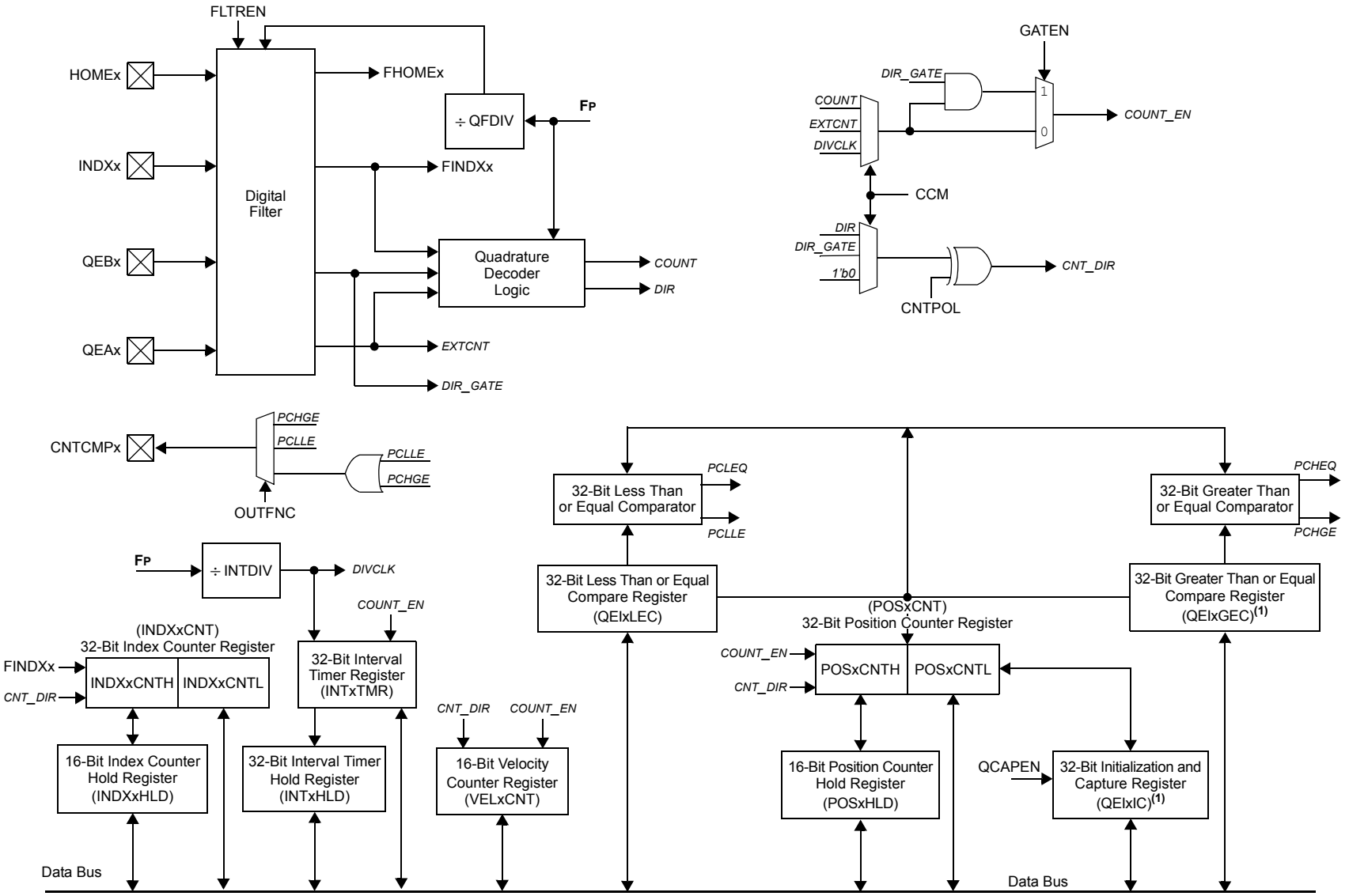
The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High Register
- 32-Bit Position Compare Low Register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

**Note:** An 'x' used in the names of pins, control/status bits and registers denotes a particular Quadrature Encoder Interface (QEI) module number (x = 1 or 2).

**FIGURE 17-1: QEI BLOCK DIAGRAM**




**Note 1:** These registers map to the same memory location.



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## 17.1 QEI Resources

Many useful resources related to QEI are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 17.1.1 KEY RESOURCES

- **Section 15. "Quadrature Encoder Interface (QEI)"** (DS70601) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 17.2 QEI Control Registers

**REGISTER 17-1: QEIxCON: QEIx CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIEN | — | QEISIDL | PIMOD<2:0>(1) | | | IMV<1:0>(2) | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | INTDIV<2:0>(3) | | | CNTPOL | GATEN | CCM<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **QEIEN:** Quadrature Encoder Interface Module Counter Enable bit
1 = Module counters are enabled
0 = Module counters are disabled, but SFRs can be read or written to

bit 14 **Unimplemented:** Read as '0'

bit 13 **QEISIDL:** QEI Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **PIMOD<2:0>:** Position Counter Initialization Mode Select bits(1)
111 = Reserved
110 = Modulo Count mode for position counter
101 = Resets the position counter when the position counter equals the QEIxGEC register
100 = Second index event after home event initializes position counter with contents of the QEIxIC register
011 = First index event after home event initializes position counter with contents of the QEIxIC register
010 = Next index input event initializes the position counter with contents of the QEIxIC register
001 = Every index input event resets the position counter
000 = Index input event does not affect position counter

bit 9-8 **IMV<1:0>:** Index Match Value bits(2)
11 = Index match occurs when QEB = 1 and QEA = 1
10 = Index match occurs when QEB = 1 and QEA = 0
01 = Index match occurs when QEB = 0 and QEA = 1
00 = Index input event does not affect position counter

bit 7 **Unimplemented:** Read as '0'

**Note 1:** When CCM = 10 or CCM = 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

**2:** When CCM = 00, and QEA and QEB values match Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset.

**3:** The selected clock rate should be at least twice the expected maximum quadrature count rate.


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**REGISTER 17-1: QEIxCON: QEIx CONTROL REGISTER (CONTINUED)**

bit 6-4 **INTDIV<2:0>:** Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select)(3)
111 = 1:128 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3 **CNTPOL:** Position and Index Counter/Timer Direction Select bit
1 = Counter direction is negative unless modified by external up/down signal
0 = Counter direction is positive unless modified by external up/down signal

bit 2 **GATEN:** External Count Gate Enable bit
1 = External gate signal controls position counter operation
0 = External gate signal does not affect position counter/timer operation

bit 1-0 **CCM<1:0>:** Counter Control Mode Selection bits
11 = Internal Timer mode with optional external count is selected
10 = External clock count with optional external count is selected
01 = External clock count with external up/down direction is selected
00 = Quadrature Encoder Interface (x4 mode) Count mode is selected

**Note 1:** When CCM = 10 or CCM = 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

**2:** When CCM = 00, and QEA and QEB values match Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset.

**3:** The selected clock rate should be at least twice the expected maximum quadrature count rate.

**REGISTER 17-2: QEIxIOC: QEIx I/O CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QCAPEN | FLTREN | QFDIV<2:0> | | | OUTFNC<1:0> | | SWPAB |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| HOMPOL | IDXPOL | QEBPOL | QEAPOL | HOME | INDEX | QEB | QEA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **QCAPEN:** Position Counter Input Capture Enable bit
1 = Positive edge detect of home input triggers position capture function
0 = HOMEx input event (positive edge) does not trigger a capture event

bit 14 **FLTREN:** QEAx/QEBx/INDXx/HOMEx Digital Filter Enable bit
1 = Input pin digital filter is enabled
0 = Input pin digital filter is disabled (bypassed)

bit 13-11 **QFDIV<2:0>:** QEAx/QEBx/INDXx/HOMEx Digital Input Filter Clock Divide Select bits
111 = 1:256 clock divide
110 = 1:64 clock divide
101 = 1:32 clock divide
100 = 1:16 clock divide
011 = 1:8 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide

bit 10-9 **OUTFNC<1:0>:** QEI Module Output Function Mode Select bits
11 = The CTNCMPx pin goes high when QEIxLEC ≥ POSxCNT ≥ QEIxGEC
10 = The CTNCMPx pin goes high when POSxCNT ≤ QEIxLEC
01 = The CTNCMPx pin goes high when POSxCNT ≥ QEIxGEC
00 = Output is disabled

bit 8 **SWPAB:** Swap QEA and QEB Inputs bit
1 = QEAx and QEBx are swapped prior to quadrature decoder logic
0 = QEAx and QEBx are not swapped

bit 7 **HOMPOL:** HOMEx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 6 **IDXPOL:** HOMEx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 5 **QEBPOL:** QEBx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 4 **QEAPOL:** QEAx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 3 **HOME:** Status of HOMEx Input Pin After Polarity Control bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'


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**REGISTER 17-2: QEIxIOC: QEIx I/O CONTROL REGISTER (CONTINUED)**

bit 2 **INDEX:** Status of INDXx Input Pin After Polarity Control bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

bit 1 **QEB:** Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

**REGISTER 17-3: QEIxSTAT: QEIx STATUS REGISTER**

| U-0 | U-0 | HS, R/C-0 | R/W-0 | HS, R/C-0 | R/W-0 | HS, R/C-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | PCHEQIRQ | PCHEQIEN | PCLEQIRQ | PCLEQIEN | POSOVIRQ | POSOVIEN |
| bit 15 | | | | | | | bit 8 |

| HS, R/C-0 | R/W-0 | HS, R/C-0 | R/W-0 | HS, R/C-0 | R/W-0 | HS, R/C-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PCIIRQ(1) | PCIIEN | VELOVIRQ | VELOVIEN | HOMIRQ | HOMIEN | IDXIRQ | IDXIEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | C = Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **PCHEQIRQ:** Position Counter Greater Than or Equal Compare Status bit
1 = POSxCNT ≥ QEIxGEC
0 = POSxCNT < QEIxGEC

bit 12 **PCHEQIEN:** Position Counter Greater Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 11 **PCLEQIRQ:** Position Counter Less Than or Equal Compare Status bit
1 = POSxCNT ≤ QEIxLEC
0 = POSxCNT > QEIxLEC

bit 10 **PCLEQIEN:** Position Counter Less Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 9 **POSOVIRQ:** Position Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred

bit 8 **POSOVIEN:** Position Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 7 **PCIIRQ:** Position Counter (Homing) Initialization Process Complete Status bit(1)
1 = POSxCNT was reinitialized
0 = POSxCNT was not reinitialized

bit 6 **PCIIEN:** Position Counter **(Homing)** Initialization Process Complete interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **VELOVIRQ:** Velocity Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has not occurred

bit 4 **VELOVIEN:** Velocity Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **HOMIRQ:** Status Flag for Home Event Status bit
1 = Home event has occurred
0 = No Home event has occurred

**Note 1:** This status bit is only applicable to PIMOD<2:0> modes '011' and '100'.


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**REGISTER 17-3: QEIxSTAT: QEIx STATUS REGISTER (CONTINUED)**

bit 2 **HOMIEN:** Home Input Event Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **IDXIRQ:** Status Flag for Index Event Status bit
1 = Index event has occurred
0 = No Index event has occurred

bit 0 **IDXIEN:** Index Input Event Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

**Note 1:** This status bit is only applicable to PIMOD<2:0> modes '011' and '100'.

**REGISTER 17-4: POSxCNTH: POSITION COUNTER x HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| POSCNT<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| POSCNT<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **POSCNT<31:16>:** High Word Used to Form 32-Bit Position Counter Register (POSxCNT) bits

**REGISTER 17-5: POSxCNTL: POSITION COUNTER x LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| POSCNT<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| POSCNT<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **POSCNT<15:0>:** Low Word Used to Form 32-Bit Position Counter Register (POSxCNT) bits

**REGISTER 17-6: POSxHLD: POSITION COUNTER x HOLD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| POSHLD<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| POSHLD<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **POSHLD<15:0>:** Hold Register for Reading and Writing POSxCNTH bits


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**REGISTER 17-7: VELxCNT: VELOCITY COUNTER x REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| VELCNT<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| VELCNT<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **VELCNT<15:0>:** Velocity Counter bits

**REGISTER 17-8: INDXxCNTH: INDEX COUNTER x HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INDXCNT<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INDXCNT<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **INDXCNT<31:16>:** High Word Used to Form 32-Bit Index Counter Register (INDXxCNT) bits

**REGISTER 17-9: INDXxCNTL: INDEX COUNTER x LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INDXCNT<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INDXCNT<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **INDXCNT<15:0>:** Low Word Used to Form 32-Bit Index Counter Register (INDXxCNT) bits

**REGISTER 17-10: INDXxHLD: INDEX COUNTER x HOLD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INDXHLD<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INDXHLD<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **INDXHLD<15:0>:** Hold Register for Reading and Writing INDXxCNTH bits

**REGISTER 17-11: QEIxICH: QEIx INITIALIZATION/CAPTURE HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIIC<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIIC<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEIIC<31:16>:** QEIx High Word Used to Form 32-Bit Initialization/Capture Register (QEIxIC) bits

**REGISTER 17-12: QEIxICL: QEIx INITIALIZATION/CAPTURE LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIIC<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIIC<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEIIC<15:0>:** QEIx Low Word Used to Form 32-Bit Initialization/Capture Register (QEIxIC) bits


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**REGISTER 17-13: QEIxLECH: QEIx LESS THAN OR EQUAL COMPARE HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEILEC<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEILEC<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEILEC<31:16>:** QEIx High Word Used to Form 32-Bit Less Than or Equal Compare Register (QEIxLEC) bits

**REGISTER 17-14: QEIxLECL: QEIx LESS THAN OR EQUAL COMPARE LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEILEC<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEILEC<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEILEC<15:0>:** QEIx Low Word Used to Form 32-Bit Less Than or Equal Compare Register (QEIxLEC) bits

**REGISTER 17-15: QEIxGECH: QEIx GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIGEC<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIGEC<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEIGEC<31:16>:** QEIx High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEIxGEC) bits

**REGISTER 17-16: QEIxGECL: QEIx GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIGEC<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIGEC<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEIGEC<15:0>:** QEIx Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEIxGEC) bits

**REGISTER 17-17: INTxTMRH: INTERVAL TIMER x HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTTMR<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTTMR<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **INTTMR<31:16>:** High Word Used to Form 32-Bit Interval Timer Register (INTxTMR) bits


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**REGISTER 17-18: INTxTMRL: INTERVAL TIMER x LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTTMR<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTTMR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **INTTMR<15:0>:** Low Word Used to Form 32-Bit Interval Timer Register (INTxTMR) bits

**REGISTER 17-19: INTxHLDH: INTERVAL TIMER x HOLD HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTHLD<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTHLD<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **INTHLD<31:16>:** Hold Register for Reading and Writing INTxTMRH bits

**REGISTER 17-20: INTxHLDL: INTERVAL TIMER x HOLD LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTHLD<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTHLD<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **INTHLD<15:0>:** Hold Register for Reading and Writing INTxTMRL bits

**NOTES:**


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## 18.0 SERIAL PERIPHERAL INTERFACE (SPI)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 18. "Serial Peripheral Interface (SPI)"** (DS70569) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with the Motorola® SPI and SIOP interfaces.

Four SPI modules are provided on a single device. These modules, which are designated as SPI1, SPI2, SPI3 and SPI4, are functionally identical with the exception that SPI2 is not remappable. The dedicated SDI2, SDO2 and SCK2 connections provide improved performance over SPI1, SPI3 and SPI4 (see **Section 32.0 "Electrical Characteristics"**). Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

**Note:** In this section, the SPI modules are referred to together as SPIx, or separately as SPI1, SPI2, SPI3 and SPI4. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1, SPI2, SPI3 or SPI4 module.

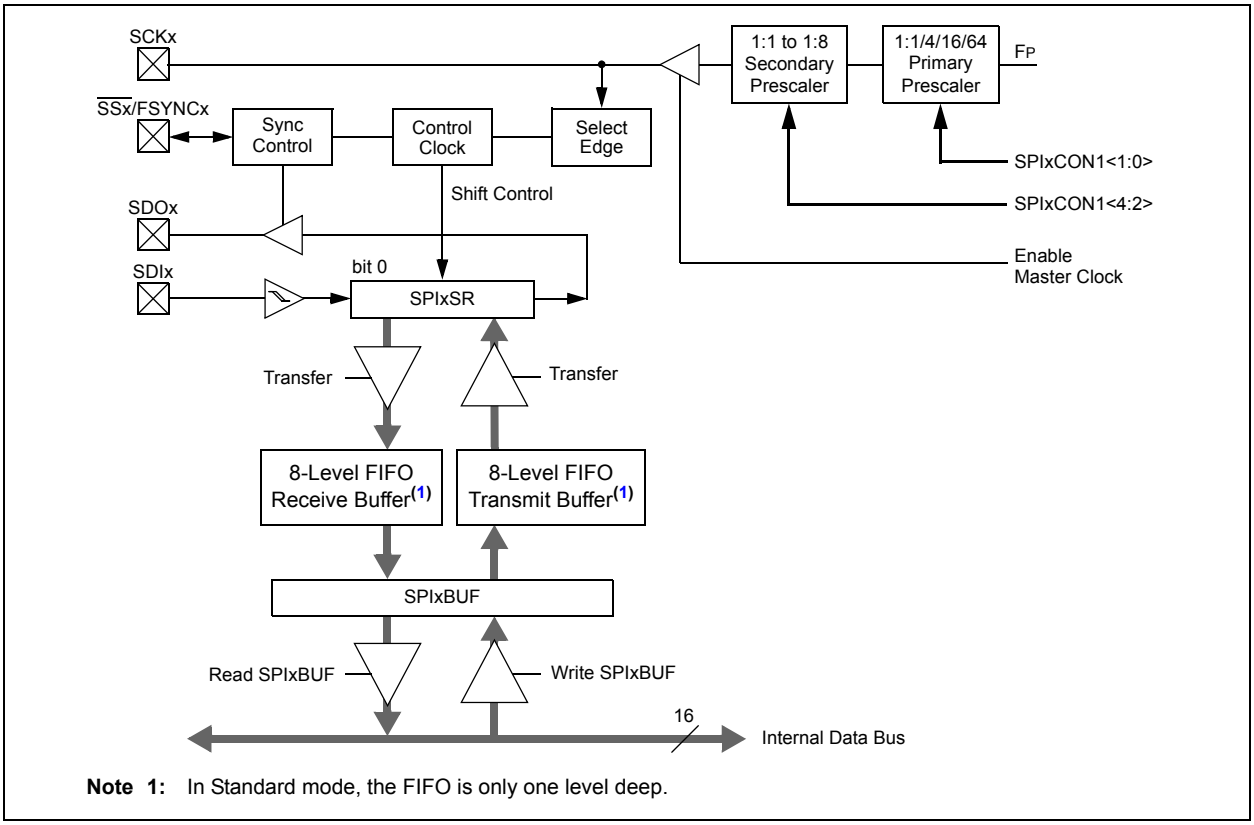
The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- $\overline{SS}$x/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, $\overline{SS}$x is not used. In 2-pin mode, neither SDOx nor $\overline{SS}$x is used.

Figure 18-1 illustrates the block diagram of the SPI module in Standard and Enhanced modes.

**FIGURE 18-1: SPIx MODULE BLOCK DIAGRAM**




**Note 1:** In Standard mode, the FIFO is only one level deep.

## 18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
   a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on SSx.
   b) If FRMPOL = 0, use a pull-up resistor on SSx.

| **Note:** | This insures that the first frame transmission after initialization is not shifted or corrupted. |
|---|---|

2. In Non-Framed 3-Wire mode, (i.e., not using SSx from a master):
   a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on SSx.
   b) If CKP = 0, always place a pull-down resistor on SSx.

| **Note:** | This will insure that during power-up and initialization, the master/slave will not lose synchronization due to an errant SCKx transition that would cause the slave to accumulate data shift errors, for both transmit and receive, appearing as corrupted data. |
|---|---|

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the SSx pin, which indicates the start of a data frame.

| **Note:** | Not all third-party devices support Frame mode timing. Refer to the SPIx electrical characteristics for details. |
|---|---|

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPI data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

## 18.2 SPI Resources

Many useful resources related to SPI are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554301 |
|---|---|

### 18.2.1 KEY RESOURCES

- **Section 18. "Serial Peripheral Interface (SPI)"** (DS70569) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools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## 18.3 SPI Control Registers

**REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SPIEN | — | SPISIDL | — | — | SPIBEC<2:0> | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/C-0, HS | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0, HS, HC | R-0, HS, HC |
|---|---|---|---|---|---|---|---|
| SRMPT | SPIROV | SRXMPT | SISEL<2:0> | | | SPITBF | SPIRBF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| HS = Hardware Settable bit | HC = Hardware Clearable bit | U = Unimplemented bit, read as '0' | |

bit 15 **SPIEN:** SPIx Enable bit
1 = Enables the module and configures SCKx, SDOx, SDIx and $\overline{SSx}$ as serial port pins
0 = Disables the module

bit 14 **Unimplemented:** Read as '0'

bit 13 **SPISIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues the module operation when device enters Idle mode
0 = Continues the module operation in Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **SPIBEC<2:0>:** SPIx Buffer Element Count bits (valid in Enhanced Buffer mode)
Master mode:
Number of SPIx transfers that are pending.
Slave mode:
Number of SPIx transfers that are unread.

bit 7 **SRMPT:** SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode)
1 = SPIx Shift register is empty and Ready-to-Send or receive the data
0 = SPIx Shift register is not empty

bit 6 **SPIROV:** SPIx Receive Overflow Flag bit
1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register
0 = No overflow has occurred

bit 5 **SRXMPT:** SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode)
1 = RX FIFO is empty
0 = RX FIFO is not empty

bit 4-2 **SISEL<2:0>:** SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)
111 = Interrupt when the SPIx transmit buffer is full
110 = Interrupt when last bit is shifted into SPIxSR, and as a result, the TX FIFO is empty
101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete
100 = Interrupt when one data is shifted into the SPIxSR, and as a result, the TX FIFO has one open memory location
011 = Interrupt when the SPIx receive buffer is full
010 = Interrupt when the SPIx receive buffer is 3/4 or more full
001 = Interrupt when data is available in the receive buffer (SRMPT bit is set)
000 = Interrupt when the last data in the receive buffer is read, and as a result, the buffer is empty (SRXMPT bit is set)

**REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit

1 = Transmit has not yet started, SPIx transmit buffer is full
0 = Transmit has started, SPIx transmit buffer is empty

Standard Buffer Mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading the SPIx transmit buffer. Automatically cleared in hardware when the SPIx module transfers data from the SPIx transmit buffer to SPIxSR.

Enhanced Buffer Mode:
Automatically set in hardware when CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit

1 = Receive complete, SPIx receive buffer is full
0 = Receive is incomplete, SPIx receive buffer is empty

Standard Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to the SPIx receive buffer. Automatically cleared in hardware when the core reads the SPIxBUF location, reading the SPIx receive buffer.

Enhanced Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.


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**REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DISSCK | DISSDO | MODE16 | SMP(4) | CKE(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SSEN(2) | CKP | MSTEN | SPRE<2:0>(3) | | | PPRE<1:0>(3) | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **DISSCK:** Disable SCKx Pin bit (SPIx Master modes only)
1 = Internal SPIx clock is disabled, pin functions as I/O
0 = Internal SPIx clock is enabled

bit 11 **DISSDO:** Disable SDOx Pin bit
1 = SDOx pin is not used by the module; pin functions as I/O
0 = SDOx pin is controlled by the module

bit 10 **MODE16:** Word/Byte Communication Select bit
1 = Communication is word-wide (16 bits)
0 = Communication is byte-wide (8 bits)

bit 9 **SMP:** SPIx Data Input Sample Phase bit(4)
Master mode:
1 = Input data is sampled at end of data output time
0 = Input data is sampled at middle of data output time
Slave mode:
The SMP bit must be cleared when SPIx module is used in Slave mode.

bit 8 **CKE:** SPIx Clock Edge Select bit(1)
1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)
0 = Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)(2)
1 = $\overline{SSx}$ pin is used for Slave mode
0 = $\overline{SSx}$ pin is not used by module, pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

**Note 1:** The CKE bit is not used in the Framed SPIx modes. Program this bit to '0' for Framed SPIx modes (FRMEN = 1).
**2:** This bit must be cleared when FRMEN = 1.
**3:** Do not set both primary and secondary prescalers to a value of 1:1.
**4:** The SMP bit must be set only after setting the MSTEN bit. The SMP bit remains cleared if MSTEN = 0.

**REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)**

bit 4-2 **SPRE<2:0>:** Secondary Prescale bits (Master mode)(3)

111 = Secondary prescale 1:1
110 = Secondary prescale 2:1
•
•
•
000 = Secondary prescale 8:1

bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)(3)

11 = Primary prescale 1:1
10 = Primary prescale 4:1
01 = Primary prescale 16:1
00 = Primary prescale 64:1

**Note 1:** The CKE bit is not used in the Framed SPIx modes. Program this bit to '0' for Framed SPIx modes (FRMEN = 1).

**2:** This bit must be cleared when FRMEN = 1.

**3:** Do not set both primary and secondary prescalers to a value of 1:1.

**4:** The SMP bit must be set only after setting the MSTEN bit. The SMP bit remains cleared if MSTEN = 0.


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**REGISTER 18-3: SPIxCON2: SPIx CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| FRMEN | SPIFSD | FRMPOL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | FRMDLY | SPIBEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FRMEN:** Framed SPIx Support bit
1 = Framed SPIx support is enabled ($\overline{SSx}$ pin is used as a Frame Sync pulse input/output)
0 = Framed SPIx support is disabled

bit 14 **SPIFSD:** Frame Sync Pulse Direction Control bit
1 = Frame Sync pulse input (slave)
0 = Frame Sync pulse output (master)

bit 13 **FRMPOL:** Frame Sync Pulse Polarity bit
1 = Frame Sync pulse is active-high
0 = Frame Sync pulse is active-low

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **FRMDLY:** Frame Sync Pulse Edge Select bit
1 = Frame Sync pulse coincides with the first bit clock
0 = Frame Sync pulse precedes the first bit clock

bit 0 **SPIBEN:** Enhanced Buffer Enable bit
1 = Enhanced Buffer is enabled
0 = Enhanced Buffer is disabled (Standard mode)

**NOTES:**


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## 19.0 INTER-INTEGRATED CIRCUIT™ ($I^2C$™)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Inter-Integrated Circuit™ ($I^2C$™)"** (DS70330) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 family of devices contain two Inter-Integrated Circuit ($I^2C$) modules: I2C1 and I2C2.

The $I^2C$ module provides complete hardware support for both Slave and Multi-Master modes of the $I^2C$ serial communication standard, with a 16-bit interface.

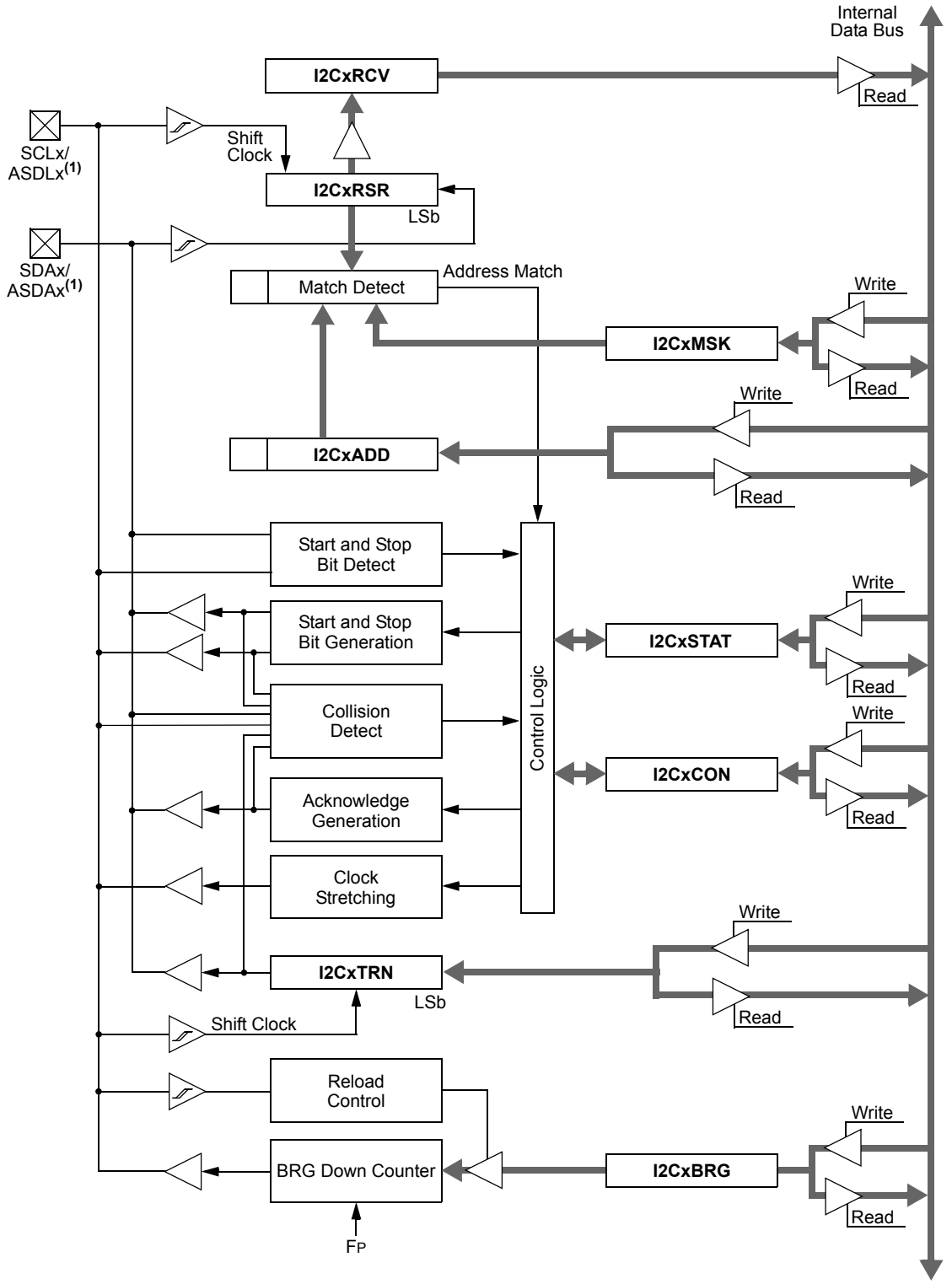
The $I^2C$ module has a 2-pin interface:

- The SCLx pin is the clock.
- The SDAx pin is the data.

The $I^2C$ module offers the following key features:

- $I^2C$ interface supporting both Master and Slave modes of operation.
- $I^2C$ Slave mode supports 7 and 10-bit addressing.
- $I^2C$ Master mode supports 7 and 10-bit addressing.
- $I^2C$ port allows bidirectional transfers between master and slaves.
- Serial clock synchronization for $I^2C$ port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control).
- $I^2C$ supports multi-master operation, detects bus collision and arbitrates accordingly.
- IPMI support
- SMBus support

**FIGURE 19-1: I²C™ BLOCK DIAGRAM (x = 1 OR 2)**




**Note 1:** The availability of I²C interfaces varies by device. Refer to the **"Pin Diagrams"** section for availability. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 29.0 "Special Features"** for more information.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## 19.1 I²C Resources

Many useful resources related to I²C are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 19.1.1 KEY RESOURCES

- **Section 19. "Inter-Integrated Circuit™ (I²C™)"** (DS70330) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 19.2 I²C Control Registers

**REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-1, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| I2CEN | — | I2CSIDL | SCLREL | IPMIEN(1) | A10M | DISSLW | SMEN |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0, HC | R/W-0, HC | R/W-0, HC | R/W-0, HC | R/W-0, HC |
|---|---|---|---|---|---|---|---|
| GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **I2CEN:** I2Cx Enable bit
1 = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins
0 = Disables the I2Cx module; all I²C™ pins are controlled by port functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **I2CSIDL:** I2Cx Stop in Idle Mode bit
1 = Discontinues module operation when device enters an Idle mode
0 = Continues module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)
1 = Releases SCLx clock
0 = Holds SCLx clock low (clock stretch)
If STREN = 1:
The bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware is clear at beginning of every slave data byte transmission. Hardware is clear at the end of every slave address byte reception. Hardware is clear at end of every slave data byte reception.
If STREN = 0:
The bit is R/S (i.e., software can only write '1' to release clock). Hardware is clear at beginning of every slave data byte transmission. Hardware is clear at the end of every slave address byte reception.

bit 11 **IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit(1)
1 = IPMI mode is enabled; all addresses Acknowledged
0 = IPMI mode is disabled

bit 10 **A10M:** 10-Bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control is disabled
0 = Slew rate control is enabled

bit 8 **SMEN:** SMBus Input Levels bit
1 = Enables I/O pin thresholds compliant with the SMBus specification
0 = Disables SMBus input thresholds

bit 7 **GCEN:** General Call Enable bit (when operating as I²C slave)
1 = Enables interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address is disabled

**Note 1:** When performing master operations, ensure that the IPMIEN bit is '0'.


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**REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)**

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as $I^2C$ slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as $I^2C$ master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (when operating as $I^2C$ master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits the ACKDT data bit. Hardware is clear at the end of a master Acknowledge sequence.
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as $I^2C$ master)
1 = Enables Receive mode for $I^2C$. Hardware is clear at the end of the eighth bit of a master receive data byte.
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as $I^2C$ master)
1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of a master Stop sequence.
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as $I^2C$ master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins. Hardware is clear at the end of a master Repeated Start sequence.
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as $I^2C$ master)
1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of a master Start sequence.
0 = Start condition is not in progress

**Note 1:** When performing master operations, ensure that the IPMIEN bit is '0'.

**REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER**

| R-0, HSC | R-0, HSC | U-0 | U-0 | U-0 | R/C-0, HS | R-0, HSC | R-0, HSC |
|---|---|---|---|---|---|---|---|
| ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 |
| bit 15 | | | | | | | bit 8 |

| R/C-0, HS | R/C-0, HS | R-0, HSC | R/C-0, HSC | R/C-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
|---|---|---|---|---|---|---|---|
| IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | U = Unimplemented bit, read as '0' | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | HS = Hardware Settable bit | HSC = Hardware Settable/Clearable bit |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as $I^2C$™ master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware is set or clear at the end of a slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as $I^2C$ master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware is set at the beginning of a master transmission. Hardware is clear at the end of a slave Acknowledge.

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware is set at detection of a bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware is set when an address matches the general call address. Hardware is clear at a Stop detection.

bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware is set at a match of the 2nd byte of a matched 10-bit address. Hardware is clear at a Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the $I^2C$ module is busy
0 = No collision
Hardware is set at an occurrence of a write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as $I^2C$ slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.


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**REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)**

bit 3 **S:** Start bit

1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

bit 2 **R_W:** Read/Write Information bit (when operating as $I^2C$ slave)

1 = Read – indicates data transfer is output from a slave
0 = Write – indicates data transfer is input to a slave
Hardware is set or clear after reception of an $I^2C$ device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit

1 = Receive is complete, I2CxRCV is full
0 = Receive is not complete, I2CxRCV is empty
Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit

1 = Transmit is in progress, I2CxTRN is full
0 = Transmit is complete, I2CxTRN is empty
Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of a data transmission.

**REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | AMSK9 | AMSK8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| AMSK7 | AMSK6 | AMSK5 | AMSK4 | AMSK3 | AMSK2 | AMSK1 | AMSK0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **AMSKx:** Mask for Address bit x Select bit

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disable masking for bit Ax + 1; bit match is required in this position


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## 20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. "UART"** (DS70582) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 family of devices contains four UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

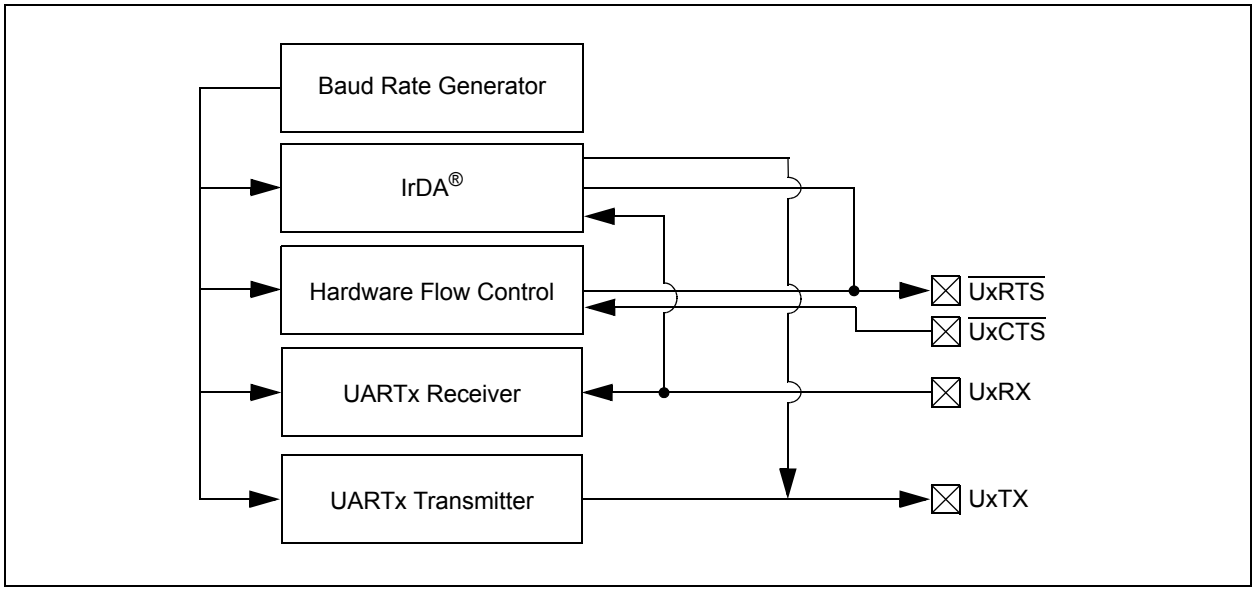
The primary features of the UARTx module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for All UARTx Error Conditions
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 20-1. The UARTx module consists of these key hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

**FIGURE 20-1: UARTx SIMPLIFIED BLOCK DIAGRAM**



## 20.1 UARTx Helpful Tips

1. In multi-node direct-connect UARTx networks, UARTx receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
   a) If URXINV = 0, use a pull-up resistor on the RX pin.
   b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on a wake-up from Sleep mode, caused by activity on the UxRX pin of the UARTx module, will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized resulting in the first character being invalid. This is to be expected.

## 20.2 UARTx Resources

Many useful resources related to the UARTx are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

### 20.2.1 KEY RESOURCES

- **Section 17. "UART"** (DS70582) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools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## 20.3 UARTx Registers

**REGISTER 20-1: UxMODE: UARTx MODE REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| UARTEN(1) | — | USIDL | IREN(2) | RTSMD | — | UEN<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0, HC | R/W-0 | R/W-0, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL<1:0> | | STSEL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **UARTEN:** UARTx Enable bit(1)
- 1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
- 0 = UARTx is disabled; all UARTx pins are controlled by port latches; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **USIDL:** UARTx Stop in Idle Mode bit
- 1 = Discontinues module operation when device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit(2)
- 1 = IrDA encoder and decoder are enabled
- 0 = IrDA encoder and decoder are disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Pin Enable bits
- 11 = UxTX, UxRX and BCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by port latches
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/BCLK pins are controlled by port latches

bit 7 **WAKE:** Wake-up on Start Bit Detect During Sleep Mode Enable bit
- 1 = UARTx continues to sample the UxRX pin; interrupt is generated on falling edge; bit is cleared in hardware on following rising edge
- 0 = No wake-up is enabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Enables Loopback mode
- 0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
- 1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion
- 0 = Baud rate measurement is disabled or has completed

**Note 1:** Refer to **Section 17. "UART"** (DS70582) in the *"dsPIC33E/PIC24E Family Reference Manual"* for information on enabling the UARTx module for receive or transmit operation.

**2:** This feature is only available for the 16x BRG mode (BRGH = 0).

**REGISTER 20-1: UxMODE: UARTx MODE REGISTER (CONTINUED)**

bit 4 **URXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

**Note 1:** Refer to **Section 17. "UART"** (DS70582) in the *"dsPIC33E/PIC24E Family Reference Manual"* for information on enabling the UARTx module for receive or transmit operation.

**2:** This feature is only available for the 16x BRG mode (BRGH = 0).


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**REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0, HC | R/W-0 | R-0 | R-1 |
|---|---|---|---|---|---|---|---|
| UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN(1) | UTXBF | TRMT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R-1 | R-0 | R-0 | R/C-0 | R-0 |
|---|---|---|---|---|---|---|---|
| URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | C = Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15,13 **UTXISEL<1:0>:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** UARTx Transmit Polarity Inversion bit

If IREN = 0:
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IREN = 1:
- 1 = IrDA encoded, UxTX Idle state is '1'
- 0 = IrDA encoded, UxTX Idle state is '0'

bit 12 **Unimplemented:** Read as '0'

bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or completed

bit 10 **UTXEN:** UARTx Transmit Enable bit(1)
- 1 = Transmit is enabled, UxTX pin is controlled by UARTx
- 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin controlled by port

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on UxRSR transfer making the receive buffer full (i.e., has 4 data characters)
- 10 = Interrupt is set on UxRSR transfer making the receive buffer 3/4 full (i.e., has 3 data characters)
- 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters

**Note 1:** Refer to **Section 17. "UART"** (DS70582) in the *"dsPIC33E/PIC24E Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

**REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
- 1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
- 0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
- 1 = Receiver is Idle
- 0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (read-only)
- 1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
- 0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
- 1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
- 0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (read/clear only)
- 1 = Receive buffer has overflowed
- 0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receiver buffer and the UxRSR to the empty state

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
- 1 = Receive buffer has data, at least one more character can be read
- 0 = Receive buffer is empty

**Note 1:** Refer to **Section 17. "UART"** (DS70582) in the *"dsPIC33E/PIC24E Family Reference Manual"* for information on enabling the UARTx module for transmit operation.


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# 21.0 ENHANCED CAN (ECAN™) MODULE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Enhanced Controller Area Network (ECAN™)"** (DS70353) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

## 21.1 Overview

The Enhanced Controller Area Network (ECAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/protocol was designed to allow communications within noisy environments. The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices contain two ECAN modules.

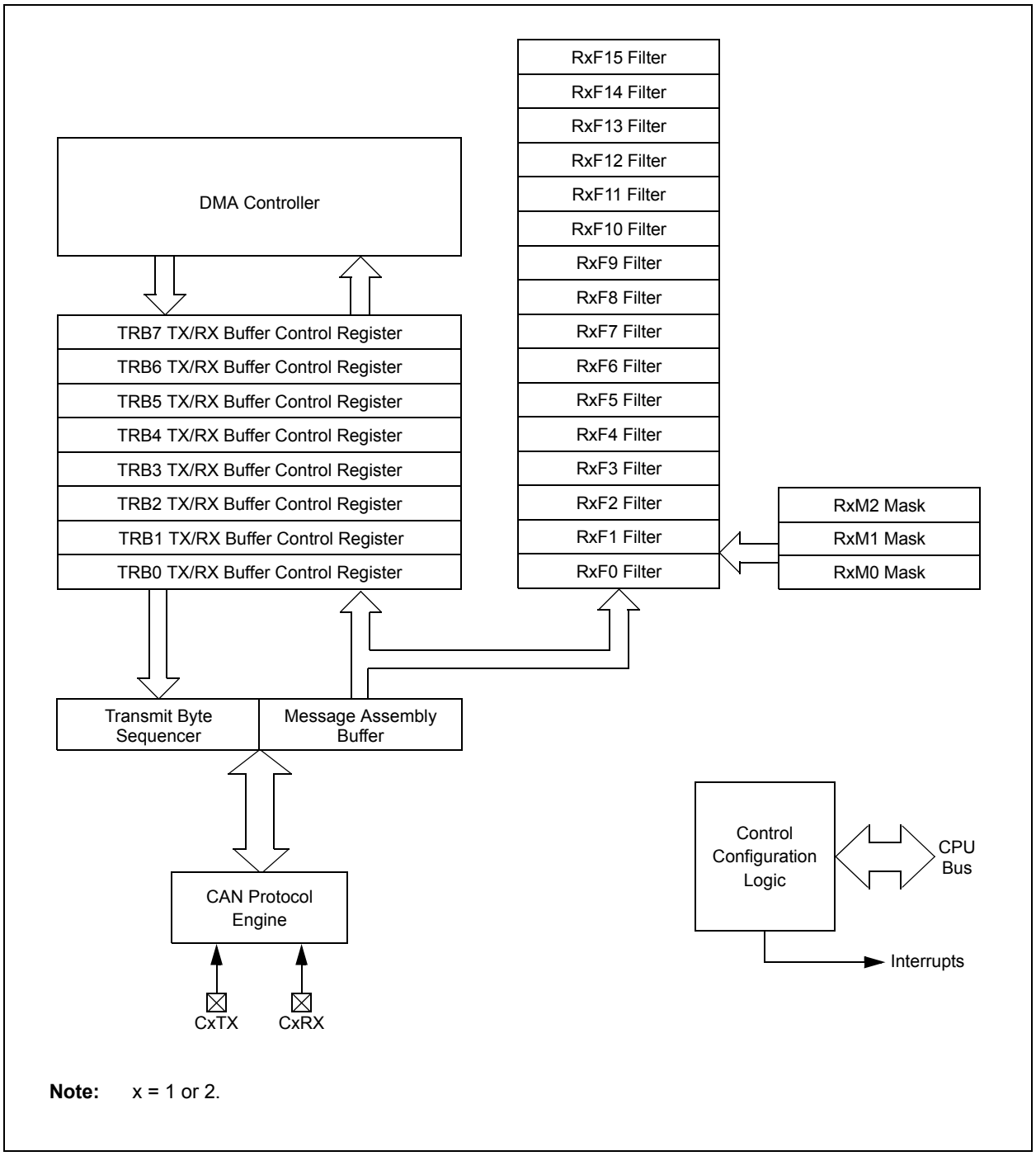
The ECANx module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN Specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN Specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details.

The ECANx module features are as follows:

- Implementation of the CAN Protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and Extended Data Frames
- 0-8 Bytes Data Length
- Programmable Bit Rate up to 1 Mbit/sec
- Automatic Response to Remote Transmission Requests
- Up to 8 Transmit Buffers with Application-Specific Prioritization and Abort Capability (each buffer can contain up to 8 bytes of data)
- Up to 32 Receive Buffers (each buffer can contain up to 8 bytes of data)
- Up to 16 Full (standard/extended identifier) Acceptance Filters
- Three Full Acceptance Filter Masks
- DeviceNet™ Addressing Support
- Programmable Wake-up Functionality with Integrated Low-Pass Filter
- Programmable Loopback mode Supports Self-Test Operation
- Signaling via Interrupt Capabilities for all CAN Receiver and Transmitter Error States
- Programmable Clock Source
- Programmable Link to Input Capture Module (IC2 for the ECAN1 and ECAN2 modules) for Time-Stamping and Network Synchronization
- Low-Power Sleep and Idle mode

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

**FIGURE 21-1: ECANx MODULE BLOCK DIAGRAM**




**Note:** x = 1 or 2.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## 21.2 Modes of Operation

The ECANx module can operate in one of several operation modes selected by the user. These modes include:

- Initialization mode
- Disable mode
- Normal Operation mode
- Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODE bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

## 21.3 ECAN Resources

Many useful resources related to ECAN are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 21.3.1 KEY RESOURCES

- **Section 21. "Enhanced Controller Area Network (ECAN™)"** (DS70353) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 21.4 ECANx Control Registers

**REGISTER 21-1: CxCTRL1: ECANx CONTROL REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | CSIDL | ABAT | CANCKS | REQOP<2:0> | | |
| bit 15 | | | | | | | bit 8 |

| R-1 | R-0 | R-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OPMODE<2:0> | | | — | CANCAP | — | — | WIN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** ECANx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ABAT:** Abort All Pending Transmissions bit
1 = Signals all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted

bit 11 **CANCKS:** ECANx Module Clock (FCAN) Source Select bit
1 = FCAN is equal to twice FP
0 = FCAN is equal to FP

bit 10-8 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Set Configuration mode
011 = Set Listen Only Mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 7-5 **OPMODE<2:0>:** Operation Mode bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 4 **Unimplemented:** Read as '0'

bit 3 **CANCAP:** CAN Message Receive Timer Capture Event Enable bit
1 = Enables input capture based on CAN message receive
0 = Disables CAN capture

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **WIN:** SFR Map Window Select bit
1 = Uses filter window
0 = Uses buffer window


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**REGISTER 21-2: CxCTRL2: ECANx CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DNCNT<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **DNCNT<4:0>**: DeviceNet™ Filter Bit Number bits

10010-11111 = Invalid selection
10001 = Compares up to Data Byte 3, bit 6 with EID<17>
•
•
•
00001 = Compares up to Data Byte 1, bit 7 with EID<0>
00000 = Does not compare data bytes

**REGISTER 21-3: CxVEC: ECANx INTERRUPT CODE REGISTER**

| U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | FILHIT<4:0> | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R-1 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | ICODE<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bits
10000-11111 = Reserved
01111 = Filter 15
•
•
•
00001 = Filter 1
00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits
1000101-1111111 = Reserved
1000100 = FIFO almost full interrupt
1000011 = Receiver overflow interrupt
1000010 = Wake-up interrupt
1000001 = Error interrupt
1000000 = No interrupt
•
•
•
0010000-0111111 = Reserved
0001111 = RB15 buffer interrupt
•
•
•
0001001 = RB9 buffer interrupt
0001000 = RB8 buffer interrupt
0000111 = TRB7 buffer interrupt
0000110 = TRB6 buffer interrupt
0000101 = TRB5 buffer interrupt
0000100 = TRB4 buffer interrupt
0000011 = TRB3 buffer interrupt
0000010 = TRB2 buffer interrupt
0000001 = TRB1 buffer interrupt
0000000 = TRB0 Buffer interrupt


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**REGISTER 21-4: CxFCTRL: ECANx FIFO CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| DMABS<2:0> | | | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | FSA<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **DMABS<2:0>:** DMA Buffer Size bits
111 = Reserved
110 = 32 buffers in DMA RAM
101 = 24 buffers in DMA RAM
100 = 16 buffers in DMA RAM
011 = 12 buffers in DMA RAM
010 = 8 buffers in DMA RAM
001 = 6 buffers in DMA RAM
000 = 4 buffers in DMA RAM

bit 12-5 **Unimplemented:** Read as '0'

bit 4-0 **FSA<4:0>:** FIFO Area Starts with Buffer bits
11111 = Read Buffer RB31
11110 = Read Buffer RB30
•
•
•
00001 = TX/RX Buffer TRB1
00000 = TX/RX Buffer TRB0

**REGISTER 21-5: CxFIFO: ECANx FIFO STATUS REGISTER**

| U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | FBP<5:0> | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | FNRB<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **FBP<5:0>:** FIFO Buffer Pointer bits

011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **FNRB<5:0>:** FIFO Next Read Buffer Pointer bits

011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer


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**REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER**

| U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | TXBO | TXBP | RXBP | TXWAR | RXWAR | EWARN |
| bit 15 | | | | | | | bit 8 |

| R/C-0 | R/C-0 | R/C-0 | U-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| IVRIF | WAKIF | ERRIF | — | FIFOIF | RBOVIF | RBIF | TBIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only ‘0’ can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **TXBO:** Transmitter in Error State Bus Off bit
1 = Transmitter is in Bus Off state
0 = Transmitter is not in Bus Off state

bit 12 **TXBP:** Transmitter in Error State Bus Passive bit
1 = Transmitter is in Bus Passive state
0 = Transmitter is not in Bus Passive state

bit 11 **RXBP:** Receiver in Error State Bus Passive bit
1 = Receiver is in Bus Passive state
0 = Receiver is not in Bus Passive state

bit 10 **TXWAR:** Transmitter in Error State Warning bit
1 = Transmitter is in Error Warning state
0 = Transmitter is not in Error Warning state

bit 9 **RXWAR:** Receiver in Error State Warning bit
1 = Receiver is in Error Warning state
0 = Receiver is not in Error Warning state

bit 8 **EWARN:** Transmitter or Receiver in Error State Warning bit
1 = Transmitter or Receiver is in Error State Warning state
0 = Transmitter or Receiver is not in Error State Warning state

bit 7 **IVRIF:** Invalid Message Interrupt Flag bit
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

bit 6 **WAKIF:** Bus Wake-up Activity Interrupt Flag bit
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

bit 5 **ERRIF:** Error Interrupt Flag bit (multiple sources in CxINTF<13:8> register)
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **FIFOIF:** FIFO Almost Full Interrupt Flag bit
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

bit 2 **RBOVIF:** RX Buffer Overflow Interrupt Flag bit
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

bit 1 **RBIF:** RX Buffer Interrupt Flag bit
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

bit 0 **TBIF:** TX Buffer Interrupt Flag bit
1 = Interrupt Request has occurred
0 = Interrupt Request has not occurred

**REGISTER 21-7: CxINTE: ECANx INTERRUPT ENABLE REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IVRIE | WAKIE | ERRIE | — | FIFOIE | RBOVIE | RBIE | TBIE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **IVRIE:** Invalid Message Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6 **WAKIE:** Bus Wake-up Activity Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **ERRIE:** Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **FIFOIE:** FIFO Almost Full Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **RBOVIE:** RX Buffer Overflow Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **RBIE:** RX Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **TBIE:** TX Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled


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**REGISTER 21-8: CxEC: ECANx TRANSMIT/RECEIVE ERROR COUNT REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| TERRCNT<7:0> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| RERRCNT<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **TERRCNT<7:0>:** Transmit Error Count bits

bit 7-0 **RERRCNT<7:0>:** Receive Error Count bits

**REGISTER 21-9: CxCFG1: ECANx BAUD RATE CONFIGURATION REGISTER 1**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SJW<1:0> | | BRP<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits

11 = Length is 4 x TQ
10 = Length is 3 x TQ
01 = Length is 2 x TQ
00 = Length is 1 x TQ

bit 5-0 **BRP<5:0>:** Baud Rate Prescaler bits

11 1111 = TQ = 2 x 64 x 1/FCAN
•
•
•
00 0010 = TQ = 2 x 3 x 1/FCAN
00 0001 = TQ = 2 x 2 x 1/FCAN
00 0000 = TQ = 2 x 1 x 1/FCAN

**REGISTER 21-10: CxCFG2: ECANx BAUD RATE CONFIGURATION REGISTER 2**

| U-0 | R/W-x | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | WAKFIL | — | — | — | SEG2PH<2:0> | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SEG2PHTS | SAM | SEG1PH<2:0> | | | PRSEG<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14 **WAKFIL:** Select CAN Bus Line Filter for Wake-up bit
1 = Uses CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 13-11 **Unimplemented:** Read as '0'

bit 10-8 **SEG2PH<2:0>:** Phase Segment 2 bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 7 **SEG2PHTS:** Phase Segment 2 Time Select bit
1 = Freely programmable
0 = Maximum of SEG1PH bits or Information Processing Time (IPT), whichever is greater

bit 6 **SAM:** Sample of the CAN Bus Line bit
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 5-3 **SEG1PH<2:0>:** Phase Segment 1 bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 2-0 **PRSEG<2:0>:** Propagation Time Segment bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ


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**REGISTER 21-11: CxFEN1: ECANx ACCEPTANCE FILTER ENABLE REGISTER 1**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| FLTEN15 | FLTEN14 | FLTEN13 | FLTEN12 | FLTEN11 | FLTEN10 | FLTEN9 | FLTEN8 |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| FLTEN7 | FLTEN6 | FLTEN5 | FLTEN4 | FLTEN3 | FLTEN2 | FLTEN1 | FLTEN0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **FLTENn:** Enable Filter n to Accept Messages bits
1 = Enables Filter n
0 = Disables Filter n

**REGISTER 21-12: CxBUFPNT1: ECANx FILTER 0-3 BUFFER POINTER REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F3BP<3:0> | | | | F2BP<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F1BP<3:0> | | | | F0BP<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **F3BP<3:0>:** RX Buffer Mask for Filter 3 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F2BP<3:0>:** RX Buffer Mask for Filter 2 bits (same values as bit 15-12)

bit 7-4 **F1BP<3:0>:** RX Buffer Mask for Filter 1 bits (same values as bit 15-12)

bit 3-0 **F0BP<3:0>:** RX Buffer Mask for Filter 0 bits (same values as bit 15-12)

**REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F7BP<3:0> | | | | F6BP<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F5BP<3:0> | | | | F4BP<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **F7BP<3:0>:** RX Buffer Mask for Filter 7 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>:** RX Buffer Mask for Filter 6 bits (same values as bit 15-12)

bit 7-4 **F5BP<3:0>:** RX Buffer Mask for Filter 5 bits (same values as bit 15-12)

bit 3-0 **F4BP<3:0>:** RX Buffer Mask for Filter 4 bits (same values as bit 15-12)

**REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F11BP<3:0> | | | | F10BP<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F9BP<3:0> | | | | F8BP<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **F11BP<3:0>:** RX Buffer Mask for Filter 11 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F10BP<3:0>:** RX Buffer Mask for Filter 10 bits (same values as bit 15-12)

bit 7-4 **F9BP<3:0>:** RX Buffer Mask for Filter 9 bits (same values as bit 15-12)

bit 3-0 **F8BP<3:0>:** RX Buffer Mask for Filter 8 bits (same values as bit 15-12)


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**REGISTER 21-15: CxBUFPNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F15BP<3:0> | | | | F14BP<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F13BP<3:0> | | | | F12BP<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **F15BP<3:0>:** RX Buffer Mask for Filter 15 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F14BP<3:0>:** RX Buffer Mask for Filter 14 bits (same values as bit 15-12)

bit 7-4 **F13BP<3:0>:** RX Buffer Mask for Filter 13 bits (same values as bit 15-12)

bit 3-0 **F12BP<3:0>:** RX Buffer Mask for Filter 12 bits (same values as bit 15-12)

**REGISTER 21-16: CxRXFnSID: ECANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER n (n = 0-15)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | U-0 | R/W-x | U-0 | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-5 **SID<10:0>:** Standard Identifier bits
1 = Message address bit, SIDx, must be '1' to match filter
0 = Message address bit, SIDx, must be '0' to match filter

bit 4 **Unimplemented:** Read as '0'

bit 3 **EXIDE:** Extended Identifier Enable bit
If MIDE = 1:
1 = Matches only messages with extended identifier addresses
0 = Matches only messages with standard identifier addresses
If MIDE = 0:
Ignores EXIDE bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID<17:16>:** Extended Identifier bits
1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter


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**REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER n (n = 0-15)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **EID<15:0>:** Extended Identifier bits
1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

**REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F7MSK<1:0> | | F6MSK<1:0> | | F5MSK<1:0> | | F4MSK<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F3MSK<1:0> | | F2MSK<1:0> | | F1MSK<1:0> | | F0MSK<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only '0' can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **F7MSK<1:0>:** Mask Source for Filter 7 bit
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F6MSK<1:0>:** Mask Source for Filter 6 bit (same values as bit 15-14)

bit 11-10 **F5MSK<1:0>:** Mask Source for Filter 5 bit (same values as bit 15-14)

bit 9-8 **F4MSK<1:0>:** Mask Source for Filter 4 bit (same values as bit 15-14)

bit 7-6 **F3MSK<1:0>:** Mask Source for Filter 3 bit (same values as bit 15-14)

bit 5-4 **F2MSK<1:0>:** Mask Source for Filter 2 bit (same values as bit 15-14)

bit 3-2 **F1MSK<1:0>:** Mask Source for Filter 1 bit (same values as bit 15-14)

bit 1-0 **F0MSK<1:0>:** Mask Source for Filter 0 bit (same values as bit 15-14)

**REGISTER 21-19: CxFMSKSEL2: ECANx FILTER 15-8 MASK SELECTION REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F15MSK<1:0> | | F14MSK<1:0> | | F13MSK<1:0> | | F12MSK<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F11MSK<1:0> | | F10MSK<1:0> | | F9MSK<1:0> | | F8MSK<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **F15MSK<1:0>:** Mask Source for Filter 15 bit
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F14MSK<1:0>:** Mask Source for Filter 14 bit (same values as bit 15-14)

bit 11-10 **F13MSK<1:0>:** Mask Source for Filter 13 bit (same values as bit 15-14)

bit 9-8 **F12MSK<1:0>:** Mask Source for Filter 12 bit (same values as bit 15-14)

bit 7-6 **F11MSK<1:0>:** Mask Source for Filter 11 bit (same values as bit 15-14)

bit 5-4 **F10MSK<1:0>:** Mask Source for Filter 10 bit (same values as bit 15-14)

bit 3-2 **F9MSK<1:0>:** Mask Source for Filter 9 bit (same values as bit 15-14)

bit 1-0 **F8MSK<1:0>:** Mask Source for Filter 8 bit (same values as bit 15-14)


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**REGISTER 21-20: CxRXMnSID: ECANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER n (n = 0-2)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | U-0 | R/W-x | U-0 | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-5 **SID<10:0>:** Standard Identifier bits
1 = Includes bit, SIDx, in filter comparison
0 = Bit, SIDx, is a don't care in filter comparison

bit 4 **Unimplemented:** Read as '0'

bit 3 **MIDE:** Identifier Receive Mode bit
1 = Matches only message types (standard or extended address) that correspond to EXIDE bit in filter
0 = Matches either standard or extended address message if filters match
(i.e., if (Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID))

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID<17:16>:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = Bit, EIDx, is a don't care in filter comparison

**REGISTER 21-21: CxRXMnEID: ECANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER n (n = 0-2)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **EID<15:0>:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = Bit, EIDx, is a don't care in filter comparison

**REGISTER 21-22: CxRXFUL1: ECANx RECEIVE BUFFER FULL REGISTER 1**

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXFUL15 | RXFUL14 | RXFUL13 | RXFUL12 | RXFUL11 | RXFUL10 | RXFUL9 | RXFUL8 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXFUL7 | RXFUL6 | RXFUL5 | RXFUL4 | RXFUL3 | RXFUL2 | RXFUL1 | RXFUL0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only '0' can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **RXFUL<15:0>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)

**REGISTER 21-23: CxRXFUL2: ECANx RECEIVE BUFFER FULL REGISTER 2**

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXFUL31 | RXFUL30 | RXFUL29 | RXFUL28 | RXFUL27 | RXFUL26 | RXFUL25 | RXFUL24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXFUL23 | RXFUL22 | RXFUL21 | RXFUL20 | RXFUL19 | RXFUL18 | RXFUL17 | RXFUL16 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only '0' can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **RXFUL<31:16>:** Receive Buffer n Full bits

1 = Buffer is full (set by module)

0 = Buffer is empty (cleared by user software)


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**REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1**

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF9 | RXOVF8 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only ‘0’ can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

**REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2**

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only ‘0’ can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **RXOVF<31:16>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

**REGISTER 21-26: CxTRmnCON: ECANx TX/RX BUFFER m CONTROL REGISTER (m = 0, 2, 4, 6; n = 1, 3, 5, 7)**

| R/W-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TXENn | TXABTn | TXLARBn | TXERRn | TXREQn | RTRENn | TXnPRI<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TXENm | TXABTm(1) | TXLARBm(1) | TXERRm(1) | TXREQm | RTRENm | TXmPRI<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 See definition for bits 7-0, controls Buffer n

bit 7 **TXENm:** TX/RX Buffer Selection bit
1 = Buffer TRBn is a transmit buffer
0 = Buffer TRBn is a receive buffer

bit 6 **TXABTm:** Message Aborted bit(1)
1 = Message was aborted
0 = Message completed transmission successfully

bit 5 **TXLARBm:** Message Lost Arbitration bit(1)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERRm:** Error Detected During Transmission bit(1)
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQm:** Message Send Request bit
1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent
0 = Clearing the bit to '0' while set requests a message abort

bit 2 **RTRENm:** Auto-Remote Transmit Enable bit
1 = When a remote transmit is received, TXREQm will be set
0 = When a remote transmit is received, TXREQm will be unaffected

bit 1-0 **TXmPRI<1:0>:** Message Transmission Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

**Note 1:** This bit is cleared when TXREQm is set.

**Note:** The buffers, SID, EID, DLC, Data Field and Receive Status registers are located in DMA RAM.


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## 21.5 ECAN Message Buffers

ECAN Message Buffers are part of DMA RAM memory. They are not ECAN Special Function Registers. The user application must directly write into the DMA RAM area that is configured for ECAN Message Buffers. The location and size of the buffer area is defined by the user application.

**BUFFER 21-1: ECAN™ MESSAGE BUFFER WORD 0**

| U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | SID10 | SID9 | SID8 | SID7 | SID6 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | SRR | IDE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-2 **SID<10:0>:** Standard Identifier bits

bit 1 **SRR:** Substitute Remote Request bit

When TXIDE = 0:
1 = Message will request remote transmission
0 = Normal message

When TXIDE = 1:
The SRR bit must be set to ‘1’.

bit 0 **IDE:** Extended Identifier bit

1 = Message will transmit extended identifier
0 = Message will transmit standard identifier

**BUFFER 21-2: ECAN™ MESSAGE BUFFER WORD 1**

| U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | — | EID17 | EID16 | EID15 | EID14 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID13 | EID12 | EID11 | EID10 | EID9 | EID8 | EID7 | EID6 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-0 **EID<17:6>:** Extended Identifier bits

**BUFFER 21-3: ECAN™ MESSAGE BUFFER WORD 2**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID5 | EID4 | EID3 | EID2 | EID1 | EID0 | RTR | RB1 |
| bit 15 | | | | | | | bit 8 |

| U-x | U-x | U-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | RB0 | DLC3 | DLC2 | DLC1 | DLC0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-10 **EID<5:0>:** Extended Identifier bits

bit 9 **RTR:** Remote Transmission Request bit
When TXIDE = 1:
1 = Message will request remote transmission
0 = Normal message
When TXIDE = 0:
The RTR bit is ignored.

bit 8 **RB1:** Reserved Bit 1
User must set this bit to '0' per CAN protocol.

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **RB0:** Reserved Bit 0
User must set this bit to '0' per CAN protocol.

bit 3-0 **DLC<3:0>:** Data Length Code bits

**BUFFER 21-4: ECAN™ MESSAGE BUFFER WORD 3**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 1 | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 0 | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Byte 1<15:8>:** ECAN Message Byte 0

bit 7-0 **Byte 0<7:0>:** ECAN Message Byte 1


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**BUFFER 21-5: ECAN™ MESSAGE BUFFER WORD 4**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 3 | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 2 | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Byte 3<15:8>:** ECAN Message Byte 3

bit 7-0 **Byte 2<7:0>:** ECAN Message Byte 2

**BUFFER 21-6: ECAN™ MESSAGE BUFFER WORD 5**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 5 | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 4 | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Byte 5<15:8>:** ECAN Message Byte 5

bit 7-0 **Byte 4<7:0>:** ECAN Message Byte 4

**BUFFER 21-7: ECAN™ MESSAGE BUFFER WORD 6**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 7 | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 6 | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Byte 7<15:8>:** ECAN Message Byte 7

bit 7-0 **Byte 6<7:0>:** ECAN Message Byte 6

**BUFFER 21-8: ECAN™ MESSAGE BUFFER WORD 7**

| U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | FILHIT<4:0>(1) | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Code bits(1)
Encodes the number of the filter that resulted in writing this buffer.

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** Only written by the module for receive buffers, unused for transmit buffers.


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# 22.0 USB ON-THE-GO (OTG) MODULE (dsPIC33EPXXXMU8XX AND PIC24EPGU8XX DEVICES ONLY)

**Note 1:** This data sheet is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 25. "USB On-The-Go (OTG)"** (DS70571) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

## 22.1 Overview

The Universal Serial Bus (USB) On-The-Go (OTG) module includes the following features:

- USB Full-Speed Support for Host and Device
- Low-Speed Host Support
- USB On-The-Go Support
- Integrated Signaling Resistors
- Integrated Analog Comparators for VBUS Monitoring
- Integrated USB Transceiver
- Hardware Performs Transaction Handshaking
- Endpoint Buffering Anywhere in System RAM
- Integrated DMA Controller to Access System RAM
- Support for all four transfer types:
  - Control
  - Interrupt
  - Bulk Data
  - Isochronous
- Queueing of up to Four Endpoint Transfers without Servicing
- USB 5V Charge Pump Controller

The USB module contains the analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host, full-speed device or OTG implementation with a minimum of external components.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), pull-up and pull-down resistors, and the register interface. Figure 22-1 illustrates the block diagram of the USB OTG module.

The device auxiliary clock generator provides the 48 MHz clock required for USB communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the protocol for data transfers. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

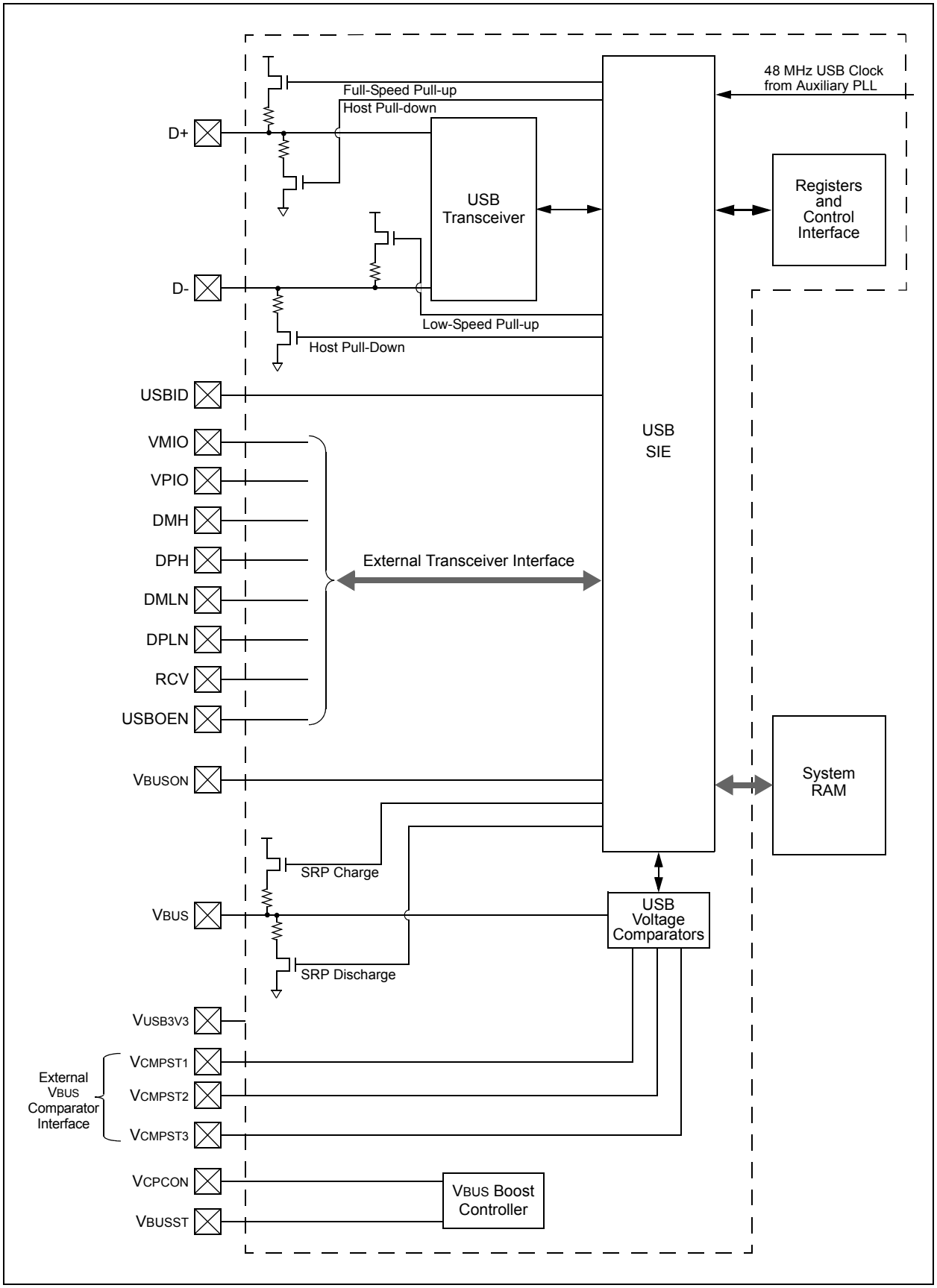
**Note:** The implementation and use of the USB specifications and other third party specifications or technology may require a license from various entities, including, but not limited to USB Implementers Forum, Inc. (also referred to as USB-IF). It is your responsibility to obtain more information regarding any applicable licensing obligations.

## 22.2 Clearing USB OTG Interrupts

Unlike device level interrupts, the USB OTG interrupt status flags are not freely writable in software. All USB OTG flag bits are implemented as hardware set-only bits. Additionally, these bits can only be cleared in software by writing a '1' to their locations (i.e., performing a BSET instruction). Writing a '0' to a flag bit (i.e., a BCLR instruction) has no effect.

**Note:** Throughout this section, a bit that can only be cleared by writing a '1' to its location is referred to as "Write '1' to clear bit". In register descriptions, this function is indicated by the descriptor, "K".

**FIGURE 22-1: USB INTERFACE DIAGRAM**





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## 22.3 USB OTG Resources

Many useful resources related to USB OTG are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

### 22.3.1 KEY RESOURCES

- **Section 11. "USB On-The-Go (OTG)"** (DS70571) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 22.4 USB Control Registers

**REGISTER 22-1: UxOTGSTAT: USB OTG STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R-0, HSC | U-0 | R-0, HSC | U-0 | R-0, HSC | R-0, HSC | U-0 | R-0, HSC |
|---|---|---|---|---|---|---|---|
| ID | — | LSTATE | — | SESVD | SESEND | — | VBUSVD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | U = Unimplemented bit, read as '0' | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | HSC = Hardware Settable/Clearable bit | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ID:** ID Pin State Indicator bit
1 = No cable is attached or a Type B plug has been plugged into the USB receptacle
0 = A Type A plug has been plugged into the USB receptacle

bit 6 **Unimplemented:** Read as '0'

bit 5 **LSTATE:** Line State Stable Indicator bit
1 = The USB line state (as defined by SE0 and JSTATE) has been stable for the previous 1 ms
0 = The USB line state has NOT been stable for the previous 1 ms

bit 4 **Unimplemented:** Read as '0'

bit 3 **SESVD:** Session Valid Indicator bit
1 = The VBUS voltage is above VA_SESS_VLD (as defined in the USB OTG Specification) on the A or B device
0 = The VBUS voltage is below VA_SESS_VLD on the A or B device

bit 2 **SESEND:** B-Session End Indicator bit
1 = The VBUS voltage is below VB_SESS_END (as defined in the USB OTG Specification) on the B device
0 = The VBUS voltage is above VB_SESS_END on the B device

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVD:** A-VBUS Valid Indicator bit
1 = The VBUS voltage is above VA_VBUS_VLD (as defined in the USB OTG Specification) on the A device
0 = The VBUS voltage is below VA_VBUS_VLD on the A device


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**REGISTER 22-2: UxOTGCON: USB ON-THE-GO CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DPPULUP | DMPULUP | DPPULDWN(1) | DMPULDWN(1) | VBUSON(1) | OTGEN(1) | VBUSCHG(1) | VBUSDIS(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **DPPULUP:** D+ Pull-Up Enable bit
1 = D+ data line pull-up resistor is enabled
0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit
1 = D- data line pull-up resistor is enabled
0 = D- data line pull-up resistor is disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit(1)
1 = D+ data line pull-down resistor is enabled
0 = D+ data line pull-down resistor is disabled

bit 4 **DMPULDWN:** D- Pull-Down Enable bit(1)
1 = D- data line pull-down resistor is enabled
0 = D- data line pull-down resistor is disabled

bit 3 **VBUSON:** VBUS Power-on bit(1)
1 = VBUS line is powered
0 = VBUS line is not powered

bit 2 **OTGEN:** OTG Features Enable bit(1)
1 = USB OTG is enabled; all D+/D- pull-ups and pull-downs are enabled
0 = USB OTG is disabled; D+/D- pull-ups and pull-downs are controlled in hardware by the settings of the HOSTEN and USBEN bits (UxCON<3,0>)

bit 1 **VBUSCHG:** VBUS Charge Selection bit(1)
1 = VBUS line is set to charge to 3.3V
0 = VBUS line is set to charge to 5V

bit 0 **VBUSDIS:** VBUS Discharge Enable bit(1)
1 = VBUS line is discharged through a resistor
0 = VBUS line is not discharged

**Note 1:** These bits are only used in Host mode; do not use in Device mode.

**REGISTER 22-3: UxPWRC: USB POWER CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| HS, HC | U-0 | U-0 | R/W | U-0 | U-0 | R/W-0, HC | R/W-0 |
|---|---|---|---|---|---|---|---|
| UACTPND | — | — | USLPGRD | — | — | USUSPND | USBPWR(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | HC = Hardware Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
1 = Module should not be suspended at the moment (requires the USLPGRD bit to be set)
0 = Module may be suspended or powered down

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Guard bit
1 = Indicates to the USB module that it is about to be suspended or powered down
0 = No suspend

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **USUSPND:** USB Suspend Mode Enable bit
1 = USB OTG module is in Suspend mode
0 = Normal USB OTG operation

bit 0 **USBPWR:** USB Operation Enable bit(1)
1 = USB OTG module is enabled
0 = USB OTG module is disabled

**Note 1:** Do not clear this bit unless the HOSTEN, USBEN and OTGEN bits (UxCON<3,0> and UxOTGCON<2>) are also cleared.


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**REGISTER 22-4: UxSTAT: USB STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| ENDPT<3:0>(2) | | | | DIR | PPBI(1) | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | U = Unimplemented bit, read as '0' | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | HSC = Hardware Settable/Clearable bit | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **ENDPT<3:0>:** Last Endpoint Activity Number bits
(represents the number of the endpoint BDT updated by the last USB transfer)(2)
1111 = Endpoint 15
1110 = Endpoint 14
•
•
•
0001 = Endpoint 1
0000 = Endpoint 0

bit 3 **DIR:** Last Buffer Descriptor Direction Indicator bit
1 = The last transaction was a transmit transfer (TX)
0 = The last transaction was a receive transfer (RX)

bit 2 **PPBI:** Ping-Pong Buffer Descriptor Pointer Indicator bit(1)
1 = The last transaction was to the ODD buffer descriptor bank
0 = The last transaction was to the EVEN buffer descriptor bank

bit 1-0 **Unimplemented:** Read as '0'

**Note 1:** This bit is only valid for endpoints with available EVEN and ODD buffer descriptor registers.

**2:** In Host mode, all transactions are processed through Endpoint 0 and the Endpoint 0 BDTs. Therefore, ENDPT<3:0> will always read as '0000'.

**REGISTER 22-5: UxCON: USB CONTROL REGISTER (DEVICE MODE)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R-x, HSC | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SE0 | PKTDIS | — | HOSTEN(1) | RESUME | PPBRST | USBEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | U = Unimplemented bit, read as '0' | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | HSC = Hardware Settable/Clearable bit | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **SE0:** Live Single-Ended Zero Flag bit
1 = Single-ended zero is active on the USB bus
0 = No single-ended zero is detected

bit 5 **PKTDIS:** Packet Transfer Disable bit
1 = SIE token and packet processing are disabled; automatically set when a SETUP token is received
0 = SIE token and packet processing are enabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **HOSTEN:** USB Host Mode Enable bit(1)
1 = USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
0 = USB host capability is disabled

bit 2 **RESUME:** USB Resume Signaling Enable bit
1 = Resume signaling is activated
0 = Resume signaling is disabled

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Resets all Ping-Pong Buffer Pointers to the EVEN buffer descriptor banks
0 = Ping-Pong Buffer Pointers are not reset

bit 0 **USBEN:** USB Module Enable bit
1 = USB module and supporting circuitry are enabled (device attached); D+ pull-up is activated in hardware
0 = USB module and supporting circuitry are disabled (device detached)

**Note 1:** This bit should be '0' in Device mode.


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**REGISTER 22-6: UxCON: USB CONTROL REGISTER (HOST MODE)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R-x, HSC | R-x, HSC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| JSTATE | SE0 | TOKBUSY | USBRST | HOSTEN | RESUME | PPBRST | SOFEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | U = Unimplemented bit, read as '0' | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | HSC = Hardware Settable/Clearable bit | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver J State Flag bit
1 = J state (differential '0' in low-speed, differential '1' in full-speed) is detected on the USB
0 = No J state is detected

bit 6 **SE0:** Live Single-Ended Zero Flag bit
1 = Single-ended zero is active on the USB bus
0 = No single-ended zero is detected

bit 5 **TOKBUSY:** Token Busy Status bit
1 = Token is being executed by the USB module in On-The-Go state
0 = No token is being executed

bit 4 **USBRST:** USB Reset bit
1 = USB Reset has been generated; for Software Reset, application must set this bit for 50 ms and then clear it
0 = USB Reset is terminated

bit 3 **HOSTEN:** USB Host Mode Enable bit
1 = USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
0 = USB host capability is disabled

bit 2 **RESUME:** USB Resume Signaling Enable bit
1 = Resume signaling is activated; software must set the bit for 10 ms and then clear to enable remote wake-up
0 = Resume signaling is disabled

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Resets all Ping-Pong Buffer Pointers to the EVEN buffer descriptor banks
0 = Ping-Pong Buffer Pointers are not reset

bit 0 **SOFEN:** USB Start-of-Frame (SOF) Enable bit
1 = Start-of-Frame token is sent every one 1 ms
0 = Start-of-Frame token is disabled

**REGISTER 22-7: UxADDR: USB ADDRESS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| LSPDEN(1) | DEVADDR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** USB Low-Speed Enable Indicator bit(1)
1 = USB module operates at low-speed
0 = USB module operates at full-speed

bit 6-0 **DEVADDR<6:0>:** USB Device Address bits

**Note 1:** Host mode only. In Device mode, this bit is unimplemented.

**REGISTER 22-8: UxTOK: USB TOKEN REGISTER (HOST MODE ONLY)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PID<3:0>(1) | | | | EP<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Identifier bits(1)
1101 = SETUP (TX) token type transaction
1001 = IN (RX) token type transaction
0001 = OUT (TX) token type transaction

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits
This value must specify a valid endpoint on the attached device.

**Note 1:** All other combinations are reserved and are not to be used.


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**REGISTER 22-9: UxSOF: USB OTG START-OF-TOKEN THRESHOLD REGISTER (HOST MODE ONLY)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CNT<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** Start-of-Frame Count bits
Value represents 10 + (packet size of n bytes); for example:
0100 1010 = 64-byte packet
0010 1010 = 32-byte packet
0001 0010 = 8-byte packet

**REGISTER 22-10: UxCNFG1: USB CONFIGURATION REGISTER 1**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| UTEYE | UOEMON(1) | — | USBSIDL | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye Pattern Test Enable bit
1 = Eye pattern test is enabled
0 = Eye pattern test is disabled

bit 6 **UOEMON:** USB $\overline{OE}$ Monitor Enable bit(1)
1 = $\overline{OE}$ signal is active; it indicates intervals during which the D+/D- lines are driving
0 = $\overline{OE}$ signal is inactive(1)

bit 5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** USB OTG Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 3-0 **Unimplemented:** Read as '0'

**Note 1:** When the UTRIS (UxCNFG2<0>) bit is set, the $\overline{OE}$ signal is active regardless of the setting of UOEMON.

**REGISTER 22-11: UxCNFG2: USB CONFIGURATION REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | UVCMPSEL | PUVBUS | EXTI2CEN | UVBUSDIS(1) | UVCMPDIS(1) | UTRDIS(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **UVCMPSEL:** USB External Comparator Input Mode Select bit

When UVCMPDIS is Set:

1 = Use 3-pin input for external comparators
0 = Use 2-pin input for external comparators

bit 4 **PUVBUS:** VBUS Pull-up Enable bit

1 = Pull-up on VBUS pin is enabled
0 = Pull-up on VBUS pin is disabled

bit 3 **EXTI2CEN:** I2C™ Interface for External Module Control Enable bit

1 = External module(s) controlled via I2C interface
0 = External module(s) controlled via dedicated pins

bit 2 **UVBUSDIS:** USB On-Chip 5V Boost Regulator Builder Disable bit(1)

1 = On-chip boost regulator builder is disabled; digital output control interface is enabled
0 = On-chip boost regulator builder is active

bit 1 **UVCMPDIS:** USB On-Chip VBUS Comparator Disable bit(1)

1 = On-chip charge VBUS comparator is disabled; digital input status interface is enabled
0 = On-chip charge VBUS comparator is active

bit 0 **UTRDIS:** USB On-Chip Transceiver Disable bit(1)

1 = On-chip transceiver is disabled; digital transceiver interface is enabled
0 = On-chip transceiver is active

**Note 1:** Do not change this bit while the USBPWR bit is set (UxPWRC<0> = 1).


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**REGISTER 22-12: UxOTGIR: USB OTG INTERRUPT STATUS REGISTER (HOST MODE ONLY)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | U-0 | R/K-0, HS |
|---|---|---|---|---|---|---|---|
| IDIF | T1MSECIF | LSTATEIF | ACTVIF | SESVDIF | SESENDIF | — | VBUSVDIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | U = Unimplemented bit, read as '0' | | |
|---|---|---|---|
| R = Readable bit | K = Write '1' to clear bit | HS = Hardware Settable bit | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
1 = Change in ID state is detected
0 = No ID state change

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
1 = The 1 millisecond timer has expired
0 = The 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
1 = USB line state (as defined by the SE0 and JSTATE bits) has been stable for 1 ms, but different from last time
0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit
1 = Activity on the D+/D- lines or VBUS is detected
0 = No activity on the D+/D- lines or VBUS is detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
1 = VBUS has crossed VA_SESS_VLD (as defined in the USB OTG Specification)(1)
0 = VBUS has not crossed VA_SESS_VLD

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
1 = VBUS change on B-device is detected; VBUS has crossed VB_SESS_END (as defined in the USB OTG Specification)(1)
0 = VBUS has not crossed VA_SESS_END

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
1 = VBUS change on A-device is detected; VBUS has crossed VA_VBUS_VLD (as defined in the USB OTG Specification)(1)
0 = No VBUS change on A-device is detected

**Note 1:** VBUS threshold crossings may be either rising or falling.

**REGISTER 22-13: UxOTGIE: USB OTG INTERRUPT ENABLE REGISTER (HOST MODE ONLY)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IDIE | T1MSECIE | LSTATEIE | ACTVIE | SESVDIE | SESENDIE | — | VBUSVDIE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **LSTATEIE:** Line State Stable Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **SESVDIE:** Session Valid Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **SESENDIE:** B-Device Session End Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-Device VBUS Valid Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled


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**REGISTER 22-14: UxIR: USB INTERRUPT STATUS REGISTER (DEVICE MODE ONLY)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/K-0, HS | U-0 | R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R-0 | R/K-0, HS |
|---|---|---|---|---|---|---|---|
| STALLIF | — | RESUMEIF | IDLEIF | TRNIF | SOFIF | UERRIF | URSTIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | U = Unimplemented bit, read as '0' | | |
|---|---|---|---|
| R = Readable bit | K = Write '1' to clear bit | HS = Hardware Settable bit | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit
- 1 = A STALL handshake was sent by the peripheral during the handshake phase of the transaction in Device mode
- 0 = A STALL handshake has not been sent

bit 6 **Unimplemented:** Read as '0'

bit 5 **RESUMEIF:** Resume Interrupt bit
- 1 = A K-State is observed on the D+ or D- pin for 2.5 μs (differential '1' for low speed, differential '0' for full speed)
- 0 = No K-State is observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit
- 1 = Idle condition is detected (constant Idle state of 3 ms or more)
- 0 = No Idle condition is detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit
- 1 = Processing of current token is complete; read UxSTAT register for endpoint BDT information
- 0 = Processing of current token is not complete; clear UxSTAT register or load next token from STAT (clearing this bit causes the the STAT FIFO to advance)

bit 2 **SOFIF:** Start-of-Frame Token Interrupt bit
- 1 = A Start-of-Frame token was received by the peripheral
- 0 = A Start-of-Frame token has not been received by the peripheral

bit 1 **UERRIF:** USB Error Condition Interrupt bit (read-only)
- 1 = An unmasked error condition has occurred; only error states enabled in the UxEIE register can set this bit
- 0 = No unmasked error condition has occurred

bit 0 **URSTIF:** USB Reset Interrupt bit
- 1 = Valid USB Reset has occurred for at least 2.5 μs; Reset state must be cleared before this bit can be reasserted
- 0 = No USB Reset has occurred

**REGISTER 22-15: UxIR: USB INTERRUPT STATUS REGISTER (HOST MODE ONLY)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R-0 | R/K-0, HS |
|---|---|---|---|---|---|---|---|
| STALLIF | ATTACHIF | RESUMEIF | IDLEIF | TRNIF | SOFIF | UERRIF | DETACHIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | U = Unimplemented bit, read as '0' | | |
|---|---|---|---|
| R = Readable bit | K = Write '1' to clear bit | HS = Hardware Settable bit | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit
- 1 = A STALL handshake was sent by the peripheral device during the handshake phase of the transaction in Device mode
- 0 = A STALL handshake has not been sent

bit 6 **ATTACHIF:** Peripheral Attach Interrupt bit
- 1 = A peripheral attachment has been detected by the module; set if the bus state is not SE0 and there has been no bus activity for 2.5 μs
- 0 = No peripheral attachment is detected

bit 5 **RESUMEIF:** Resume Interrupt bit
- 1 = A K-State is observed on the D+ or D- pin for 2.5 μs (differential '1' for low speed, differential '0' for full speed)
- 0 = No K-State is observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit
- 1 = Idle condition is detected (constant Idle state of 3 ms or more)
- 0 = No Idle condition is detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit
- 1 = Processing of current token is complete; read USTAT register for endpoint BDT information
- 0 = Processing of current token is not complete; clear USTAT register or load next token from STAT

bit 2 **SOFIF:** Start-of-Frame Token Interrupt bit
- 1 = Start-of-Frame threshold is reached by the host
- 0 = No Start-of-Frame token threshold is reached

bit 1 **UERRIF:** USB Error Condition Interrupt bit
- 1 = An unmasked error condition has occurred; only error states enabled in the UxEIE register can set this bit
- 0 = No unmasked error condition has occurred

bit 0 **DETACHIF:** Detach Interrupt bit
- 1 = A peripheral detachment has been detected by the module
- 0 = No peripheral detachment has been detected


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**REGISTER 22-16: UxIE: USB INTERRUPT ENABLE REGISTER (DEVICE MODE)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STALLIE | — | RESUMEIE | IDLEIE | TRNIE | SOFIE | UERRIE | URSTIE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **RESUMEIE:** Resume Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **SOFIE:** Start-of-Frame Token Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **UERRIE:** USB Error Condition Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

**REGISTER 22-17: UxIE: USB INTERRUPT ENABLE REGISTER (HOST MODE)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STALLIE | ATTACHIE(1) | RESUMEIE | IDLEIE | TRNIE | SOFIE | UERRIE | DETACHIE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **ATTACHIE:** Peripheral Attach Interrupt bit(1)
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **RESUMEIE:** Resume Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **SOFIE:** Start-of-Frame Token Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **UERRIE:** USB Error Condition Interrupt bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 0 **DETACHIE:** USB Detach Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

**Note 1:** Unimplemented in OTG mode, read as '0'.


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**REGISTER 22-18: UxEIR: USB ERROR INTERRUPT STATUS REGISTER (DEVICE MODE)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/K-0, HS | R/K-0,HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS |
|---|---|---|---|---|---|---|---|
| BTSEF | BUSACCEF | DMAEF | BTOEF | DFN8EF | CRC16EF | CRC5EF | PIDEF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | U = Unimplemented bit, read as '0' | | |
|---|---|---|---|
| R = Readable bit | K = Write '1' to clear bit | HS = Hardware Settable bit | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **BTSEF:** Bit Stuff Error Flag bit
1 = Bit stuff error has been detected
0 = No bit stuff error has been detected

bit 6 **BUSACCEF:** Bus Access Error Flag bit
1 = Peripheral tried to access an unimplemented RAM location
0 = RAM location access was successful

bit 5 **DMAEF:** DMA Error Flag bit
1 = A USB DMA error condition is detected; the data size indicated by the buffer descriptor byte count field is less than the number of received bytes; the received data is truncated
0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-out Error Flag bit
1 = Bus turnaround time-out has occurred
0 = No bus turnaround time-out has occurred

bit 3 **DFN8EF:** Data Field Size Error Flag bit
1 = Data field was not an integral number of bytes
0 = Data field was an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit
1 = CRC16 failed
0 = CRC16 passed

bit 1 **CRC5EF:** CRC5 Host Error Flag bit
1 = Token packet rejected due to CRC5 error
0 = Token packet accepted (no CRC5 error)

bit 0 **PIDEF:** PID Check Failure Flag bit
1 = PID check failed
0 = PID check passed

**REGISTER 22-19: UxEIR: USB ERROR INTERRUPT STATUS REGISTER (HOST MODE)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/K-0, HS | R/K-0,HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS | R/K-0, HS |
|---|---|---|---|---|---|---|---|
| BTSEF | BUSACCEF | DMAEF | BTOEF | DFN8EF | CRC16EF | EOFEF | PIDEF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | U = Unimplemented bit, read as ‘0’ | | |
|---|---|---|---|
| R = Readable bit | K = Write ‘1’ to clear bit | HS = Hardware Settable bit | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **BTSEF:** Bit Stuff Error Flag bit
1 = Bit stuff error has been detected
0 = No bit stuff error has been detected

bit 6 **BUSACCEF:** Bus Access Error Flag bit
1 = Peripheral tried to access an unimplemented RAM location
0 = RAM location access was successful

bit 5 **DMAEF:** DMA Error Flag bit
1 = A USB DMA error condition is detected; the data size indicated by the buffer descriptor byte count field is less than the number of received bytes, the received data is truncated
0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-out Error Flag bit
1 = Bus turnaround time-out has occurred
0 = No bus turnaround time-out has occurred

bit 3 **DFN8EF:** Data Field Size Error Flag bit
1 = Data field was not an integral number of bytes
0 = Data field was an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit
1 = CRC16 failed
0 = CRC16 passed

bit 1 **EOFEF:** End-of-Frame (EOF) Error Flag bit
1 = End-of-Frame error has occurred
0 = End-of-Frame interrupt is disabled

bit 0 **PIDEF:** PID Check Failure Flag bit
1 = PID check failed
0 = PID check passed


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**REGISTER 22-20: UxEIE: USB ERROR INTERRUPT ENABLE REGISTER (DEVICE MODE)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| BTSEE | BUSACCEE | DMAEE | BTOEE | DFN8EE | CRC16EE | CRC5EE | PIDEE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **BUSACCEE:** Bus Access Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

**REGISTER 22-21: UxEIE: USB ERROR INTERRUPT ENABLE REGISTER (HOST MODE)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| BTSEE | BUSACCEE | DMAEE | BTOEE | DFN8EE | CRC16EE | EOFEE | PIDEE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 6 **BUSACCEE:** Bus Access Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **EOFEE:** End-of-Frame Error interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled


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**REGISTER 22-22: UxEPn: USB ENDPOINT n CONTROL REGISTERS (n = 0 TO 15)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| LSPD(1) | RETRYDIS(1) | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **LSPD:** Low-Speed Direct Connection Enable bit (UEP0 only)(1)
1 = Direct connection to a low-speed device is enabled
0 = Direct connection to a low-speed device is disabled

bit 6 **RETRYDIS:** Retry Disable bit (UEP0 only)(1)
1 = Retry NAK transactions is disabled
0 = Retry NAK transactions is enabled; retry done in hardware

bit 5 **Unimplemented:** Read as '0'

bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit
If EPTXEN and EPRXEN = 1:
1 = Disable Endpoint n from control transfers; only TX and RX transfers are allowed
0 = Enable Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed
For all other combinations of EPTXEN and EPRXEN:
This bit is ignored.

bit 3 **EPRXEN:** Endpoint Receive Enable bit
1 = Endpoint n receive is enabled
0 = Endpoint n receive is disabled

bit 2 **EPTXEN:** Endpoint Transmit Enable bit
1 = Endpoint n transmit is enabled
0 = Endpoint n transmit is disabled

bit 1 **EPSTALL:** Endpoint Stall Status bit
1 = Endpoint n was stalled
0 = Endpoint n was not stalled

bit 0 **EPHSHK:** Endpoint Handshake Enable bit
1 = Endpoint handshake is enabled
0 = Endpoint handshake is disabled (typically used for isochronous endpoints)

**Note 1:** These bits are available only for UxEP0 and only in Host mode. For all other UxEPn registers, these bits are always unimplemented and read as '0'.

**REGISTER 22-23: UxBDTP1: USB BUFFER DESCRIPTION TABLE REGISTER 1**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| BDTPTRL<15:9> | | | | | | | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W =Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-1 **BDTPTRL<15:9>:** Endpoint BDT Start Address bits
Defines bits 15-9 of the 32-bit endpoint buffer descriptor table start address.

bit 0 **Unimplemented:** Read as ‘0’

**REGISTER 22-24: UxBDTP2: USB BUFFER DESCRIPTION TABLE REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| BDTPTRH<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **BDTPTRH<23:16>:** Endpoint BDT Start Address bits
Defines bits 23-16 of the 32-bit endpoint buffer descriptor table start address.


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**REGISTER 22-25: UxBDTP3: USB BUFFER DESCRIPTION TABLE REGISTER 3**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| BDTPTRU<31:24> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **BDTPTRU<31:24>:** Endpoint BDT Start Address bits
Defines bits 31-24 of the 32-bit endpoint buffer descriptor table start address.

**REGISTER 22-26: UxPWMCON: USB VBUS PWM GENERATOR CONTROL REGISTER**

| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PWMEN | — | — | — | — | — | PWMPOL | CNTEN |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **PWMEN:** PWM Enable bit
1 = PWM generator is enabled
0 = PWM generator is disabled; output is held in the Reset state specified by PWMPOL

bit 14-10 **Unimplemented:** Read as ‘0’

bit 9 **PWMPOL:** PWM Polarity bit
1 = PWM output is active-low and resets high
0 = PWM output is active-high and resets low

bit 8 **CNTEN:** PWM Counter Enable bit
1 = Counter is enabled
0 = Counter is disabled

bit 7-0 **Unimplemented:** Read as ‘0’

**REGISTER 22-27: UxPWMRRS: DUTY CYCLE AND PWM PERIOD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DC<7:0> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PER<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **DC<7:0>:** Duty Cycle bits
These bits select the PWM duty cycle.

bit 7-0 **PER<7:0>:** PWM Period bits
These bits select the PWM period.

**REGISTER 22-28: UxFRMH: USB FRAME NUMBER HIGH REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | FRM<10:8> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **FRM<10:8>:** 11-Bit Frame Number Upper 3 bits
These register bits are updated with the current frame number whenever a SOF token is received.


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**REGISTER 22-29: UxFRML: USB FRAME NUMBER LOW REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| FRM<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **FRM<7:0>:** 11-Bit Frame Number Lower 8 bits
These register bits are updated with the current frame number whenever a SOF token is received.

**NOTES:**


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# 23.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Analog-to-Digital Converter (ADC)"** (DS70621) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices have two ADC modules, ADC1 and ADC2. The ADC1 module supports up to 32 analog input channels. The ADC2 module supports up to 16 analog input channels.

On ADC1, the AD12B bit (AD1CON1<10>) allows each of the ADC modules to be configured by the user as either a 10-bit, 4 Sample-and-Hold (S&H) ADC (default configuration) or a 12-bit, 1 S&H ADC.

**Note:** The ADC1 module needs to be disabled before modifying the AD12B bit.

The ADC2 module only supports 10-bit operation with 4 S&H.

## 23.1 Key Features

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) Conversion
- Conversion Speeds of up to 1.1 Msps
- Up to 32 Analog Input Pins
- External Voltage Reference Input Pins
- Simultaneous Sampling of up to Four Analog Input Pins
- Automatic Channel Scan mode
- Selectable Conversion Trigger Source
- Selectable Buffer Fill modes
- Four Result Alignment Options (signed/unsigned, fractional/integer)
- Operation during CPU Sleep and Idle modes

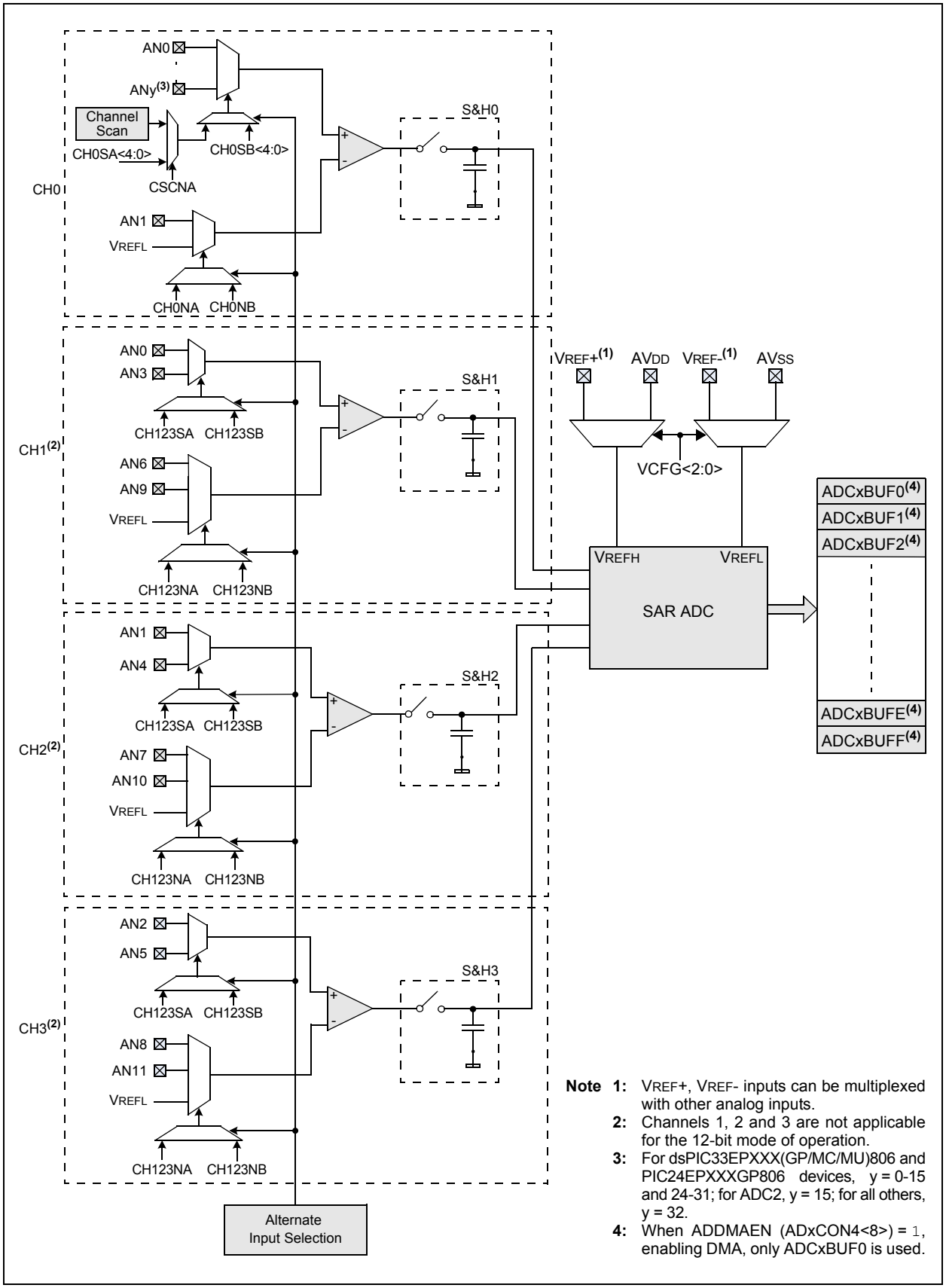
The 12-bit ADC configuration supports all the above features, except:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only one S&H amplifier in the 12-bit configuration, so simultaneous sampling of multiple channels is not supported.

Depending on the particular device pinout, the ADC can have up to 32 analog input pins, designated AN0 through AN31. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs can be shared with other analog input pins. The actual number of analog input pins and external voltage reference input configuration depends on the specific device.

A block diagram of the ADC module is shown in Figure 23-1. Figure 23-2 provides a diagram of the ADC conversion clock period.

**FIGURE 23-1: ADCx MODULE BLOCK DIAGRAM**




**Note 1:** VREF+, VREF- inputs can be multiplexed with other analog inputs.

**2:** Channels 1, 2 and 3 are not applicable for the 12-bit mode of operation.

**3:** For dsPIC33EPXXX(GP/MC/MU)806 and PIC24EPXXXGP806 devices, y = 0-15 and 24-31; for ADC2, y = 15; for all others, y = 32.

**4:** When ADDMAEN (ADxCON4<8>) = 1, enabling DMA, only ADCxBUF0 is used.


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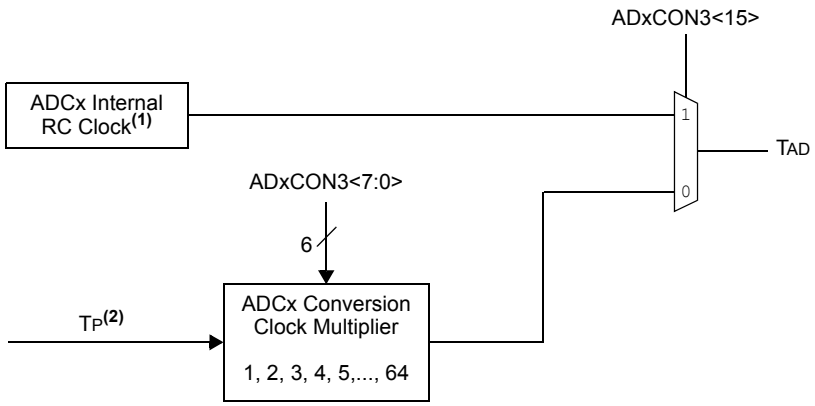
**FIGURE 23-2: ADCx CONVERSION CLOCK PERIOD BLOCK DIAGRAM**




**Note 1:** See the ADC electrical characteristics in **Section 32.0 "Electrical Characteristics"** for the exact RC clock value.
**2:** $T_P = 1/F_P$.

## 23.2 ADC Helpful Tips

1. The SMPIx control bits in the ADxCON2 registers:
   a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
   b) When the CSCNA bit in the ADxCON2 register is set to '1', this determines when the ADC analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.
   c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
   d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.
2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
3. When the DMA module is disabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADC1BUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA controller, before the next ADC conversion is complete to avoid overwriting the previous value.
4. The DONE bit (ADxCON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (ADxCON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.

## 23.3 ADC Resources

Many useful resources related to Analog-to-Digital conversion are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |
|---|---|

### 23.3.1 KEY RESOURCES

- **Section 16. "Analog-to-Digital Converter (ADC)"** (DS70621) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools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## 23.4 ADC Control Registers

**REGISTER 23-1: ADxCON1: ADCx CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADON | — | ADSIDL | ADDMABM | — | AD12B(1) | FORM<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0, HSC | R/C-0, HSC |
|---|---|---|---|---|---|---|---|
| SSRC<2:0> | | | SSRCG | SIMSAM | ASAM(3) | SAMP | DONE(3) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | HSC = Hardware Settable/Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ADON:** ADC Operating Mode bit
1 = ADC module is operating
0 = ADC is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** ADC Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ADDMABM:** DMA Buffer Build Mode bit
1 = DMA buffers are written in the order of conversion; the module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer
0 = DMA buffers are written in Scatter/Gather mode; the module provides a Scatter/Gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer

bit 11 **Unimplemented:** Read as '0'

bit 10 **AD12B:** ADC 10-Bit or 12-Bit Operation Mode bit(1)
1 = 12-bit, 1-channel ADC operation
0 = 10-bit, 4-channel ADC operation

bit 9-8 **FORM<1:0>:** Data Output Format bits
For 10-Bit Operation:
11 = Signed fractional (DOUT = sddd dddd dd00 0000, where s = .NOT.d<9>)
10 = Fractional (DOUT = dddd dddd dd00 0000)
01 = Signed integer (DOUT = ssss sssd dddd dddd, where s = .NOT.d<9>)
00 = Integer (DOUT = 0000 00dd dddd dddd)
For 12-Bit Operation:
11 = Signed fractional (DOUT = sddd dddd dddd 0000, where s = .NOT.d<11>)
10 = Fractional (DOUT = dddd dddd dddd 0000)
01 = Signed Integer (DOUT = ssss sddd dddd dddd, where s = .NOT.d<11>)
00 = Integer (DOUT = 0000 dddd dddd dddd)

**Note 1:** This bit is only available in the ADC1 module. In the ADC2 module, this bit is unimplemented and is read as '0'.
**2:** This setting is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.
**3:** Do not clear the DONE bit in software if ADC Sample Auto-Start is enabled (ASAM = 1).

**REGISTER 23-1: ADxCON1: ADCx CONTROL REGISTER 1 (CONTINUED)**

bit 7-5 **SSRC<2:0>:** Sample Clock Source Select bits

If SSRCG = 1:
111 = Reserved
110 = PWM Generator 7 primary trigger compare ends sampling and starts conversion(2)
101 = PWM Generator 6 primary trigger compare ends sampling and starts conversion(2)
100 = PWM Generator 5 primary trigger compare ends sampling and starts conversion(2)
011 = PWM Generator 4 primary trigger compare ends sampling and starts conversion(2)
010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion(2)
001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion(2)
000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion(2)

If SSRCG = 0:
111 = Internal counter ends sampling and starts conversion (auto-convert)
110 = Reserved
101 = PWM secondary Special Event Trigger ends sampling and starts conversion(2)
100 = Timer5 compare ends sampling and starts conversion
011 = PWM primary Special Event Trigger ends sampling and starts conversion(2)
010 = Timer3 compare ends sampling and starts conversion
001 = Active transition on the INT0 pin ends sampling and starts conversion
000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)

bit 4 **SSRCG:** Sample Clock Source Group bit

(See bits<7-5> for details.)

bit 3 **SIMSAM:** Simultaneous Sample Select bit (only applicable when CHPS<1:0> = 01 or 1x)

When AD12B = 1, SIMSAM is: U-0, Unimplemented, Read as '0'
1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS<1:0> = 1x); or samples CH0 and CH1 simultaneously (when CHPS<1:0> = 01)
0 = Samples multiple channels individually in sequence

bit 2 **ASAM:** ADC Sample Auto-Start bit(3)

1 = Sampling begins immediately after the last conversion; SAMP bit is auto-set
0 = Sampling begins when the SAMP bit is set

bit 1 **SAMP:** ADC Sample Enable bit

1 = ADC S&H amplifiers are sampling
0 = ADC S&H amplifiers are holding
If ASAM = 0, software can write '1' to begin sampling. Automatically set by hardware if ASAM = 1.
If SSRC = 000, software can write '0' to end sampling and start conversion. If SSRC ≠ 000, automatically cleared by hardware to end sampling and start conversion.

bit 0 **DONE:** ADC Conversion Status bit(3)

1 = ADC conversion cycle is completed.
0 = ADC conversion has not started or is in progress
Automatically set by hardware when ADC conversion is complete. Software can write '0' to clear the DONE status (software not allowed to write '1'). Clearing this bit does NOT affect any operation in progress. Automatically cleared by hardware at the start of a new conversion.

**Note 1:** This bit is only available in the ADC1 module. In the ADC2 module, this bit is unimplemented and is read as '0'.

**2:** This setting is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

**3:** Do not clear the DONE bit in software if ADC Sample Auto-Start is enabled (ASAM = 1).


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**REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| VCFG<2:0> | | | — | — | CSCNA | CHPS<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| BUFS | SMPI<4:0> | | | | | BUFM | ALTS |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **VCFG<2:0>:** Converter Voltage Reference Configuration bits

| | VREFH | VREFL |
|---|---|---|
| 000 | AVDD | Avss |
| 001 | External VREF+ | Avss |
| 010 | AVDD | External VREF- |
| 011 | External VREF+ | External VREF- |
| 1xx | AVDD | Avss |

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit
1 = Scans inputs for CH0+ during Sample A bit
0 = Does not scan inputs

bit 9-8 **CHPS<1:0>:** Channel Select bits
When AD12B = 1, CHPS<1:0> is: U-0, Unimplemented, Read as '0':
1x = Converts CH0, CH1, CH2 and CH3
01 = Converts CH0 and CH1
00 = Converts CH0

bit 7 **BUFS:** Buffer Fill Status bit (only valid when BUFM = 1)
1 = ADC is currently filling the second half of the buffer; the user application should access data in the first half of the buffer
0 = ADC is currently filling the first half of the buffer; the user application should access data in the second half of the buffer

bit 6-2 **SMPI<4:0>:** Increment Rate bits
When ADDMAEN = 0:
01111 = Generates interrupt after completion of every 16th sample/conversion operation
01110 = Generates interrupt after completion of every 15th sample/conversion operation
•
•
•
00001 = Generates interrupt after completion of every 2nd sample/conversion operation
00000 = Generates interrupt after completion of every sample/conversion operation
When ADDMAEN = 1:
11111 = Increments the DMA address after completion of every 32nd sample/conversion operation
11110 = Increments the DMA address after completion of every 31st sample/conversion operation
•
•
•
00001 = Increments the DMA address after completion of every 2nd sample/conversion operation
00000 = Increments the DMA address after completion of every sample/conversion operation

**REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2 (CONTINUED)**

bit 1 **BUFM:** Buffer Fill Mode Select bit
1 = Starts filling the first half of the buffer on the first interrupt and the second half of the buffer on the next interrupt
0 = Always starts filling the buffer from the Start address.

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses channel input selects for Sample A on the first sample and Sample B on the next sample
0 = Always uses channel input selects for Sample A


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**REGISTER 23-3: AD2CON2: ADC2 CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| VCFG<2:0> | | | — | — | CSCNA | CHPS<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| BUFS | — | SMPI<3:0> | | | | BUFM | ALTS |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **VCFG<2:0>:** Converter Voltage Reference Configuration bits

| | VREFH | VREFL |
|---|---|---|
| 000 | AVDD | Avss |
| 001 | External VREF+ | Avss |
| 010 | AVDD | External VREF- |
| 011 | External VREF+ | External VREF- |
| 1xx | AVDD | Avss |

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit
1 = Scans inputs for CH0+ during Sample A bit
0 = Does not scan inputs

bit 9-8 **CHPS<1:0>:** Channel Select bits
When AD12B = 1, CHPS<1:0> is: U-0, Unimplemented, Read as '0':
1x = Converts CH0, CH1, CH2 and CH3
01 = Converts CH0 and CH1
00 = Converts CH0

bit 7 **BUFS:** Buffer Fill Status bit (only valid when BUFM = 1)
1 = ADC is currently filling the second half of the buffer; the user application should access data in the first half of the buffer
0 = ADC is currently filling the first half of the buffer; the user application should access data in the second half of the buffer

bit 6-2 **SMPI<3:0>:** Increment Rate bits
When ADDMAEN = 0:
1111 = Generates interrupt after completion of every 16th sample/conversion operation
1110 = Generates interrupt after completion of every 15th sample/conversion operation
•
•
•
0001 = Generates interrupt after completion of every 2nd sample/conversion operation
0000 = Generates interrupt after completion of every sample/conversion operation
When ADDMAEN = 1:
1111 = Increments the DMA address after completion of every 16th sample/conversion operation
1110 = Increments the DMA address after completion of every 15th sample/conversion operation
•
•
•
0001 = Increments the DMA address after completion of every 2nd sample/conversion operation
0000 = Increments the DMA address after completion of every sample/conversion operation

**REGISTER 23-3: AD2CON2: ADC2 CONTROL REGISTER 2 (CONTINUED)**

bit 1 **BUFM:** Buffer Fill Mode Select bit
1 = Starts buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on the next interrupt
0 = Always starts filling the buffer from the Start address

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses channel input selects for Sample A on first sample and Sample B on next sample
0 = Always uses channel input selects for Sample A


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**REGISTER 23-4: ADxCON3: ADCx CONTROL REGISTER 3**

| R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADRC | — | — | SAMC<4:0>(1) | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADCS<7:0>(2,3) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ADRC:** ADC Conversion Clock Source bit
1 = ADC internal RC clock
0 = Clock Derived From System Clock

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits(1)
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits(2,3)
11111111 = TP • (ADCS<7:0> + 1) = 256 • TCY = TAD
•
•
•
00000010 = TP • (ADCS<7:0> + 1) = 3 • TCY = TAD
00000001 = TP • (ADCS<7:0> + 1) = 2 • TCY = TAD
00000000 = TP • (ADCS<7:0> + 1) = 1 • TCY = TAD

**Note 1:** This bit is only used if ADxCON1<7:5> (SSRC<2:0>) = 111 and ADxCON1<4> (SSRCG) = 0.
**2:** This bit is not used if ADxCON3<15> (ADRC) = 1.
**3:** TP = 1/FP.

**REGISTER 23-5: ADxCON4: ADCx CONTROL REGISTER 4**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | ADDMAEN |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | DMABL<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **ADDMAEN:** ADC DMA Enable bit
1 = Conversion results are stored in ADCxBUF0 register for transferring to RAM using DMA
0 = Conversion results are stored in ADCxBUF0 through ADCxBUFF registers; DMA will not be used

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **DMABL<2:0>:** Selects Number of DMA Buffer Locations per Analog Input bits
111 = Allocates 128 words of buffer to each analog input
110 = Allocates 64 words of buffer to each analog input
101 = Allocates 32 words of buffer to each analog input
100 = Allocates 16 words of buffer to each analog input
011 = Allocates 8 words of buffer to each analog input
010 = Allocates 4 words of buffer to each analog input
001 = Allocates 2 words of buffer to each analog input
000 = Allocates 1 word of buffer to each analog input


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**REGISTER 23-6: ADxCHS123: ADCx INPUT CHANNEL 1, 2, 3 SELECT REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | CH123NB<1:0> | | CH123SB |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | CH123NA<1:0> | | CH123SA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10-9 **CH123NB<1:0>:** Channel 1, 2, 3 Negative Input Select for Sample B bits

When AD12B = 1, CHxNB is: U-0, Unimplemented, Read as '0':

11 = CH1 negative input is AN9, CH2 negative input is AN10, CH3 negative input is AN11

10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is AN8

0x = CH1, CH2, CH3 negative input is $V_{REFL}$

bit 8 **CH123SB:** Channel 1, 2, 3 Positive Input Select for Sample B bit

When AD12B = 1, CHxSA is: U-0, Unimplemented, Read as '0':

1 = CH1 positive input is AN3, CH2 positive input is AN4, CH3 positive input is AN5

0 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2

bit 7-3 **Unimplemented:** Read as '0'

bit 2-1 **CH123NA<1:0>:** Channel 1, 2, 3 Negative Input Select for Sample A bits

When AD12B = 1, CHxNA is: U-0, Unimplemented, Read as '0':

11 = CH1 negative input is AN9, CH2 negative input is AN10, CH3 negative input is AN11

10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is AN8

0x = CH1, CH2, CH3 negative input is $V_{REFL}$

bit 0 **CH123SA:** Channel 1, 2, 3 Positive Input Select for Sample A bit

When AD12B = 1, CHxSA is: U-0, Unimplemented, Read as '0':

1 = CH1 positive input is AN3, CH2 positive input is AN4, CH3 positive input is AN5

0 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2

**REGISTER 23-7: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER**

| R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CH0NB | — | — | CH0SB<4:0>(1) | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CH0NA | — | — | CH0SA<4:0>(1) | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CH0NB:** Channel 0 Negative Input Select for Sample B bit
Same definition as bit 7.

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **CH0SB<4:0>:** Channel 0 Positive Input Select for Sample B bits(1)
Same definition as bits<4:0>.

bit 7 **CH0NA:** Channel 0 Negative Input Select for Sample A bit
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL

bit 6-5 **Unimplemented:** Read as '0'

bit 4-0 **CH0SA<4:0>:** Channel 0 Positive Input Select for Sample A bits(1)
11111 = Channel 0 positive input is AN31
11110 = Channel 0 positive input is AN30
•
•
•
00010 = Channel 0 positive input is AN2
00001 = Channel 0 positive input is AN1
00000 = Channel 0 positive input is AN0

**Note 1:** The AN16 through AN31 pins are not available for the ADC2 module. The AN16 through AN23 pins are not available for dsPIC33EP256MU806 (64-pin) devices.


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**REGISTER 23-8: AD1CSSH: ADC1 INPUT SCAN SELECT REGISTER HIGH(1,2,3)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSS31 | CSS30 | CSS29 | CSS28 | CSS27 | CSS26 | CSS25 | CSS24 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSS23 | CSS22 | CSS21 | CSS20 | CSS19 | CSS18 | CSS17 | CSS16 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **CSS<31:16>:** ADC1 Input Scan Selection bits
1 = Selects ANx for input scan
0 = Skips ANx for input scan

**Note 1:** On devices with less than 32 analog inputs, all ADxCSSH bits can be selected by user software. However, inputs selected for scan without a corresponding input on the device converts to VREFL.
**2:** CSSx = ANx, where x = 16-31.
**3:** ADC2 only supports analog inputs, AN0-AN15; therefore, no ADC2 Input Scan Select register exists.

**REGISTER 23-9: ADxCSSL: ADCx INPUT SCAN SELECT REGISTER LOW(1,2)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSS15 | CSS14 | CSS13 | CSS12 | CSS11 | CSS10 | CSS9 | CSS8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSS7 | CSS6 | CSS5 | CSS4 | CSS3 | CSS2 | CSS1 | CSS0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **CSS<15:0>:** ADC Input Scan Selection bits
1 = Selects ANx for input scan
0 = Skips ANx for input scan

**Note 1:** On devices with less than 16 analog inputs, all ADxCSSL bits can be selected by the user. However, inputs selected for scan without a corresponding input on the device converts to VREFL.
**2:** CSSx = ANx, where x = 0-15.

**NOTES:**


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# 24.0 DATA CONVERTER INTERFACE (DCI) MODULE

**Note 1:** This data sheet is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Section 20. Data Converter Interface (DCI)"** (DS70356) of the *"dsPIC33E/PIC24E Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

## 24.1 Module Introduction

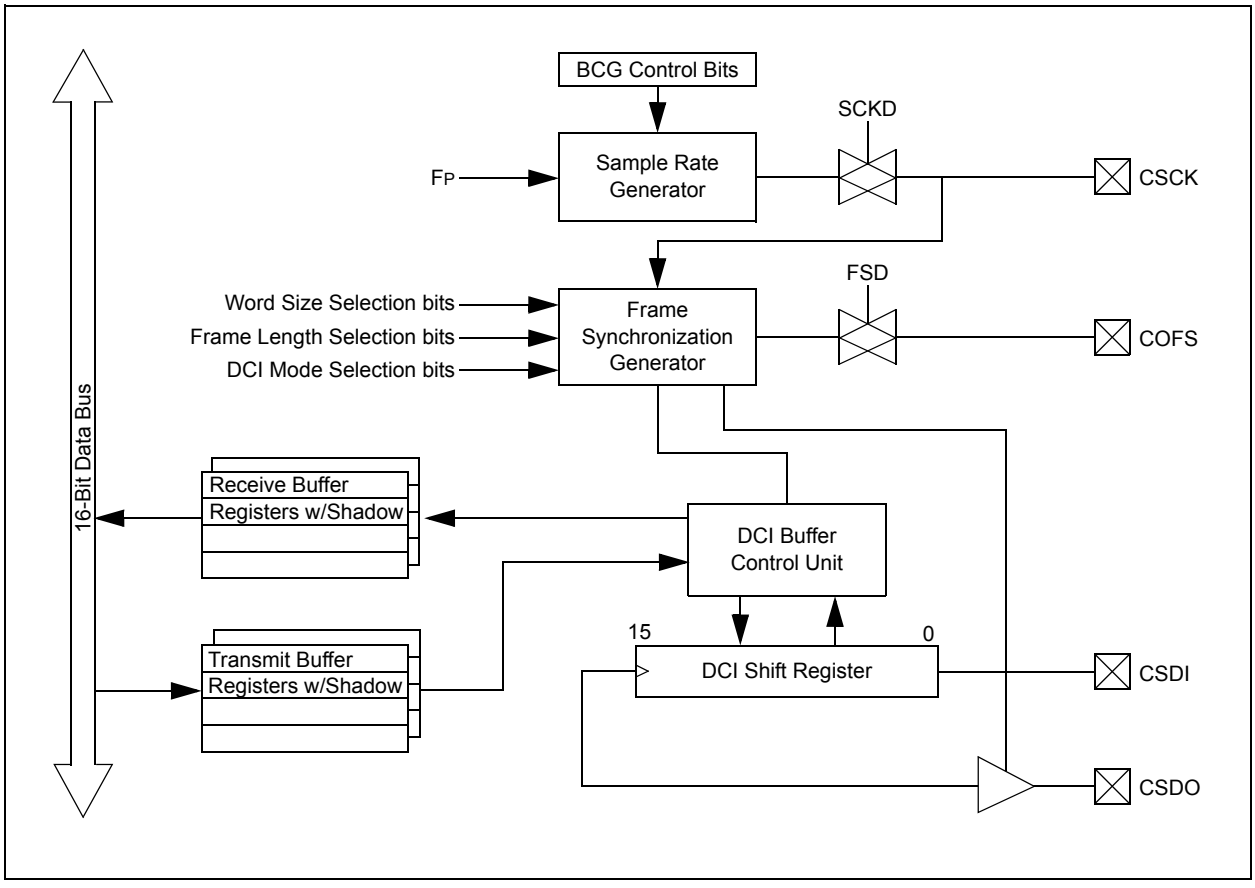
The Data Converter Interface (DCI) module allows simple interfacing of devices, such as audio coder/decoders (Codecs), ADC and D/A Converters. The following interfaces are supported:

- Framed Synchronous Serial Transfer (Single or Multi-Channel)
- Inter-IC Sound ($I^2S$) Interface
- AC-Link Compliant mode

General features include:

- Programmable word size up to 16 bits
- Supports up to 16 time slots, for a maximum frame size of 256 bits
- Data buffering for up to 4 samples without CPU overhead

**FIGURE 24-1: DCI MODULE BLOCK DIAGRAM**



## 24.2 DCI Resources

Many useful resources related to DCI are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 24.2.1 KEY RESOURCES

- **Section 20. "Data Converter Interface (DCI)"** (DS70356) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools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## 24.3 DCI Control Registers

**REGISTER 24-1: DCICON1: DCI CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DCIEN | r | DCISIDL | r | DLOOP | CSCKD | CSCKE | COFSD |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| UNFM | CSDOM | DJST | r | r | r | COFSM<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | r = Reserved bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **DCIEN:** DCI Module Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Reserved:** Read as '0'

bit 13 **DCISIDL:** DCI Stop in Idle Control bit
1 = Module will halt in CPU Idle mode
0 = Module will continue to operate in CPU Idle mode

bit 12 **Reserved:** Read as '0'

bit 11 **DLOOP:** Digital Loopback Mode Control bit
1 = Digital Loopback mode is enabled; CSDI and CSDO pins are internally connected
0 = Digital Loopback mode is disabled

bit 10 **CSCKD:** Sample Clock Direction Control bit
1 = CSCK pin is an input when DCI module is enabled
0 = CSCK pin is an output when DCI module is enabled

bit 9 **CSCKE:** Sample Clock Edge Control bit
1 = Data changes on serial clock falling edge, sampled on serial clock rising edge
0 = Data changes on serial clock rising edge, sampled on serial clock falling edge

bit 8 **COFSD:** Frame Synchronization Direction Control bit
1 = COFS pin is an input when DCI module is enabled
0 = COFS pin is an output when DCI module is enabled

bit 7 **UNFM:** Underflow Mode bit
1 = Transmits last value written to the Transmit registers on a transmit underflow
0 = Transmits '0's on a transmit underflow

bit 6 **CSDOM:** Serial Data Output Mode bit
1 = CSDO pin will be tri-stated during disabled transmit time slots
0 = CSDO pin drives '0's during disabled transmit time slots

bit 5 **DJST:** DCI Data Justification Control bit
1 = Data transmission/reception begins during the same serial clock cycle as the frame synchronization pulse
0 = Data transmission/reception begins one serial clock cycle after the frame synchronization pulse

bit 4-2 **Reserved:** Read as '0'

bit 1-0 **COFSM<1:0>:** Frame Sync Mode bits
11 = 20-Bit AC-Link mode
10 = 16-Bit AC-Link mode
01 = $I^2S$ Frame Sync mode
00 = Multi-Channel Frame Sync mode

**REGISTER 24-2: DCICON2: DCI CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| r | r | r | r | BLEN<1:0> | | r | COFSG3 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| COFSG<2:0> | | | r | WS<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | r = Reserved bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Reserved:** Read as '0'

bit 11-10 **BLEN<1:0>:** Buffer Length Control bits
11 = Four data words will be buffered between interrupts
10 = Three data words will be buffered between interrupts
01 = Two data words will be buffered between interrupts
00 = One data word will be buffered between interrupts

bit 9 **Reserved:** Read as '0'

bit 8-5 **COFSG<3:0>:** Frame Sync Generator Control bits
1111 = Data frame has 16 words
•
•
•
0010 = Data frame has 3 words
0001 = Data frame has 2 words
0000 = Data frame has 1 word

bit 4 **Reserved:** Read as '0'

bit 3-0 **WS<3:0>:** DCI Data Word Size bits
1111 = Data word size is 16 bits
•
•
•
0100 = Data word size is 5 bits
0011 = Data word size is 4 bits
0010 = **Invalid Selection**. Do not use. Unexpected results may occur.
0001 = **Invalid Selection**. Do not use. Unexpected results may occur.
0000 = **Invalid Selection**. Do not use. Unexpected results may occur.


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**REGISTER 24-3: DCICON3: DCI CONTROL REGISTER 3**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| r | r | r | r | BCG<11:8> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| BCG<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | r = Reserved bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Reserved:** Read as '0'

bit 11-0 **BCG<11:0>:** DCI Clock Generator Control bits

**REGISTER 24-4: DCISTAT: DCI STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| r | r | r | r | SLOT<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| r | r | r | r | ROV | RFUL | TUNF | TMPTY |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | r = Reserved bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Reserved:** Read as '0'

bit 11-8 **SLOT<3:0>:** DCI Slot Status bits
1111 = Slot 15 is currently active
•
•
•
0010 = Slot 2 is currently active
0001 = Slot 1 is currently active
0000 = Slot 0 is currently active

bit 7-4 **Reserved:** Read as '0'

bit 3 **ROV:** Receive Overflow Status bit
1 = A receive overflow has occurred for at least one Receive register
0 = A receive overflow has not occurred

bit 2 **RFUL:** Receive Buffer Full Status bit
1 = New data is available in the Receive registers
0 = The Receive registers have old data

bit 1 **TUNF:** Transmit Buffer Underflow Status bit
1 = A transmit underflow has occurred for at least one Transmit register
0 = A transmit underflow has not occurred

bit 0 **TMPTY:** Transmit Buffer Empty Status bit
1 = The Transmit registers are empty
0 = The Transmit registers are not empty


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**REGISTER 24-5: RSCON: DCI RECEIVE SLOT CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| RSE15 | RSE14 | RSE13 | RSE12 | RSE11 | RSE10 | RSE9 | RSE8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| RSE7 | RSE6 | RSE5 | RSE4 | RSE3 | RSE2 | RSE1 | RSE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **RSE<15:0>:** Receive Slot Enable bits

1 = CSDI data is received during the individual time slot n

0 = CSDI data is ignored during the individual time slot n

**REGISTER 24-6: TSCON: DCI TRANSMIT SLOT CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TSE15 | TSE14 | TSE13 | TSE12 | TSE11 | TSE10 | TSE9 | TSE8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TSE7 | TSE6 | TSE5 | TSE4 | TSE3 | TSE2 | TSE1 | TSE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **TSE<15:0>:** Transmit Slot Enable Control bits

1 = Transmit buffer contents are sent during the individual time slot n

0 = CSDO pin is tri-stated or driven to logic ‘0’ during the individual time slot, depending on the state of the CSDOM bit

**NOTES:**


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## 25.0 COMPARATOR MODULE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 26. "Op Amp/Comparator"** (DS70357) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

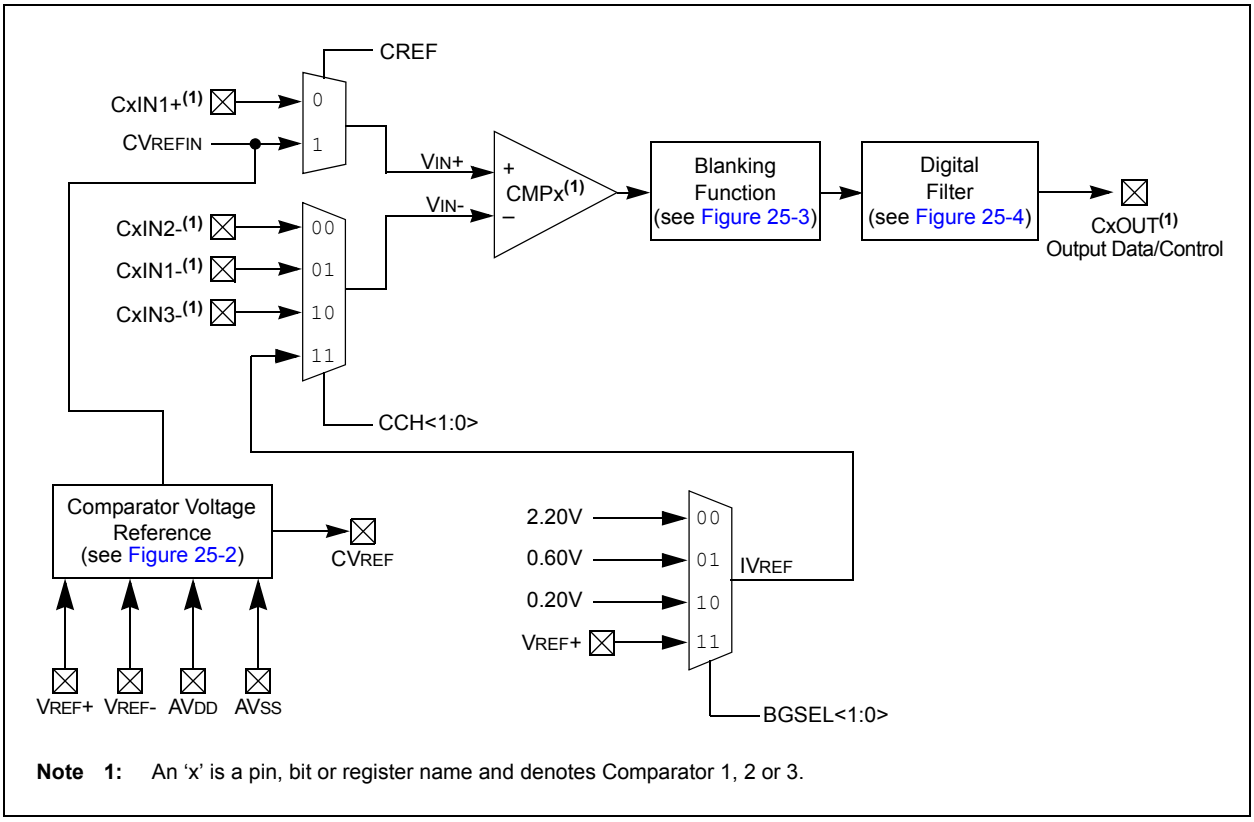
The comparator module provides three comparators that can be configured in different ways. As shown in Figure 25-1, individual comparator options are specified by the comparator module's Special Function Register (SFR) control bits.

These options allow users to:

- Select the edge for trigger and interrupt generation
- Configure the comparator voltage reference and band gap
- Configure output blanking and masking

The comparator operating mode is determined by the input selections (i.e., whether the input voltage is compared to a second input voltage or to an internal voltage reference).

**FIGURE 25-1: COMPARATOR I/O OPERATING MODES**




**Note 1:** An 'x' is a pin, bit or register name and denotes Comparator 1, 2 or 3.

**FIGURE 25-2: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM**

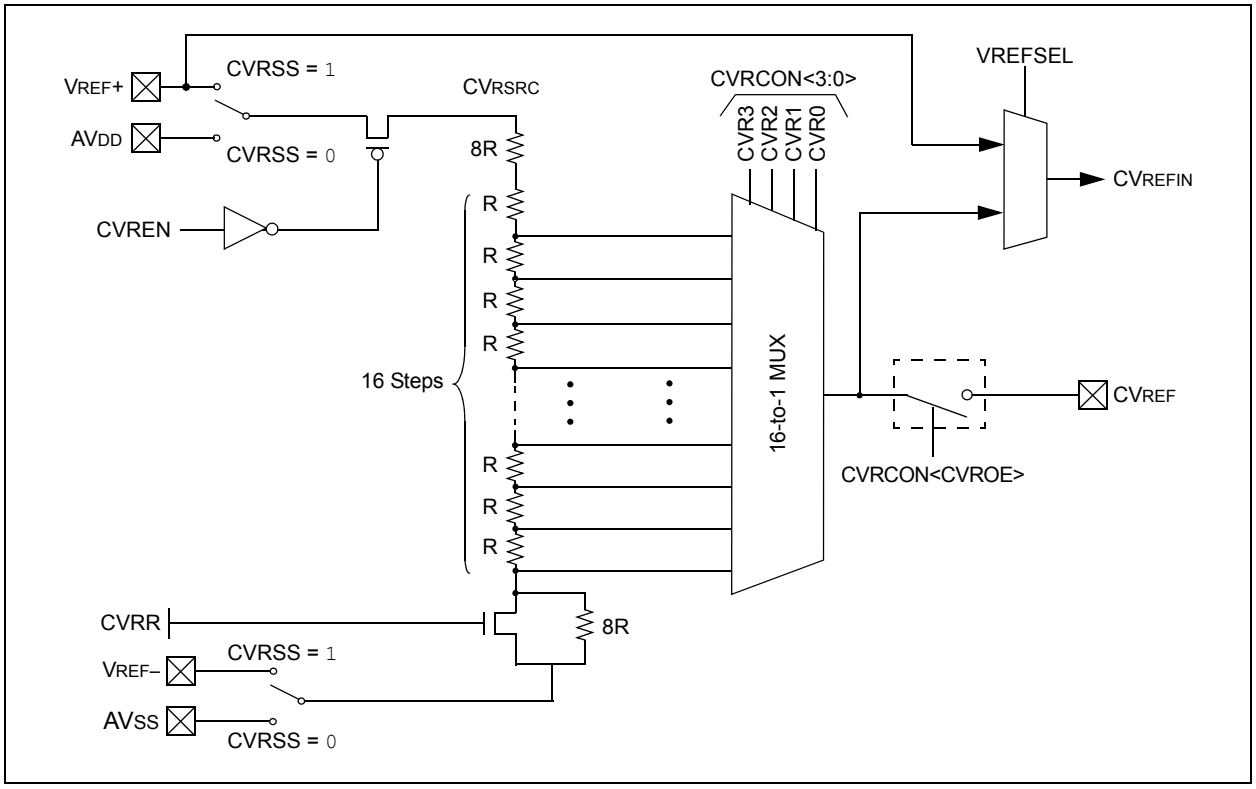



**FIGURE 25-3: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM**

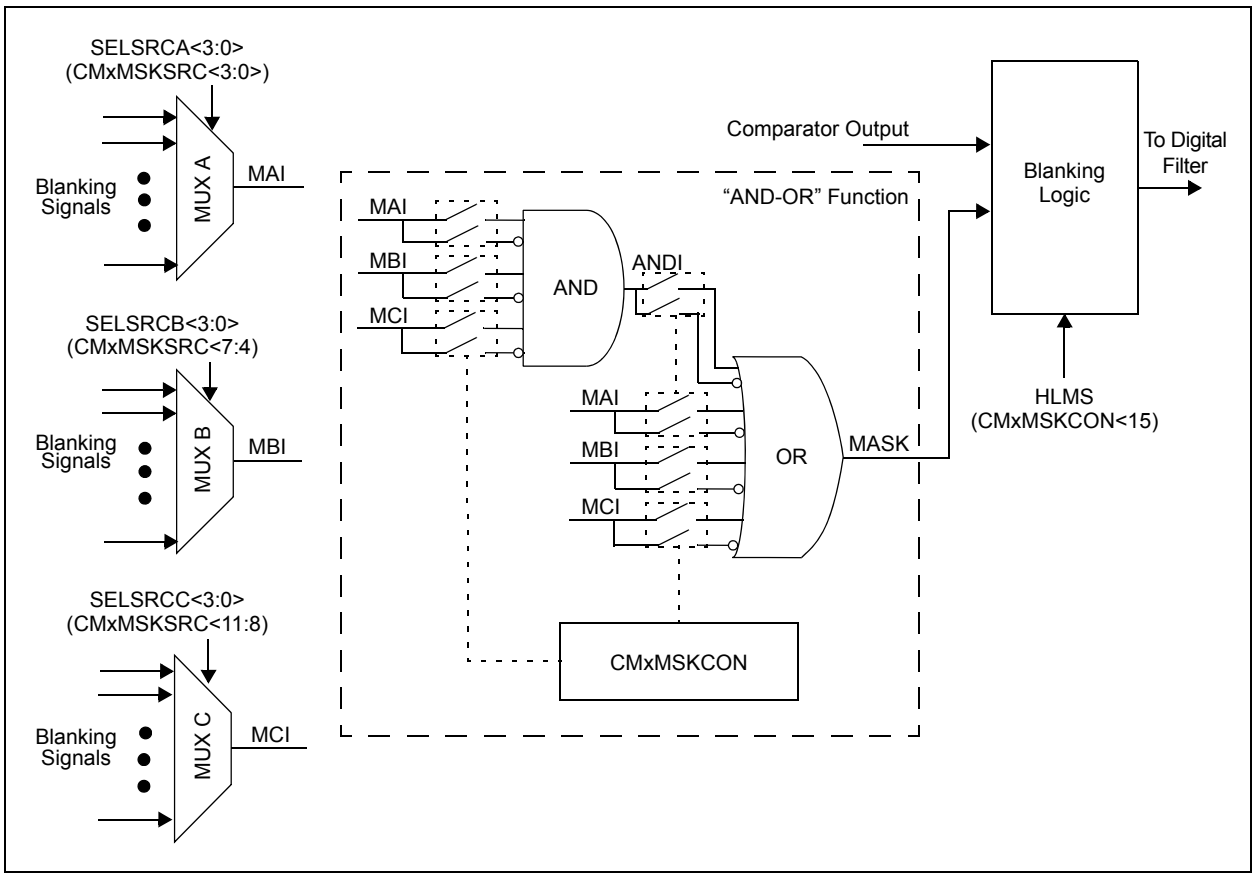




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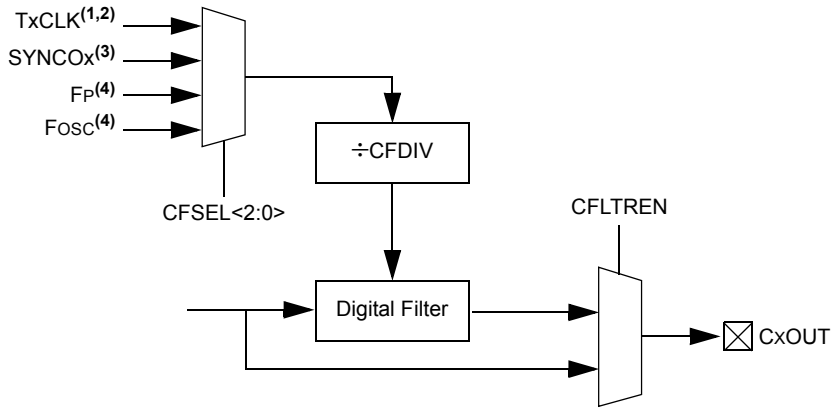
**FIGURE 25-4: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM**




**Note 1:** See the Type C Timer Block Diagram (Figure 13-2).

**2:** See the Type B Timer Block Diagram (Figure 13-1).

**3:** See the PWM Module Register Interconnect Diagram (Figure 16-2).

**4:** See the Oscillator System Diagram (Figure 9-1).

## 25.1 Comparator Resources

Many useful resources related to the Comparator are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

### 25.1.1 KEY RESOURCES

- **Section 26. "Op Amp/Comparator"** (DS70357) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 25.2 Comparator Control Registers

**REGISTER 25-1: CMSTAT: COMPARATOR STATUS REGISTER**

| R/W-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| CMSIDL | — | — | — | — | C3EVT | C2EVT | C1EVT |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | C3OUT | C2OUT | C1OUT |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CMSIDL:** Comparator Stop in Idle Mode bit
1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all comparators in Idle mode

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **C3EVT:** Comparator 3 Event Status bit
1 = Comparator event occurred
0 = Comparator event did not occur

bit 9 **C2EVT:** Comparator 2 Event Status bit
1 = Comparator event occurred
0 = Comparator event did not occur

bit 8 **C1EVT:** Comparator 1 Event Status bit
1 = Comparator event occurred
0 = Comparator event did not occur

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **C3OUT:** Comparator 3 Output Status bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 1 **C2OUT:** Comparator 2 Output Status bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 0 **C1OUT:** Comparator 1 Output Status bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-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**REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CON | COE | CPOL | — | — | — | CEVT | COUT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event according to EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1 (inverted polarity):
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/Event/Interrupt generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/Event/Interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output.
If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output.
01 = Trigger/Event/Interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)
If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output.
If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output.
00 = Trigger/Event/Interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

**REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (CONTINUED)**

bit 4 **CREF:** Comparator Reference Select bit ($V_{IN}$+ input)
1 = $V_{IN}$+ input connects to internal $CV_{REFIN}$ voltage
0 = $V_{IN}$+ input connects to CxIN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Channel Select bits
11 = $V_{IN}$- input of comparator connects to $IV_{REF}$
10 = $V_{IN}$- input of comparator connects to CxIN3- pin
01 = $V_{IN}$- input of comparator connects to CxIN1- pin
00 = $V_{IN}$- input of comparator connects to CxIN2- pin


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**REGISTER 25-3: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | RW-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | SELSRCC<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SELSRCB<3:0> | | | | SELSRCA<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-8 **SELSRCC<3:0>:** Mask C Input Select bits
1111 = FLT4
1110 = FLT2
1101 = PWM7H
1100 = PWM7L
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

bit 7-4 **SELSRCB<3:0>:** Mask B Input Select bits
1111 = FLT4
1110 = FLT2
1101 = PWM7H
1100 = PWM7L
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

**REGISTER 25-3: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER (CONTINUED)**

bit 3-0 **SELSRCA<3:0>:** Mask A Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PWM7H
1100 = PWM7L
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L


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**REGISTER 25-4: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| HLMS | — | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **HLMS:** High or Low-Level Masking Select bits
1 = The masking (blanking) function will prevent any asserted (‘0’) comparator signal from propagating
0 = The masking (blanking) function will prevent any asserted (‘1’) comparator signal from propagating

bit 14 **Unimplemented:** Read as '0'

bit 13 **OCEN:** OR Gate C Input Enable bit
1 = MCI is connected to OR gate
0 = MCI is not connected to OR gate

bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to OR gate
0 = Inverted MCI is not connected to OR gate

bit 11 **OBEN:** OR Gate B Input Enable bit
1 = MBI is connected to OR gate
0 = MBI is not connected to OR gate

bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to OR gate
0 = Inverted MBI is not connected to OR gate

bit 9 **OAEN:** OR Gate A Input Enable bit
1 = MAI is connected to OR gate
0 = MAI is not connected to OR gate

bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to OR gate
0 = Inverted MAI is not connected to OR gate

bit 7 **NAGS:** AND Gate Output Inverted Enable bit
1 = Inverted ANDI is connected to OR gate
0 = Inverted ANDI is not connected to OR gate

bit 6 **PAGS:** AND Gate Output Enable bit
1 = ANDI is connected to OR gate
0 = ANDI is not connected to OR gate

bit 5 **ACEN:** AND Gate C Input Enable bit
1 = MCI is connected to AND gate
0 = MCI is not connected to AND gate

bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to AND gate
0 = Inverted MCI is not connected to AND gate

**REGISTER 25-4: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER (CONTINUED)**

bit 3 **ABEN:** AND Gate B Input Enable bit
1 = MBI is connected to AND gate
0 = MBI is not connected to AND gate

bit 2 **ABNEN:** AND Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to AND gate
0 = Inverted MBI is not connected to AND gate

bit 1 **AAEN:** AND Gate A Input Enable bit
1 = MAI is connected to AND gate
0 = MAI is not connected to AND gate

bit 0 **AANEN:** AND Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to AND gate
0 = Inverted MAI is not connected to AND gate


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**REGISTER 25-5: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | I-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | CFSEL<2:0> | | | CFLTREN | CFDIV<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **CFSEL<2:0>:** Comparator Filter Input Clock Select bits
111 = T5CLK(1)
110 = T4CLK(2)
101 = T3CLK(1)
100 = T2CLK(2)
011 = SYNCO2(3)
010 = SYNCO1(3)
001 = FOSC(4)
000 = FP(4)

bit 3 **CFLTREN:** Comparator Filter Enable bit
1 = Digital filter is enabled
0 = Digital filter is disabled

bit 2-0 **CFDIV<2:0>:** Comparator Filter Clock Divide Select bits
111 = Clock Divide 1:128
110 = Clock Divide 1:64
101 = Clock Divide 1:32
100 = Clock Divide 1:16
011 = Clock Divide 1:8
010 = Clock Divide 1:4
001 = Clock Divide 1:2
000 = Clock Divide 1:1

**Note 1:** See the Type C Timer Block Diagram (Figure 13-2).
**2:** See the Type B Timer Block Diagram (Figure 13-1).
**3:** See the PWM Module Register Interconnect Diagram (Figure 16-2).
**4:** See the Oscillator System Diagram (Figure 9-1).

**REGISTER 25-6: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | VREFSEL | BGSEL<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CVREN | CVROE(1) | CVRR | CVRSS | CVR<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **VREFSEL:** Voltage Reference Select bit
1 = CVREFIN = VREF+
0 = CVREFIN is generated by the resistor network

bit 9-8 **BGSEL<1:0>:** Band Gap Reference Source Select bits
11 = IVREF = VREF+(2)
10 = IVREF = 0.20V (nominal)
01 = IVREF = 0.60V (nominal)
00 = IVREF = 2.20V (nominal)

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit powered on
0 = Comparator voltage reference circuit powered down

bit 6 **CVROE:** Comparator Voltage Reference Output Enable bit(1)
1 = Voltage level is output on CVREF pin
0 = Voltage level is disconnected from CVREF pin

bit 5 **CVRR:** Comparator Voltage Reference Range Selection bit
1 = CVRSRC/24 step-size
0 = CVRSRC/32 step-size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator voltage reference source, CVRSRC = (VREF+) – (VREF-)(2)
0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection 0 ≤ CVR<3:0> ≤ 15 bits
When CVRR = 1:
CVREFIN = (CVR<3:0>/24) • (CVRSRC)
When CVRR = 0:
CVREFIN = 1/4 • (CVRSRC) + (CVR<3:0>/32) • (CVRSRC)

**Note 1:** CVROE overrides the TRIS bit setting.
**2:** Selecting BGSEL<1:0> = 11 and CVRSS = 1 is invalid and will produce unpredictable results.


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## 26.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS70584) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This chapter discusses the Real-Time Clock and Calendar (RTCC) module and its operation.

Some of the key features of this module are:

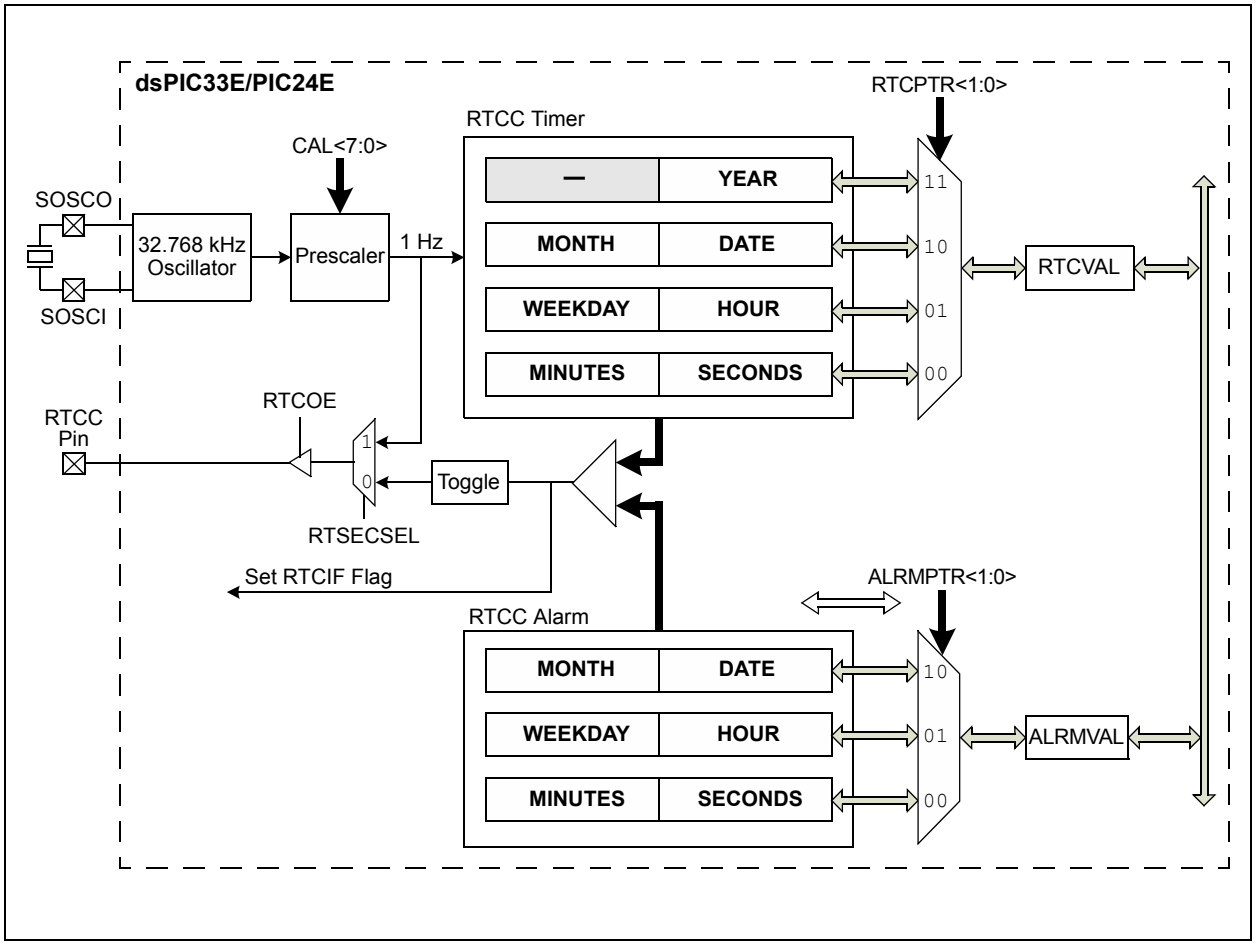
- Time: Hours, Minutes and Seconds
- 24-Hour Format (military time)
- Calendar: Weekday, Date, Month and Year
- Alarm Configurable
- Year Range: 2000 to 2099
- Leap Year Correction
- BCD Format for Compact Firmware
- Optimized for Low-Power Operation
- User Calibration with Auto-Adjust
- Calibration Range: ±2.64 Seconds Error per Month
- Requirements: External 32.768 kHz Clock Crystal
- Alarm Pulse or Seconds Clock Output on RTCC Pin

The RTCC module is intended for applications where accurate time must be maintained for extended periods with minimum to no intervention from the CPU. The RTCC module is optimized for low-power usage to provide extended battery lifetime while keeping track of time.

The RTCC module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

The hours are available in 24-hour (military time) format. The clock provides a granularity of one second with half-second visibility to the user.

**FIGURE 26-1: RTCC BLOCK DIAGRAM**





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## 26.1 Writing to the RTCC Timer

**Note:** To allow the RTCC module to be clocked by the secondary crystal oscillator, the Secondary Oscillator Enable (LPOSCEN) bit in the Oscillator Control (OSCCON<1>) register must be set. For further details, refer to **Section 7. "Oscillator"** (DS70580) in the *"dsPIC33E/PIC24E Family Reference Manual"*.

The user application can configure the time and calendar by writing the desired seconds, minutes, hours, weekday, date, month and year to the RTCC registers. Under normal operation, writes to the RTCC Timer registers are not allowed. Attempted writes will appear to execute normally, but the contents of the registers will remain unchanged. To write to the RTCC register, the RTCWREN bit (RCFGCAL<13>) must be set. Setting the RTCWREN bit allows writes to the RTCC registers. Conversely, clearing the RTCWREN bit prevents writes.

To set the RTCWREN bit, the following procedure must be executed. The RTCWREN bit can be cleared at any time:

1. Write 0x55 to NVMKEY.
2. Write 0xAA to NVMKEY.
3. Set the RTCWREN bit using a single-cycle instruction.

The RTCC module is enabled by setting the RTCEN bit (RCFGCAL<15>). To set or clear the RTCEN bit, the RTCWREN bit (RCFGCAL<13>) must be set.

If the entire clock (hours, minutes and seconds) needs to be corrected, it is recommended that the RTCC module should be disabled to avoid coincidental write operation when the timer increments. Therefore, it stops the clock from counting while writing to the RTCC Timer register.

## 26.2 RTCC Resources

Many useful resources related to RTCC are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

### 26.2.1 KEY RESOURCES

- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS70584) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools

## 26.3 RTCC Registers

**REGISTER 26-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER(1)**

| R/W-0 | U-0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| RTCEN(2) | — | RTCWREN | RTCSYNC | HALFSEC(3) | RTCOE | RTCPTR<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CAL<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **RTCEN:** RTCC Enable bit(2)
1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **RTCWREN:** RTCC Value Registers Write Enable bit
1 = RTCVAL register can be written to by the user application
0 = RTCVAL register is locked out from being written to by the user application

bit 12 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
1 = A rollover is about to occur in 32 clock edges (approximately 1 ms)
0 = A rollover will not occur

bit 11 **HALFSEC:** Half-Second Status bit(3)
1 = Second half period of a second
0 = First half period of a second

bit 10 **RTCOE:** RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is disabled

bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Pointer bits
Points to the corresponding RTCC Value register when reading the RTCVAL register; the RTCPTR<1:0> value decrements on every access of the RTCVAL register until it reaches '00'.

**Note 1:** The RCFGCAL register is only affected by a POR.
**2:** A write to the RTCEN bit is only allowed when RTCWREN = 1.
**3:** This bit is read-only. It is cleared when the lower half of the MINSEC register is written.


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**REGISTER 26-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER(1) (CONTINUED)**

bit 7-0 **CAL<7:0>:** RTCC Drift Calibration bits

01111111 = Maximum positive adjustment; adds 508 RTCC clock pulses every one minute
•
•
•
00000001 = Minimum positive adjustment; adds four RTCC clock pulses every one minute
00000000 = No adjustment
11111111 = Minimum negative adjustment; subtracts four RTCC clock pulses every one minute
•
•
•
10000000 = Maximum negative adjustment; subtracts 512 RTCC clock pulses every one minute

**Note 1:** The RCFGCAL register is only affected by a POR.

**2:** A write to the RTCEN bit is only allowed when RTCWREN = 1.

**3:** This bit is read-only. It is cleared when the lower half of the MINSEC register is written.

**REGISTER 26-2: PADCFG1: PAD CONFIGURATION CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | RTSECSEL(1) | PMPTTL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-2 **Unimplemented:** Read as ‘0’

bit 1 **RTSECSEL:** RTCC Seconds Clock Output Select bit(1)
1 = RTCC seconds clock is selected for the RTCC pin
0 = RTCC alarm pulse is selected for the RTCC pin

bit 0 Not used by the RTCC module.

**Note 1:** To enable the actual RTCC output, the RTCOE bit (RCFGCAL<10>) must be set.


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**REGISTER 26-3: ALCFGRPT: ALARM CONFIGURATION REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ALRMEN | CHIME | AMASK<3:0> | | | | ALRMPTR<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ARPT<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ALRMEN:** Alarm Enable bit

1 = Alarm is enabled (cleared automatically after an alarm event whenever ARPT<7:0> = 0x00 and CHIME = 0)
0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit

1 = Chime is enabled; ARPT<7:0> bits are allowed to roll over from 0x00 to 0xFF
0 = Chime is disabled; ARPT<7:0> bits stop once they reach 0x00

bit 13-10 **AMASK<3:0>:** Alarm Mask Configuration bits

0000 = Every half second
0001 = Every second
0010 = Every 10 seconds
0011 = Every minute
0100 = Every 10 minutes
0101 = Every hour
0110 = Once a day
0111 = Once a week
1000 = Once a month
1001 = Once a year (except when configured for February 29th, once every 4 years)
101x = Reserved – do not use
11xx = Reserved – do not use

bit 9-8 **ALRMPTR<1:0>:** Alarm Value Register Window Pointer bits

Points to the corresponding Alarm Value registers when reading the ALRMVAL register. The ALRMPTR<1:0> value decrements on every read or write of ALRMVAL until it reaches '00'.

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits

11111111 = Alarm will repeat 255 more times
•
•
•
00000000 = Alarm will not repeat

The counter decrements on any alarm event. The counter is prevented from rolling over from 0x00 to 0xFF unless CHIME = 1.

**REGISTER 26-4: RTCVAL (WHEN RTCPTR<1:0> = 11): YEAR VALUE REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| YRTEN<3:0> | | | | YRONE<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit bits
Contains a value from 0 to 9.

bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit bits
Contains a value from 0 to 9.

**Note 1:** A write to the YEAR register is only allowed when RTCWREN = 1.

**REGISTER 26-5: RTCVAL (WHEN RTCPTR<1:0> = 10): MONTH AND DAY VALUE REGISTER(1)**

| U-0 | U-0 | U-0 | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| — | — | — | MTHTEN0 | MTHONE<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | DAYTEN<1:0> | | DAYONE<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of 0 or 1.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

**Note 1:** A write to this register is only allowed when RTCWREN = 1.


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**REGISTER 26-6: RTCVAL (WHEN RTCPTR<1:0> = 01): WEEKDAY AND HOURS VALUE REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | WDAY<2:0> | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | HRTEN<1:0> | | HRONE<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits
Contains a value from 0 to 9.

**Note 1:** A write to this register is only allowed when RTCWREN = 1.

**REGISTER 26-7: RTCVAL (WHEN RTCPTR<1:0> = 00): MINUTES AND SECONDS VALUE REGISTER**

| U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | MINTEN<2:0> | | | MINONE<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | SECTEN<2:0> | | | SECONE<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit bits
Contains a value from 0 to 5.

bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit bits
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit bits
Contains a value from 0 to 5.

bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit bits
Contains a value from 0 to 9.

**REGISTER 26-8: ALRMVAL (WHEN ALRMPTR<1:0> = 10): ALARM MONTH AND DAY VALUE REGISTER(1)**

| U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | MTHTEN0 | MTHONE<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | DAYTEN<1:0> | | DAYONE<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of 0 or 1.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

**Note 1:** A write to this register is only allowed when RTCWREN = 1.


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**REGISTER 26-9: ALRMVAL (WHEN ALRMPTR<1:0> = 01): ALARM WEEKDAY AND HOURS VALUE REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | WDAY2 | WDAY1 | WDAY0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | HRTEN<1:0> | | HRONE<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits
Contains a value from 0 to 9.

**Note 1:** A write to this register is only allowed when RTCWREN = 1.

**REGISTER 26-10: ALRMVAL (WHEN ALRMPTR<1:0> = 00): ALARM MINUTES AND SECONDS VALUE REGISTER**

| U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | MINTEN<2:0> | | | MINONE<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | SECTEN<2:0> | | | SECONE<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit bits
Contains a value from 0 to 5.

bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit bits
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit bits
Contains a value from 0 to 5.

bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit bits
Contains a value from 0 to 9.


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## 27.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "Programmable Cyclic Redundancy Check (CRC)"** (DS70346) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

- User-Programmable (up to 32nd order) Polynomial CRC Equation
- Interrupt Output
- Data FIFO

The programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, up to 32 bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 27-1. A simple version of the CRC shift engine is shown in Figure 27-2.

**FIGURE 27-1: PROGRAMMABLE CRC BLOCK DIAGRAM**

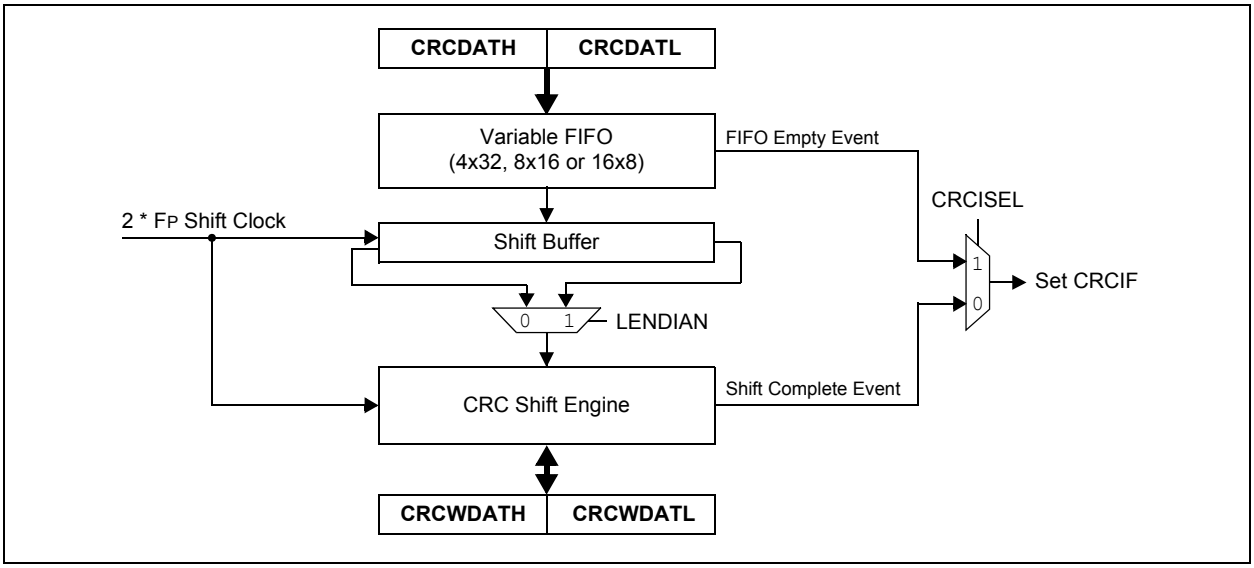
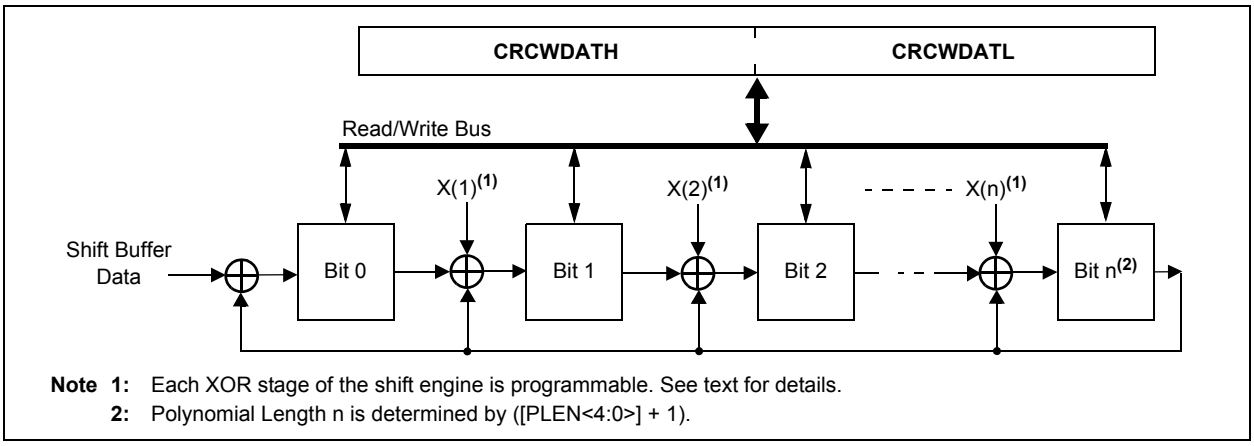



**FIGURE 27-2: CRC SHIFT ENGINE DETAIL**




**Note 1:** Each XOR stage of the shift engine is programmable. See text for details.

**2:** Polynomial Length n is determined by ([PLEN<4:0>] + 1).

## 27.1 Overview

The CRC module can be programmed for CRC polynomials of up to the 32nd order, using up to 32 bits. Polynomial length, which reflects the highest exponent in the equation, is selected by the PLEN<4:0> bits (CRCCON2<4:0>).

The CRCXORL and CRCXORH registers control which exponent terms are included in the equation. Setting a particular bit includes that exponent term in the equation; functionally, this includes an XOR operation on the corresponding bit in the CRC engine. Clearing the bit disables the XOR.

For example, consider two CRC polynomials, one a 16-bit equation and the other a 32-bit equation:

$$x16 + x12 + x5 + 1$$

and

$$x32 + x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x + 1$$

To program these polynomials into the CRC generator, set the register bits as shown in Table 27-1.

Note that the appropriate positions are set to '1' to indicate that they are used in the equation (for example, X26 and X23). The 0 bit required by the equation is always XORed; thus, X0 is a don't care. For a polynomial of length, N, it is assumed that the *N*th bit will always be used, regardless of the bit setting. Therefore, for a polynomial length of 32, there is no 32nd bit in the CRCxOR register.

**TABLE 27-1: CRC SETUP EXAMPLES FOR 16 AND 32-BIT POLYNOMIAL**

| CRC Control Bits | Bit Values | |
|---|---|---|
| | 16-Bit Polynomial | 32-Bit Polynomial |
| PLEN<4:0> | 01111 | 11111 |
| X<31:16> | 0000 0000<br>0000 000x | 0000 0100<br>1100 0001 |
| X<15:0> | 0001 0000<br>0010 000x | 0001 1101<br>1011 011x |

## 27.2 Programmable CRC Resources

Many useful resources related to Programmable CRC are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310

### 27.2.1 KEY RESOURCES

- **Section 27. "Programmable Cyclic Redundancy Check (CRC)"** (DS70346) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools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## 27.3 Programmable CRC Registers

**REGISTER 27-1: CRCCON1: CRC CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| CRCEN | — | CSIDL | VWORD<4:0> | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-1 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CRCFUL | CRCMPT | CRCISEL | CRCGO | LENDIAN | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CRCEN:** CRC Enable bit
1 = CRC module is enabled
0 = CRC module is disabled, all state machines, pointers and CRCWDAT/CRCDAT are reset; other SFRs are not reset

bit 14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** CRC Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-8 **VWORD<4:0>:** Pointer Value bits
Indicates the number of valid words in the FIFO. Has a maximum value of 8 when PLEN<4:0> > 7 or 16 when PLEN<4:0> ≤ 7.

bit 7 **CRCFUL:** FIFO Full bit
1 = FIFO is full
0 = FIFO is not full

bit 6 **CRCMPT:** FIFO Empty Bit
1 = FIFO is empty
0 = FIFO is not empty

bit 5 **CRCISEL:** CRC Interrupt Selection bit
1 = Interrupt on FIFO is empty; final word of data is still shifting through CRC
0 = Interrupt on shift is complete and CRCWDAT results are ready

bit 4 **CRCGO:** Start CRC bit
1 = Starts CRC serial shifter
0 = CRC serial shifter is turned off

bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit
1 = Data word is shifted into the CRC starting with the LSb (little endian)
0 = Data word is shifted into the CRC starting with the MSb (big endian)

bit 2-0 **Unimplemented:** Read as '0'

**REGISTER 27-2: CRCCON2: CRC CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DWIDTH<4:0> | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | PLEN<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **DWIDTH<4:0>:** Data Width Select bits
These bits set the width of the data word (DWIDTH<4:0> + 1).

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **PLEN<4:0>:** Polynomial Length Select bits
These bits set the length of the polynomial (Polynomial Length = PLEN<4:0> + 1).


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**REGISTER 27-3: CRCXORH: CRC XOR POLYNOMIAL HIGH REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| X<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| X<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **X<31:16>:** XOR of Polynomial Term $X^n$ Enable bits

**REGISTER 27-4: CRCXORL: CRC XOR POLYNOMIAL LOW REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| X<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| X<7:1> | | | | | | | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-1 **X<15:1>:** XOR of Polynomial Term $X^n$ Enable bits

bit 0 **Unimplemented:** Read as '0'

**NOTES:**


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## 28.0 PARALLEL MASTER PORT (PMP)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 28. "Parallel Master Port (PMP)"** (DS70576) of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

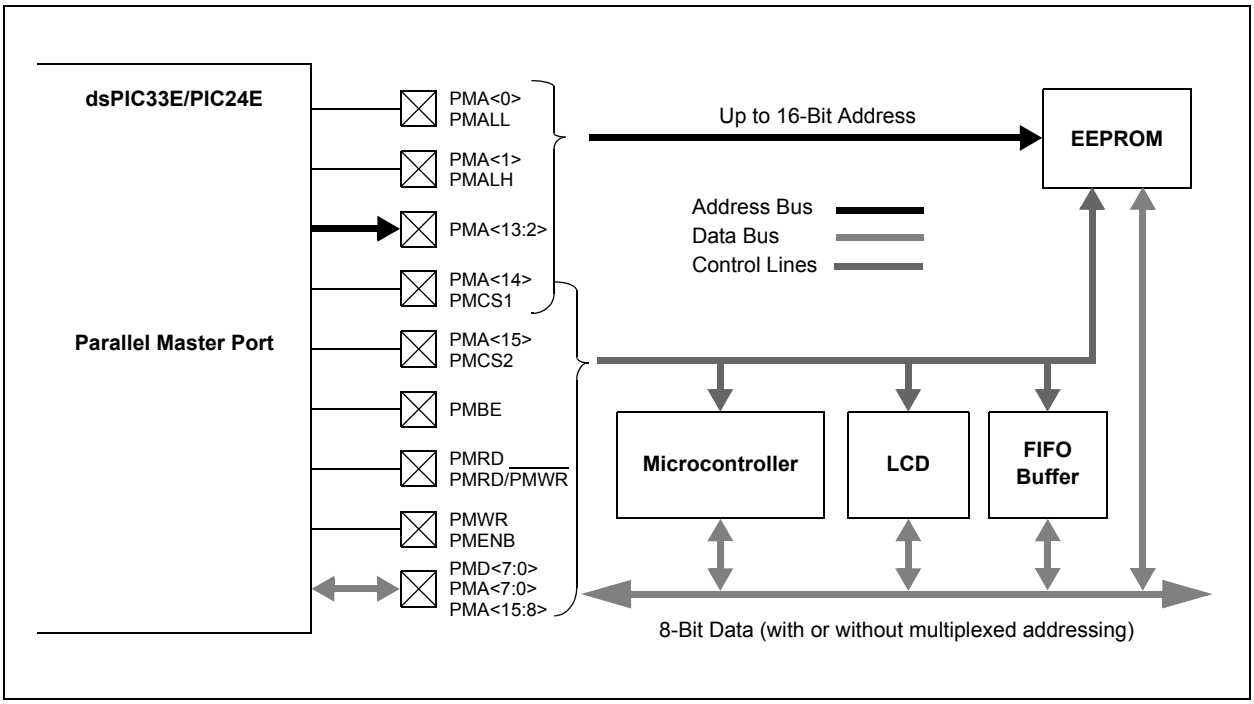
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Parallel Master Port (PMP) module is a parallel 8-bit I/O module, specifically designed to communicate with a wide variety of parallel devices, such as communication peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP is highly configurable.

Key features of the PMP module include:

- Eight Data Lines
- Up to 16 Programmable Address Lines
- Up to 2 Chip Select Lines
- Programmable Strobe Options:
  - Individual read and write strobes, or
  - Read/$\overline{\text{Write}}$ strobe with enable strobe
- Address Auto-Increment/Auto-Decrement
- Programmable Address/Data Multiplexing
- Programmable Polarity on Control Signals
- Legacy Parallel Slave Port (PSP) Support
- Enhanced Parallel Slave Support:
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait States

**FIGURE 28-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES**



## 28.1 PMP Resources

Many useful resources related to PMP are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en554310 |

### 28.1.1 KEY RESOURCES

- **Section 28. "Parallel Master Port (PMP)"** (DS70576) in the *"dsPIC33E/PIC24E Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33E/PIC24E Family Reference Manual"* Sections
- Development Tools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## 28.2 PMP Control Registers

**REGISTER 28-1: PMCON: PARALLEL MASTER PORT CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PMPEN | — | PSIDL | ADRMUX<1:0> | | PTBEEN | PTWREN | PTRDEN |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0(1) | R/W-0(1) | R/W-0(1) | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSF<1:0> | | ALP | CS2P | CS1P | BEP | WRSP | RDSP |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at Reset | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PMPEN:** Parallel Master Port Enable bit
1 = PMP module is enabled
0 = PMP module is disabled, no off-chip access is performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **PSIDL:** PMP Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
11 = Reserved
10 = All 16 bits of address are multiplexed on PMD<7:0> pins
01 = Lower eight bits of address are multiplexed on PMD<7:0> pins, upper eight bits are on PMA<15:8>
00 = Address and data appear on separate pins

bit 10 **PTBEEN:** Byte Enable Port Enable bit (16-Bit Master mode)
1 = PMBE port is enabled
0 = PMBE port is disabled

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
1 = PMWR/PMENB port is enabled
0 = PMWR/PMENB port is disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/$\overline{\text{PMWR}}$ port is enabled
0 = PMRD/$\overline{\text{PMWR}}$ port is disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits
11 = Reserved
10 = PMCS1 and PMCS2 function as Chip Select
01 = PMCS2 functions as Chip Select, PMCS1 functions as Address Bit 14
00 = PMCS1 and PMCS2 function as Address Bits 15 and 14

bit 5 **ALP:** Address Latch Polarity bit(1)
1 = Active-high ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)
0 = Active-low ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)

bit 4 **CS2P:** Chip Select 1 Polarity bit(1)
1 = Active-high ($\overline{\text{PMCS2}}$)
0 = Active-low ($\overline{\text{PMCS2}}$)

**Note 1:** These bits have no effect when their corresponding pins are used as address lines.
**2:** PMCS1 applies to Master mode and PMCS applies to Slave mode.

**REGISTER 28-1: PMCON: PARALLEL MASTER PORT CONTROL REGISTER (CONTINUED)**

bit 3 **CS1P:** Chip Select 0 Polarity bit(1)
1 = Active-high (PMCS1/PMCS)(2)
0 = Active-low (PMCS1/PMCS)

bit 2 **BEP:** Byte Enable Polarity bit
1 = Byte enable active-high (PMBE)
0 = Byte enable active-low (PMBE)

bit 1 **WRSP:** Write Strobe Polarity bit
For Slave Modes and Master Mode 2 (PMMODE<9:8> = 00, 01, 10):
1 = Write strobe is active-high (PMWR)
0 = Write strobe is active-low (PMWR)
For Master Mode 1 (PMMODE<9:8> = 11):
1 = Enables strobe active-high (PMENB)
0 = Enables strobe active-low (PMENB)

bit 0 **RDSP:** Read Strobe Polarity bit
For Slave Modes and Master Mode 2 (PMMODE<9:8> = 00, 01, 10):
1 = Read strobe is active-high (PMRD)
0 = Read strobe is active-low (PMRD)
For Master Mode 1 (PMMODE<9:8> = 11):
1 = Enables strobe active-high (PMRD/PMWR)
0 = Enables strobe active-low (PMRD/PMWR)

**Note 1:** These bits have no effect when their corresponding pins are used as address lines.
**2:** PMCS1 applies to Master mode and PMCS applies to Slave mode.


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**REGISTER 28-2: PMMODE: PARALLEL MASTER PORT MODE REGISTER**

| R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| BUSY | IRQM<1:0> | | INCM<1:0> | | MODE16 | MODE<1:0> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| WAITB<1:0>(1,2,3) | | WAITM<3:0> | | | | WAITE<1:0>(1,2,3) | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at Reset | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **BUSY:** Busy bit (Master mode only)
1 = Port is busy
0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits
11 = Interrupt is generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode), or on a read/write operation when PMA<1:0> = 11 (Addressable PSP mode only)
10 = Reserved
01 = Interrupt is generated at the end of the read/write cycle
00 = No Interrupt is generated

bit 12-11 **INCM<1:0>:** Increment Mode bits
11 = PSP read and write buffers auto-increment (Legacy PSP mode only)
10 = Decrements ADDR by 1 every read/write cycle
01 = Increments ADDR by 1 every read/write cycle
00 = No increment or decrement of address

bit 10 **MODE16:** Parallel Master Port Mode 8/16-Bit Mode bit
1 = 16-bit mode: data register is 16 bits, a read/write to the data register invokes two 8-bit transfers
0 = 8-bit mode: data register is 8 bits, a read/write to the data register invokes one 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Master Port Mode Select bits
11 = Master Mode 1 (PMCSx, PMRD/$\overline{\text{PMWR}}$, PMENB, PMBE, PMA<x:0> and PMD<7:0>)
10 = Master Mode 2 (PMCSx, PMRD, PMWR, PMBE, PMA<x:0> and PMD<7:0>)
01 = Enhanced PSP, controls signals (PMRD, PMWR, PMCSx, PMD<7:0> and PMA<1:0>)
00 = Legacy Parallel Slave Port, controls signals (PMRD, PMWR, PMCSx and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write/Address Phase Wait State Configuration bits(1,2,3)
11 = Data wait of 4 TP (demultiplexed/multiplexed); address phase of 4 TP (multiplexed)
10 = Data wait of 3 TP (demultiplexed/multiplexed); address phase of 3 TP (multiplexed)
01 = Data wait of 2 TP (demultiplexed/multiplexed); address phase of 2 TP (multiplexed)
00 = Data wait of 1 TP (demultiplexed/multiplexed); address phase of 1 TP (multiplexed)

bit 5-2 **WAITM<3:0>:** Read to Byte Enable Strobe Wait State Configuration bits
1111 = Wait of additional 15 TP
•
•
•
0001 = Wait of additional 1 TP
0000 = No additional Wait cycles (operation forced into one TP)

**Note 1:** The applied Wait state depends on whether data and address are multiplexed or demultiplexed. See **Section 28.4.1.8. "Wait States"** in **Section 28. "Parallel Master Port (PMP)"** (DS70576) in the *"dsPIC33E/PIC24E Family Reference Manual"* for more information.

**2:** WAITB<1:0> and WAITE<1:0> bits are ignored whenever WAITM<3:0> = 0000.

**3:** TP = 1/FP.

**REGISTER 28-2: PMMODE: PARALLEL MASTER PORT MODE REGISTER (CONTINUED)**

bit 1-0 **WAITE<1:0>:** Data Hold After Strobe Wait State Configuration bits(1,2,3)

11 = Wait of 4 TP
10 = Wait of 3 TP
01 = Wait of 2 TP
00 = Wait of 1 TP

**Note 1:** The applied Wait state depends on whether data and address are multiplexed or demultiplexed. See **Section 28.4.1.8. "Wait States"** in **Section 28. "Parallel Master Port (PMP)"** (DS70576) in the *"dsPIC33E/PIC24E Family Reference Manual"* for more information.

**2:** WAITB<1:0> and WAITE<1:0> bits are ignored whenever WAITM<3:0> = 0000.

**3:** TP = 1/FP.


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**REGISTER 28-3: PMADDR: PARALLEL MASTER PORT ADDRESS REGISTER (MASTER MODES ONLY)(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CS2 | CS1 | ADDR<13:8> | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADDR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at Reset | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CS2:** Chip Select 2 bit
If PMCON<7:6> = 10 or 01:
1 = Chip Select 2 is active
0 = Chip Select 2 is inactive
If PMCON<7:6> = 11 or 00:
Bit functions as ADDR<15>.

bit 14 **CS1:** Chip Select 1 bit
If PMCON<7:6> = 10:
1 = Chip Select 1 is active
0 = Chip Select 1 is inactive
If PMCON<7:6> = 11 or 0x:
Bit functions as ADDR<14>.

bit 13-0 **ADDR<13:0>:** Destination Address bits

**Note 1:** In Enhanced Slave mode, PMADDR functions as PMDOUT1, one of the two Data Buffer registers.

**REGISTER 28-4: PMAEN: PARALLEL MASTER PORT ADDRESS ENABLE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTEN15 | PTEN14 | PTEN13 | PTEN12 | PTEN11 | PTEN10 | PTEN9 | PTEN8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTEN7 | PTEN6 | PTEN5 | PTEN4 | PTEN3 | PTEN2 | PTEN1 | PTEN0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at Reset | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PTEN15:** PMCS2 Strobe Enable bit
1 = PMA15 functions as either PMA<15> or PMCS2
0 = PMA15 functions as port I/O

bit 14 **PTEN14:** PMCS1 Strobe Enable bit
1 = PMA14 functions as either PMA<14> or PMCS1
0 = PMA14 functions as port I/O

bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
1 = PMA<13:2> function as PMP address lines
0 = PMA<13:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Strobe Enable bits
1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL
0 = PMA1 and PMA0 function as port I/O


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**REGISTER 28-5: PMSTAT: PARALLEL MASTER PORT STATUS REGISTER (SLAVE MODE ONLY)**

| R-0 | R/W-0, HS | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| IBF | IBOV | — | — | IB3F | IB2F | IB1F | IB0F |
| bit 15 | | | | | | | bit 8 |

| R-1 | R/W-0, HS | U-0 | U-0 | R-1 | R-1 | R-1 | R-1 |
|---|---|---|---|---|---|---|---|
| OBE | OBUF | — | — | OB3E | OB2E | OB1E | OB0E |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at Reset | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **IBF:** Input Buffer Full Status bit
1 = All writable Input Buffer registers are full
0 = Some or all of the Writable Input Buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
1 = A write attempt to a full Input Byte register occurred (must be cleared in software)
0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IB3F:IB0F:** Input Buffer x Status Full bits
1 = Input buffer contains data that has not been read (reading the buffer will clear this bit)
0 = Input buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
1 = All readable Output Buffer registers are empty
0 = Some or all of the readable Output Buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
1 = A read occurred from an empty output byte register (must be cleared in software)
0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OB3E:OB0E:** Output Buffer x Status Empty bits
1 = Output buffer is empty (writing data to the buffer will clear this bit)
0 = Output buffer contains data that has not been transmitted

**REGISTER 28-6: PADCFG1: PAD CONFIGURATION CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | RTSECSEL | PMPTTL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-2 **Unimplemented:** Read as '0'

bit 1 Not used by the PMP module.

bit 0 **PMPTTL:** PMP Module TTL Input Buffer Select bit
1 = PMP module uses TTL input buffers
0 = PMP module uses Schmitt Trigger input buffers


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# 29.0 SPECIAL FEATURES

**Note:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

## 29.1 Configuration Bits

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices provide nonvolatile memory implementation for device Configuration bits. Refer to **Section 30. "Device Configuration"** (DS70618) of the *"dsPIC33E/PIC24E Family Reference Manual"* for more information on this implementation.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped, starting at program memory location, 0xF80000.

The individual Configuration bit descriptions for the Configuration registers are shown in Table 29-2.

Note that address, 0xF80000, is beyond the user program memory space. It belongs to the configuration memory space (0x800000-0xFFFFFF), which can only be accessed using table reads and table writes.

To prevent inadvertent configuration changes during code execution, some programmable Configuration bits are write-once. For such bits, changing a device configuration requires that the device be reset. For other Configuration bits, the device configuration changes immediately after an RTSP operation. The RTSP effect column in Table 29-2 indicates when the device configuration changes after a bit is modified using RTSP.

The device Configuration register map is shown in Table 29-1.

**TABLE 29-1: DEVICE CONFIGURATION REGISTER MAP**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| 0xF80000 | Reserved | — | — | — | — | — | — | — | — |
| 0xF80002 | Reserved | — | — | — | — | — | — | — | — |
| 0xF80004 | FGS | — | — | GSSK<1:0> | | — | — | GSS | GWRP |
| 0xF80006 | FOSCSEL | IESO | — | — | — | — | FNOSC<2:0> | | |
| 0xF80008 | FOSC | FCKSM<1:0> | | IOL1WAY | — | — | OSCIOFNC | POSCMD<1:0> | |
| 0xF8000A | FWDT | FWDTEN | WINDIS | PLLKEN | WDTPRE | WDTPOST<3:0> | | | |
| 0xF8000C | FPOR | — | — | ALTI2C2 | ALTI2C1 | BOREN(2) | FPWRT<2:0> | | |
| 0xF8000E | FICD | Reserved(1) | | JTAGEN | Reserved(1) | — | RSTPRI | ICS<1:0> | |
| 0xF80010 | FAS | — | — | APLK<1:0> | | — | — | APL | AWRP |
| 0xF80012 | FUID0 | User Unit ID Byte 0 | | | | | | | |

**Legend:** — = unimplemented bit, read as '0'

**Note 1:** These bits are reserved for use by development tools and must be programmed as '1'.

**2:** BOR should always be enabled for proper operation (BOREN = 1).

**TABLE 29-2: CONFIGURATION BITS DESCRIPTION**

| Bit Field | Register | RTSP Effect | Description |
|---|---|---|---|
| GSSK<1:0> | FGS | Immediate | General Segment Key bits<br>These bits must be set to '00' if GWRP = 1 and GSS = 1. These bits must be set to '11' for any other value of the GWRP and GSS bits.<br>Any mismatch between either the GWRP or GSS bits, and the GSSK bits (as described above), will result in code protection becoming enabled for the General Segment. A Flash bulk erase will be required to unlock the device. |
| GSS | FGS | Immediate | General Segment Code-Protect bit<br>1 = User program memory is not code-protected<br>0 = User program memory is code-protected |
| GWRP | FGS | Immediate | General Segment Write-Protect bit<br>1 = User program memory is not write-protected<br>0 = User program memory is write-protected |
| IESO | FOSCSEL | Immediate | Two-Speed Oscillator Start-up Enable bit<br>1 = Start-up device with FRC, then automatically switch to the user-selected oscillator source when ready<br>0 = Start-up device with user-selected oscillator source |
| FNOSC<2:0> | FOSCSEL | If clock switch is enabled, the RTSP effect is on any device Reset; otherwise, immediate | Initial Oscillator Source Selection bits<br>111 = Internal Fast RC (FRC) Oscillator with Postscaler<br>110 = Internal Fast RC (FRC) Oscillator with Divide-by-16<br>101 = LPRC Oscillator<br>100 = Secondary (LP) Oscillator<br>011 = Primary (XT, HS, EC) Oscillator with PLL<br>010 = Primary (XT, HS, EC) Oscillator<br>001 = Internal Fast RC (FRC) Oscillator with PLL<br>000 = FRC Oscillator |
| FCKSM<1:0> | FOSC | Immediate | Clock Switching Mode bits<br>1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled<br>01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled<br>00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled |
| IOL1WAY | FOSC | Immediate | Peripheral Pin Select Configuration bit<br>1 = Allows only one reconfiguration<br>0 = Allows multiple reconfigurations |
| OSCIOFNC | FOSC | Immediate | OSC2 Pin Function bit (except in XT and HS modes)<br>1 = OSC2 is the clock output<br>0 = OSC2 is the general purpose digital I/O pin |
| POSCMD<1:0> | FOSC | Immediate | Primary Oscillator Mode Select bits<br>11 = Primary Oscillator is disabled<br>10 = HS Crystal Oscillator mode<br>01 = XT Crystal Oscillator mode<br>00 = EC (External Clock) mode |
| FWDTEN | FWDT | Immediate | Watchdog Timer Enable bit<br>1 = Watchdog Timer is always enabled (LPRC Oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register has no effect.)<br>0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register.) |

**Note 1:** BOR should always be enabled for proper operation (BOREN = 1).

**2:** This register can only be modified when code protection and write protection are disabled for both the General and Auxiliary Segments (APL = 1, AWRP = 1, APLK = 0, GSS = 1, GWRP = 1 and GSSK = 0).


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**TABLE 29-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)**

| Bit Field | Register | RTSP Effect | Description |
|---|---|---|---|
| WINDIS | FWDT | Immediate | Watchdog Timer Window Enable bit<br>1 = Watchdog Timer is in Non-Window mode<br>0 = Watchdog Timer is in Window mode |
| PLLKEN | FWDT | Immediate | PLL Lock Wait Enable bit<br>1 = Clock switches to the PLL source will wait until the PLL lock signal is valid<br>0 = Clock switch will not wait for PLL lock |
| WDTPRE | FWDT | Immediate | Watchdog Timer Prescaler bit<br>1 = 1:128<br>0 = 1:32 |
| APLK<1:0> | FAS(2) | Immediate | Auxiliary Segment Key bits<br>These bits must be set to '00' if AWRP = 1 and APL = 1. These bits must be set to '11' for any other value of the AWRP and APL bits.<br>Any mismatch between either the AWRP or APL bits and the APLK bits (as described above), will result in code protection becoming enabled for the Auxiliary Segment. A Flash bulk erase will be required to unlock the device. |
| APL | FAS(2) | Immediate | Auxiliary Segment Code-Protect bit<br>1 = Auxiliary program memory is not code-protected<br>0 = Auxiliary program memory is code-protected |
| AWRP | FAS(2) | Immediate | Auxiliary Segment Write-Protect bit<br>1 = Auxiliary program memory is not write-protected<br>0 = Auxiliary program memory is write-protected |
| WDTPOST<3:0> | FWDT | Immediate | Watchdog Timer Postscaler bits<br>1111 = 1:32,768<br>1110 = 1:16,384<br>•<br>•<br>•<br>0001 = 1:2<br>0000 = 1:1 |
| FPWRT<2:0> | FPOR | Immediate | Power-on Reset Timer Value Select bits<br>111 = PWRT = 128 ms<br>110 = PWRT = 64 ms<br>101 = PWRT = 32 ms<br>100 = PWRT = 16 ms<br>011 = PWRT = 8 ms<br>010 = PWRT = 4 ms<br>001 = PWRT = 2 ms<br>000 = PWRT = Disabled |
| BOREN(1) | FPOR | Immediate | Brown-out Reset (BOR) Detection Enable bit<br>1 = BOR is enabled<br>0 = BOR is disabled |
| ALTI2C2 | FPOR | Immediate | Alternate $I^2C$™ pins for I2C2 bit<br>1 = I2C2 is mapped to the SDA2/SCL2 pins<br>0 = I2C2 is mapped to the ASDA2/ASCL2 pins |
| ALTI2C1 | FPOR | Immediate | Alternate $I^2C$ pins for I2C1 bit<br>1 = I2C1 is mapped to the SDA1/SCL1 pins<br>0 = I2C1 is mapped to the ASDA1/ASCL1 pins |

**Note 1:** BOR should always be enabled for proper operation (BOREN = 1).

**2:** This register can only be modified when code protection and write protection are disabled for both the General and Auxiliary Segments (APL = 1, AWRP = 1, APLK = 0, GSS = 1, GWRP = 1 and GSSK = 0).

**TABLE 29-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)**

| Bit Field | Register | RTSP Effect | Description |
|---|---|---|---|
| JTAGEN | FICD | Immediate | JTAG Enable bit<br>1 = JTAG is enabled<br>0 = JTAG is disabled |
| RSTPRI | FICD | On any device Reset | Reset Target Vector Select bit<br>1 = Device will reset to Primary Flash Reset location<br>0 = Device will reset to Auxiliary Flash Reset location |
| ICS<1:0> | FICD | Immediate | ICD Communication Channel Select bits<br>11 = Communicate on PGEC1 and PGED1<br>10 = Communicate on PGEC2 and PGED2<br>01 = Communicate on PGEC3 and PGED3<br>00 = Reserved, do not use |

**Note 1:** BOR should always be enabled for proper operation (BOREN = 1).

**2:** This register can only be modified when code protection and write protection are disabled for both the General and Auxiliary Segments (APL = 1, AWRP = 1, APLK = 0, GSS = 1, GWRP = 1 and GSSK = 0).


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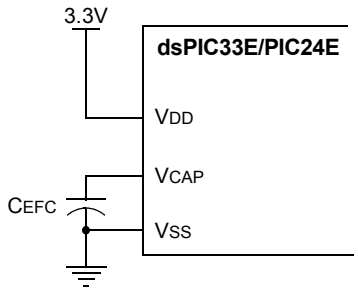
## 29.2 On-Chip Voltage Regulator

All of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohms) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 29-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 32-13 located in **Section 32.0 "Electrical Characteristics"**.

| **Note:** | It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin. |
|---|---|

**FIGURE 29-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR(1,2,3)**




**Note 1:** These are typical operating voltages. Refer to Table 32-13 located in **Section 32.1 "DC Characteristics"** for the full operating ranges of VDD and VCAP.

**2:** It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

**3:** Typical VCAP pin voltage is 1.8V when VDD ≥ VDDMIN.

## 29.3 Brown-out Reset (BOR)

The Brown-out Reset module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines, or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the Power-up Timer (PWRT) Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 32-22 of **Section 32.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR Status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit, continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

## 29.4 Watchdog Timer (WDT)

For dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices, the WDT is driven by the LPRC Oscillator. When the WDT is enabled, the clock source is also enabled.

### 29.4.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a nominal WDT Time-out (TWDT) period of 1 ms in 5-bit mode or 4 ms in 7-bit mode.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSC bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

**Note:** The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

### 29.4.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bits (RCON<3,2>) need to be cleared in software after the device wakes up.

### 29.4.3 ENABLING WDT

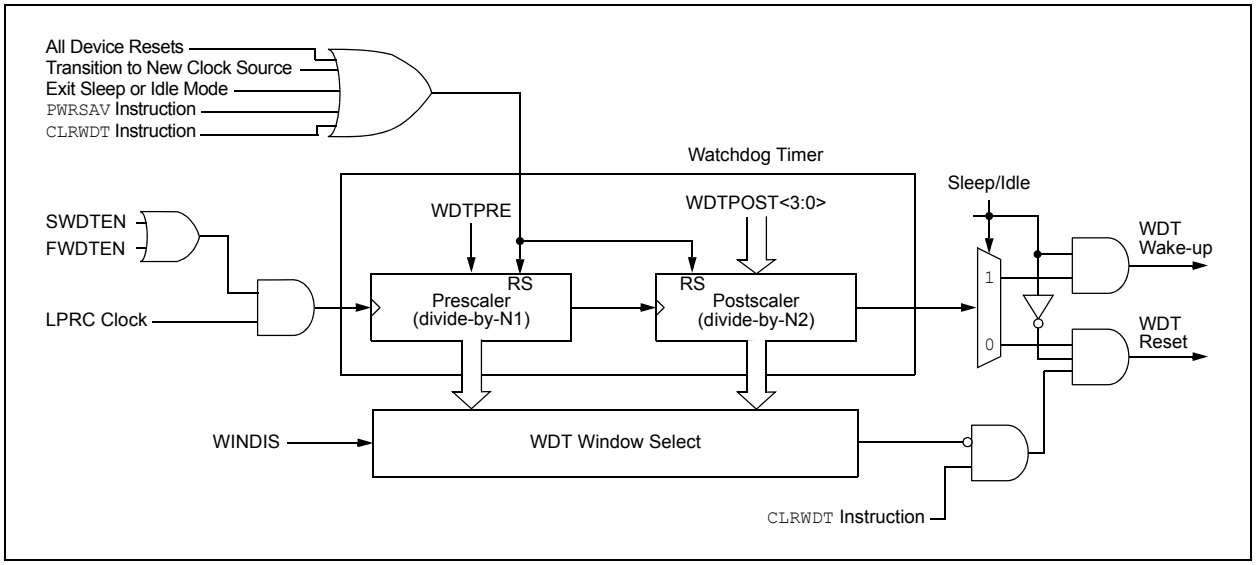
The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

**Note:** If the WINDIS bit (FWDT<6>) is cleared, the CLRWDT instruction should be executed by the application software only during the last 1/4 of the WDT period. This CLRWDT instruction window can be determined by using a timer. If a CLRWDT instruction is executed before this window, a WDT Reset occurs.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

**FIGURE 29-2: WDT BLOCK DIAGRAM**





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## 29.5 JTAG Interface

dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface is provided in future revisions of the document.

**Note:** Refer to **Section 24. "Programming and Diagnostics"** (DS70608) of the *"dsPIC33E/PIC24E Family Reference Manual"* for further information on usage, configuration and operation of the JTAG interface.

## 29.6 In-Circuit Serial Programming

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the digital signal controller just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the *"dsPIC33E/PIC24E Flash Programming Specification"* (DS70619) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

## 29.7 In-Circuit Debugger

When MPLAB® ICD 3 or REAL ICE™ is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, $V_{DD}$, $V_{SS}$ and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

## 29.8 Code Protection and CodeGuard™ Security

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices offer basic implementation of CodeGuard Security that supports only General Segment (GS) security. This feature helps protect individual Intellectual Property in collaborative system designs.

When coupled with software encryption libraries, CodeGuard Security can be used to securely update Flash even when multiple IPs reside on the single chip. The code protection features vary depending on the actual dsPIC33E implemented. The following sections provide an overview of these features.

The dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices do not support Boot Segment (BS), Secure Segment (SS) and RAM protection.

**Note:** Refer to **Section 23. "CodeGuard™ Security"** (DS70634) of the *"dsPIC33E/PIC24E Family Reference Manual"* for further information on usage, configuration and operation of CodeGuard Security.

**NOTES:**


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## 30.0 INSTRUCTION SET SUMMARY

**Note:** This data sheet summarizes the features of the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "*dsPIC33E/PIC24E Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

The dsPIC33EP instruction set is almost identical to that of the dsPIC30F and dsPIC33F. The PIC24EP instruction set is almost identical to that of the PIC24F and PIC24H.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- DSP operations
- Control operations

Table 30-1 lists the general symbols used in describing the instructions.

The dsPIC33E instruction set summary in Table 30-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register 'Wb' without any address modifier
- The second source operand, which is typically a register 'Ws' with or without an address modifier
- The destination of the result, which is typically a register 'Wd' with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value 'f'
- The destination, which could be either the file register 'f' or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register 'Wb')

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register 'Wb' without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register 'Wd' with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write-back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register 'Wn' or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the table read and table write instructions

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction, or a PSV or table read is performed. In these cases, the execution takes multiple instruction cycles with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

**Note:** For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

**TABLE 30-1: SYMBOLS USED IN OPCODE DESCRIPTIONS**

| Field | Description |
|---|---|
| #text | Means literal defined by "text" |
| (text) | Means "content of text" |
| [text] | Means "the location addressed by text" |
| { } | Optional field or operation |
| a ∈ {b, c, d} | a is selected from the set of values b, c, d |
| <n:m> | Register bit field |
| .b | Byte mode selection |
| .d | Double-Word mode selection |
| .S | Shadow register select |
| .w | Word mode selection (default) |
| Acc | One of two accumulators {A, B} |
| AWB | Accumulator Write-Back Destination Address register ∈ {W13, [W13]+ = 2} |
| bit4 | 4-bit bit selection field (used in word addressed instructions) ∈ {0...15} |
| C, DC, N, OV, Z | MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero |
| Expr | Absolute address, label or expression (resolved by the linker) |
| f | File register address ∈ {0x0000...0x1FFF} |
| lit1 | 1-bit unsigned literal ∈ {0,1} |
| lit4 | 4-bit unsigned literal ∈ {0...15} |
| lit5 | 5-bit unsigned literal ∈ {0...31} |
| lit8 | 8-bit unsigned literal ∈ {0...255} |
| lit10 | 10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode |
| lit14 | 14-bit unsigned literal ∈ {0...16384} |
| lit16 | 16-bit unsigned literal ∈ {0...65535} |
| lit23 | 23-bit unsigned literal ∈ {0...8388608}; LSb must be '0' |
| None | Field does not require an entry, can be blank |
| OA, OB, SA, SB | DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate |
| PC | Program Counter |
| Slit10 | 10-bit signed literal ∈ {-512...511} |
| Slit16 | 16-bit signed literal ∈ {-32768...32767} |
| Slit6 | 6-bit signed literal ∈ {-16...16} |
| Wb | Base W register ∈ {W0...W15} |
| Wd | Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] } |
| Wdo | Destination W register ∈<br>{ Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] } |
| Wm,Wn | Dividend, Divisor Working register pair (Direct Addressing) |


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**TABLE 30-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)**

| Field | Description |
|---|---|
| Wm*Wm | Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7} |
| Wm*Wn | Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7} |
| Wn | One of 16 working registers ∈ {W0...W15} |
| Wnd | One of 16 destination working registers ∈ {W0...W15} |
| Wns | One of 16 source working registers ∈ {W0...W15} |
| WREG | W0 (working register used in file register instructions) |
| Ws | Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] } |
| Wso | Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] } |
| Wx | X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none} |
| Wxd | X Data Space Prefetch Destination register for DSP instructions ∈ {W4...W7} |
| Wy | Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none} |
| Wyd | Y Data Space Prefetch Destination register for DSP instructions ∈ {W4...W7} |

**TABLE 30-2: INSTRUCTION SET OVERVIEW**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles(2) | Status Flags Affected |
|---|---|---|---|---|---|---|
| 1 | ADD | ADD Acc(1) | Add Accumulators | 1 | 1 | OA,OB,SA,SB |
| | | ADD f | f = f + WREG | 1 | 1 | C,DC,N,OV,Z |
| | | ADD f,WREG | WREG = f + WREG | 1 | 1 | C,DC,N,OV,Z |
| | | ADD #lit10,Wn | Wd = lit10 + Wd | 1 | 1 | C,DC,N,OV,Z |
| | | ADD Wb,Ws,Wd | Wd = Wb + Ws | 1 | 1 | C,DC,N,OV,Z |
| | | ADD Wb,#lit5,Wd | Wd = Wb + lit5 | 1 | 1 | C,DC,N,OV,Z |
| | | ADD Wso,#Slit4,Acc | 16-bit Signed Add to Accumulator | 1 | 1 | OA,OB,SA,SB |
| 2 | ADDC | ADDC f | f = f + WREG + (C) | 1 | 1 | C,DC,N,OV,Z |
| | | ADDC f,WREG | WREG = f + WREG + (C) | 1 | 1 | C,DC,N,OV,Z |
| | | ADDC #lit10,Wn | Wd = lit10 + Wd + (C) | 1 | 1 | C,DC,N,OV,Z |
| | | ADDC Wb,Ws,Wd | Wd = Wb + Ws + (C) | 1 | 1 | C,DC,N,OV,Z |
| | | ADDC Wb,#lit5,Wd | Wd = Wb + lit5 + (C) | 1 | 1 | C,DC,N,OV,Z |
| 3 | AND | AND f | f = f .AND. WREG | 1 | 1 | N,Z |
| | | AND f,WREG | WREG = f .AND. WREG | 1 | 1 | N,Z |
| | | AND #lit10,Wn | Wd = lit10 .AND. Wd | 1 | 1 | N,Z |
| | | AND Wb,Ws,Wd | Wd = Wb .AND. Ws | 1 | 1 | N,Z |
| | | AND Wb,#lit5,Wd | Wd = Wb .AND. lit5 | 1 | 1 | N,Z |
| 4 | ASR | ASR f | f = Arithmetic Right Shift f | 1 | 1 | C,N,OV,Z |
| | | ASR f,WREG | WREG = Arithmetic Right Shift f | 1 | 1 | C,N,OV,Z |
| | | ASR Ws,Wd | Wd = Arithmetic Right Shift Ws | 1 | 1 | C,N,OV,Z |
| | | ASR Wb,Wns,Wnd | Wnd = Arithmetic Right Shift Wb by Wns | 1 | 1 | N,Z |
| | | ASR Wb,#lit5,Wnd | Wnd = Arithmetic Right Shift Wb by lit5 | 1 | 1 | N,Z |
| 5 | BCLR | BCLR f,#bit4 | Bit Clear f | 1 | 1 | None |
| | | BCLR Ws,#bit4 | Bit Clear Ws | 1 | 1 | None |
| 6 | BRA | BRA C,Expr | Branch if Carry | 1 | 1 (4) | None |
| | | BRA GE,Expr | Branch if greater than or equal | 1 | 1 (4) | None |
| | | BRA GEU,Expr | Branch if unsigned greater than or equal | 1 | 1 (4) | None |
| | | BRA GT,Expr | Branch if greater than | 1 | 1 (4) | None |
| | | BRA GTU,Expr | Branch if unsigned greater than | 1 | 1 (4) | None |
| | | BRA LE,Expr | Branch if less than or equal | 1 | 1 (4) | None |
| | | BRA LEU,Expr | Branch if unsigned less than or equal | 1 | 1 (4) | None |
| | | BRA LT,Expr | Branch if less than | 1 | 1 (4) | None |
| | | BRA LTU,Expr | Branch if unsigned less than | 1 | 1 (4) | None |
| | | BRA N,Expr | Branch if Negative | 1 | 1 (4) | None |
| | | BRA NC,Expr | Branch if Not Carry | 1 | 1 (4) | None |
| | | BRA NN,Expr | Branch if Not Negative | 1 | 1 (4) | None |
| | | BRA NOV,Expr | Branch if Not Overflow | 1 | 1 (4) | None |
| | | BRA NZ,Expr | Branch if Not Zero | 1 | 1 (4) | None |
| | | BRA OA,Expr(1) | Branch if Accumulator A overflow | 1 | 1 (4) | None |
| | | BRA OB,Expr(1) | Branch if Accumulator B overflow | 1 | 1 (4) | None |
| | | BRA OV,Expr(1) | Branch if Overflow | 1 | 1 (4) | None |
| | | BRA SA,Expr(1) | Branch if Accumulator A saturated | 1 | 1 (4) | None |
| | | BRA SB,Expr(1) | Branch if Accumulator B saturated | 1 | 1 (4) | None |
| | | BRA Expr | Branch Unconditionally | 1 | 4 | None |
| | | BRA Z,Expr | Branch if Zero | 1 | 1 (4) | None |
| | | BRA Wn | Computed Branch | 1 | 4 | None |
| 7 | BSET | BSET f,#bit4 | Bit Set f | 1 | 1 | None |
| | | BSET Ws,#bit4 | Bit Set Ws | 1 | 1 | None |

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**TABLE 30-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles(2) | Status Flags Affected |
|---|---|---|---|---|---|---|
| 8 | BSW | BSW.C Ws,Wb | Write C bit to Ws<Wb> | 1 | 1 | None |
| | | BSW.Z Ws,Wb | Write Z bit to Ws<Wb> | 1 | 1 | None |
| 9 | BTG | BTG f,#bit4 | Bit Toggle f | 1 | 1 | None |
| | | BTG Ws,#bit4 | Bit Toggle Ws | 1 | 1 | None |
| 10 | BTSC | BTSC f,#bit4 | Bit Test f, Skip if Clear | 1 | 1 (2 or 3) | None |
| | | BTSC Ws,#bit4 | Bit Test Ws, Skip if Clear | 1 | 1 (2 or 3) | None |
| 11 | BTSS | BTSS f,#bit4 | Bit Test f, Skip if Set | 1 | 1 (2 or 3) | None |
| | | BTSS Ws,#bit4 | Bit Test Ws, Skip if Set | 1 | 1 (2 or 3) | None |
| 12 | BTST | BTST f,#bit4 | Bit Test f | 1 | 1 | Z |
| | | BTST.C Ws,#bit4 | Bit Test Ws to C | 1 | 1 | C |
| | | BTST.Z Ws,#bit4 | Bit Test Ws to Z | 1 | 1 | Z |
| | | BTST.C Ws,Wb | Bit Test Ws<Wb> to C | 1 | 1 | C |
| | | BTST.Z Ws,Wb | Bit Test Ws<Wb> to Z | 1 | 1 | Z |
| 13 | BTSTS | BTSTS f,#bit4 | Bit Test then Set f | 1 | 1 | Z |
| | | BTSTS.C Ws,#bit4 | Bit Test Ws to C, then Set | 1 | 1 | C |
| | | BTSTS.Z Ws,#bit4 | Bit Test Ws to Z, then Set | 1 | 1 | Z |
| 14 | CALL | CALL lit23 | Call subroutine | 2 | 4 | SFA |
| | | CALL Wn | Call indirect subroutine | 1 | 4 | SFA |
| | | CALL.L Wn | Call indirect subroutine (long address) | 1 | 4 | SFA |
| 15 | CLR | CLR f | f = 0x0000 | 1 | 1 | None |
| | | CLR WREG | WREG = 0x0000 | 1 | 1 | None |
| | | CLR Ws | Ws = 0x0000 | 1 | 1 | None |
| | | CLR Acc,Wx,Wxd,Wy,Wyd,AWB(1) | Clear Accumulator | 1 | 1 | OA,OB,SA,SB |
| 16 | CLRWDT | CLRWDT | Clear Watchdog Timer | 1 | 1 | WDTO,Sleep |
| 17 | COM | COM f | $f = \overline{f}$ | 1 | 1 | N,Z |
| | | COM f,WREG | $WREG = \overline{f}$ | 1 | 1 | N,Z |
| | | COM Ws,Wd | $Wd = \overline{Ws}$ | 1 | 1 | N,Z |
| 18 | CP | CP f | Compare f with WREG | 1 | 1 | C,DC,N,OV,Z |
| | | CP Wb,#lit8 | Compare Wb with lit8 | 1 | 1 | C,DC,N,OV,Z |
| | | CP Wb,Ws | Compare Wb with Ws (Wb – Ws) | 1 | 1 | C,DC,N,OV,Z |
| 19 | CP0 | CP0 f | Compare f with 0x0000 | 1 | 1 | C,DC,N,OV,Z |
| | | CP0 Ws | Compare Ws with 0x0000 | 1 | 1 | C,DC,N,OV,Z |
| 20 | CPB | CPB f | Compare f with WREG, with Borrow | 1 | 1 | C,DC,N,OV,Z |
| | | CPB Wb,#lit8 | Compare Wb with lit8, with Borrow | 1 | 1 | C,DC,N,OV,Z |
| | | CPB Wb,Ws | Compare Wb with Ws, with Borrow ($Wb – Ws – \overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 21 | CPSEQ | CPSEQ Wb,Wn | Compare Wb with Wn, skip if = | 1 | 1 (2 or 3) | None |
| | CPBEQ | CPBEQ Wb,Wn,Expr | Compare Wb with Wn, branch if = | 1 | 1 (5) | None |
| 22 | CPSGT | CPSGT Wb,Wn | Compare Wb with Wn, skip if > | 1 | 1 (2 or 3) | None |
| | CPBGT | CPBGT Wb,Wn,Expr | Compare Wb with Wn, branch if > | 1 | 1 (5) | None |
| 23 | CPSLT | CPSLT Wb,Wn | Compare Wb with Wn, skip if < | 1 | 1 (2 or 3) | None |
| | CPBLT | CPBLT Wb,Wn,Expr | Compare Wb with Wn, branch if < | 1 | 1 (5) | None |
| 24 | CPSNE | CPSNE Wb,Wn | Compare Wb with Wn, skip if ≠ | 1 | 1 (2 or 3) | None |
| | CPBNE | CPBNE Wb,Wn,Expr | Compare Wb with Wn, branch if ≠ | 1 | 1 (5) | None |

**Note 1:** This instruction is available in dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

**TABLE 30-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles(2) | Status Flags Affected |
|---|---|---|---|---|---|---|
| 25 | DAW | DAW Wn | Wn = decimal adjust Wn | 1 | 1 | C |
| 26 | DEC | DEC f | f = f – 1 | 1 | 1 | C,DC,N,OV,Z |
| | | DEC f,WREG | WREG = f – 1 | 1 | 1 | C,DC,N,OV,Z |
| | | DEC Ws,Wd | Wd = Ws – 1 | 1 | 1 | C,DC,N,OV,Z |
| 27 | DEC2 | DEC2 f | f = f – 2 | 1 | 1 | C,DC,N,OV,Z |
| | | DEC2 f,WREG | WREG = f – 2 | 1 | 1 | C,DC,N,OV,Z |
| | | DEC2 Ws,Wd | Wd = Ws – 2 | 1 | 1 | C,DC,N,OV,Z |
| 28 | DISI | DISI #lit14 | Disable Interrupts for k instruction cycles | 1 | 1 | None |
| 29 | DIV | DIV.S Wm,Wn | Signed 16/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| | | DIV.SD Wm,Wn | Signed 32/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| | | DIV.U Wm,Wn | Unsigned 16/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| | | DIV.UD Wm,Wn | Unsigned 32/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| 30 | DIVF | DIVF Wm,Wn(1) | Signed 16/16-bit Fractional Divide | 1 | 18 | N,Z,C,OV |
| 31 | DO | DO #lit15,Expr(1) | Do code to PC + Expr, lit15 + 1 times | 2 | 2 | None |
| | | DO Wn,Expr(1) | Do code to PC + Expr, (Wn) + 1 times | 2 | 2 | None |
| 32 | ED | ED Wm*Wm,Acc,Wx,Wy,Wxd(1) | Euclidean Distance (no accumulate) | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 33 | EDAC | EDAC Wm*Wm,Acc,Wx,Wy,Wxd(1) | Euclidean Distance | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 34 | EXCH | EXCH Wns,Wnd | Swap Wns with Wnd | 1 | 1 | None |
| 35 | FBCL | FBCL Ws,Wnd | Find Bit Change from Left (MSb) Side | 1 | 1 | C |
| 36 | FF1L | FF1L Ws,Wnd | Find First One from Left (MSb) Side | 1 | 1 | C |
| 37 | FF1R | FF1R Ws,Wnd | Find First One from Right (LSb) Side | 1 | 1 | C |
| 38 | GOTO | GOTO Expr | Go to address | 2 | 4 | None |
| | | GOTO Wn | Go to indirect | 1 | 4 | None |
| | | GOTO.L Wn | Go to indirect (long address) | 1 | 4 | None |
| 39 | INC | INC f | f = f + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | INC f,WREG | WREG = f + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | INC Ws,Wd | Wd = Ws + 1 | 1 | 1 | C,DC,N,OV,Z |
| 40 | INC2 | INC2 f | f = f + 2 | 1 | 1 | C,DC,N,OV,Z |
| | | INC2 f,WREG | WREG = f + 2 | 1 | 1 | C,DC,N,OV,Z |
| | | INC2 Ws,Wd | Wd = Ws + 2 | 1 | 1 | C,DC,N,OV,Z |
| 41 | IOR | IOR f | f = f .IOR. WREG | 1 | 1 | N,Z |
| | | IOR f,WREG | WREG = f .IOR. WREG | 1 | 1 | N,Z |
| | | IOR #lit10,Wn | Wd = lit10 .IOR. Wd | 1 | 1 | N,Z |
| | | IOR Wb,Ws,Wd | Wd = Wb .IOR. Ws | 1 | 1 | N,Z |
| | | IOR Wb,#lit5,Wd | Wd = Wb .IOR. lit5 | 1 | 1 | N,Z |
| 42 | LAC | LAC Wso,#Slit4,Acc | Load Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 43 | LNK | LNK #lit14 | Link Frame Pointer | 1 | 1 | SFA |
| 44 | LSR | LSR f | f = Logical Right Shift f | 1 | 1 | C,N,OV,Z |
| | | LSR f,WREG | WREG = Logical Right Shift f | 1 | 1 | C,N,OV,Z |
| | | LSR Ws,Wd | Wd = Logical Right Shift Ws | 1 | 1 | C,N,OV,Z |
| | | LSR Wb,Wns,Wnd | Wnd = Logical Right Shift Wb by Wns | 1 | 1 | N,Z |
| | | LSR Wb,#lit5,Wnd | Wnd = Logical Right Shift Wb by lit5 | 1 | 1 | N,Z |
| 45 | MAC | MAC Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB(1) | Multiply and Accumulate | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | MAC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd(1) | Square and Accumulate | 1 | 1 | OA,OB,OAB, SA,SB,SAB |

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**TABLE 30-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles(2) | Status Flags Affected |
|---|---|---|---|---|---|---|
| 46 | MOV | MOV f,Wn | Move f to Wn | 1 | 1 | None |
| | | MOV f | Move f to f | 1 | 1 | None |
| | | MOV f,WREG | Move f to WREG | 1 | 1 | None |
| | | MOV #lit16,Wn | Move 16-bit literal to Wn | 1 | 1 | None |
| | | MOV.b #lit8,Wn | Move 8-bit literal to Wn | 1 | 1 | None |
| | | MOV Wn,f | Move Wn to f | 1 | 1 | None |
| | | MOV Wso,Wdo | Move Ws to Wd | 1 | 1 | None |
| | | MOV WREG,f | Move WREG to f | 1 | 1 | None |
| | | MOV.D Wns,Wd | Move Double from W(ns):W(ns + 1) to Wd | 1 | 2 | None |
| | | MOV.D Ws,Wnd | Move Double from Ws to W(nd + 1):W(nd) | 1 | 2 | None |
| 47 | MOVPAG | MOVPAG #lit10,DSRPAG | Move 10-bit literal to DSRPAG | 1 | 1 | None |
| | | MOVPAG #lit9,DSWPAG | Move 9-bit literal to DSWPAG | 1 | 1 | None |
| | | MOVPAG #lit8,TBLPAG | Move 8-bit literal to TBLPAG | 1 | 1 | None |
| | | MOVPAGW Ws, DSRPAG | Move Ws<9:0> to DSRPAG | 1 | 1 | None |
| | | MOVPAGW Ws, DSWPAG | Move Ws<8:0> to DSWPAG | 1 | 1 | None |
| | | MOVPAGW Ws, TBLPAG | Move Ws<7:0> to TBLPAG | 1 | 1 | None |
| 48 | MOVSAC | MOVSAC Acc,Wx,Wxd,Wy,Wyd,AWB(1) | Prefetch and store accumulator | 1 | 1 | None |
| 49 | MPY | MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd(1) | Multiply Wm by Wn to Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | MPY Wm*Wm,Acc,Wx,Wxd,Wy,Wyd(1) | Square Wm to Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 50 | MPY.N | MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd(1) | -(Multiply Wm by Wn) to Accumulator | 1 | 1 | None |
| 51 | MSC | MSC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd,AWB(1) | Multiply and Subtract from Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 52 | MUL | MUL.SS Wb,Ws,Wnd | {Wnd + 1, Wnd} = signed(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.SS Wb,Ws,Acc(1) | Accumulator = signed(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.SU Wb,Ws,Wnd | {Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.SU Wb,Ws,Acc(1) | Accumulator = signed(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.SU Wb,#lit5,Acc(1) | Accumulator = signed(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.US Wb,Ws,Wnd | {Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.US Wb,Ws,Acc(1) | Accumulator = unsigned(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.UU Wb,Ws,Wnd | {Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.UU Wb,#lit5,Acc(1) | Accumulator = unsigned(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.UU Wb,Ws,Acc(1) | Accumulator = unsigned(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MULW.SS Wb,Ws,Wnd | Wnd = signed(Wb) * signed(Ws) | 1 | 1 | None |
| | | MULW.SU Wb,Ws,Wnd | Wnd = signed(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MULW.US Wb,Ws,Wnd | Wnd = unsigned(Wb) * signed(Ws) | 1 | 1 | None |
| | | MULW.UU Wb,Ws,Wnd | Wnd = unsigned(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.SU Wb,#lit5,Wnd | {Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.SU Wb,#lit5,Wnd | Wnd = signed(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.UU Wb,#lit5,Wnd | {Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.UU Wb,#lit5,Wnd | Wnd = unsigned(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL f | W3:W2 = f * WREG | 1 | 1 | None |

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**TABLE 30-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles(2) | Status Flags Affected |
|---|---|---|---|---|---|---|
| 53 | NEG | NEG Acc(1) | Negate Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | NEG f | f = $\bar{f}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | NEG f,WREG | WREG = $\bar{f}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | NEG Ws,Wd | Wd = $\overline{Ws}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| 54 | NOP | NOP | No Operation | 1 | 1 | None |
| | | NOPR | No Operation | 1 | 1 | None |
| 55 | POP | POP f | Pop f from Top-of-Stack (TOS) | 1 | 1 | None |
| | | POP Wdo | Pop from Top-of-Stack (TOS) to Wdo | 1 | 1 | None |
| | | POP.D Wnd | Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1) | 1 | 2 | None |
| | | POP.S | Pop Shadow Registers | 1 | 1 | All |
| 56 | PUSH | PUSH f | Push f to Top-of-Stack (TOS) | 1 | 1 | None |
| | | PUSH Wso | Push Wso to Top-of-Stack (TOS) | 1 | 1 | None |
| | | PUSH.D Wns | Push W(ns):W(ns + 1) to Top-of-Stack (TOS) | 1 | 2 | None |
| | | PUSH.S | Push Shadow Registers | 1 | 1 | None |
| 57 | PWRSAV | PWRSAV #lit1 | Go into Sleep or Idle mode | 1 | 1 | WDTO,Sleep |
| 58 | RCALL | RCALL Expr | Relative Call | 1 | 4 | SFA |
| | | RCALL Wn | Computed Call | 1 | 4 | SFA |
| 59 | REPEAT | REPEAT #lit15 | Repeat Next Instruction lit15 + 1 times | 1 | 1 | None |
| | | REPEAT Wn | Repeat Next Instruction (Wn) + 1 times | 1 | 1 | None |
| 60 | RESET | RESET | Software device Reset | 1 | 1 | None |
| 61 | RETFIE | RETFIE | Return from interrupt | 1 | 6 (5) | SFA |
| 62 | RETLW | RETLW #lit10,Wn | Return with literal in Wn | 1 | 6 (5) | SFA |
| 63 | RETURN | RETURN | Return from Subroutine | 1 | 6 (5) | SFA |
| 64 | RLC | RLC f | f = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC f,WREG | WREG = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC Ws,Wd | Wd = Rotate Left through Carry Ws | 1 | 1 | C,N,Z |
| 65 | RLNC | RLNC f | f = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC f,WREG | WREG = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC Ws,Wd | Wd = Rotate Left (No Carry) Ws | 1 | 1 | N,Z |
| 66 | RRC | RRC f | f = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC f,WREG | WREG = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC Ws,Wd | Wd = Rotate Right through Carry Ws | 1 | 1 | C,N,Z |
| 67 | RRNC | RRNC f | f = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC f,WREG | WREG = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC Ws,Wd | Wd = Rotate Right (No Carry) Ws | 1 | 1 | N,Z |
| 68 | SAC | SAC Acc,#Slit4,Wdo(1) | Store Accumulator | 1 | 1 | None |
| | | SAC.R Acc,#Slit4,Wdo(1) | Store Rounded Accumulator | 1 | 1 | None |
| 69 | SE | SE Ws,Wnd | Wnd = sign-extended Ws | 1 | 1 | C,N,Z |
| 70 | SETM | SETM f | f = 0xFFFF | 1 | 1 | None |
| | | SETM WREG | WREG = 0xFFFF | 1 | 1 | None |
| | | SETM Ws | Ws = 0xFFFF | 1 | 1 | None |
| 71 | SFTAC | SFTAC Acc,Wn(1) | Arithmetic Shift Accumulator by (Wn) | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | SFTAC Acc,#Slit6(1) | Arithmetic Shift Accumulator by Slit6 | 1 | 1 | OA,OB,OAB, SA,SB,SAB |

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| Base Instr # | Assembly Mnemonic | Assembly Syntax | | Description | # of Words | # of Cycles(2) | Status Flags Affected |
|---|---|---|---|---|---|---|---|
| 72 | SL | SL | f | f = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL | f,WREG | WREG = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL | Ws,Wd | Wd = Left Shift Ws | 1 | 1 | C,N,OV,Z |
| | | SL | Wb,Wns,Wnd | Wnd = Left Shift Wb by Wns | 1 | 1 | N,Z |
| | | SL | Wb,#lit5,Wnd | Wnd = Left Shift Wb by lit5 | 1 | 1 | N,Z |
| 73 | SUB | SUB | Acc(1) | Subtract Accumulators | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | SUB | f | f = f – WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | f,WREG | WREG = f – WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | #lit10,Wn | Wn = Wn – lit10 | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | Wb,Ws,Wd | Wd = Wb – Ws | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | Wb,#lit5,Wd | Wd = Wb – lit5 | 1 | 1 | C,DC,N,OV,Z |
| 74 | SUBB | SUBB | f | f = f – WREG – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | f,WREG | WREG = f – WREG – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | #lit10,Wn | Wn = Wn – lit10 – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | Wb,Ws,Wd | Wd = Wb – Ws – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | Wb,#lit5,Wd | Wd = Wb – lit5 – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 75 | SUBR | SUBR | f | f = WREG – f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | f,WREG | WREG = WREG – f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | Wb,Ws,Wd | Wd = Ws – Wb | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | Wb,#lit5,Wd | Wd = lit5 – Wb | 1 | 1 | C,DC,N,OV,Z |
| 76 | SUBBR | SUBBR | f | f = WREG – f – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | f,WREG | WREG = WREG – f – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | Wb,Ws,Wd | Wd = Ws – Wb – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | Wb,#lit5,Wd | Wd = lit5 – Wb – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 77 | SWAP | SWAP.b | Wn | Wn = nibble swap Wn | 1 | 1 | None |
| | | SWAP | Wn | Wn = byte swap Wn | 1 | 1 | None |
| 78 | TBLRDH | TBLRDH | Ws,Wd | Read Prog<23:16> to Wd<7:0> | 1 | 5 | None |
| 79 | TBLRDL | TBLRDL | Ws,Wd | Read Prog<15:0> to Wd | 1 | 5 | None |
| 80 | TBLWTH | TBLWTH | Ws,Wd | Write Ws<7:0> to Prog<23:16> | 1 | 2 | None |
| 81 | TBLWTL | TBLWTL | Ws,Wd | Write Ws to Prog<15:0> | 1 | 2 | None |
| 82 | ULNK | ULNK | | Unlink Frame Pointer | 1 | 1 | SFA |
| 83 | XOR | XOR | f | f = f .XOR. WREG | 1 | 1 | N,Z |
| | | XOR | f,WREG | WREG = f .XOR. WREG | 1 | 1 | N,Z |
| | | XOR | #lit10,Wn | Wd = lit10 .XOR. Wd | 1 | 1 | N,Z |
| | | XOR | Wb,Ws,Wd | Wd = Wb .XOR. Ws | 1 | 1 | N,Z |
| | | XOR | Wb,#lit5,Wd | Wd = Wb .XOR. lit5 | 1 | 1 | N,Z |
| 84 | ZE | ZE | Ws,Wnd | Wnd = Zero-Extend Ws | 1 | 1 | C,Z,N |

**Note 1:** This instruction is available in dsPIC33EPXXX(GP/MC/MU)806/810/814 devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

**NOTES:**


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# 31.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C® for Various Device Families
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICkit™ 3 Debug Express
- Device Programmers
  - PICkit™ 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits

## 31.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

## 31.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

## 31.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

## 31.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

## 31.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 31.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility


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## 31.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

## 31.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 31.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 31.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

## 31.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

## 31.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at $V_{DDMIN}$ and $V_{DDMAX}$ for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

## 31.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.


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# 32.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

## Absolute Maximum Ratings

**(See Note 1)**

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to $V_{SS}$(3) ..... -0.3V to ($V_{DD}$ + 0.3V)
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} \geq 3.0V$(3) ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when $V_{DD} < 3.0V$(3) ..... -0.3V to 3.6V
Voltage on D+ OR D- pin with respect to $V_{USB3V3}$ ..... -0.3V to ($V_{USB3V3}$ +0.3V)
Voltage on $V_{BUS}$ with respect to $V_{SS}$ ..... -0.3V to +5.5V
Maximum current out of $V_{SS}$ pin ..... 320 mA
Maximum current into $V_{DD}$ pin(2) ..... 320 mA
Maximum current sourced/sunk by any 4x I/O pin(4) ..... 15 mA
Maximum current sourced/sunk by any 8x I/O pin(4) ..... 25 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports(2) ..... 200 mA

**Note 1:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 32-2).

**3:** See the **“Pin Diagrams”** section for the 5V tolerant pins.

**4:** Characterized but not tested.

## 32.1 DC Characteristics

**TABLE 32-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts) | Temp Range (in °C) | Maximum MIPS |
|---|---|---|---|
| | | | dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 |
| — | 2.95V-3.6V(1) | -40°C to +85°C | 70 |
| — | 2.95V-3.6V(1) | -40°C to +125°C | 60 |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

**TABLE 32-2: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Industrial Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +125 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +85 | °C |
| Extended Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +140 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +125 | °C |
| Power Dissipation:<br>Internal chip power dissipation:<br>PINT = VDD x (IDD – Σ IOH)<br>I/O Pin Power Dissipation:<br>I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL) | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | (TJ – TA)/θJA | | | W |

**TABLE 32-3: THERMAL PACKAGING CHARACTERISTICS**

| Characteristic | Symbol | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Package Thermal Resistance, 64-pin QFN (9x9 mm) | θJA | 28 | — | °C/W | 1 |
| Package Thermal Resistance, 64-pin TQFP (10x10 mm) | θJA | 47 | — | °C/W | 1 |
| Package Thermal Resistance, 100-pin TQFP (12x12 mm) | θJA | 43 | — | °C/W | 1 |
| Package Thermal Resistance, 100-pin TQFP (14x14 mm) | θJA | 43 | — | °C/W | 1 |
| Package Thermal Resistance, 121-pin TFBGA (10x10 mm) | θJA | 40 | — | °C/W | 1 |
| Package Thermal Resistance, 144-pin LQFP (20x20 mm) | θJA | 33 | — | °C/W | 1 |
| Package Thermal Resistance, 144-pin TQFP (16x16 mm) | θJA | 33 | — | °C/W | 1 |

**Note 1:** Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.


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**TABLE 32-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| **Operating Voltage** | | | | | | | |
| DC10 | VDD | **Supply Voltage(3)** | 3.0 | — | 3.6 | V | |
| DC12 | VDR | **RAM Data Retention Voltage(2)** | 1.8 | — | — | V | |
| DC16 | VPOR | **VDD Start Voltage** to Ensure Internal Power-on Reset Signal | — | — | VSS | V | |
| DC17 | SVDD | **VDD Rise Rate** to Ensure Internal Power-on Reset Signal | 1.0 | — | — | V/ms | 0-3.0V in 3 ms |

**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**2:** This is the limit to which VDD may be lowered without losing RAM data.

**3:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

**TABLE 32-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Param.(2)** | **Typ.(3)** | **Max.** | **Units** | **Conditions** | | |
| **Operating Current (IDD)(1)** | | | | | | |
| DC20d | 12 | 18 | mA | -40°C | 3.3V | 10 MIPS |
| DC20a | 12 | 18 | mA | +25°C | | |
| DC20b | 13 | 20 | mA | +85°C | | |
| DC20c | 14 | 21 | mA | +125°C | | |
| DC22d | 23 | 35 | mA | -40°C | 3.3V | 20 MIPS |
| DC22a | 24 | 36 | mA | +25°C | | |
| DC22b | 24 | 36 | mA | +85°C | | |
| DC22c | 25 | 38 | mA | +125°C | | |
| DC24d | 42 | 63 | mA | -40°C | 3.3V | 40 MIPS |
| DC24a | 43 | 65 | mA | +25°C | | |
| DC24b | 44 | 66 | mA | +85°C | | |
| DC24c | 45 | 68 | mA | +125°C | | |
| DC25d | 61 | 92 | mA | -40°C | 3.3V | 60 MIPS |
| DC25a | 62 | 93 | mA | +25°C | | |
| DC25b | 62 | 93 | mA | +85°C | | |
| DC25c | 63 | 95 | mA | +125°C | | |
| DC26d | 69 | 104 | mA | -40°C | 3.3V | 70 MIPS |
| DC26a | 70 | 105 | mA | +25°C | | |
| DC26b | 70 | 105 | mA | +85°C | | |

**Note 1:** IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
- CPU is executing `while(1)` statement
- JTAG is disabled

**2:** These parameters are characterized but not tested in manufacturing.

**3:** Data in "Typ" column is at 3.3V, +25ºC unless otherwise stated.


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**TABLE 32-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Param.(2)** | **Typ.(3)** | **Max.** | **Units** | **Conditions** | | |
| **Idle Current (IIDLE)(1)** | | | | | | |
| DC40d | 6 | 10 | mA | -40°C | 3.3V | 10 MIPS |
| DC40a | 7 | 12 | mA | +25°C | | |
| DC40b | 8 | 13 | mA | +85°C | | |
| DC40c | 9 | 15 | mA | +125°C | | |
| DC42d | 11 | 18 | mA | -40°C | 3.3V | 20 MIPS |
| DC42a | 12 | 20 | mA | +25°C | | |
| DC42b | 13 | 21 | mA | +85°C | | |
| DC42c | 15 | 24 | mA | +125°C | | |
| DC44d | 23 | 37 | mA | -40°C | 3.3V | 40 MIPS |
| DC44a | 24 | 39 | mA | +25°C | | |
| DC44b | 25 | 40 | mA | +85°C | | |
| DC44c | 27 | 44 | mA | +125°C | | |
| DC45d | 34 | 55 | mA | -40°C | 3.3V | 60 MIPS |
| DC45a | 35 | 56 | mA | +25°C | | |
| DC45b | 36 | 58 | mA | +85°C | | |
| DC45c | 38 | 61 | mA | +125°C | | |
| DC46d | 39 | 63 | mA | -40°C | 3.3V | 70 MIPS |
| DC46a | 41 | 66 | mA | +25°C | | |
| DC46b | 42 | 68 | mA | +85°C | | |

**Note 1:** Base IIDLE current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- External Secondary Oscillator (SOSC) is disabled (i.e., SOSCO and SOSCI pins are configured as digital I/O inputs)
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to stand-by while the device is in Idle mode)
- JTAG is disabled

**2:** These parameters are characterized but not tested in manufacturing.

**3:** Data in “Typ” column is at 3.3V, +25ºC unless otherwise stated.

**TABLE 32-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Param.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** | | |
| **Power-Down Current (IPD)(1)** | | | | | | |
| DC60d | 50 | 100 | µA | -40°C | 3.3V | Base Power-Down Current(1,4) |
| DC60a | 60 | 200 | µA | +25°C | | |
| DC60b | 250 | 500 | µA | +85°C | | |
| DC60c | 1600 | 3000 | µA | +125°C | | |
| DC61d | 8 | 10 | µA | -40°C | 3.3V | Watchdog Timer Current: ΔIWDT(3) |
| DC61a | 10 | 15 | µA | +25°C | | |
| DC61b | 12 | 20 | µA | +85°C | | |
| DC61c | 13 | 25 | µA | +125°C | | |

**Note 1:** IPD (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- External Secondary Oscillator (SOSC) is disabled (i.e., SOSCO and SOSCI pins are configured as digital I/O inputs)
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled, all peripheral modules are disabled (PMDx bits are all ones)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to stand-by while the device is in Sleep mode)
- RTCC is disabled
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to stand-by while the device is in Sleep mode)
- JTAG is disabled

**2:** Data in the "Typ" column is at 3.3V, +25ºC unless otherwise stated.

**3:** The Watchdog Timer current is the additional current consumed when the WDT module is enabled. This current should be added to the base IPD current.

**4:** These currents are measured on the device containing the most memory in this family.


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**TABLE 32-8: DC CHARACTERISTICS: DOZE CURRENT ($I_{DOZE}$)(1)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Typ.(2)** | **Max.** | **Doze Ratio** | **Units** | **Conditions** | | |
| DC73a | 57 | 86 | 1:2 | mA | -40°C | 3.3V | 70 MIPS |
| DC73g | 40 | 60 | 1:128 | mA | | | |
| DC70a | 58 | 87 | 1:2 | mA | +25°C | 3.3V | 70 MIPS |
| DC70g | 41 | 62 | 1:128 | mA | | | |
| DC71a | 58 | 87 | 1:2 | mA | +85°C | 3.3V | 70 MIPS |
| DC71g | 42 | 63 | 1:128 | mA | | | |
| DC72a | 53 | 80 | 1:2 | mA | +125°C | 3.3V | 60 MIPS |
| DC72g | 38 | 57 | 1:128 | mA | | | |

**Note 1:** $I_{DOZE}$ is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all $I_{DOZE}$ measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail with Overshoot/Undershoot < 250 mV
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to $V_{SS}$
- $\overline{MCLR}$ = $V_{DD}$, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (defined PMDx bits are set to zero and unimplemented PMDx bits are set to one)
- CPU executing `while(1)` statement
- JTAG is disabled

**2:** Data in the “Typ” column is at 3.3V, +25ºC unless otherwise stated.

**TABLE 32-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage** | | | | | |
| DI10 | | I/O Pins | VSS | — | 0.2 VDD | V | |
| DI11 | | PMP Pins | VSS | — | 0.15 VDD | V | PMPTTL = 1 |
| DI15 | | $\overline{\text{MCLR}}$ | VSS | — | 0.2 VDD | V | |
| DI16 | | I/O Pins with OSC1 or SOSCI | VSS | — | 0.2 VDD | V | |
| DI18 | | I/O Pins with SDAx, SCLx | VSS | — | 0.3 VDD | V | SMBus disabled |
| DI19 | | I/O Pins with SDAx, SCLx | VSS | — | 0.8 | V | SMBus enabled |
| | VIH | **Input High Voltage** | | | | | |
| DI20 | | I/O Pins Not 5V Tolerant(4) | 0.7 VDD | — | VDD | V | |
| | | I/O Pins 5V Tolerant(4) | 0.7 VDD | — | 5.3 | V | |
| | | PMP Pins | 0.25 VDD + 0.8 | — | — | V | PMPTTL = 1 |
| | | I/O Pins with SDAx, SCLx | 0.7 VDD | — | 5.3 | V | SMBus disabled |
| | | I/O Pins with SDAx, SCLx | 2.1 | — | 5.3 | V | SMBus enabled |
| | ICNPU | **Change Notification Pull-up Current** | | | | | |
| DI30 | | | 50 | 250 | 400 | µA | VDD = 3.3V, VPIN = VSS |
| | ICNPD | **Change Notification Pull-down Current(10)** | | | | | |
| DI31 | | | — | 50 | — | µA | VDD = 3.3V, VPIN = VDD |

**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

**4:** See **"Pin Diagrams"** for the 5V tolerant I/O pins.

**5:** VIL source < (VSS – 0.3). Characterized but not tested.

**6:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

**7:** Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

**8:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted, provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

**10:** These parameters are characterized, but not tested.


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**TABLE 32-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| | IIL | **Input Leakage Current(2,3)** | | | | | |
| DI50 | | I/O Pins 5V Tolerant(4) | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance |
| DI51 | | I/O Pins Not 5V Tolerant(4) | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance, -40°C ≤ TA ≤ +85°C |
| DI51a | | I/O Pins Not 5V Tolerant(4) | — | — | ±1 | μA | Analog pins shared with external reference pins, -40°C ≤ TA ≤ +85°C |
| DI51b | | I/O Pins Not 5V Tolerant(4) | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance, -40°C ≤ TA ≤ +125°C |
| DI51c | | I/O Pins Not 5V Tolerant(4) | — | — | ±1 | μA | Analog pins shared with external reference pins, -40°C ≤ TA ≤ +125°C |
| DI55 | | $\overline{\text{MCLR}}$ | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD |
| DI56 | | OSC1 | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD, XT and HS modes |

**Note 1:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

**4:** See **“Pin Diagrams”** for the 5V tolerant I/O pins.

**5:** VIL source < (VSS – 0.3). Characterized but not tested.

**6:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

**7:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.

**8:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted, provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

**10:** These parameters are characterized, but not tested.

**TABLE 32-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| DI60a | IICL | **Input Low Injection Current** | 0 | — | -5(5,8) | mA | All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB11, SOSCI, SOSCO, D+, D-, VUSB3V3 and VBUS |
| DI60b | IICH | **Input High Injection Current** | 0 | — | +5(6,7,4) | mA | All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB11, SOSCI, SOSCO, D+, D-, VUSB3V3 and VBUS, and all 5V tolerant pins(7) |
| DI60c | ∑IICT | **Total Input Injection Current (sum of all I/O and control pins)** | -20(9) | — | +20(9) | mA | Absolute instantaneous sum of all ± input injection currents from all I/O pins<br>( \| IICL + \| IICH \| ) ≤ ∑IICT |

**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

**4:** See **"Pin Diagrams"** for the 5V tolerant I/O pins.

**5:** VIL source < (VSS – 0.3). Characterized but not tested.

**6:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

**7:** Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

**8:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted, provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

**10:** These parameters are characterized, but not tested.


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**TABLE 32-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| DO10 | VOL | **Output Low Voltage**<br>I/O Pins:<br>4x Sink Driver Pins – All I/O Pins except OSC2 and SOSCO | — | — | 0.4 | V | IOL ≤ 10 mA, VDD = 3.3V |
| | | **Output Low Voltage**<br>I/O Pins:<br>8x Sink Driver Pins – OSC2 and SOSCO | — | — | 0.4 | V | IOL ≤ 15 mA, VDD = 3.3V |
| DO20 | VOH | **Output High Voltage**<br>I/O Pins:<br>4x Sink Driver Pins – All I/O Pins except OSC2 and SOSCO | 2.4 | — | — | V | IOH ≥ -10 mA, VDD = 3.3V |
| | | **Output High Voltage**<br>I/O Pins:<br>8x Sink Driver Pins – OSC2 and SOSCO | 2.4 | — | — | V | IOH ≥ -15 mA, VDD = 3.3V |
| DO20A | VOH1 | **Output High Voltage**<br>I/O Pins:<br>4x Sink Driver Pins – All I/O Pins except OSC2 and SOSCO | 1.5(1) | — | — | V | IOH ≥ -14 mA, VDD = 3.3V |
| | | | 2.0(1) | — | — | | IOH ≥ -12 mA, VDD = 3.3V |
| | | | 3.0(1) | — | — | | IOH ≥ -7 mA, VDD = 3.3V |
| | | **Output High Voltage**<br>I/O Pins:<br>8x Sink Driver Pins – OSC2 and SOSCO | 1.5(1) | — | — | V | IOH ≥ -22 mA, VDD = 3.3V |
| | | | 2.0(1) | — | — | | IOH ≥ -18 mA, VDD = 3.3V |
| | | | 3.0(1) | — | — | | IOH ≥ -10 mA, VDD = 3.3V |

**Note 1:** Parameters are characterized, but not tested.

**TABLE 32-11: ELECTRICAL CHARACTERISTICS: BOR**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V(2) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.(1)** | **Typ.** | **Max.** | **Units** | **Conditions** |
| BO10 | VBOR | BOR Event on VDD Transition High-to-Low | 2.7 | — | 2.9 | V | VDD |

**Note 1:** Parameters are for design guidance only and are not tested in manufacturing.

**2:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized.

**TABLE 32-12: DC CHARACTERISTICS: PROGRAM MEMORY**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| | | **Program Flash Memory** | | | | | |
| D130 | EP | Cell Endurance | 10,000 | — | — | E/W | -40°C to +125°C |
| D131 | VPR | VDD for Read | 3.0 | — | 3.6 | V | |
| D132b | VPEW | VDD for Self-Timed Write | 3.0 | — | 3.6 | V | |
| D134 | TRETD | Characteristic Retention | 20 | — | — | Year | Provided no other specifications are violated, -40°C to +125°C |
| D135 | IDDP | Supply Current during Programming | — | 10 | — | mA | |
| D136a | TRW | Row Write Time | 1.32 | — | 1.74 | ms | TRW = 11064 FRC cycles, TA = +85°C, See **Note 2** |
| D136b | TRW | Row Write Time | 1.28 | — | 1.79 | ms | TRW = 11064 FRC cycles, TA = +125°C, See **Note 2** |
| D137a | TPE | Page Erase Time | 20.1 | — | 26.5 | ms | TPE = 168517 FRC cycles, TA = +85°C, See **Note 2** |
| D137b | TPE | Page Erase Time | 19.5 | — | 27.3 | ms | TPE = 168517 FRC cycles, TA = +125°C, See **Note 2** |
| D138a | TWW | Word Write Cycle Time | 42.3 | — | 55.9 | µs | TWW = 355 FRC cycles, TA = +85°C, See **Note 2** |
| D138b | TWW | Word Write Cycle Time | 41.1 | — | 57.6 | µs | TWW = 355 FRC cycles, TA = +125°C, See **Note 2** |

**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**2:** Other conditions: FRC = 7.37 MHz, TUN<5:0> = `'b011111` (for Minimum), TUN<5:0> = `'b100000` (for Maximum). This parameter depends on the FRC accuracy (see Table 32-20) and the value of the FRC Oscillator Tuning register (see Register 9-4). For complete details on calculating the Minimum and Maximum time, see **Section 5.3 "Programming Operations"**.

**TABLE 32-13: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS**

| Standard Operating Conditions (unless otherwise stated):<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristics** | **Min.** | **Typ** | **Max.** | **Units** | **Comments** |
| — | CEFC(1) | External Filter Capacitor Value | 4.7 | 10 | — | µF | Capacitor must have a low series resistance (< 1 Ohm) |

**Note 1:** Typical VCAP (CEFC) voltage = 1.8V when VDD ≥ VDDMIN.


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## 32.2 AC Characteristics and Timing Parameters

This section defines the dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 AC characteristics and timing parameters.

**TABLE 32-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC**

| | |
|---|---|
| **AC CHARACTERISTICS** | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended<br>Operating voltage VDD range as described in **Section 32.1 "DC Characteristics"**. |

**FIGURE 32-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

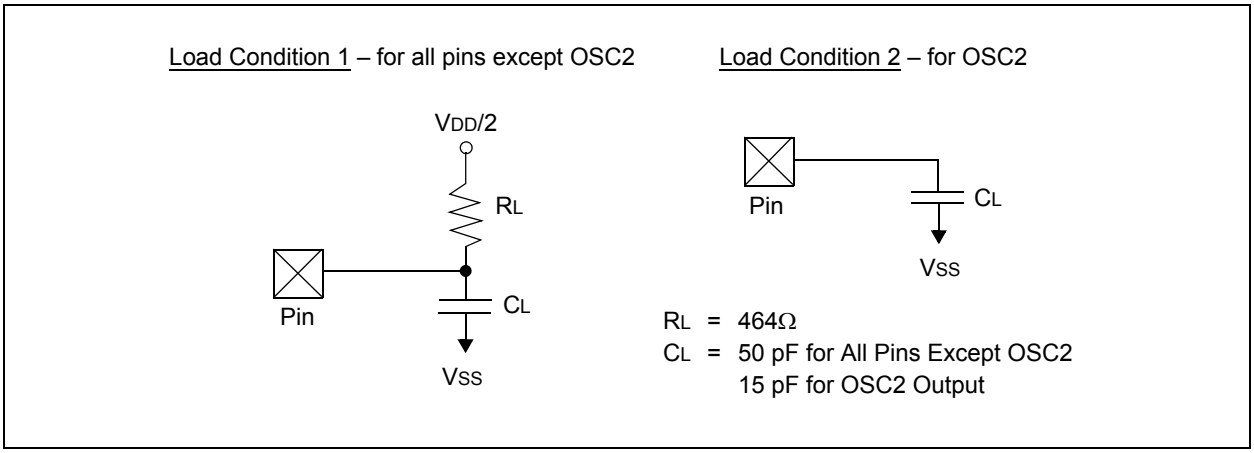


**TABLE 32-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS**

| Param. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| DO50 | COSCO | OSC2 Pin | — | — | 15 | pF | In XT and HS modes when external clock is used to drive OSC1 |
| DO56 | CIO | All I/O Pins and OSC2 | — | — | 50 | pF | EC mode |
| DO58 | CB | SCLx, SDAx | — | — | 400 | pF | In $I^2C$™ mode |

**FIGURE 32-2: EXTERNAL CLOCK TIMING**

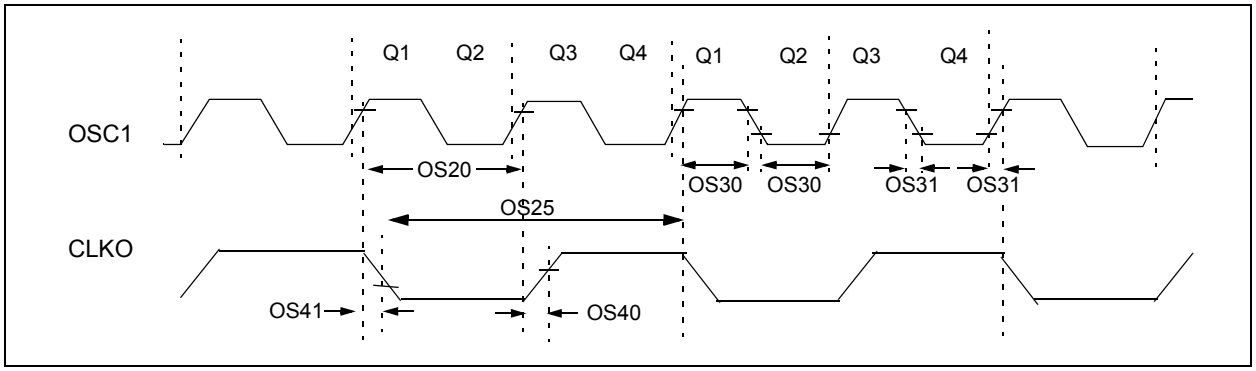


**TABLE 32-16: EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| OS10 | FIN | External CLKI Frequency (External clocks allowed only in EC and ECPLL modes) | DC | — | 60 | MHz | EC |
| | | Oscillator Crystal Frequency | 3.5<br>10<br>32.4 | —<br>—<br>32.768 | 10<br>40<br>33.1 | MHz<br>MHz<br>kHz | XT<br>HS<br>SOSC |
| OS20 | TOSC | TOSC = 1/FOSC | 8.33<br>7.14 | —<br>— | DC<br>DC | ns<br>ns | +125ºC<br>+85ºC |
| OS25 | TCY | Instruction Cycle Time(2) | 16.67<br>14.28 | —<br>— | DC<br>DC | ns<br>ns | +125ºC<br>+85ºC |
| OS30 | TosL, TosH | External Clock In (OSC1) High or Low Time | 0.375 x TOSC | — | 0.625 x TOSC | ns | EC |
| OS31 | TosR, TosF | External Clock In (OSC1) Rise or Fall Time | — | — | 20 | ns | EC |
| OS40 | TckR | CLKO Rise Time(3) | — | 5.2 | — | ns | |
| OS41 | TckF | CLKO Fall Time(3) | — | 5.2 | — | ns | |
| OS42 | GM | External Oscillator Transconductance(4) | — | 12 | — | mA/V | HS, VDD = 3.3V, TA = +25ºC |
| | | | — | 6 | — | mA/V | XT, VDD = 3.3V, TA = +25ºC |

**Note 1:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**2:** Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Minimum” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “Maximum” cycle time limit is “DC” (no clock) for all devices.

**3:** Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

**4:** This parameter is characterized, but not tested in manufacturing.


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**TABLE 32-17: PLL CLOCK TIMING SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| OS50 | FPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range | 0.8 | — | 8.0 | MHz | ECPLL, XTPLL modes |
| OS51 | FSYS | On-Chip VCO System Frequency | 120 | — | 340 | MHz | |
| OS52 | TLOCK | PLL Start-up Time (Lock Time) | 0.9 | 1.5 | 3.1 | mS | |
| OS53 | DCLK | CLKO Stability (Jitter)(2) | -5 | 0.5 | 5 | % | |

**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases or communication clocks used by the application, use the following formula:

$$\text{Effective Jitter} = \frac{DCLK}{\sqrt{\frac{FOSC}{\text{Time Base or Communication Clock}}}}$$

For example, if FOSC = 120 MHz and the SPI bit rate = 10 MHz, the effective jitter is as follows:

$$\text{Effective Jitter} = \frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

**TABLE 32-18: AUXILIARY PLL CLOCK TIMING SPECIFICATIONS (dsPIC33EPXXXMU8XX AND PIC24EPXXXGU8XX DEVICES ONLY)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| OS54 | AFPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range | 3 | — | 5.5 | MHz | ECPLL, XTPLL modes |
| OS55 | AFSYS | On-Chip VCO System Frequency | 60 | — | 120 | MHz | |
| OS56 | ATLOCK | PLL Start-up Time (Lock Time) | 0.9 | 1.5 | 3.1 | mS | |
| OS57 | ADCLK | CLKO Stability (Jitter) | -2 | 0.25 | 2 | % | |

**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**TABLE 32-19: INTERNAL FRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| | **Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1)** | | | | | | |
| F20a | FRC | -2 | — | +2 | % | -40°C ≤ TA ≤ +85°C | VDD = 3.0-3.6V |
| F20b | FRC | -5 | — | +5 | % | -40°C ≤ TA ≤ +125°C | VDD = 3.0-3.6V |

**Note 1:** Frequency calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

**TABLE 32-20: INTERNAL LPRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| | **LPRC @ 32.768 kHz(1)** | | | | | | |
| F21a | LPRC | -20 | ±6 | +20 | % | -40°C ≤ TA ≤ +85°C | VDD = 3.0-3.6V |
| F21b | LPRC | -50 | — | +50 | % | -40°C ≤ TA ≤ +125°C | VDD = 3.0-3.6V |

**Note 1:** Change of LPRC frequency as VDD changes.


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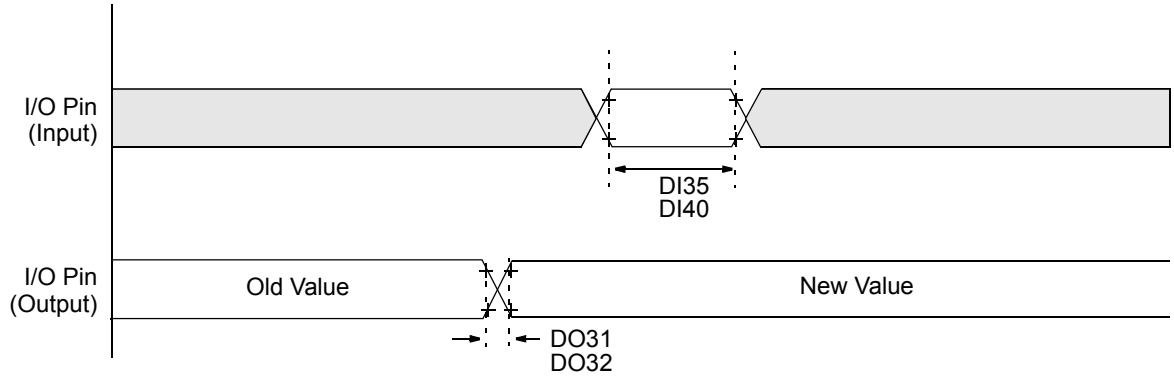
**FIGURE 32-3: I/O TIMING CHARACTERISTICS**



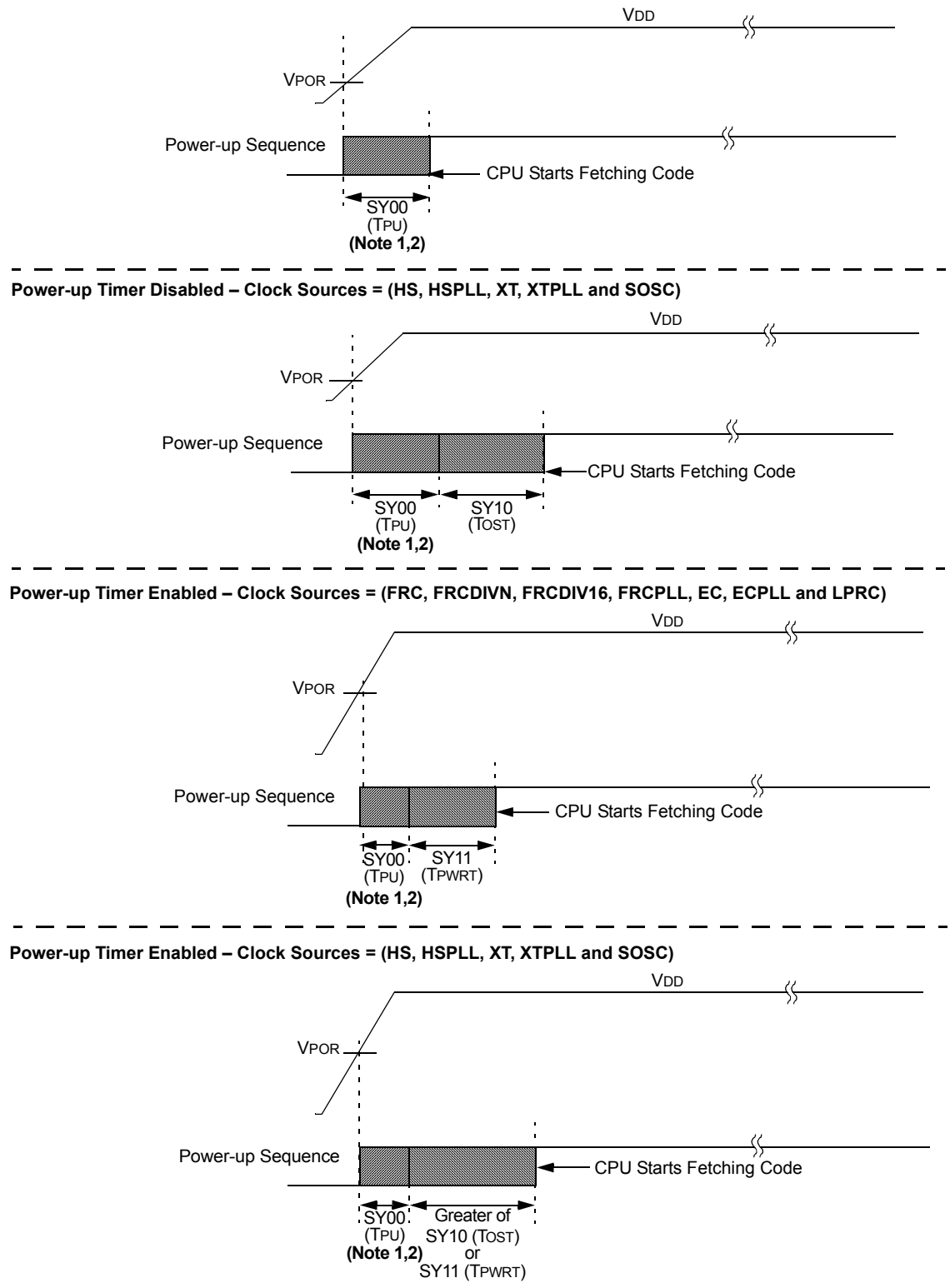

**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-21: I/O TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| DO31 | TIOR | Port Output Rise Time | — | 5 | 10 | ns | |
| DO32 | TIOF | Port Output Fall Time | — | 5 | 10 | ns | |
| DI35 | TINP | INTx Pin High or Low Time (input) | 20 | — | — | ns | |
| DI40 | TRBP | CNx High or Low Time (input) | 2 | — | — | TCY | |

**Note 1:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**FIGURE 32-4: POWER-ON RESET TIMING CHARACTERISTICS**




**Note 1:** The power-up period will be extended if the power-up sequence completes before the device exits from BOR ($V_{DD} < V_{BOR}$).

**2:** The power-up period includes internal voltage regulator stabilization delay.


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**FIGURE 32-5: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS**

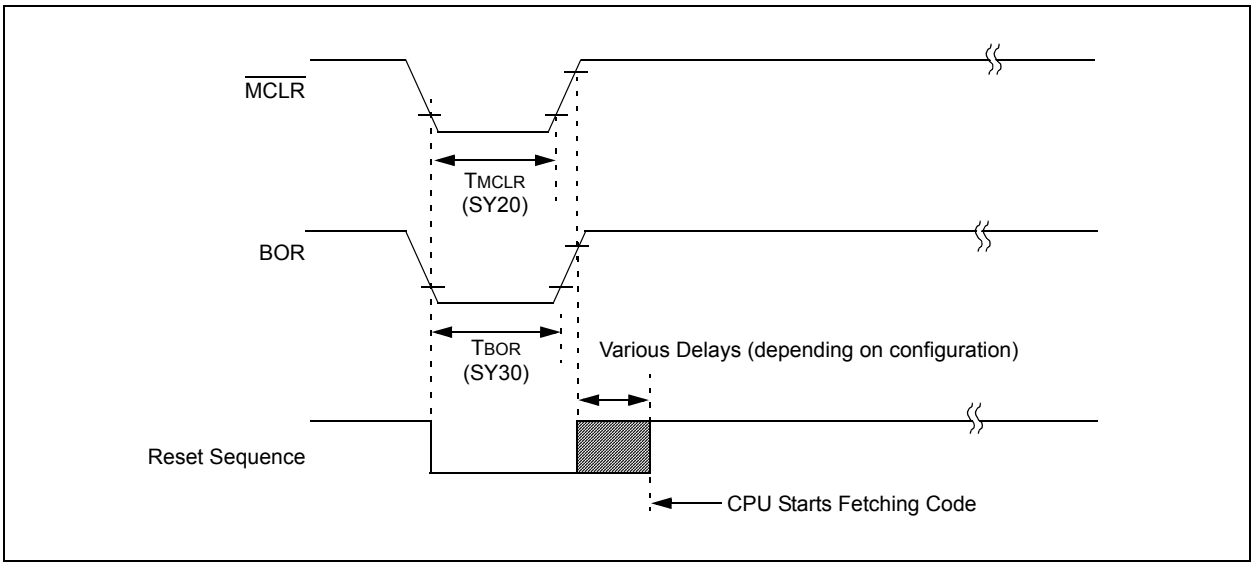
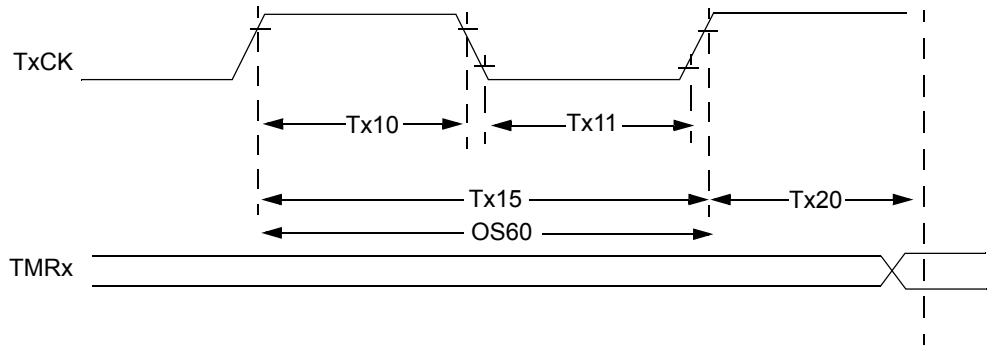



**TABLE 32-22: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SY00 | TPU | Power-up Period | — | 400 | 600 | µs | |
| SY10 | TOST | Oscillator Start-up Time | — | 1024 TOSC | — | — | TOSC = OSC1 period |
| SY11 | TPWRT | Power-up Timer Period | — | — | — | — | See **Section 29.1 "Configuration Bits"** and LPRC Parameters F21a and F21b (Table 32-20) |
| SY12 | TWDT | Watchdog Timer Time-out Period | — | — | — | — | See **Section 29.4 "Watchdog Timer (WDT)"** and LPRC Parameters F21a and F21b (Table 32-20) |
| SY13 | TIOZ | I/O High-Impedance from MCLR Low or Watchdog Timer Reset | 0.68 | 0.72 | 1.2 | µs | |
| SY20 | TMCLR | MCLR Pulse Width (low) | 2 | — | — | µs | |
| SY30 | TBOR | BOR Pulse Width (low) | 1 | — | — | µs | |
| SY35 | TFSCM | Fail-Safe Clock Monitor Delay | — | 500 | 900 | µs | -40°C to +85°C |
| SY36 | TVREG | Voltage Regulator Standby-to-Active Mode Transition Time | — | — | 30 | µs | |
| SY37 | TOSCDFRC | FRC Oscillator Start-up Delay | — | — | 29 | µs | |
| SY38 | TOSCDLPRC | LPRC Oscillator Start-up Delay | — | — | 70 | µs | |

**Note 1:** These parameters are characterized but not tested in manufacturing.
**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**FIGURE 32-6: TIMER1-TIMER9 EXTERNAL CLOCK TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(2)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TA10 | TTXH | TxCK High Time | Synchronous mode | Greater of: 20 or (TCY + 20)/N | — | — | ns | Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256) |
| | | | Asynchronous | 35 | — | — | ns | |
| TA11 | TTXL | TxCK Low Time | Synchronous mode | Greater of: 20 or (TCY + 20)/N | — | — | ns | Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256) |
| | | | Asynchronous | 10 | — | — | ns | |
| TA15 | TTXP | TxCK Input Period | Synchronous mode | Greater of: 40 or (2 TCY + 40)/N | — | — | ns | N = prescale value (1, 8, 64, 256) |
| OS60 | Ft1 | SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>)) | | DC | — | 50 | kHz | |
| TA20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | 0.75 TCY + 40 | — | 1.75 TCY + 40 | ns | |

**Note 1:** Timer1 is a Type A.

**2:** These parameters are characterized, but are not tested in manufacturing.


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**TABLE 32-24: TIMER2, TIMER4, TIMER6, TIMER8 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TB10 | TtxH | TxCK High Time | Synchronous mode | Greater of: 20 or (TCY + 20)/N | — | — | ns | Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256) |
| TB11 | TtxL | TxCK Low Time | Synchronous mode | Greater of: 20 or (TCY + 20)/N | — | — | ns | Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256) |
| TB15 | TtxP | TxCK Input Period | Synchronous mode | Greater of: 40 or (2 TCY + 40)/N | — | — | ns | N = prescale value (1, 8, 64, 256) |
| TB20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | 0.75 TCY + 40 | — | 1.75 TCY + 40 | ns | |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**TABLE 32-25: TIMER3, TIMER5, TIMER7, TIMER9 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TC10 | TtxH | TxCK High Time | Synchronous | TCY + 20 | — | — | ns | Must also meet Parameter TC15 |
| TC11 | TtxL | TxCK Low Time | Synchronous | TCY + 20 | — | — | ns | Must also meet Parameter TC15 |
| TC15 | TtxP | TxCK Input Period | Synchronous, with Prescaler | 2 TCY + 40 | — | — | ns | N = prescale value (1, 8, 64, 256) |
| TC20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | 0.75 TCY + 40 | — | 1.75 TCY + 40 | ns | |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**FIGURE 32-7: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS**

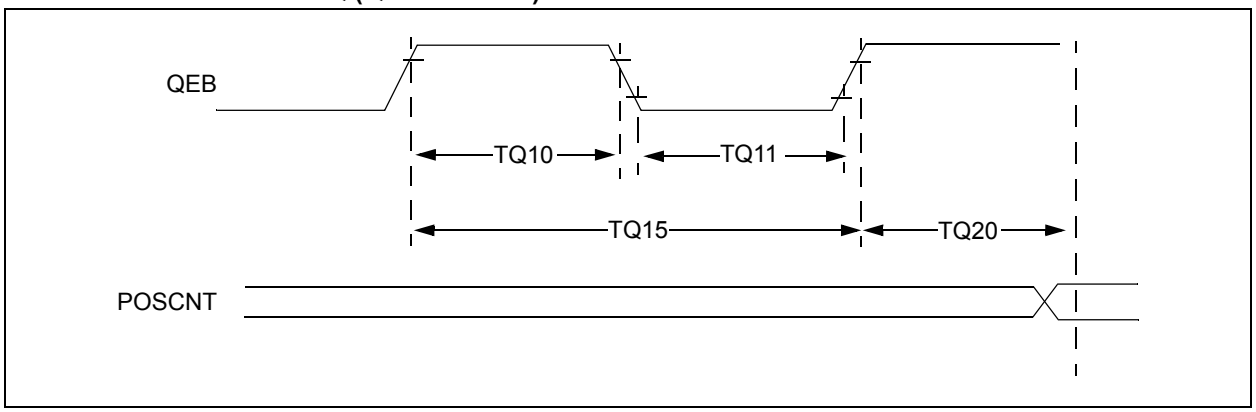


**TABLE 32-26: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TQ10 | TtQH | TQCK High Time | Synchronous, with Prescaler | [Greater of (12.5 or 0.5 TCY)/N] + 25 | — | — | ns | Must also meet Parameter TQ15 |
| TQ11 | TtQL | TQCK Low Time | Synchronous, with Prescaler | [Greater of (12.5 or 0.5 TCY)/N] + 25 | — | — | ns | Must also meet Parameter TQ15 |
| TQ15 | TtQP | TQCP Input Period | Synchronous, with Prescaler | [Greater of ( 25 or TCY)/N] + 50 | — | — | ns | |
| TQ20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | — | 1 | TCY | — | |

**Note 1:** These parameters are characterized but not tested in manufacturing.


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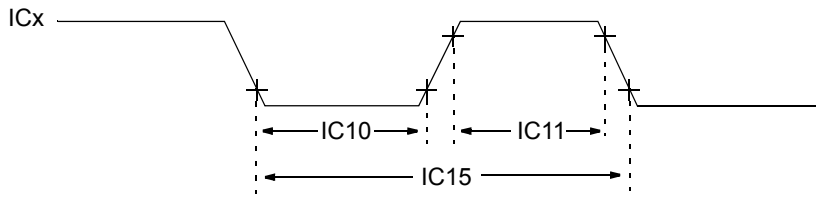
**FIGURE 32-8: INPUT CAPTURE (ICx) TIMING CHARACTERISTICS**



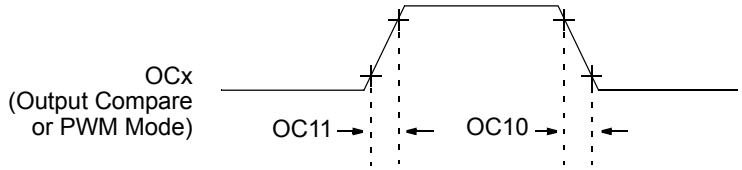

**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-27: INPUT CAPTURE MODULE (ICx) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristics(1)** | **Min.** | **Max.** | **Units** | **Conditions** | |
| IC10 | TccL | ICx Input Low Time | [Greater of (12.5 or 0.5 TCY)/N] + 25 | — | ns | Must also meet Parameter IC15 | N = prescale value (1, 4, 16) |
| IC11 | TccH | ICx Input High Time | [Greater of (12.5 or 0.5 TCY)/N] + 25 | — | ns | Must also meet Parameter IC15 | |
| IC15 | TccP | ICx Input Period | [Greater of (25 or 1 TCY)/N] + 50 | — | ns | | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 32-9: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-28: OUTPUT COMPARE MODULE (OCx) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| OC10 | TccF | OCx Output Fall Time | — | — | — | ns | See Parameter DO32 |
| OC11 | TccR | OCx Output Rise Time | — | — | — | ns | See Parameter DO31 |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**FIGURE 32-10: OCx/PWMx MODULE TIMING CHARACTERISTICS**

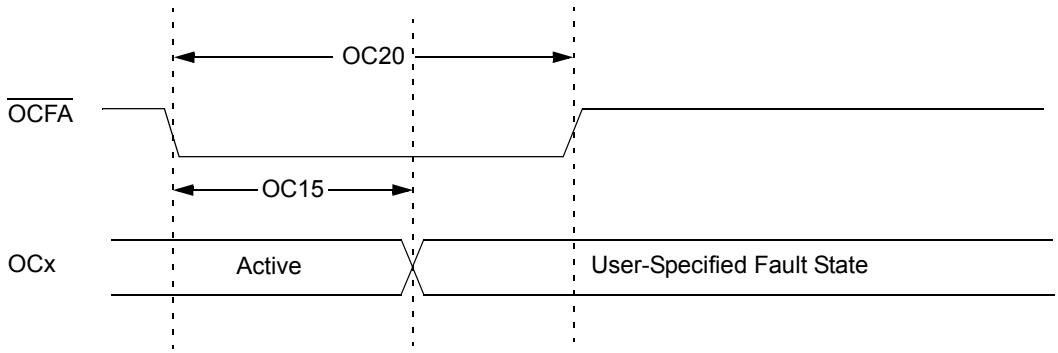



**TABLE 32-29: OCx/PWMx MODE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| OC15 | TFD | Fault Input to PWM I/O Change | — | — | TCY + 20 | ns | |
| OC20 | TFLT | Fault Input Pulse Width | TCY + 20 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.


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**FIGURE 32-11: HIGH-SPEED PWMx MODULE FAULT TIMING CHARACTERISTICS (dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY)**

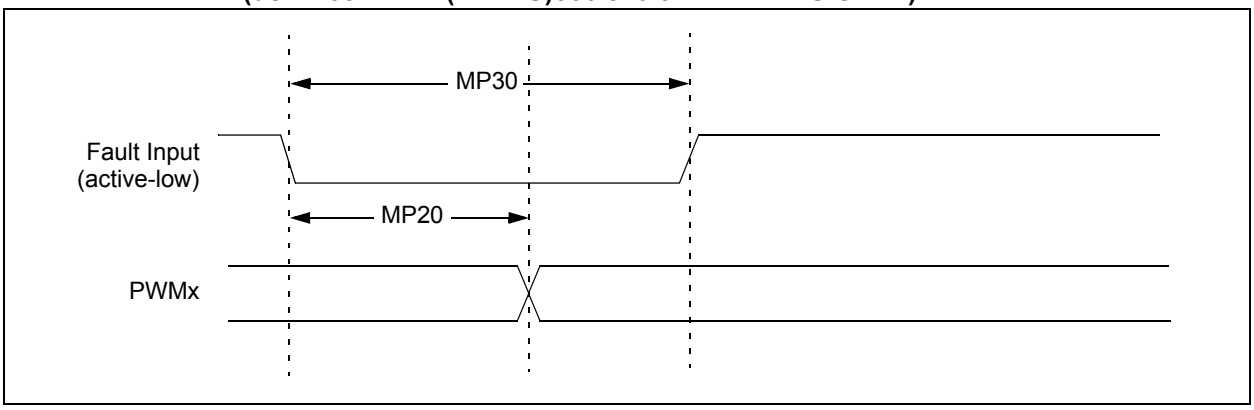
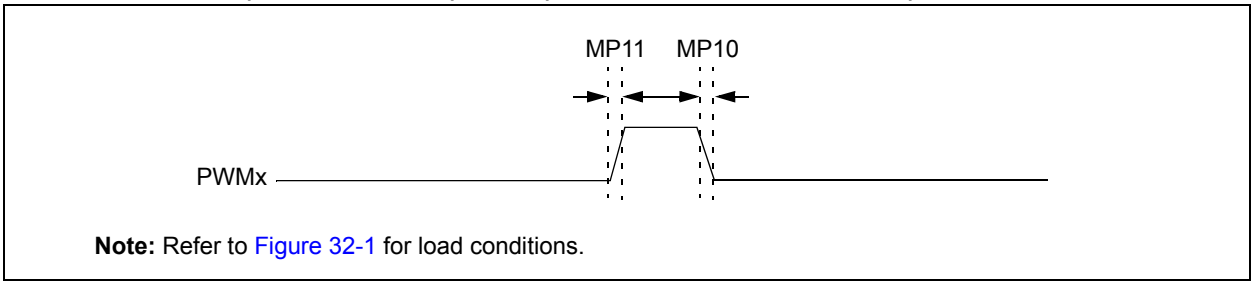



**FIGURE 32-12: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS (dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY)**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-30: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS (dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| MP10 | TFPWM | PWM Output Fall Time | — | — | — | ns | See Parameter DO32 |
| MP11 | TRPWM | PWM Output Rise Time | — | — | — | ns | See Parameter DO31 |
| MP20 | TFD | Fault Input ↓ to PWM I/O Change | — | — | 15 | ns | |
| MP30 | TFH | Fault Input Pulse Width | 15 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**FIGURE 32-13: QEA/QEB INPUT CHARACTERISTICS (dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY)**

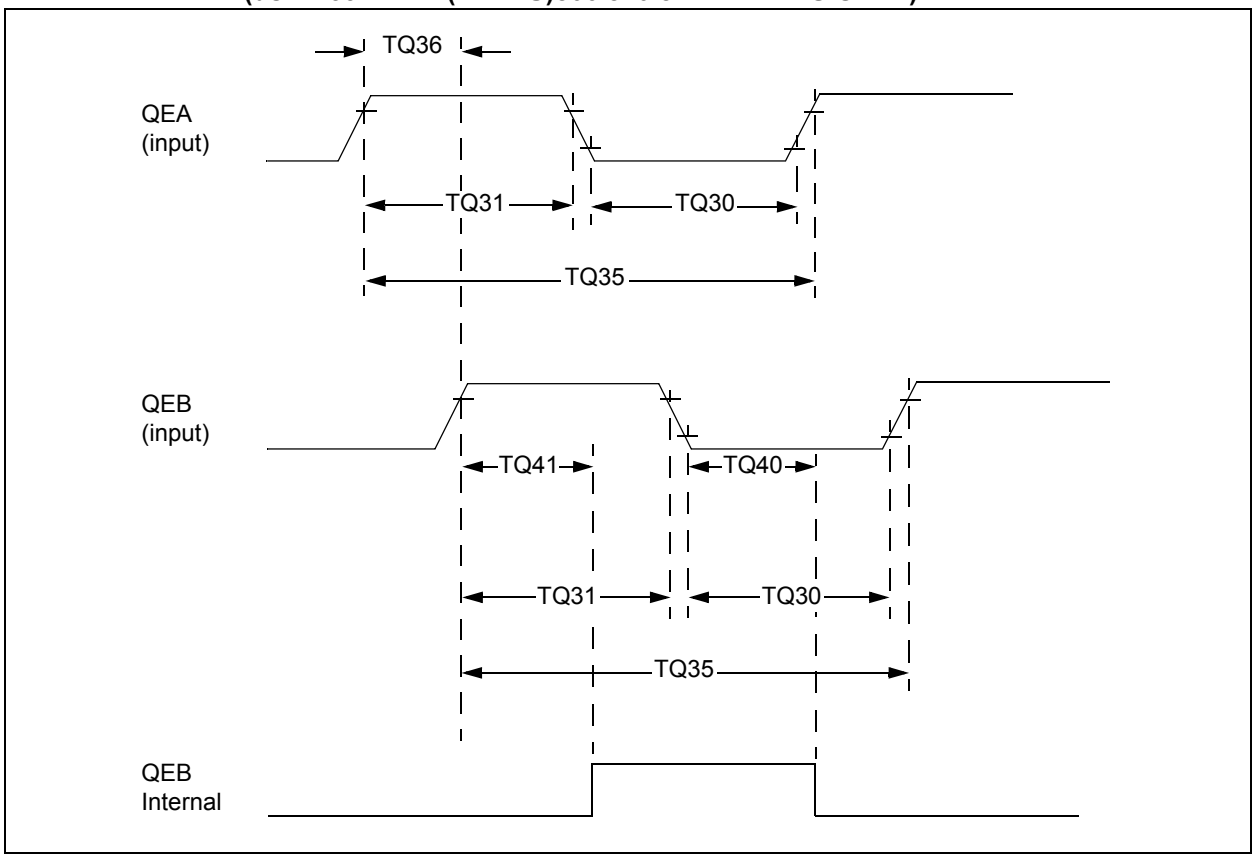



**TABLE 32-31: QUADRATURE DECODER TIMING REQUIREMENTS (dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| TQ30 | TQUL | Quadrature Input Low Time | 6 TCY | — | ns | |
| TQ31 | TQUH | Quadrature Input High Time | 6 TCY | — | ns | |
| TQ35 | TQUIN | Quadrature Input Period | 12 TCY | — | ns | |
| TQ36 | TQUP | Quadrature Phase Period | 3 TCY | — | ns | |
| TQ40 | TQUFL | Filter Time to Recognize Low with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)** |
| TQ41 | TQUFH | Filter Time to Recognize High with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)** |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** N = Index Channel Digital Filter Clock Divide Select bits. Refer to **Section 15. "Quadrature Encoder Interface (QEI)"** (DS70601) in the "*dsPIC33E/PIC24E Family Reference Manual*". Please see the Microchip web site for the latest family reference manual sections.


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**FIGURE 32-14: QEI MODULE INDEX PULSE TIMING CHARACTERISTICS (dsPIC33EPXXX(MC/MU)806/810/814 DEVICES ONLY)**

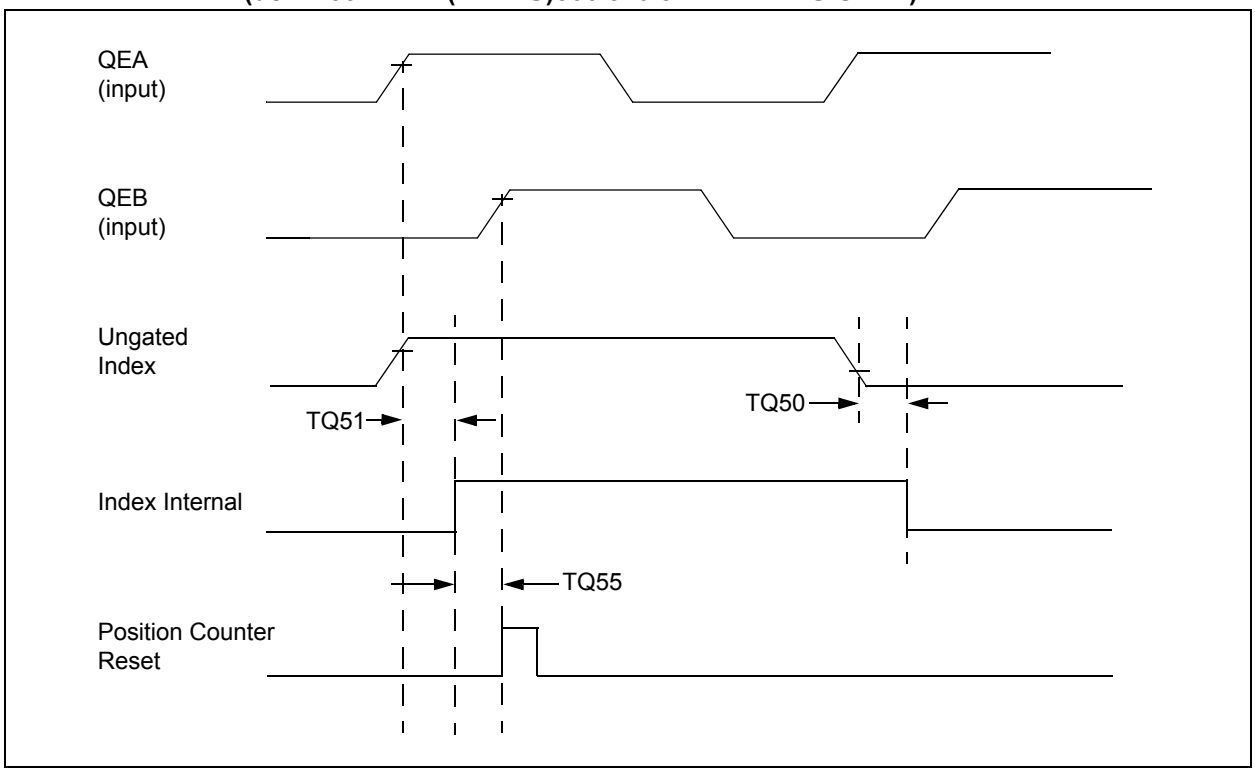



**TABLE 32-32: QEI INDEX PULSE TIMING REQUIREMENTS (dsPIC33EPXXX(MC/MU)MU806/810/814 DEVICES ONLY)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Max.** | **Units** | **Conditions** |
| TQ50 | TqIL | Filter Time to Recognize Low with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)** |
| TQ51 | TqiH | Filter Time to Recognize High with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)** |
| TQ55 | Tqidxr | Index Pulse Recognized to Position Counter Reset (ungated index) | 3 TCY | — | ns | |

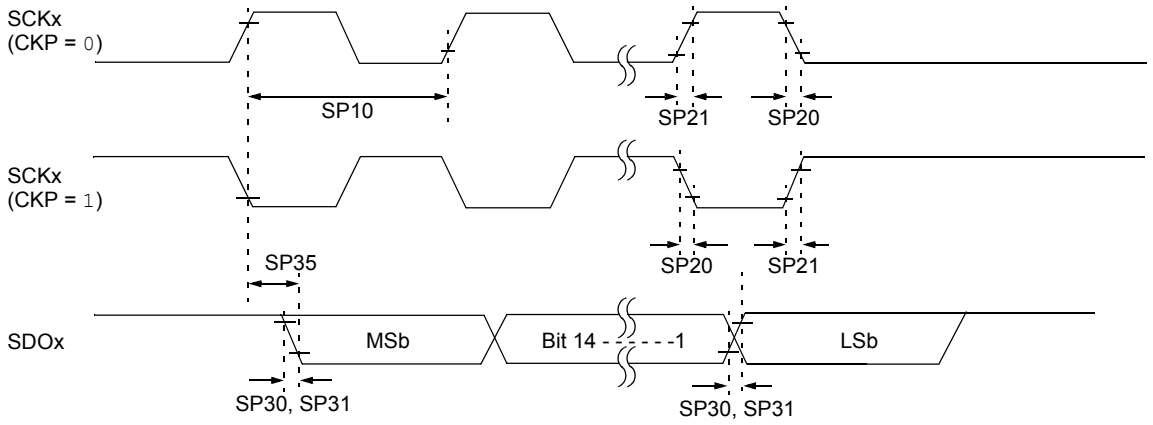
**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Alignment of index pulses to QEA and QEB is shown for position counter Reset timing only. Shown for forward direction only (QEA leads QEB). Same timing applies for reverse direction (QEA lags QEB) but index pulse recognition occurs on the falling edge.

**TABLE 32-33: SPI1, SPI3 AND SPI4 MAXIMUM DATA/CLOCK RATE SUMMARY**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Maximum Data Rate** | **Master Transmit Only (Half-Duplex)** | **Master Transmit/Receive (Full-Duplex)** | **Slave Transmit/Receive (Full-Duplex)** | **CKE** | **CKP** | **SMP** |
| 15 MHz | Table 32-33 | — | — | 0,1 | 0,1 | 0,1 |
| 9 MHz | — | Table 32-34 | — | 1 | 0,1 | 1 |
| 9 MHz | — | Table 32-35 | — | 0 | 0,1 | 1 |
| 15 MHz | — | — | Table 32-36 | 1 | 0 | 0 |
| 11 MHz | — | — | Table 32-37 | 1 | 1 | 0 |
| 15 MHz | — | — | Table 32-38 | 0 | 1 | 0 |
| 11 MHz | — | — | Table 32-39 | 0 | 0 | 0 |

**FIGURE 32-15: SPI1, SPI3 AND SPI4 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.


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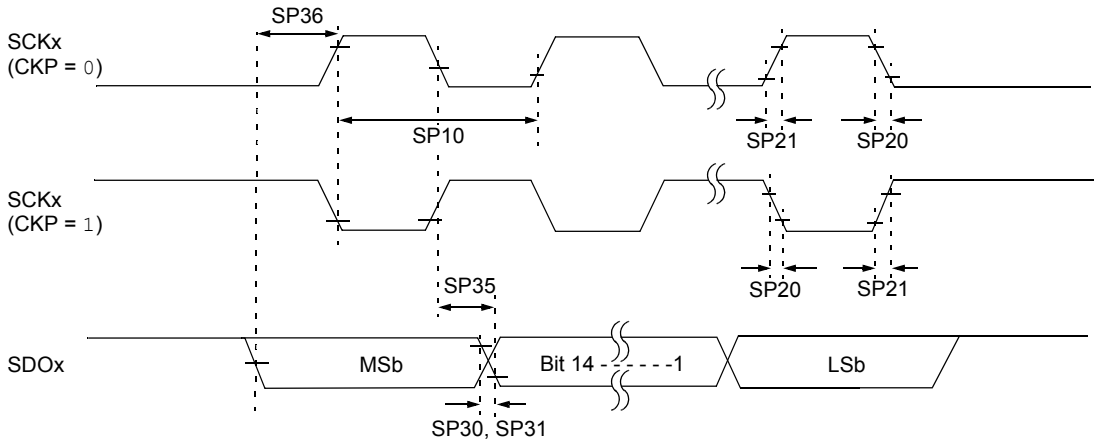
**FIGURE 32-16: SPI1, SPI3 AND SPI4 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-34: SPI1, SPI3 AND SPI4 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscP | Maximum SCKx Frequency | — | — | 15 | MHz | See **Note 3** |
| SP20 | TscF | SCKx Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP21 | TscR | SCKx Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdiV2scH, TdiV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |

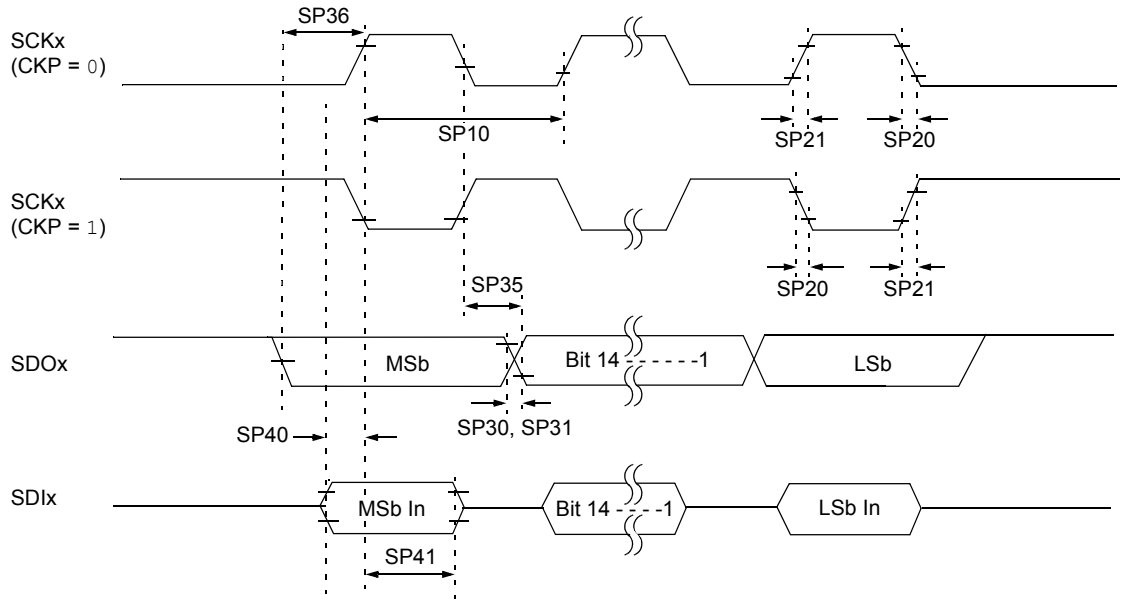
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-17: SPI1, SPI3 AND SPI4 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-35: SPI1, SPI3 AND SPI4 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscP | Maximum SCKx Frequency | — | — | 9 | MHz | See **Note 3** |
| SP20 | TscF | SCKx Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP21 | TscR | SCKx Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid After SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2sc, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.


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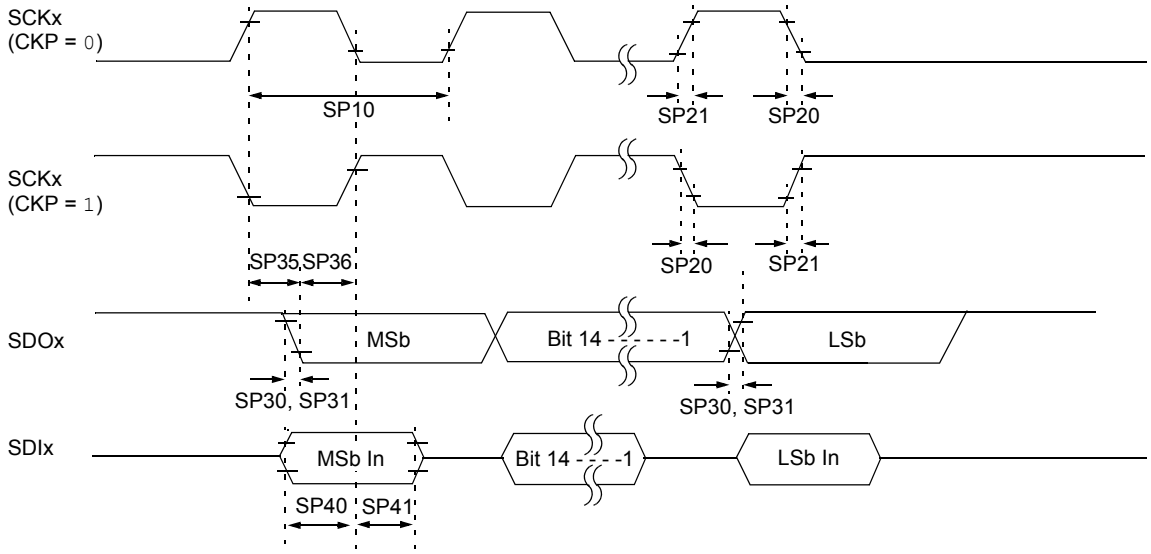
**FIGURE 32-18: SPI1, SPI3 AND SPI4 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-36: SPI1, SPI3 AND SPI4 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscP | Maximum SCKx Frequency | — | — | 9 | MHz | -40ºC to +125ºC and see **Note 3** |
| SP20 | TscF | SCKx Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP21 | TscR | SCKx Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid After SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |

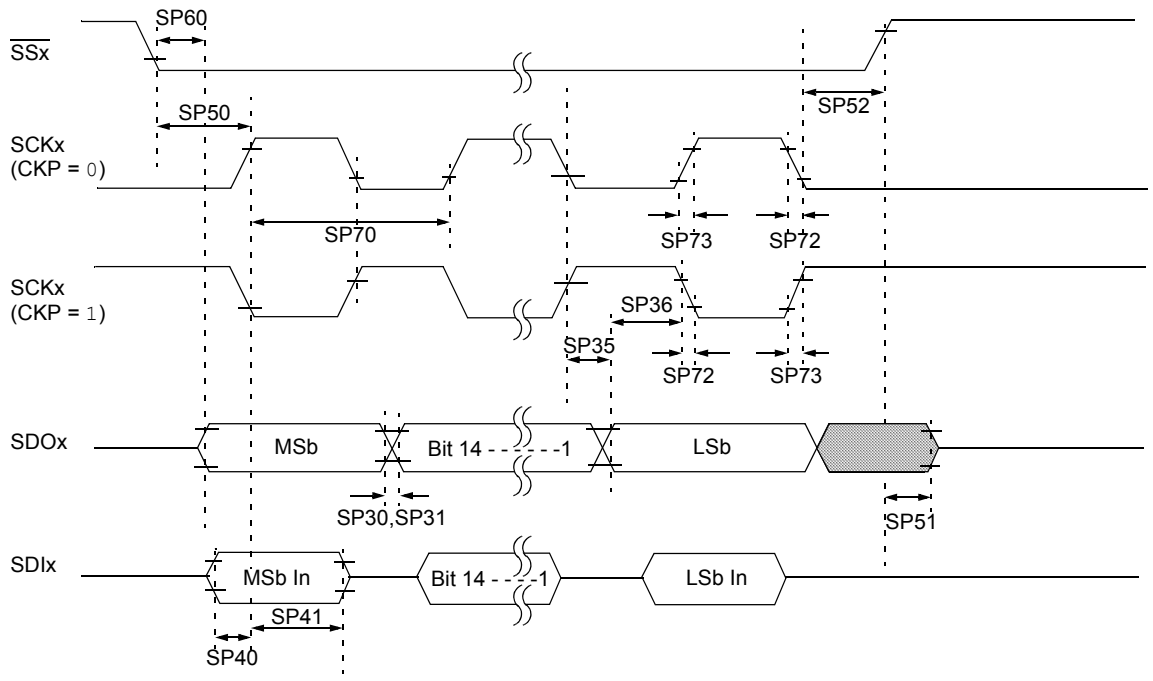
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 111 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-19: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.


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**TABLE 32-37: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscP | Maximum SCKx Input Frequency | — | — | 15 | MHz | See **Note 3** |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output, High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SSx}$ ↑ after SCKx Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |
| SP60 | TssL2doV | SDOx Data Output Valid after $\overline{SSx}$ Edge | — | — | 50 | ns | |

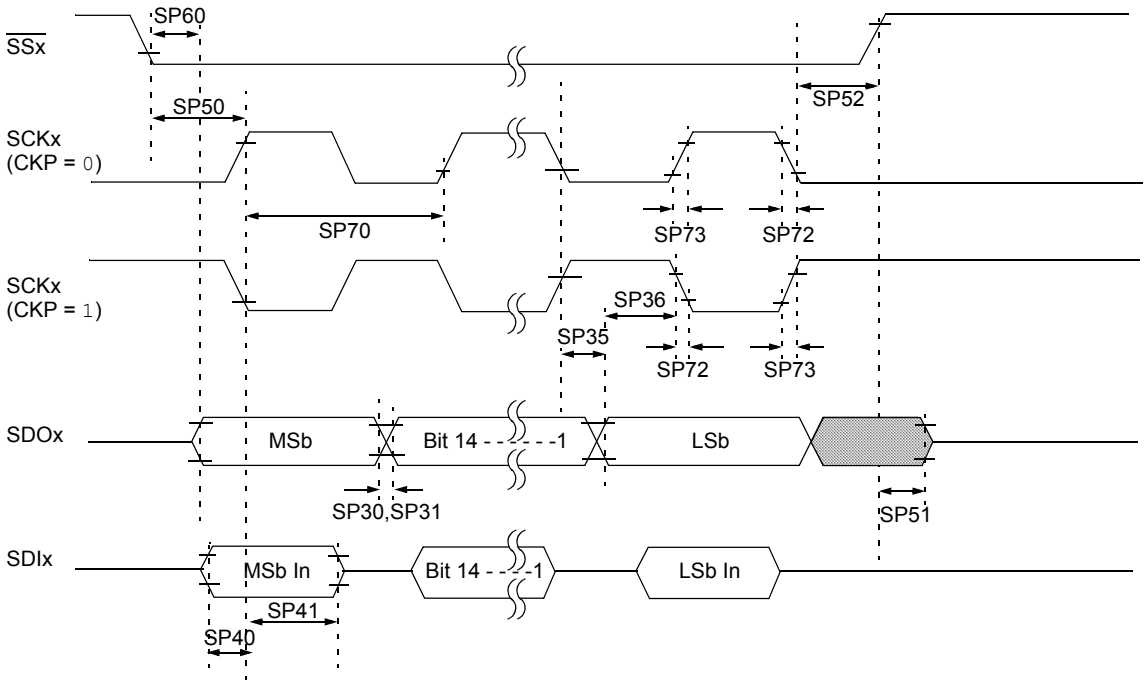
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-20: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.


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**TABLE 32-38: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscP | Maximum SCKx Input Frequency | — | — | 11 | MHz | See **Note 3** |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output, High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SSx}$ ↑ after SCKx Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |
| SP60 | TssL2doV | SDOx Data Output Valid after $\overline{SSx}$ Edge | — | — | 50 | ns | |

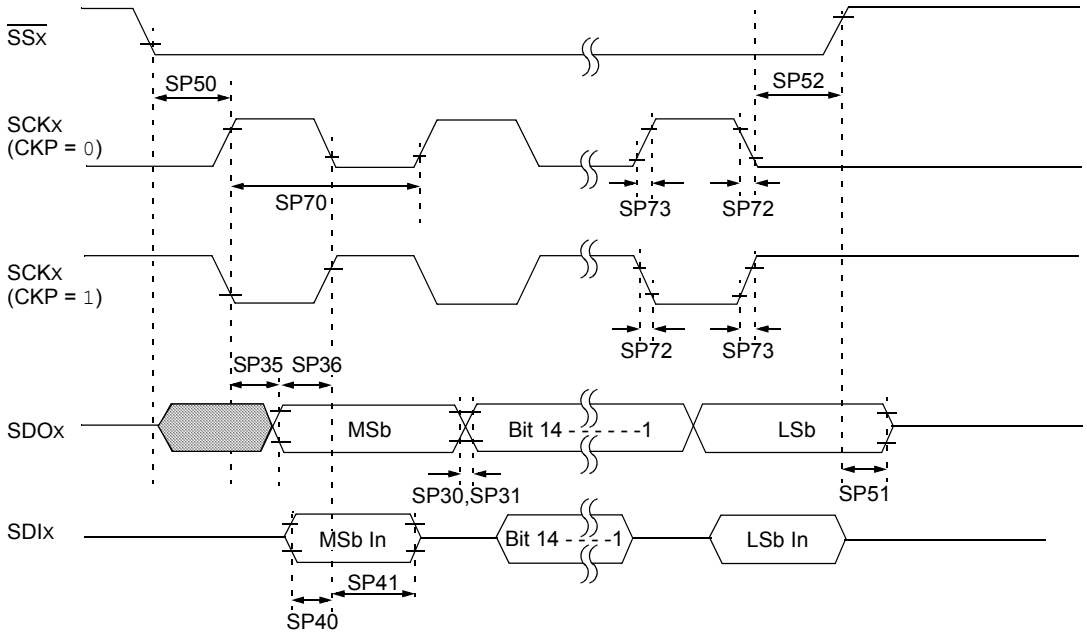
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-21: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.


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**TABLE 32-39: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscP | Maximum SCKx Input Frequency | — | — | 15 | MHz | See **Note 3** |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SSx}$ ↑ after SCKx Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |

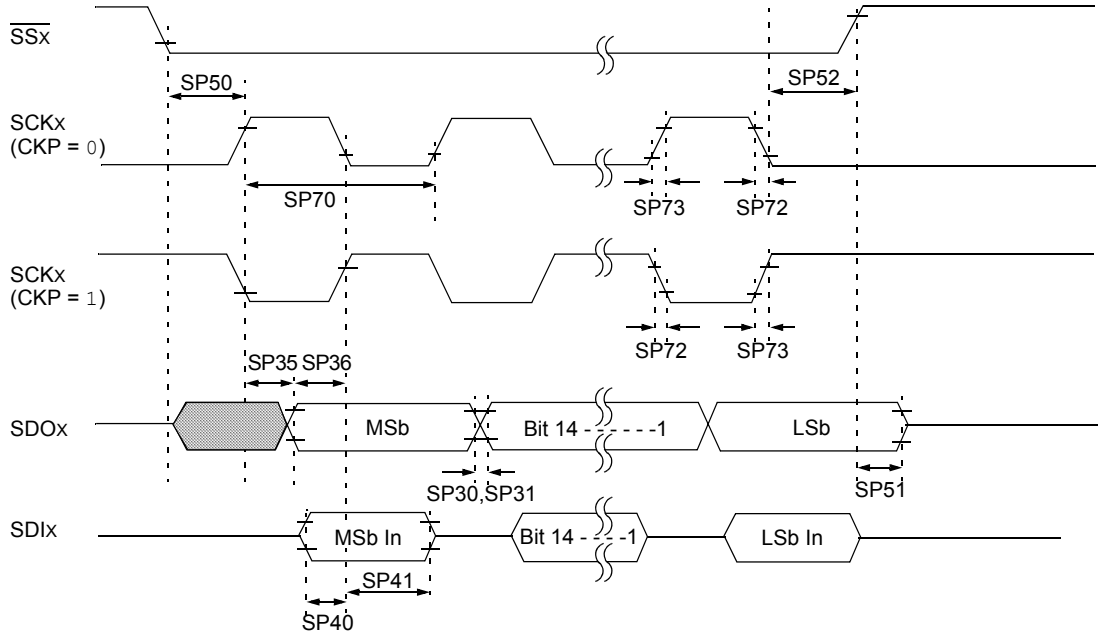
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-22: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.


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**TABLE 32-40: SPI1, SPI3 AND SPI4 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscP | Maximum SCKx Input Frequency | — | — | 11 | MHz | See **Note 3** |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SSx}$ ↑ after SCKx Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

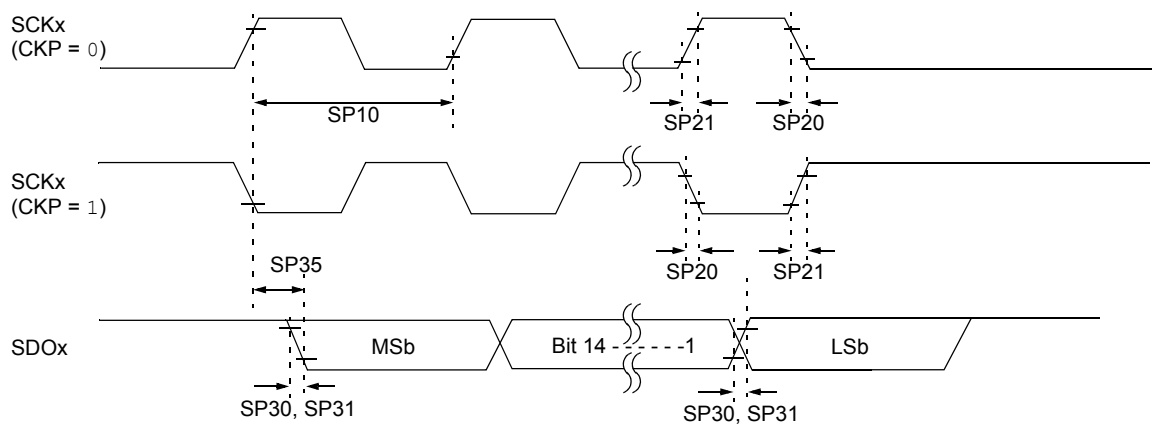
**3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**TABLE 32-41: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Maximum Data Rate** | **Master Transmit Only (Half-Duplex)** | **Master Transmit/Receive (Full-Duplex)** | **Slave Transmit/Receive (Full-Duplex)** | **CKE** | **CKP** | **SMP** |
| 15 MHz | Table 32-42 | — | — | 0,1 | 0,1 | 0,1 |
| 10 MHz | — | Table 32-43 | — | 1 | 0,1 | 1 |
| 10 MHz | — | Table 32-44 | — | 0 | 0,1 | 1 |
| 15 MHz | — | — | Table 32-45 | 1 | 0 | 0 |
| 11 MHz | — | — | Table 32-46 | 1 | 1 | 0 |
| 15 MHz | — | — | Table 32-47 | 0 | 1 | 0 |
| 11 MHz | — | — | Table 32-48 | 0 | 0 | 0 |

**FIGURE 32-23: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.


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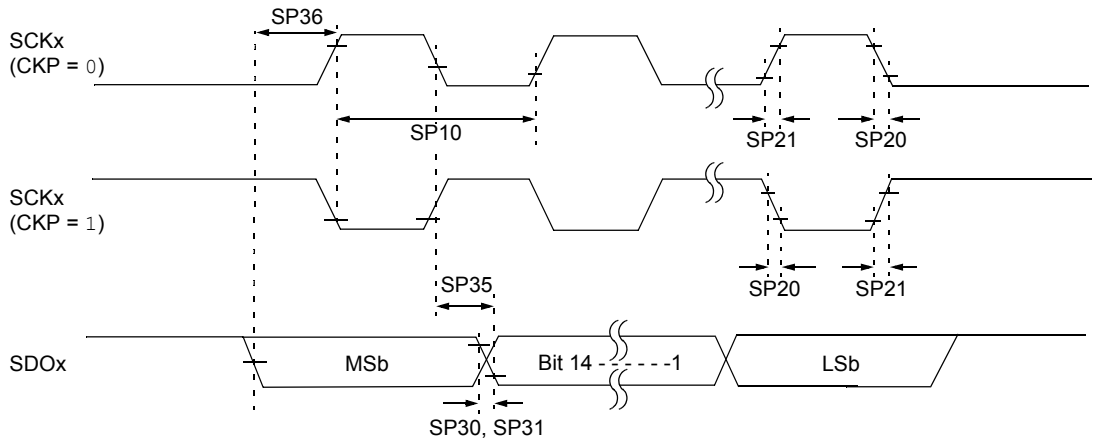
**FIGURE 32-24: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-42: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscP | Maximum SCKx Frequency | — | — | 15 | MHz | See **Note 3** |
| SP20 | TscF | SCKx Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP21 | TscR | SCKx Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdiV2scH, TdiV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |

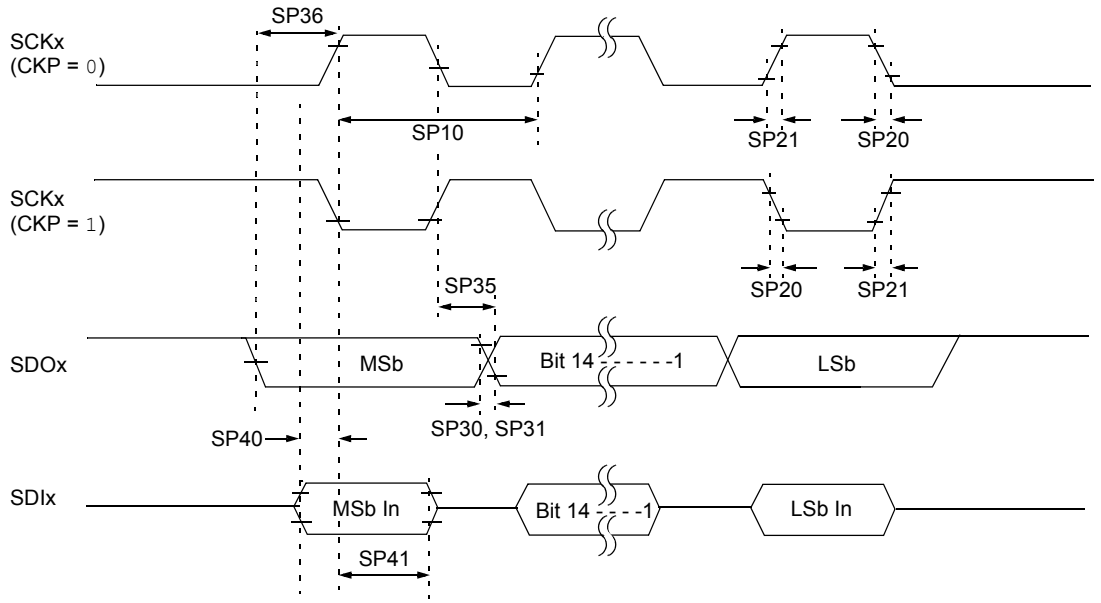
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-25: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-43: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscP | Maximum SCKx Frequency | — | — | 10 | MHz | See **Note 3** |
| SP20 | TscF | SCKx Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP21 | TscR | SCKx Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2sc, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.


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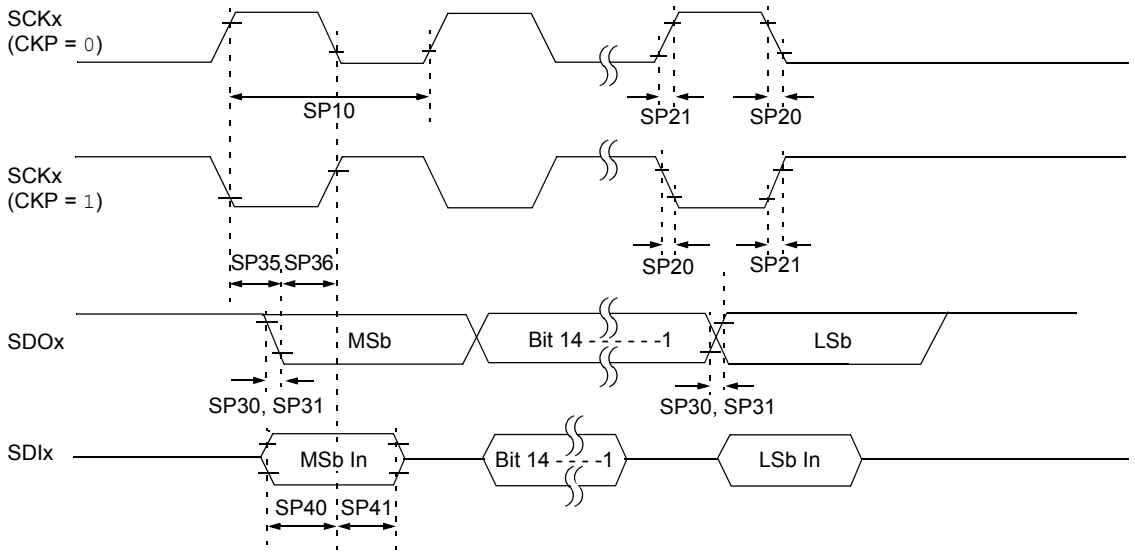
**FIGURE 32-26: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-44: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscP | Maximum SCKx Frequency | — | — | 10 | MHz | -40ºC to +125ºC and see **Note 3** |
| SP20 | TscF | SCKx Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP21 | TscR | SCKx Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |

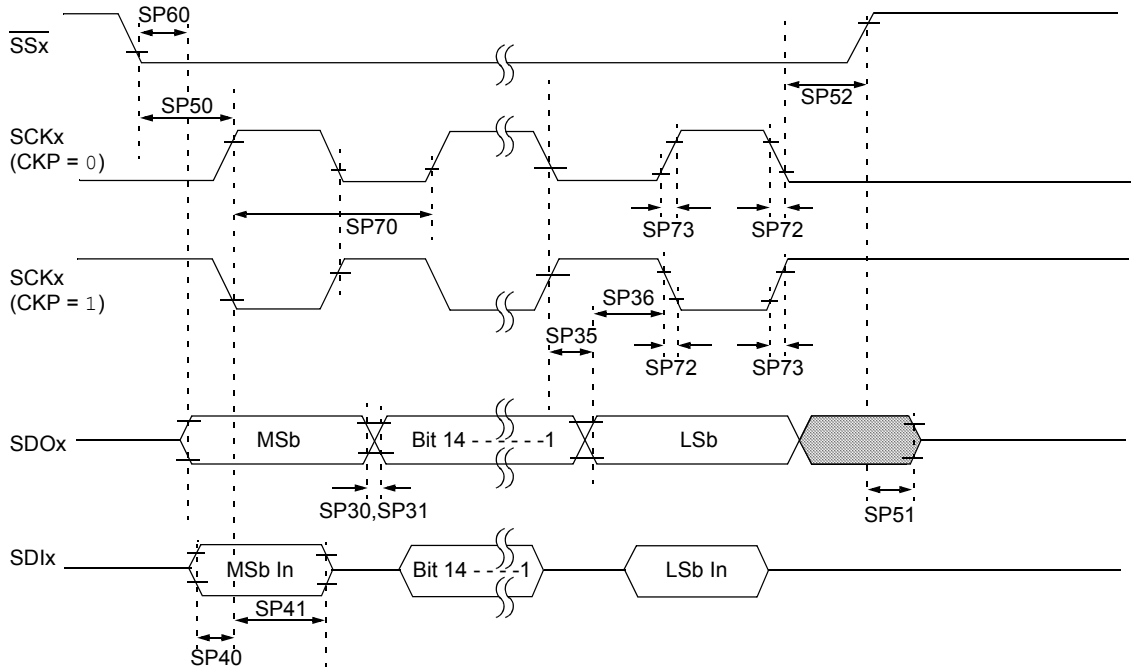
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 100 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-27: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.


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**TABLE 32-45: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscP | Maximum SCKx Input Frequency | — | — | 15 | MHz | See **Note 3** |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output, High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SSx}$ ↑ after SCKx Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |
| SP60 | TssL2doV | SDOx Data Output Valid after $\overline{SSx}$ Edge | — | — | 50 | ns | |

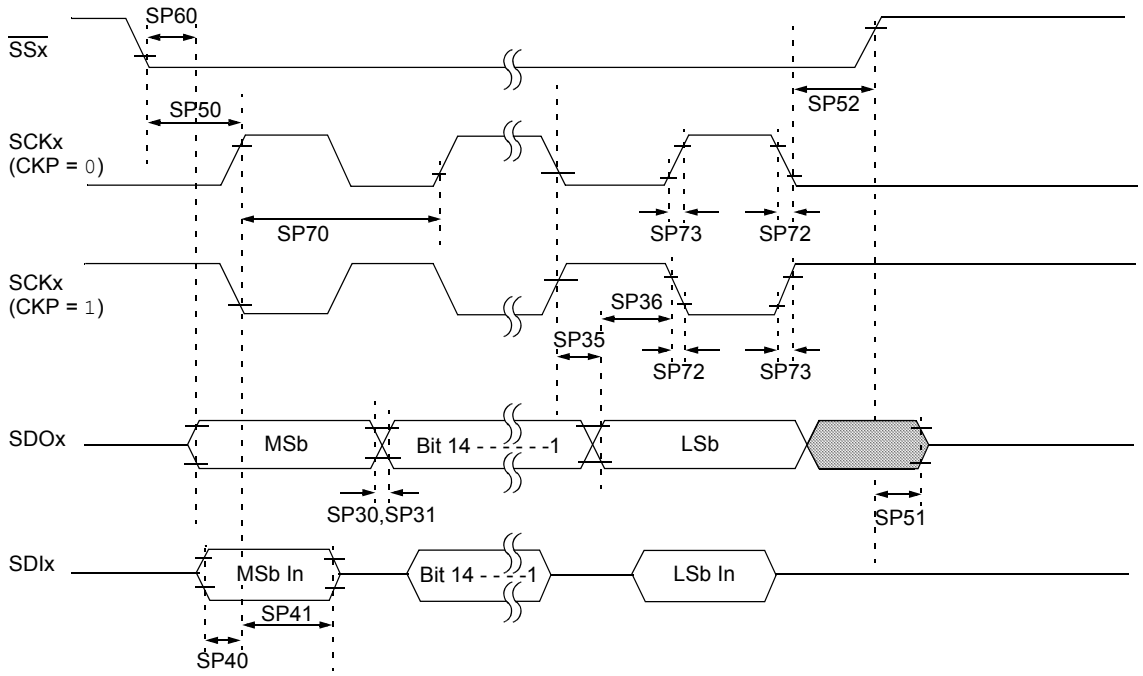
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-28: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.


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**TABLE 32-46: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscP | Maximum SCKx Input Frequency | — | — | 11 | MHz | See **Note 3** |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output, High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH, TscL2ssH | $\overline{SSx}$ ↑ after SCKx Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |
| SP60 | TssL2doV | $\overline{SDOx}$ Data Output Valid after $\overline{SSx}$ Edge | — | — | 50 | ns | |

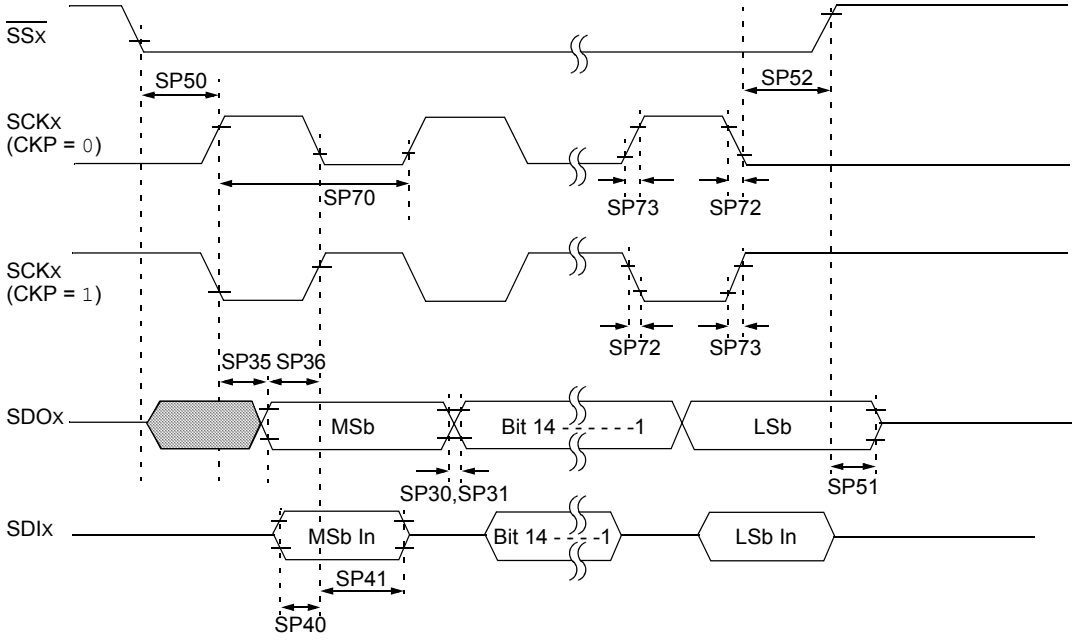
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-29: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.


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**TABLE 32-47: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscP | Maximum SCKx Input Frequency | — | — | 15 | MHz | See **Note 3** |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output, High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH, TscL2ssH | $\overline{SSx}$ ↑ after SCKx Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |

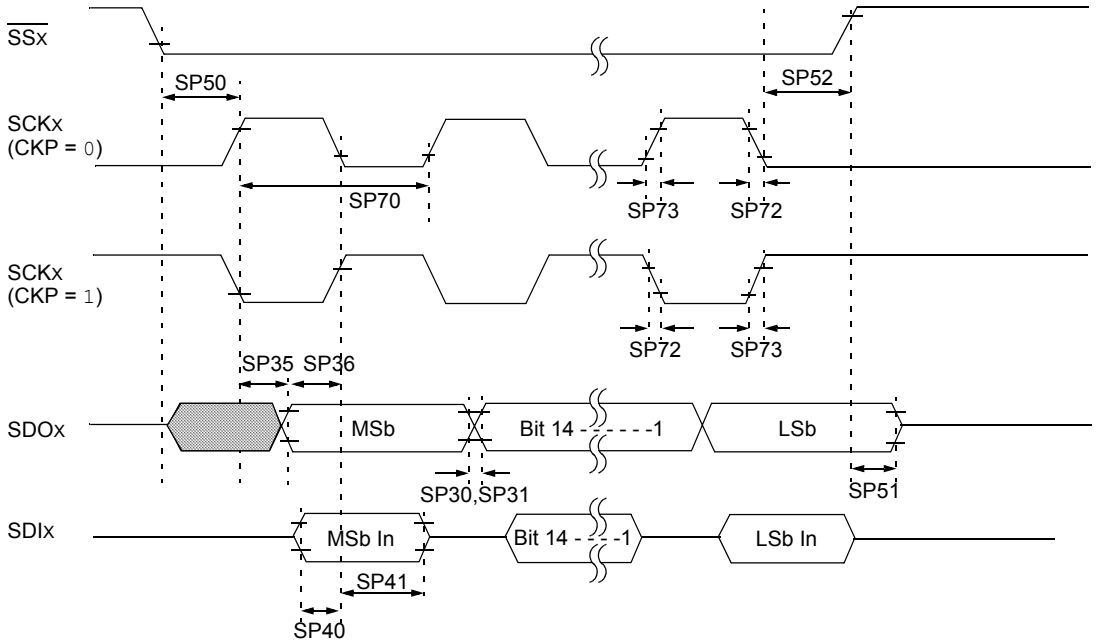
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-30: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.


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**TABLE 32-48: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscP | Maximum SCKx Input Frequency | — | — | 11 | MHz | See **Note 3** |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDOx Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDOx Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output, High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH, TscL2ssH | $\overline{SSx}$ ↑ after SCKx Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |

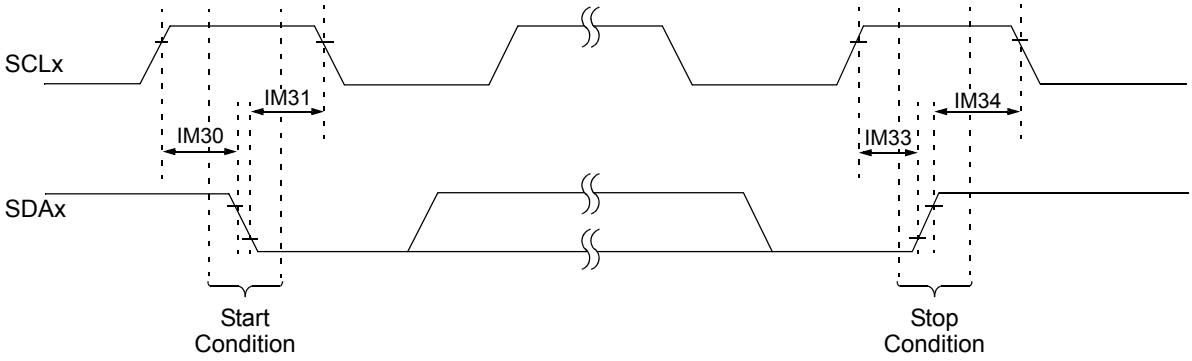
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

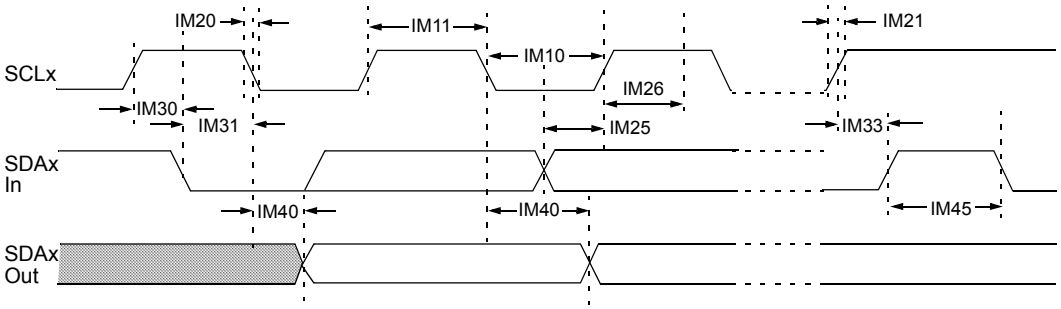
**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-31: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 32-1 for load conditions.

**FIGURE 32-32: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 32-1 for load conditions.


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**TABLE 32-49: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(4)** | | **Min.(1)** | **Max.** | **Units** | **Conditions** |
| IM10 | TLO:SCL | Clock Low Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM11 | THI:SCL | Clock High Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(2) | — | 100 | ns | |
| IM21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(2) | — | 300 | ns | |
| IM25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode(2) | 40 | — | ns | |
| IM26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | µs | |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| | | | 1 MHz mode(2) | 0.2 | — | µs | |
| IM30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM31 | THD:STA | Start Condition Hold Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | TCY/2 (BRG +2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM40 | TAA:SCL | Output Valid From Clock | 100 kHz mode | — | 3500 | ns | |
| | | | 400 kHz mode | — | 1000 | ns | |
| | | | 1 MHz mode(2) | — | 400 | ns | |
| IM45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | µs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode(2) | 0.5 | — | µs | |
| IM50 | CB | Bus Capacitive Loading | | — | 400 | pF | |
| IM51 | TPGD | Pulse Gobbler Delay | | 65 | 390 | ns | See **Note 3** |

**Note 1:** BRG is the value of the $I^2C$ Baud Rate Generator. Refer to **Section 19. "Inter-Integrated Circuit ($I^2C$™)"** (DS70330) in the "*dsPIC33E/PIC24E Family Reference Manual*". Please see the Microchip web site for the latest family reference manual sections.

**2:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**3:** Typical value for this parameter is 130 ns.

**4:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 32-33: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**

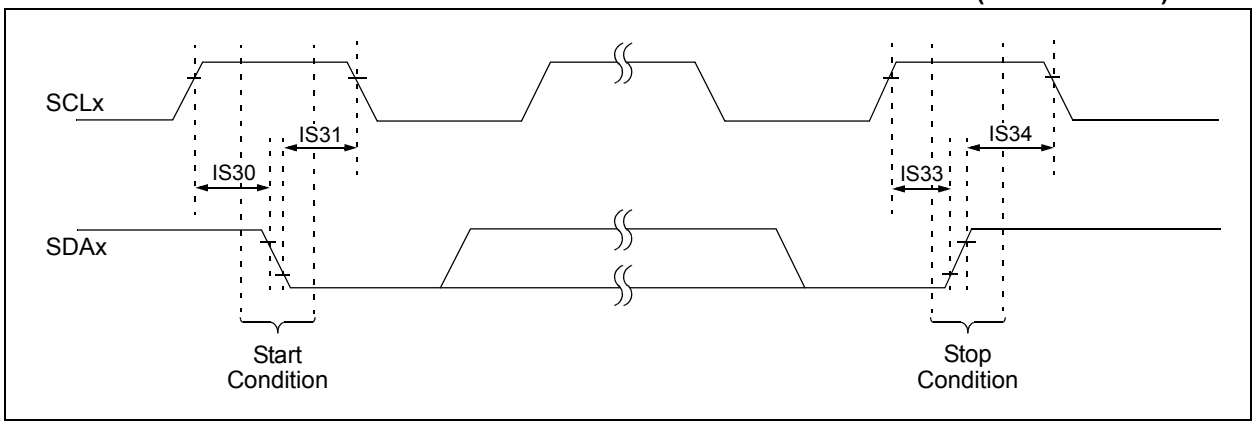


**FIGURE 32-34: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**

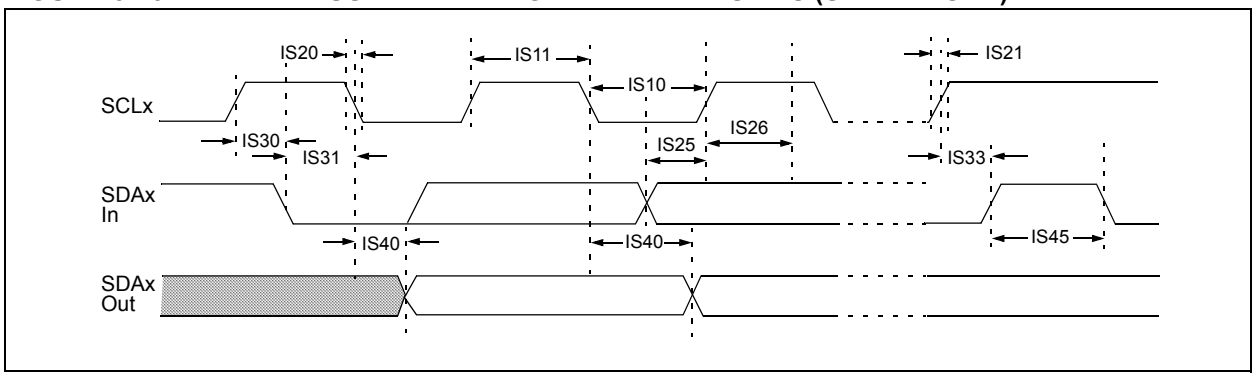



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**TABLE 32-50: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic[3]** | | **Min.** | **Max.** | **Units** | **Conditions** |
| IS10 | TLO:SCL | Clock Low Time | 100 kHz mode | 4.7 | — | µs | |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode[1] | 0.5 | — | µs | |
| IS11 | THI:SCL | Clock High Time | 100 kHz mode | 4.0 | — | µs | Device must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 0.6 | — | µs | Device must operate at a minimum of 10 MHz |
| | | | 1 MHz mode[1] | 0.5 | — | µs | |
| IS20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode[1] | — | 100 | ns | |
| IS21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode[1] | — | 300 | ns | |
| IS25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode[1] | 100 | — | ns | |
| IS26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | µs | |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| | | | 1 MHz mode[1] | 0 | 0.3 | µs | |
| IS30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | 4.7 | — | µs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode[1] | 0.25 | — | µs | |
| IS31 | THD:STA | Start Condition Hold Time | 100 kHz mode | 4.0 | — | µs | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode[1] | 0.25 | — | µs | |
| IS33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | 4.7 | — | µs | |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode[1] | 0.6 | — | µs | |
| IS34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | 4 | — | µs | |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode[1] | 0.25 | | µs | |
| IS40 | TAA:SCL | Output Valid From Clock | 100 kHz mode | 0 | 3500 | ns | |
| | | | 400 kHz mode | 0 | 1000 | ns | |
| | | | 1 MHz mode[1] | 0 | 350 | ns | |
| IS45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | µs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode[1] | 0.5 | — | µs | |
| IS50 | CB | Bus Capacitive Loading | | — | 400 | pF | |
| IS51 | TPGD | Pulse Gobbler Delay | | 65 | 390 | ns | See **Note 2** |

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**2:** The typical value for this parameter is 130 ns.

**3:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 32-35: ECAN™ MODULE I/O TIMING CHARACTERISTICS**

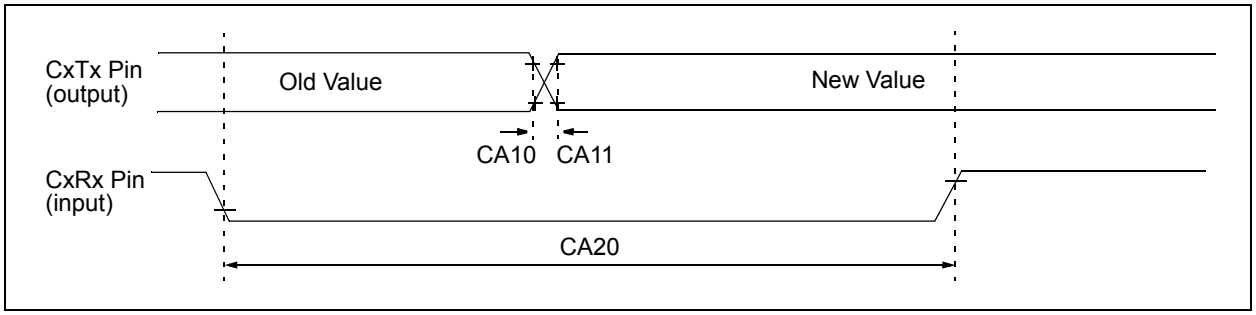


**TABLE 32-51: ECAN™ MODULE I/O TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| CA10 | TioF | Port Output Fall Time | — | — | — | ns | See Parameter DO32 |
| CA11 | TioR | Port Output Rise Time | — | — | — | ns | See Parameter DO31 |
| CA20 | TCWF | Pulse Width to Trigger CAN Wake-up Filter | 120 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 32-36: UARTx MODULE I/O TIMING CHARACTERISTICS**

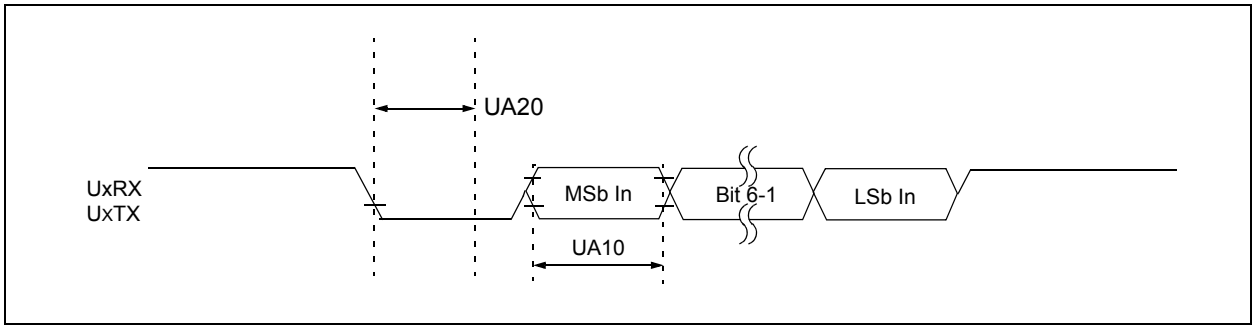


**TABLE 32-52: UARTx MODULE I/O TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| UA10 | TUABAUD | UARTx Baud Time | 66.67 | — | — | ns | |
| UA11 | FBAUD | UARTx Baud Frequency | — | — | 15 | mbps | |
| UA20 | TCWF | Start Bit Pulse Width to Trigger UARTx Wake-up | 500 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.


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**TABLE 32-53: USB OTG MODULE SPECIFICATIONS (dsPIC33EPXXXMU8XX AND PIC24EPXXXGU8XX DEVICES ONLY)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| USB313 | VUSB3V3(2) | USB Voltage | 3.0 | — | 3.6 | V | Voltage on bus must be in this range for proper USB operation |
| USB315 | VILUSB | Input Low Voltage for USB Buffer | — | — | 0.8 | V | |
| USB316 | VIHUSB | Input High Voltage for USB Buffer | 2.0 | — | — | V | |
| USB318 | VDIFS | Differential Input Sensitivity | — | — | 0.2 | V | |
| USB319 | VCM | Differential Common-Mode Range | 0.8 | — | 2.5 | V | The difference between D+ and D- must be within this range while VCM is met |
| USB320 | ZOUT | Driver Output Impedance | 28.0 | — | 44.0 | Ω | |
| USB321 | VOL | Voltage Output Low | 0.0 | — | 0.3 | V | 14.25 kΩ load connected to 3.6V |
| USB322 | VOH | Voltage Output High | 2.8 | — | 3.6 | V | 14.25 kΩ load connected to ground |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** If the USB module is not being used, this pin must be connected to VDD.

**TABLE 32-54: ADC MODULE SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (see Note 3) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Device Supply** | | | | | | | |
| AD01 | AVDD(2) | Module VDD Supply | Greater of VDD – 0.3 or 3.0 | — | Lesser of VDD + 0.3 or 3.6 | V | |
| AD02 | AVSS | Module VSS Supply | VSS – 0.3 | — | VSS + 0.3 | V | |
| **Reference Inputs** | | | | | | | |
| AD05 | VREFH | Reference Voltage High | AVSS + 2.5 | — | AVDD | V | See **Note 1**, VREFH = VREF+, VREFL = VREF- |
| AD05a | | | 3.0 | — | 3.6 | V | VREFH = AVDD, VREFL = AVSS = 0 |
| AD06 | VREFL | Reference Voltage Low | AVSS | — | AVDD – 2.5 | V | See **Note 1** |
| AD06a | | | 0 | — | 0 | V | VREFH = AVDD, VREFL = AVSS = 0 |
| AD07 | VREF | Absolute Reference Voltage | 2.5 | — | 3.6 | V | VREF = VREFH – VREFL |
| AD08 | IREF | Current Drain | —<br>— | —<br>— | 10<br>600 | µA<br>µA | ADC off<br>ADC on |
| AD09 | IAD | Operating Current | —<br>— | 9.0<br>3.2 | —<br>— | mA<br>mA | ADC operating in 10-bit mode, see **Note 1**<br>ADC operating in 12-bit mode, see **Note 1** |
| **Analog Input** | | | | | | | |
| AD12 | VINH | Input Voltage Range, VINH | VINL | — | VREFH | V | This voltage reflects Sample & Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input |
| AD13 | VINL | Input Voltage Range, VINL | VREFL | — | AVSS + 1V | V | This voltage reflects Sample & Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input |
| AD17 | RIN | Recommended Impedance of Analog Voltage Source | — | — | 200 | Ω | |

**Note 1:** These parameters are not characterized or tested in manufacturing.

**2:** The voltage difference between AVDD and VDD cannot exceed 300 mV at any time during operation or start-up.

**3:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.


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**TABLE 32-55: ADC MODULE SPECIFICATIONS (12-BIT MODE)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (see Note 1) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **ADC Accuracy (12-Bit Mode) – Measurements with External VREF+/VREF-** | | | | | | | |
| AD20a | Nr | Resolution | 12 Data Bits | | | bits | |
| AD21a | INL | Integral Nonlinearity | -2 | — | +2 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| AD22a | DNL | Differential Nonlinearity | >-1 | — | <1 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| AD23a | GERR | Gain Error | 1.25 | 1.5 | 3 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| AD24a | EOFF | Offset Error | 1.25 | 1.52 | 2 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| AD25a | — | Monotonicity | — | — | — | — | Guaranteed(2) |
| **ADC Accuracy (12-Bit Mode) – Measurements with Internal VREF+/VREF-** | | | | | | | |
| AD20a | Nr | Resolution | 12 data bits | | | bits | |
| AD21a | INL | Integral Nonlinearity | -2 | — | +2 | LSb | VINL = AVSS = 0V, AVDD = 3.6V |
| AD22a | DNL | Differential Nonlinearity | >-1 | — | <1 | LSb | VINL = AVSS = 0V, AVDD = 3.6V |
| AD23a | GERR | Gain Error | 2 | 3 | 7 | LSb | VINL = AVSS = 0V, AVDD = 3.6V |
| AD24a | EOFF | Offset Error | 2 | 3 | 5 | LSb | VINL = AVSS = 0V, AVDD = 3.6V |
| AD25a | — | Monotonicity | — | — | — | — | Guaranteed(2) |
| **Dynamic Performance (12-Bit Mode)** | | | | | | | |
| AD30a | THD | Total Harmonic Distortion | — | — | -75 | dB | |
| AD31a | SINAD | Signal to Noise and Distortion | 68.5 | 69.5 | — | dB | |
| AD32a | SFDR | Spurious Free Dynamic Range | 80 | — | — | dB | |
| AD33a | FNYQ | Input Signal Bandwidth | — | — | 250 | kHz | |
| AD34a | ENOB | Effective Number of Bits | 11.09 | 11.3 | — | bits | |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

**2:** The Analog-to-Digital conversion result never decreases with an increase in input voltage and has no missing codes.

**TABLE 32-56: ADC MODULE SPECIFICATIONS (10-BIT MODE)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (see Note 1) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **ADC Accuracy (10-Bit Mode) – Measurements with External VREF+/VREF-** | | | | | | | |
| AD20b | Nr | Resolution | 10 data bits | | | bits | |
| AD21b | INL | Integral Nonlinearity | -1 | — | +1 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| AD22b | DNL | Differential Nonlinearity | >-1 | — | <1 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| AD23b | GERR | Gain Error | 1 | 3 | 6 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| AD24b | EOFF | Offset Error | 1 | 2 | 3 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| AD25b | — | Monotonicity | — | — | — | — | Guaranteed(2) |
| **ADC Accuracy (10-Bit Mode) – Measurements with Internal VREF+/VREF-** | | | | | | | |
| AD20b | Nr | Resolution | 10 data bits | | | bits | |
| AD21b | INL | Integral Nonlinearity | -1.5 | — | +1.5 | LSb | VINL = AVSS = 0V, AVDD = 3.6V |
| AD22b | DNL | Differential Nonlinearity | >-1 | — | <1 | LSb | VINL = AVSS = 0V, AVDD = 3.6V |
| AD23b | GERR | Gain Error | 1 | 5 | 6 | LSb | VINL = AVSS = 0V, AVDD = 3.6V |
| AD24b | EOFF | Offset Error | 1 | 2 | 5 | LSb | VINL = AVSS = 0V, AVDD = 3.6V |
| AD25b | — | Monotonicity | — | — | — | — | Guaranteed(2) |
| **Dynamic Performance (10-Bit Mode)** | | | | | | | |
| AD30b | THD | Total Harmonic Distortion | — | — | -64 | dB | |
| AD31b | SINAD | Signal to Noise and Distortion | 57 | 58.5 | — | dB | |
| AD32b | SFDR | Spurious Free Dynamic Range | 72 | — | — | dB | |
| AD33b | FNYQ | Input Signal Bandwidth | — | — | 550 | kHz | |
| AD34b | ENOB | Effective Number of Bits | 9.16 | 9.4 | — | bits | |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

**2:** The Analog-to-Digital conversion result never decreases with an increase in input voltage and has no missing codes.


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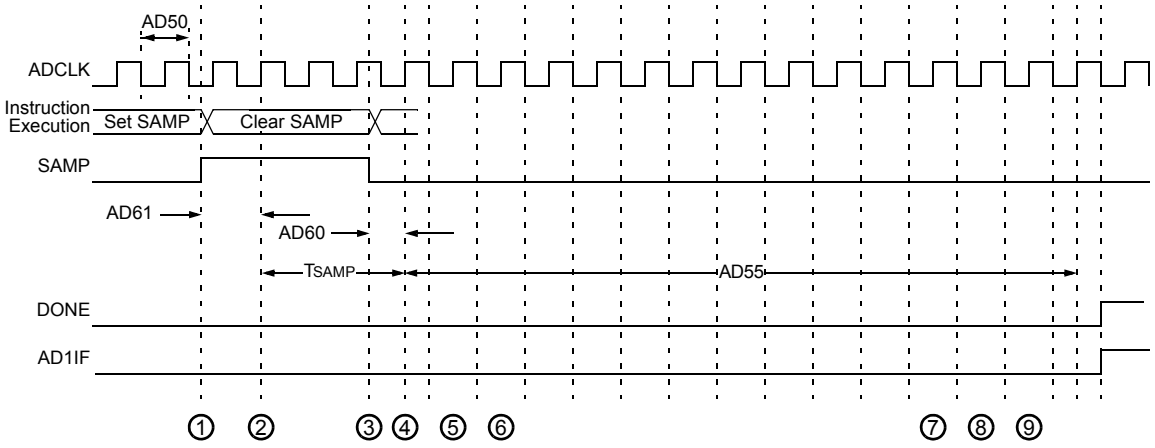
**FIGURE 32-37: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)**




① – Software sets AD1CON1. SAMP to start sampling.

② – Sampling starts after discharge period. TSAMP is described in **Section 16. "Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33E/PIC24E Family Reference Manual"*.

③ – Software clears AD1CON1. SAMP to start conversion.

④ – Sampling ends, conversion sequence starts.

⑤ – Convert bit 11.

⑥ – Convert bit 10.

⑦ – Convert bit 1.

⑧ – Convert bit 0.

⑨ – One TAD for end of conversion.

**TABLE 32-57: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (see Note 4) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| AD50 | TAD | ADC Clock Period | 117.6 | — | — | ns | |
| AD51 | tRC | ADC Internal RC Oscillator Period | — | 250 | — | ns | |
| **Conversion Rate** | | | | | | | |
| AD55 | tCONV | Conversion Time | — | 14 TAD | | ns | |
| AD56 | FCNV | Throughput Rate | — | — | 500 | Ksps | |
| AD57 | TSAMP | Sample Time | 3 TAD | — | — | — | |
| **Timing Parameters** | | | | | | | |
| AD60 | tPCS | Conversion Start from Sample Trigger(1) | 2 TAD | — | 3 TAD | — | Auto-Convert Trigger not selected |
| AD61 | tPSS | Sample Start from Setting Sample (SAMP) bit(1) | 2 TAD | — | 3 TAD | — | |
| AD62 | tCSS | Conversion Completion to Sample Start (ASAM = 1)(1) | — | 0.5 TAD | — | — | |
| AD63 | tDPU | Time to Stabilize Analog Stage from ADC Off to ADC On(1) | — | — | 20 | μs | See **Note 3** |

**Note 1:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

**2:** These parameters are characterized but not tested in manufacturing.

**3:** The tDPU parameter is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (ADxCON1<15>) = 1). During this time, the ADC result is indeterminate.

**4:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.


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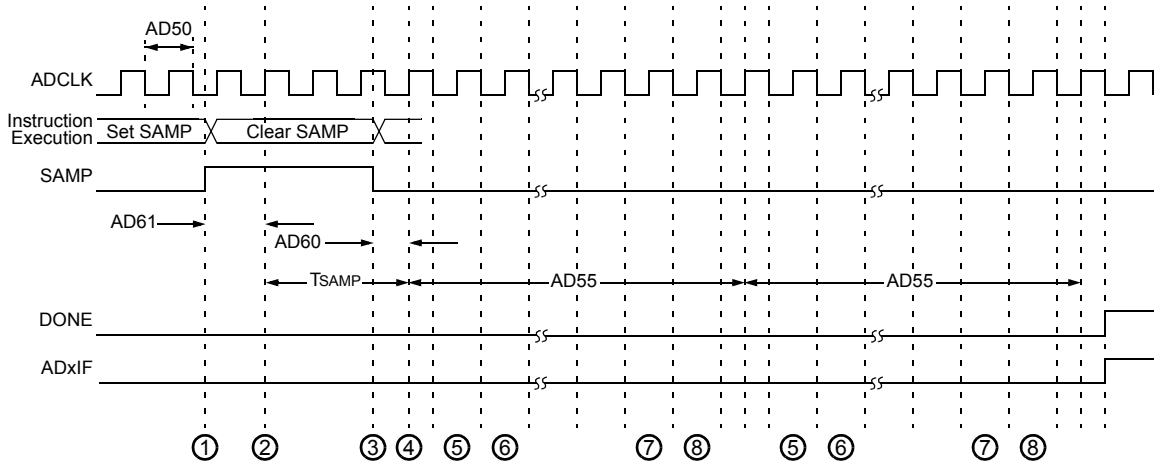
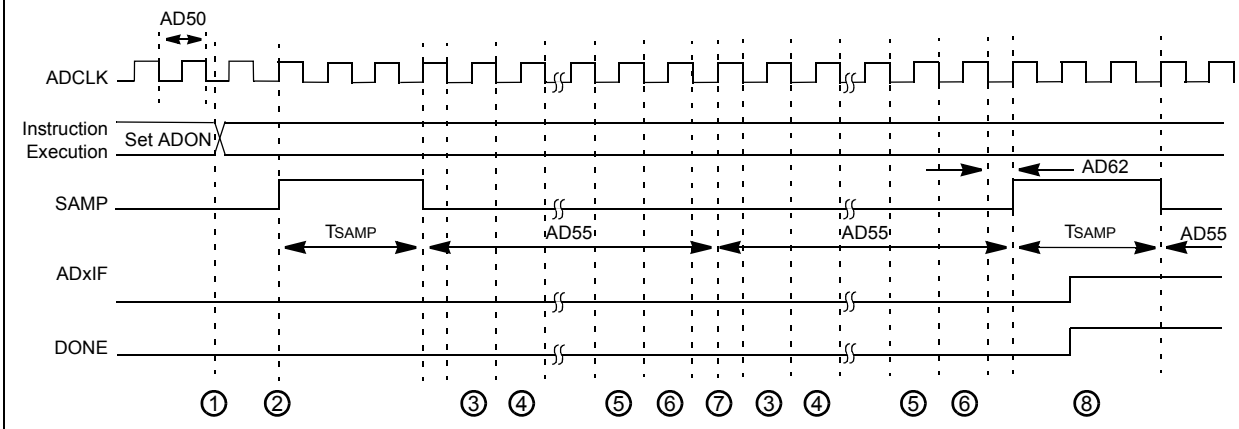
**FIGURE 32-38: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)**




1. – Software sets ADx1CON1. SAMP to start sampling.
2. – Sampling starts after discharge period. TSAMP is described in **Section 16. "Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33E/PIC24E Family Reference Manual"*.
3. – Software clears ADxCON1. SAMP to start conversion.
4. – Sampling ends, conversion sequence starts.
5. – Convert bit 9.
6. – Convert bit 8.
7. – Convert bit 0.
8. – One TAD for end of conversion.

**FIGURE 32-39: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SSRCG = 0, SAMC<4:0> = 00010)**




1. – Software sets ADxCON1. ADON to start AD operation.
2. – Sampling starts after discharge period. TSAMP is described in **Section 16. "Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33E/PIC24E Family Reference Manual"*.
3. – Convert bit 9.
4. – Convert bit 8.
5. – Convert bit 0.
6. – One TAD for end of conversion.
7. – Begin conversion of next channel.
8. – Sample for time specified by SAMC<4:0>.

**TABLE 32-58: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (see Note 4) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| AD50 | TAD | ADC Clock Period | 76 | — | — | ns | |
| AD51 | tRC | ADC Internal RC Oscillator Period | — | 250 | — | ns | |
| **Conversion Rate** | | | | | | | |
| AD55 | tCONV | Conversion Time | — | 12 TAD | — | — | |
| AD56 | FCNV | Throughput Rate | — | — | 1.1 | Msps | Using sequential sampling |
| AD57 | TSAMP | Sample Time | 2 TAD | — | — | — | |
| **Timing Parameters** | | | | | | | |
| AD60 | tPCS | Conversion Start from Sample Trigger(2) | 2 TAD | — | 3 TAD | — | Auto-Convert Trigger not selected |
| AD61 | tPSS | Sample Start from Setting Sample (SAMP) bit(2) | 2 TAD | — | 3 TAD | — | |
| AD62 | tCSS | Conversion Completion to Sample Start (ASAM = 1)(2) | — | 0.5 TAD | — | — | |
| AD63 | tDPU | Time to Stabilize Analog Stage from ADC Off to ADC On(2) | — | — | 20 | μs | See **Note 3** |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

**3:** The tDPU parameter is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (ADxCON1<15>) = 1). During this time, the ADC result is indeterminate.

**4:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.


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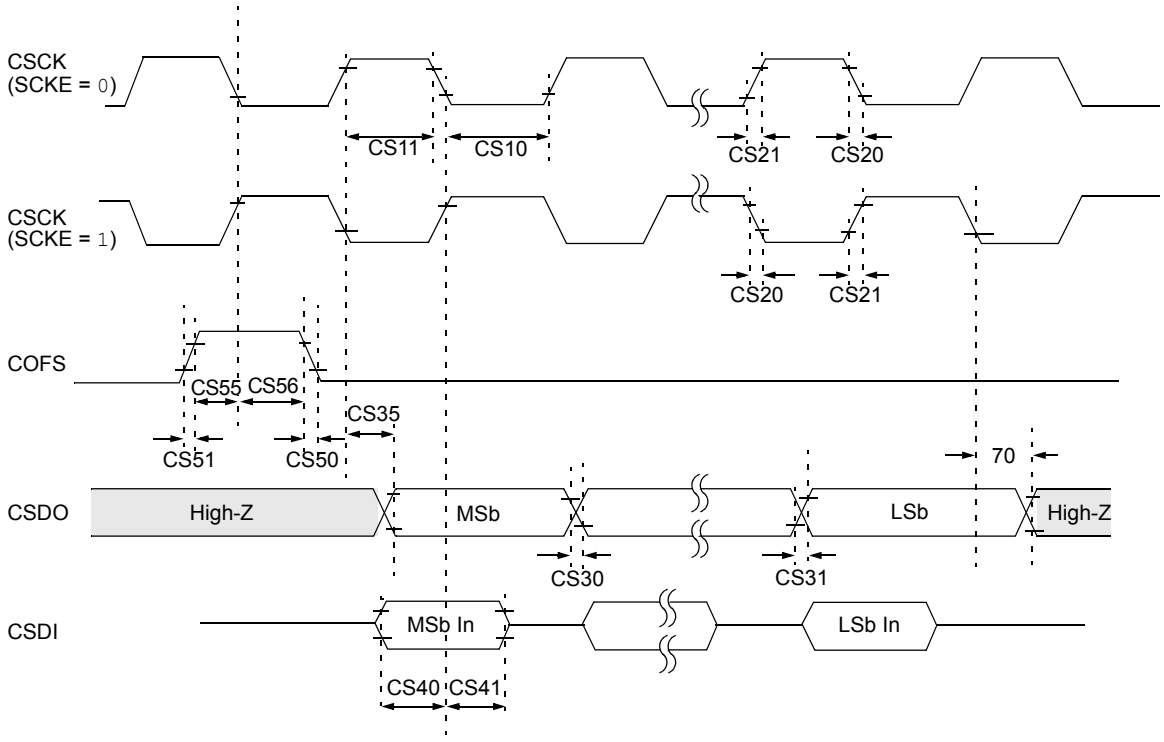
**FIGURE 32-40: DCI MODULE (MULTI-CHANNEL, I²S MODES) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-59: DCI MODULE (MULTI-CHANNEL, I²S MODES) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| CS10 | TCSCKL | CSCK Input Low Time (CSCK pin is an input) | TCY/2 + 20 | — | — | ns | |
| | | CSCK Output Low Time(3) (CSCK pin is an output) | 30 | — | — | ns | |
| CS11 | TCSCKH | CSCK Input High Time (CSCK pin is an input) | TCY/2 + 20 | — | — | ns | |
| | | CSCK Output High Time(3) (CSCK pin is an output) | 30 | — | — | ns | |
| CS20 | TCSCKF | CSCK Output Fall Time (CSCK pin is an output) | — | — | — | ns | See Parameter DO32 |
| CS21 | TCSCKR | CSCK Output Rise Time (CSCK pin is an output) | — | — | — | ns | See Parameter DO31 |
| CS30 | TCSDOF | CSDO Data Output Fall Time | — | — | — | ns | See Parameter DO32 |
| CS31 | TCSDOR | CSDO Data Output Rise Time | — | — | — | ns | See Parameter DO31 |
| CS35 | TDV | Clock Edge to CSDO Data Valid | — | — | 10 | ns | |
| CS36 | TDIV | Clock Edge to CSDO Tri-Stated | 10 | — | 20 | ns | |
| CS40 | TCSDI | Setup Time of CSDI Data Input to CSCK Edge (CSCK pin is input or output) | 20 | — | — | ns | |
| CS41 | THCSDI | Hold Time of CSDI Data Input to CSCK Edge (CSCK pin is input or output) | 20 | — | — | ns | |
| CS50 | TCOFSF | COFS Fall Time (COFS pin is output) | — | — | — | ns | See Parameter DO32 |
| CS51 | TCOFSR | COFS Rise Time (COFS pin is output) | — | — | — | ns | See Parameter DO31 |
| CS55 | TSCOFS | Setup Time of COFS Data Input to CSCK Edge (COFS pin is input) | 20 | — | — | ns | |
| CS56 | THCOFS | Hold Time of COFS Data Input to CSCK Edge (COFS pin is input) | 20 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for CSCK is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.


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**FIGURE 32-41: DCI MODULE (AC-LINK MODE) TIMING CHARACTERISTICS**

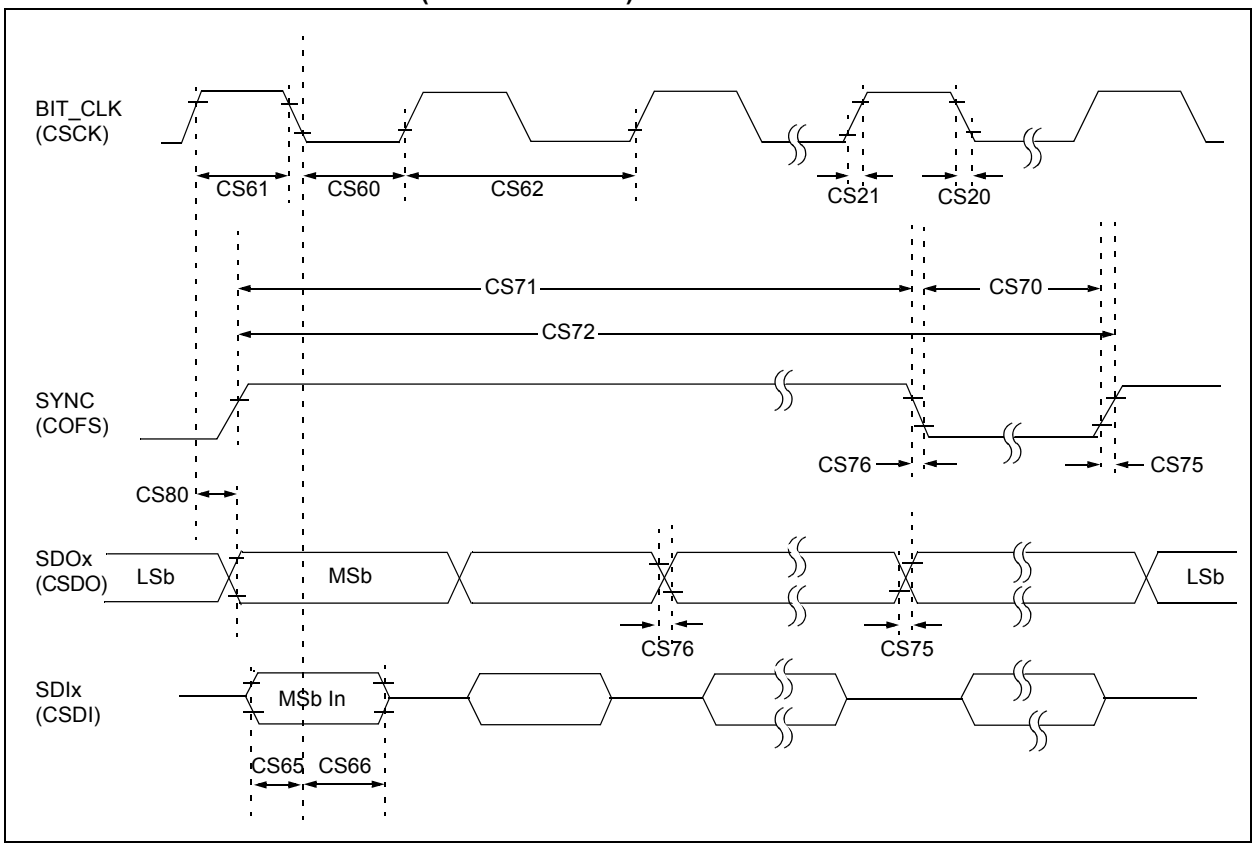

**TABLE 32-60: DCI MODULE (AC-LINK MODE) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1,2)** | **Min.** | **Typ.(3)** | **Max.** | **Units** | **Conditions** |
| CS60 | TBCLKL | BIT_CLK Low Time | 36 | 40.7 | 45 | ns | |
| CS61 | TBCLKH | BIT_CLK High Time | 36 | 40.7 | 45 | ns | |
| CS62 | TBCLK | BIT_CLK Period | — | 81.4 | — | ns | Bit clock is input |
| CS65 | TSACL | Input Setup Time to Falling Edge of BIT_CLK | — | — | 10 | ns | |
| CS66 | THACL | Input Hold Time from Falling Edge of BIT_CLK | — | — | 10 | ns | |
| CS70 | TSYNCLO | Sync Data Output Low Time | — | 19.5 | — | µs | |
| CS71 | TSYNCHI | Sync Data Output High Time | — | 1.3 | — | µs | |
| CS72 | TSYNC | Sync Data Output Period | — | 20.8 | — | µs | |
| CS77 | TRACL | Rise Time, Sync, SDATA_OUT | — | — | — | ns | See Parameter DO32 |
| CS78 | TFACL | Fall Time, Sync, SDATA_OUT | — | — | — | ns | See Parameter DO31 |
| CS80 | TOVDACL | Output Valid Delay from Rising Edge of BIT_CLK | — | — | 15 | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** These values assume the BIT_CLK frequency is 12.288 MHz.

**3:** Data in “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.


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**TABLE 32-61: COMPARATOR TIMING SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (see Note 3) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| 300 | TRESP | Response Time(2) | — | 150 | 400 | ns | |
| 301 | TMC2OV | Comparator Mode Change to Output Valid | — | — | 10 | μs | |

**Note 1:** Parameters are characterized but not tested.

**2:** Response time is measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

**3:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

**TABLE 32-62: COMPARATOR MODULE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (see Note 2) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| D300 | VIOFF | Input Offset Voltage | — | ±10 | — | mV | |
| D301 | VICM | Input Common-Mode Voltage | AVSS | — | AVDD | V | |
| D302 | CMRR | Common-Mode Rejection Ratio | -54 | — | — | dB | |
| D305 | IVREF | Internal Voltage Reference | 0.19 | 0.20 | 0.21 | V | BGSEL<1:0> = 10 |
| | | | 0.57 | 0.60 | 0.63 | V | BGSEL<1:0> = 01 |
| | | | 1.14 | 1.20 | 1.26 | V | BGSEL<1:0> = 00 |

**Note 1:** Parameters are characterized but not tested.

**2:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

**TABLE 32-63: COMPARATOR REFERENCE VOLTAGE SETTLING TIME SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (see Note 3) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(2)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| VR310 | TSET | Settling Time(1) | — | — | 10 | μs | |

**Note 1:** Setting time measured while CVRR = 1 and CVR<3:0> bits transition from '0000' to '1111'.

**2:** These parameters are characterized, but not tested in manufacturing.

**3:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.

**TABLE 32-64: COMPARATOR REFERENCE VOLTAGE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (see Note 2) (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| VRD310 | CVRES | Resolution | CVRSRC/24 | — | CVRSRC/32 | LSb | |
| VRD311 | CVRAA | Absolute Accuracy | — | — | 0.5 | LSb | |
| VRD312 | CVRL | Maximum Load on CVREF Output Pin | — | — | 0.75 | μA | AVDD = 3.6V,<br>CVRSS = 0,<br>CVRR = 0,<br>CVR<3:0> = 1111 |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, Comparator and DAC will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 32-11 for the minimum and maximum BOR values.


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**FIGURE 32-42: PARALLEL SLAVE PORT TIMING**

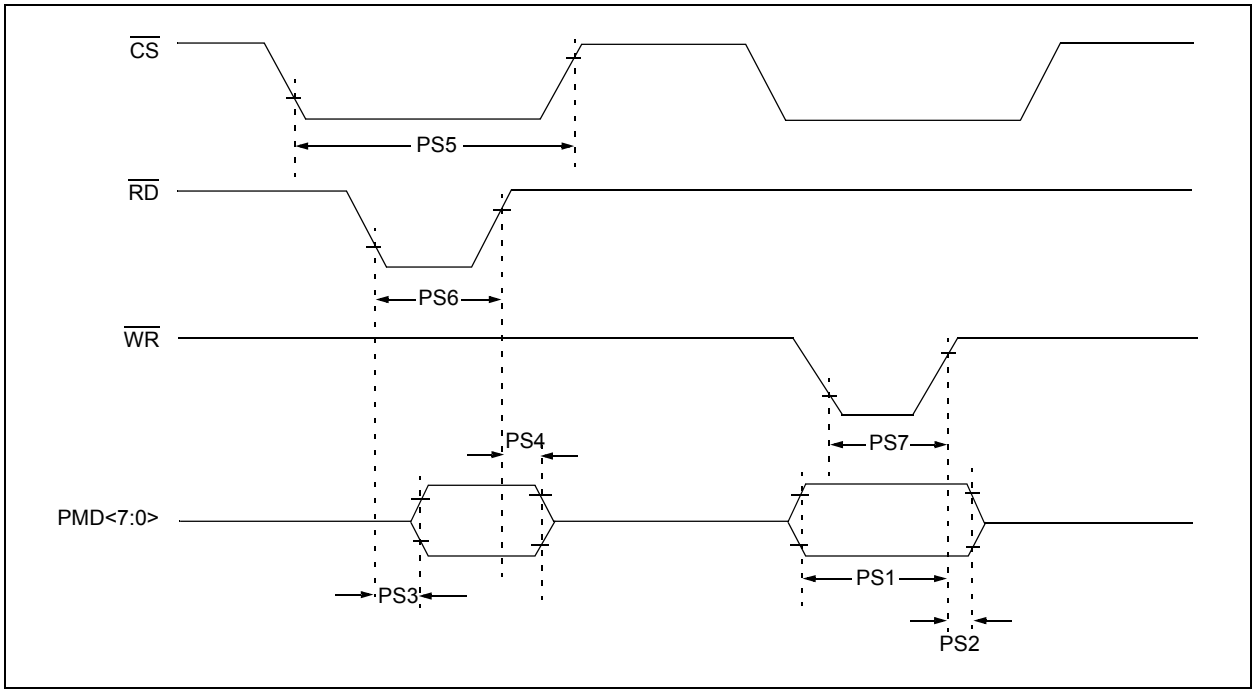


**TABLE 32-65: PARALLEL SLAVE PORT TIMING SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| PS1 | TdtV2wrH | Data In Valid Before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time) | 20 | — | — | ns | |
| PS2 | TwrH2dtI | $\overline{WR}$ or $\overline{CS}$ Inactive to Data In Invalid (hold time) | 20 | — | — | ns | |
| PS3 | TrdL2dtV | $\overline{RD}$ and $\overline{CS}$ to Active Data Out Valid | — | — | 80 | ns | |
| PS4 | TrdH2dtI | $\overline{RD}$ or $\overline{CS}$ Inactive to Data Out Invalid | 10 | — | 30 | ns | |
| PS5 | Tcs | $\overline{CS}$ Active Time | 33.33 | — | — | ns | |
| PS6 | Twr | $\overline{RD}$ Active Time | 33.33 | — | — | ns | |
| PS7 | Trd | $\overline{WR}$ Active Time | 33.33 | — | — | ns | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 32-43: PARALLEL MASTER PORT READ TIMING DIAGRAM**

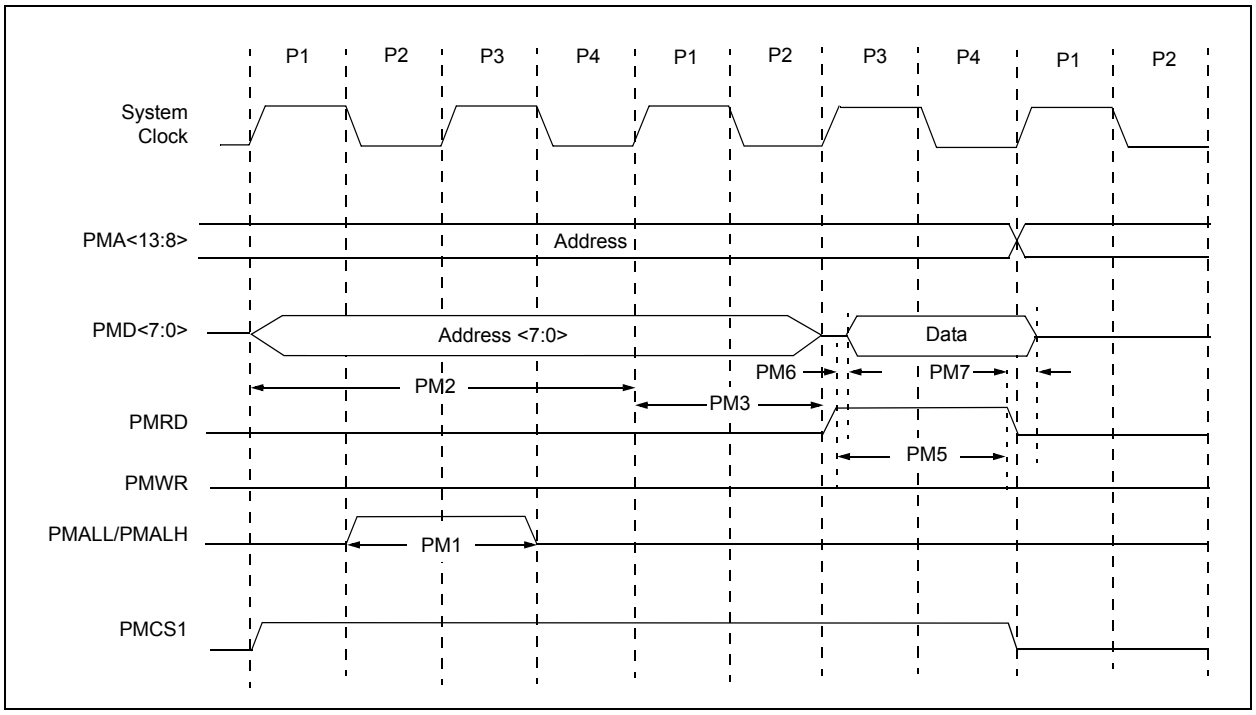


**TABLE 32-66: PARALLEL MASTER PORT READ TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|
| **Param.** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| PM1 | PMALL/PMALH Pulse Width | — | 0.5 TCY | — | ns | |
| PM2 | Address Out Valid to PMALL/PMALH Invalid (address setup time) | — | 1 TCY | — | ns | |
| PM3 | PMALL/PMALH Invalid to Address Out Invalid (address hold time) | — | 0.5 TCY | — | ns | |
| PM5 | PMRD Pulse Width | — | 0.5 TCY | — | ns | |
| PM6 | PMRD or PMENB Active to Data In Valid (data setup time) | 150 | — | — | ns | |
| PM7 | PMRD or PMENB Inactive to Data In Invalid (data hold time) | — | — | 5 | ns | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.


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**FIGURE 32-44: PARALLEL MASTER PORT WRITE TIMING DIAGRAM**

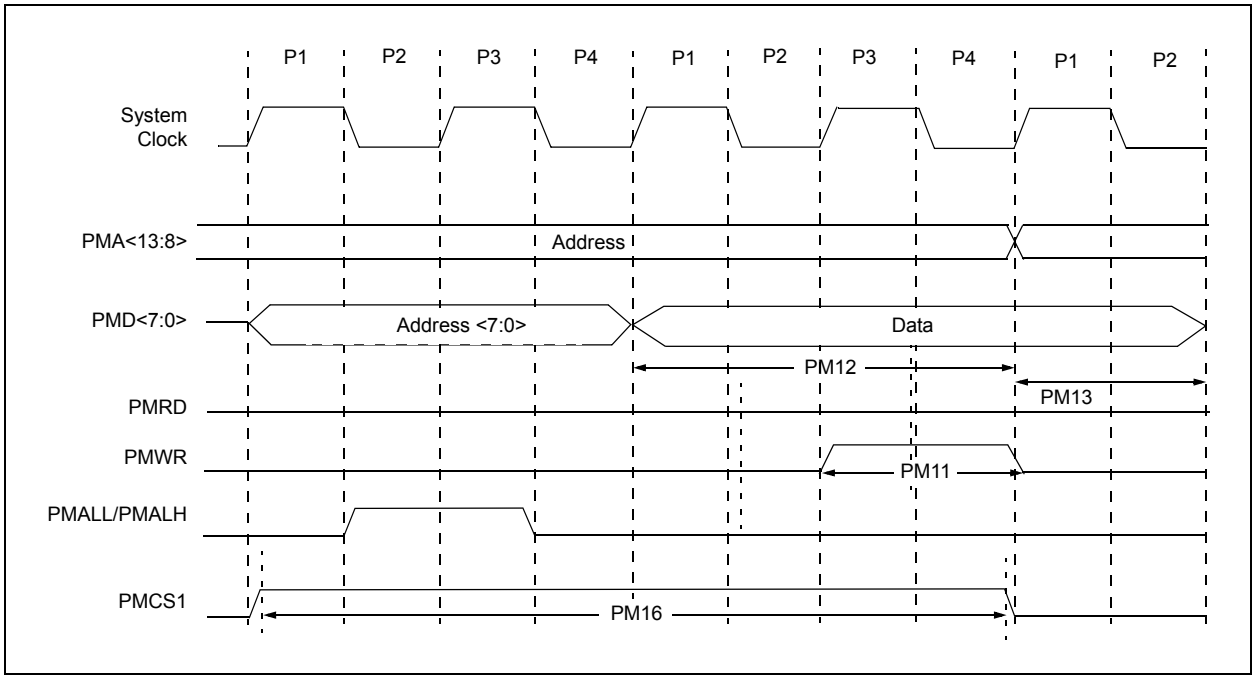


**TABLE 32-67: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|
| **Param.** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| PM11 | PMWR Pulse Width | — | 0.5 TCY | — | ns | |
| PM12 | Data Out Valid Before PMWR or PMENB goes Inactive (data setup time) | — | 1 TCY | — | ns | |
| PM13 | PMWR or PMEMB Invalid to Data Out Invalid (data hold time) | — | 0.5 TCY | — | ns | |
| PM16 | PMCSx Pulse Width | TCY - 5 | — | — | ns | ADRMUX<1:0> = 00 (demultiplexed address) |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**TABLE 32-68: DMA MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|
| **Param.** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| DM1 | DMA Byte/Word Transfer Latency | 1 TCY | — | — | ns | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**NOTES:**


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## 33.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

**Note:** The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

**FIGURE 33-1: VOH – 4x DRIVER PINS @ +85ºC**

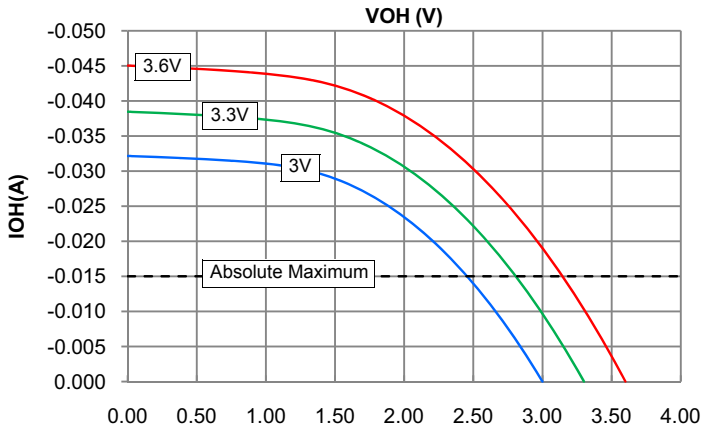


**FIGURE 33-2: VOH – 8x DRIVER PINS @ +85ºC**

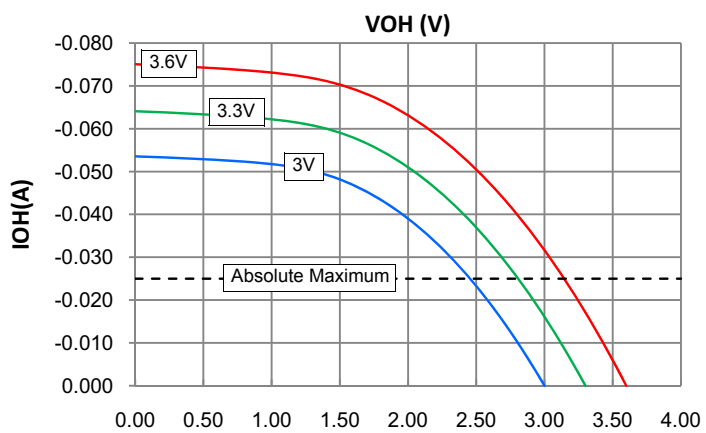


**FIGURE 33-3: VOL – 4x DRIVER PINS @ +85ºC**

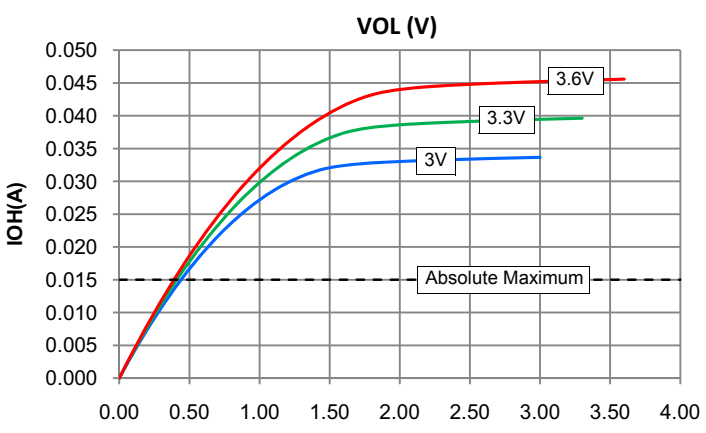


**FIGURE 33-4: VOL – 8x DRIVER PINS @ +85ºC**

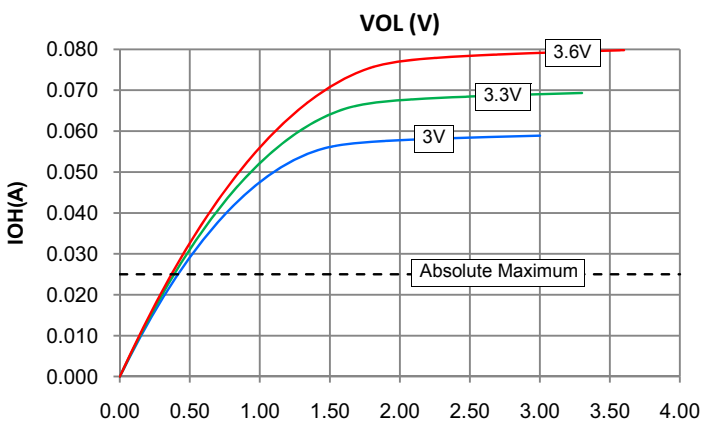


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**FIGURE 33-5: TYPICAL IPD CURRENT @ VDD = 3.3V**

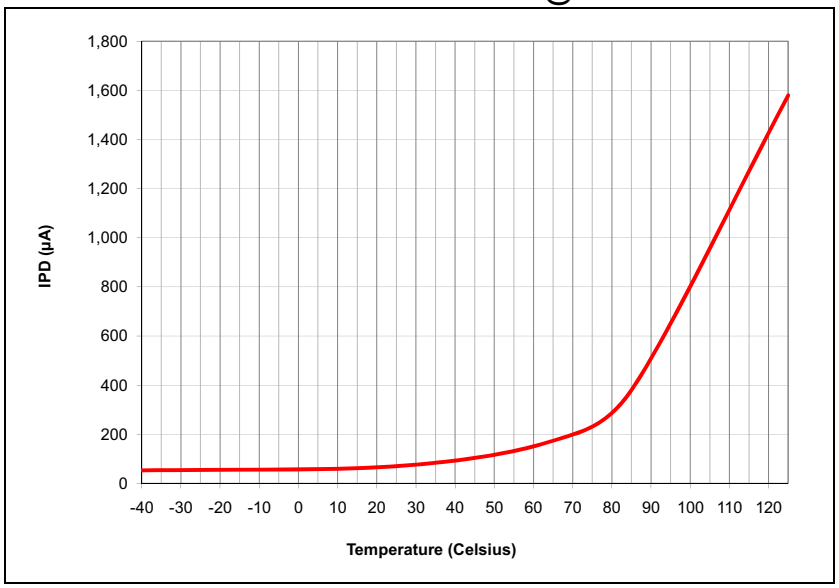


**FIGURE 33-6: TYPICAL IDD CURRENT – VDD = 3.3V @ +85ºC**

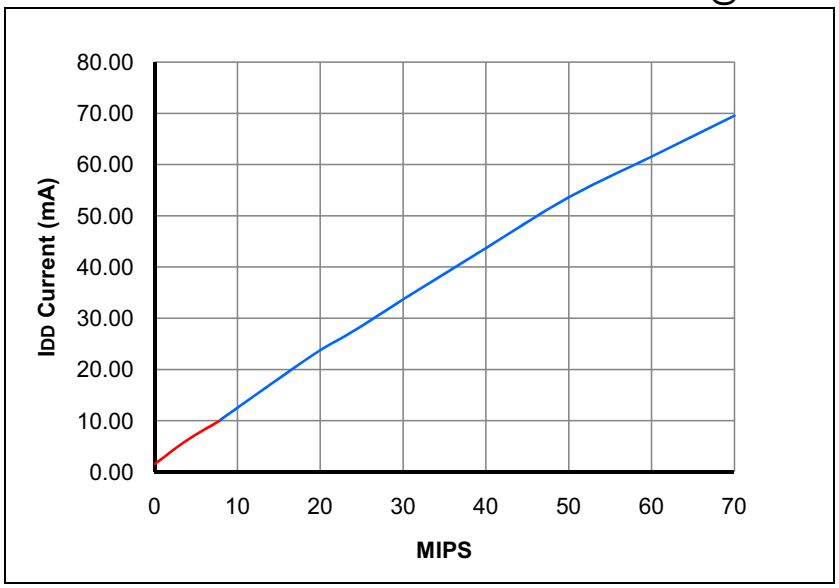


**FIGURE 33-7: TYPICAL IDOZE CURRENT @ VDD = 3.3V**

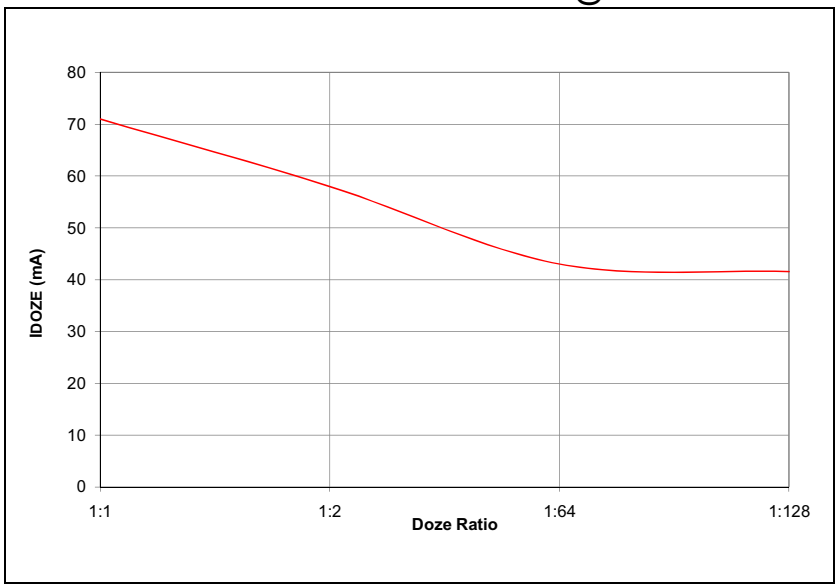


**FIGURE 33-8: TYPICAL IIDLE CURRENT – VDD = 3.3V @ +85ºC**

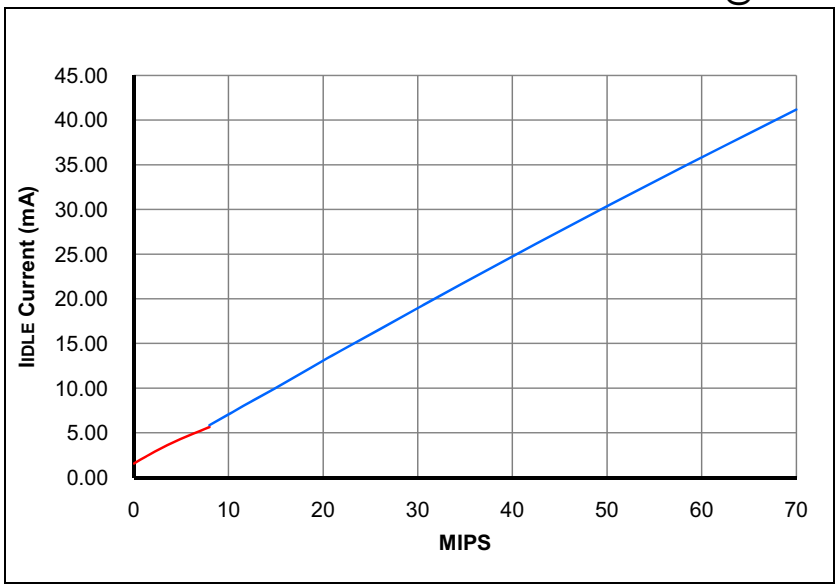




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**FIGURE 33-9: TYPICAL FRC FREQUENCY @ VDD = 3.3V**

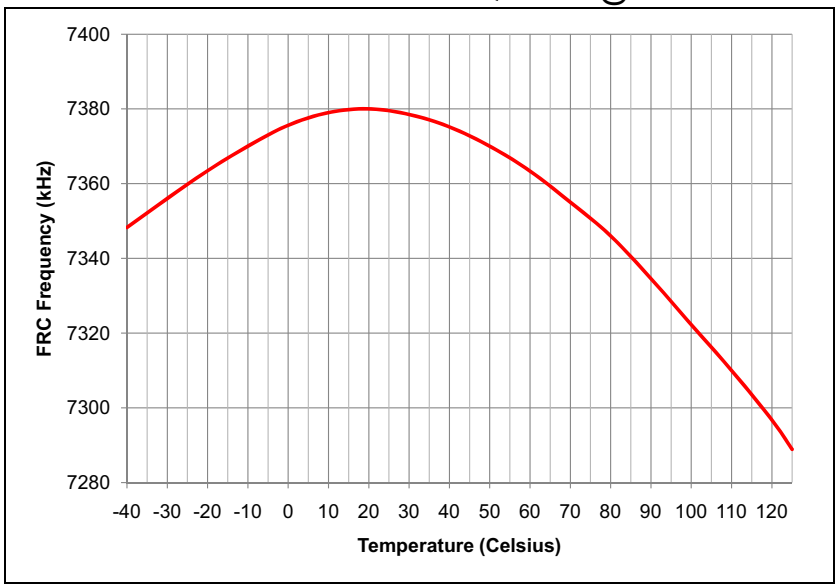
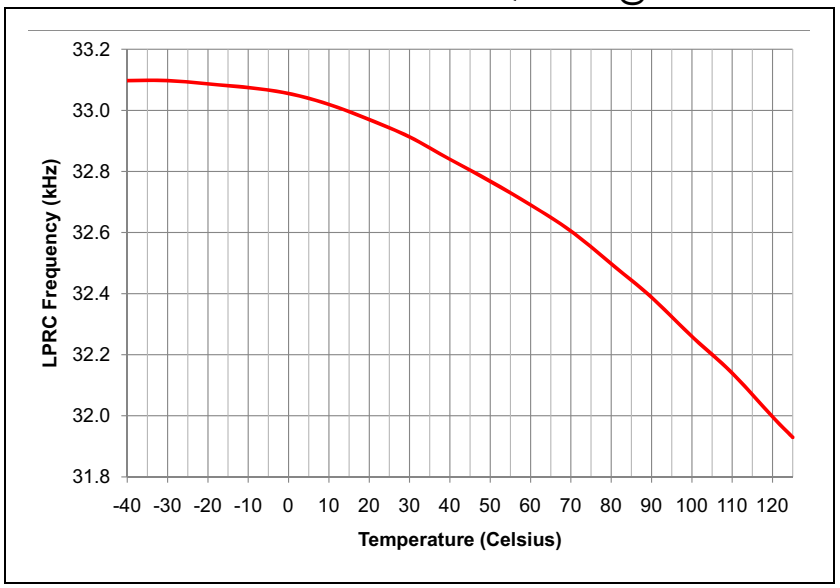



**FIGURE 33-10: TYPICAL LPRC FREQUENCY @ VDD = 3.3V**

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**NOTES:**


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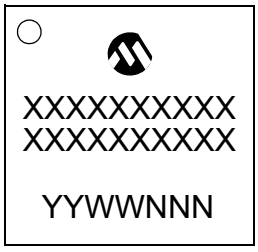
# 34.0 PACKAGING INFORMATION

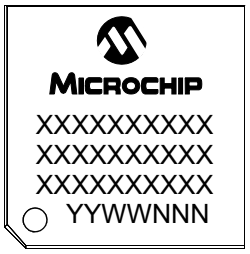
## 34.1 Package Marking Information

64-Lead QFN (9x9x0.9 mm)

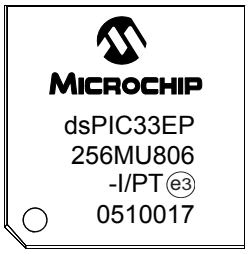



Example

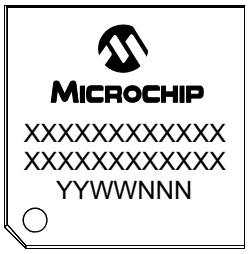
64-Lead TQFP (10x10x1 mm)



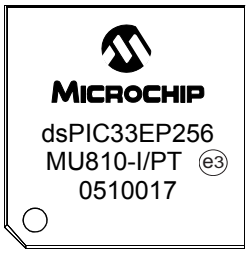

Example



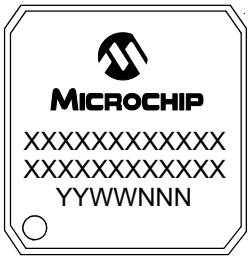

100-Lead TQFP (12x12x1 mm)




Example




100-Lead TQFP (14x14x1 mm)



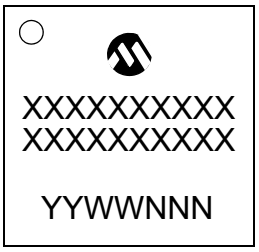

Example

| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

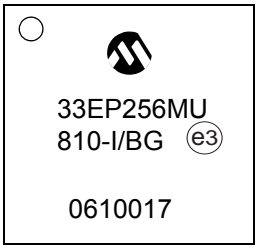
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 34.1 Package Marking Information (Continued)

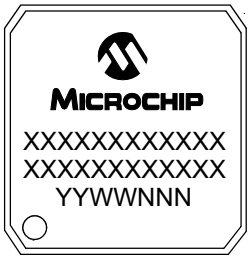
121-Lead TFBGA (10x10x1.2 mm)



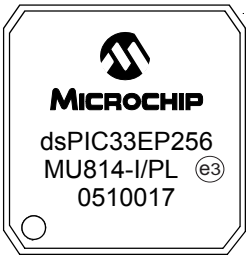

Example



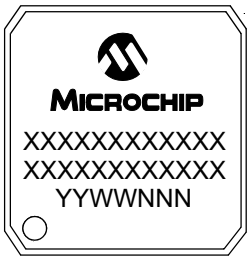

144-Lead LQFP (20x20x1.4 mm)



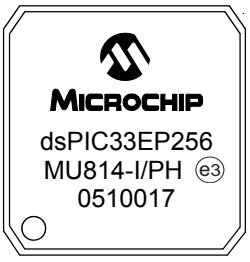

Example




144-Lead TQFP (16x16x1 mm)




Example





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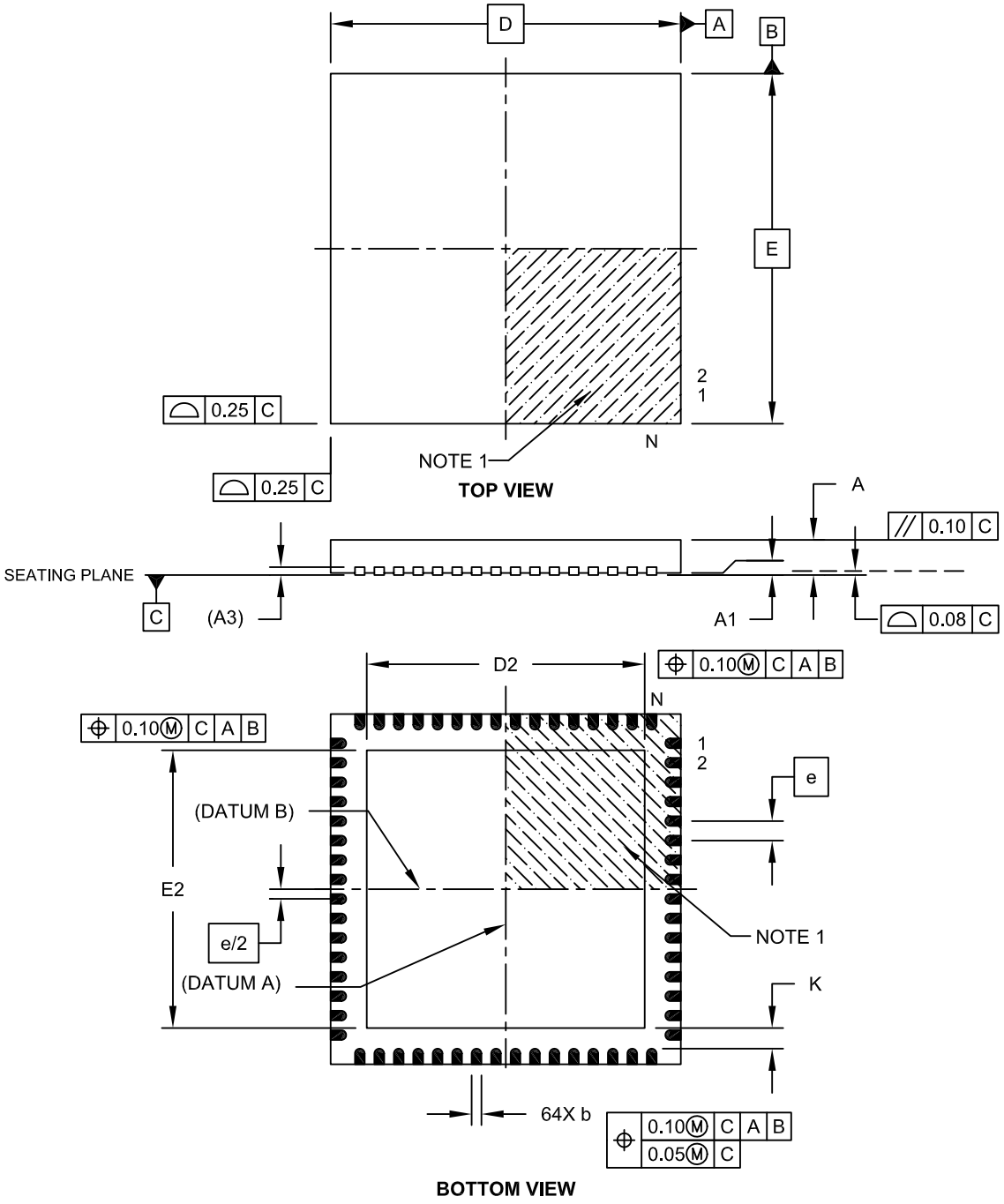
## 34.2 Package Details

### 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]

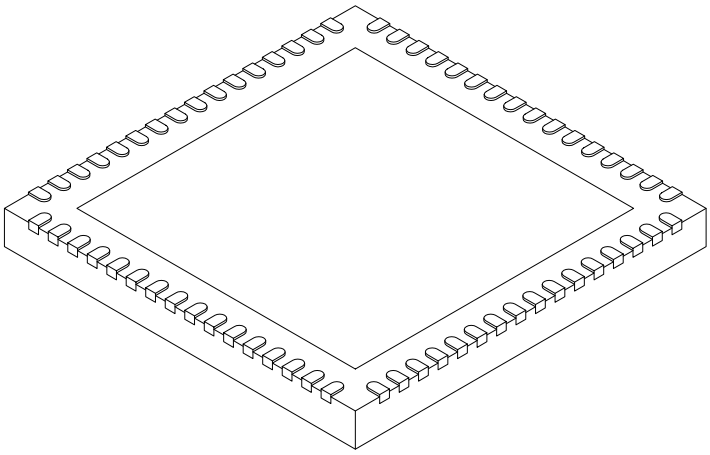
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-149C Sheet 1 of 2

## 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 64 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 9.00 BSC | |
| Exposed Pad Width | E2 | 7.05 | 7.15 | 7.50 |
| Overall Length | D | | 9.00 BSC | |
| Exposed Pad Length | D2 | 7.05 | 7.15 | 7.50 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149C Sheet 2 of 2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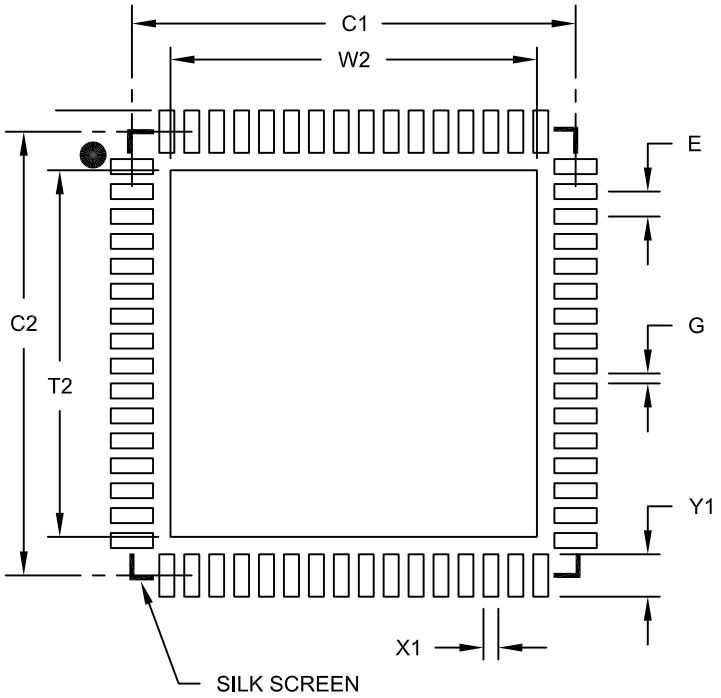
64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 7.35 |
| Optional Center Pad Length | T2 | | | 7.35 |
| Contact Pad Spacing | C1 | | 8.90 | |
| Contact Pad Spacing | C2 | | 8.90 | |
| Contact Pad Width (X64) | X1 | | | 0.30 |
| Contact Pad Length (X64) | Y1 | | | 0.85 |
| Distance Between Pads | G | 0.20 | | |

Notes:

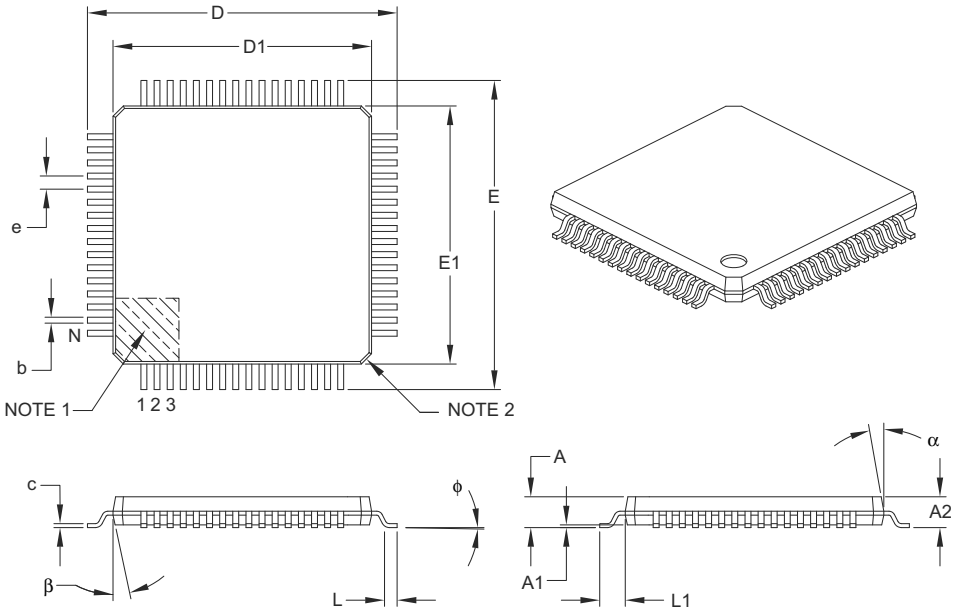
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A

## 64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 64 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 12.00 BSC | |
| Overall Length | D | | 12.00 BSC | |
| Molded Package Width | E1 | | 10.00 BSC | |
| Molded Package Length | D1 | | 10.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085B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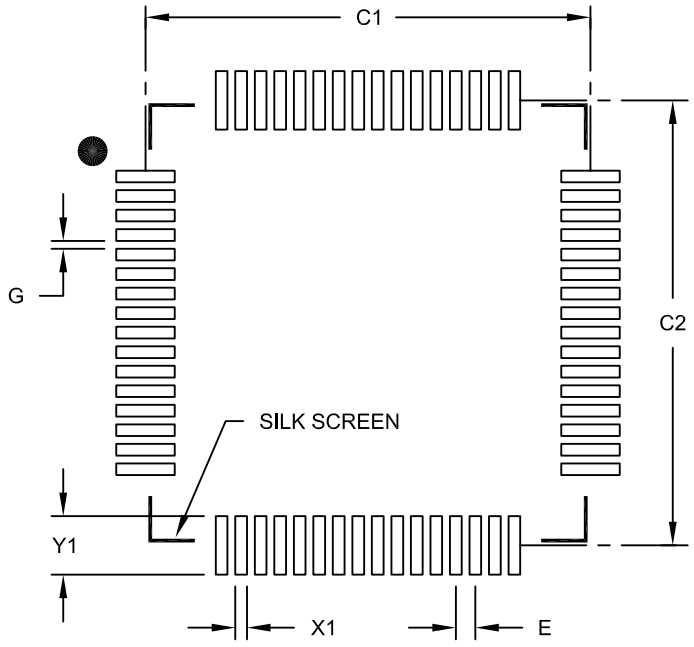
64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Contact Pad Spacing | C1 | | 11.40 | |
| Contact Pad Spacing | C2 | | 11.40 | |
| Contact Pad Width (X64) | X1 | | | 0.30 |
| Contact Pad Length (X64) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

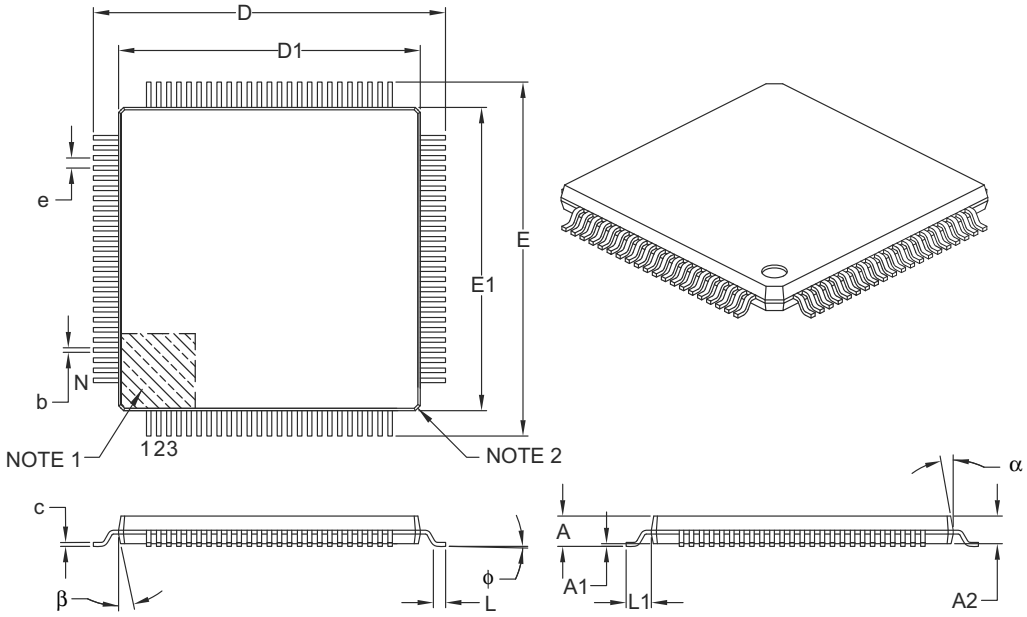
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

## 100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 100 | |
| Lead Pitch | e | | 0.40 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 14.00 BSC | |
| Overall Length | D | | 14.00 BSC | |
| Molded Package Width | E1 | | 12.00 BSC | |
| Molded Package Length | D1 | | 12.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.13 | 0.18 | 0.23 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B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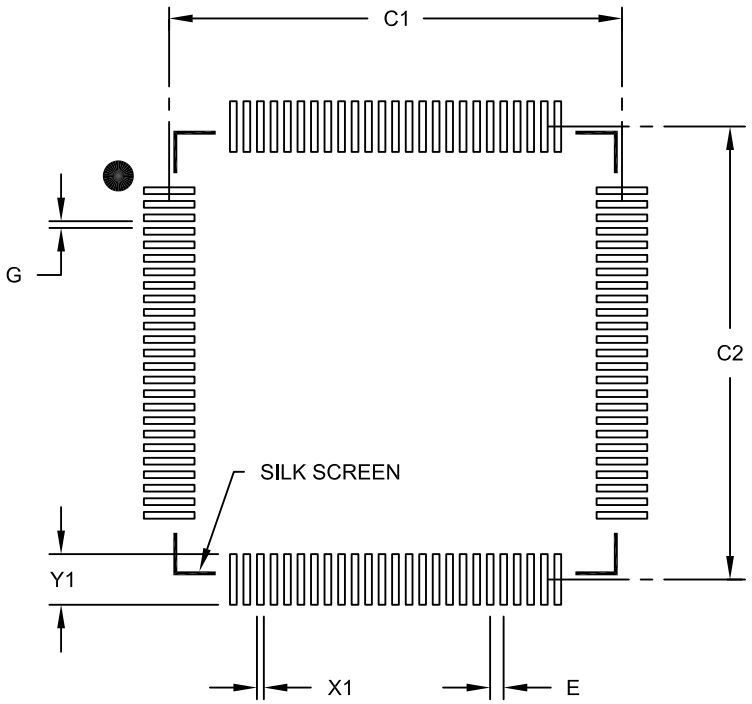
100-Lead Plastic Thin Quad Flatpack (PT)- 12x12x1mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.40 BSC | |
| Contact Pad Spacing | C1 | | 13.40 | |
| Contact Pad Spacing | C2 | | 13.40 | |
| Contact Pad Width (X100) | X1 | | | 0.20 |
| Contact Pad Length (X100) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

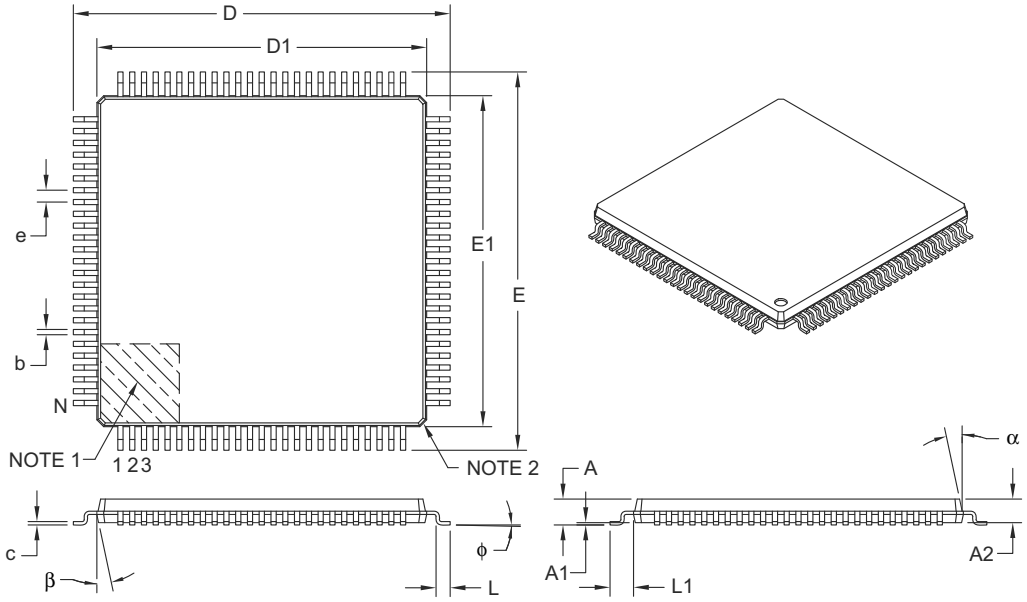
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B

## 100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 100 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 16.00 BSC | |
| Overall Length | D | | 16.00 BSC | |
| Molded Package Width | E1 | | 14.00 BSC | |
| Molded Package Length | D1 | | 14.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B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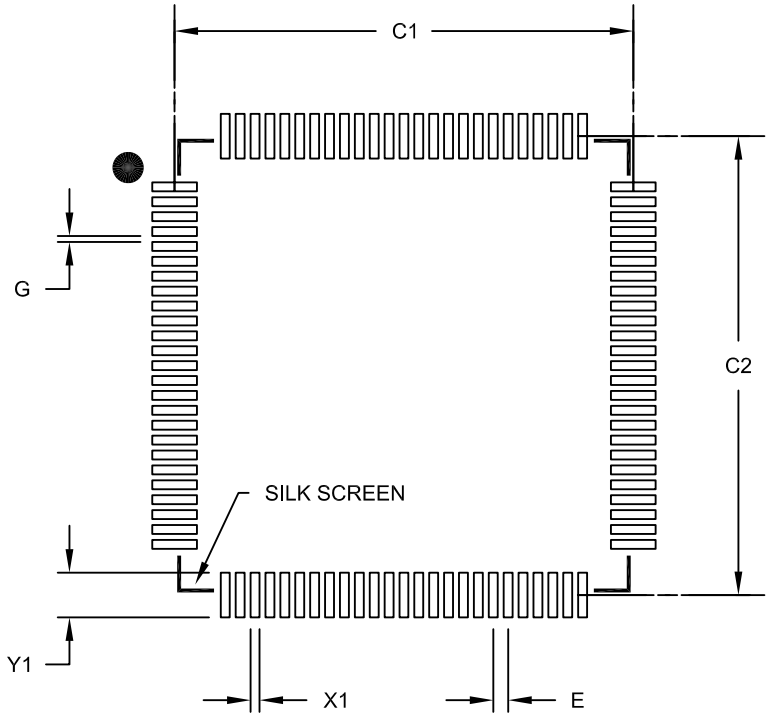
100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Contact Pad Spacing | C1 | | 15.40 | |
| Contact Pad Spacing | C2 | | 15.40 | |
| Contact Pad Width (X100) | X1 | | | 0.30 |
| Contact Pad Length (X100) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

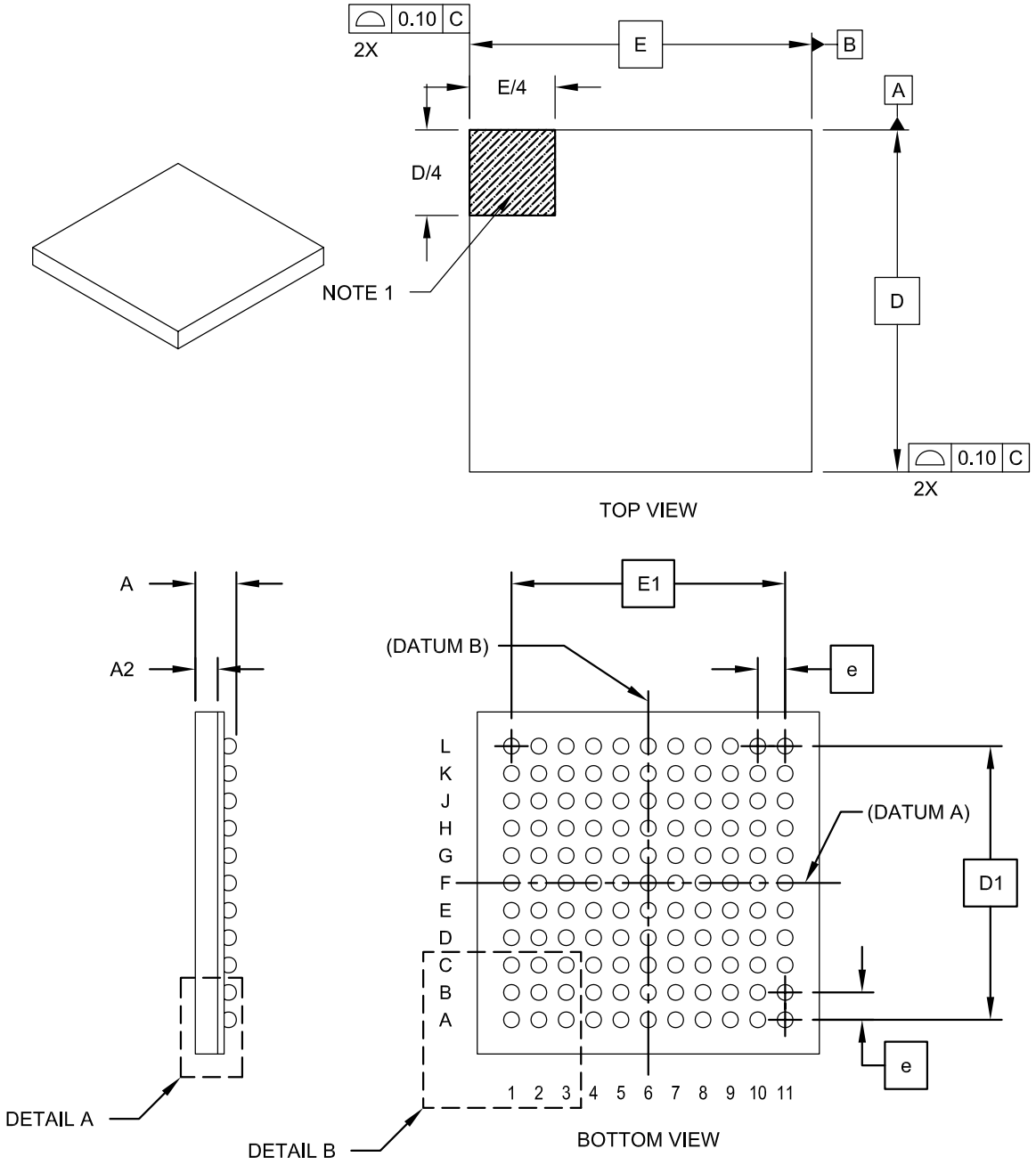
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B

## 121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA–Formerly XBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-148 Rev D Sheet 1 of 2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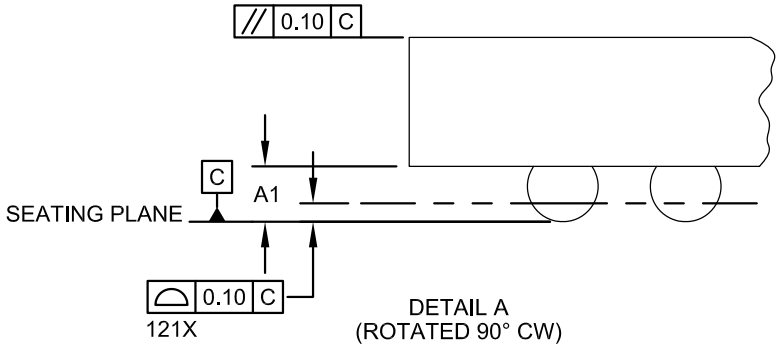
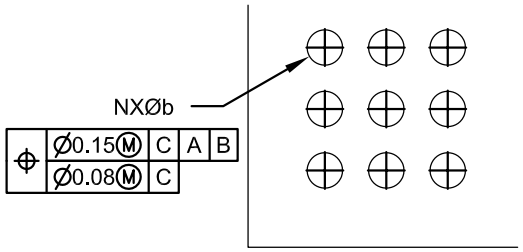
## 121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA–Formerly XBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




DETAIL B

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Contacts | N | | 121 | |
| Contact Pitch | e | | 0.80 BSC | |
| Overall Height | A | 1.00 | 1.10 | 1.20 |
| Standoff | A1 | 0.25 | 0.30 | 0.35 |
| Molded Package Thickness | A2 | 0.55 | 0.60 | 0.65 |
| Overall Width | E | | 10.00 BSC | |
| Array Width | E1 | | 8.00 BSC | |
| Overall Length | D | | 10.00 BSC | |
| Array Length | D1 | | 8.00 BSC | |
| Contact Diameter | b | | 0.40 TYP | |

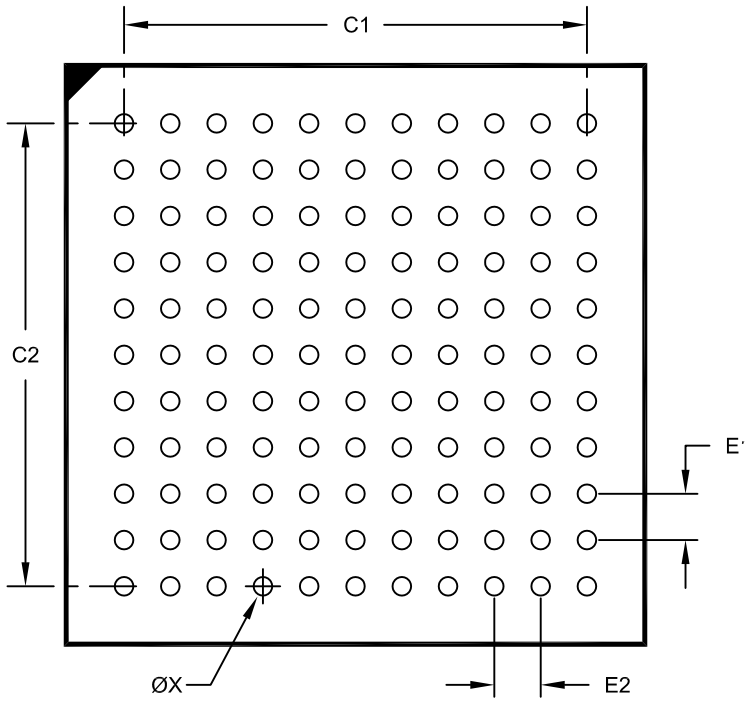
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
3. The outer rows and colums of balls are located with respect to datums A and B.

Microchip Technology Drawing C04-148 Rev D Sheet 2 of 2

## 121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA--Formerly XBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E1 | | 0.80 BSC | |
| Contact Pitch | E2 | | 0.80 BSC | |
| Contact Pad Spacing | C1 | | 8.00 | |
| Contact Pad Spacing | C2 | | 8.00 | |
| Contact Pad Diameter (X121) | X | | | 0.32 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2148 Rev D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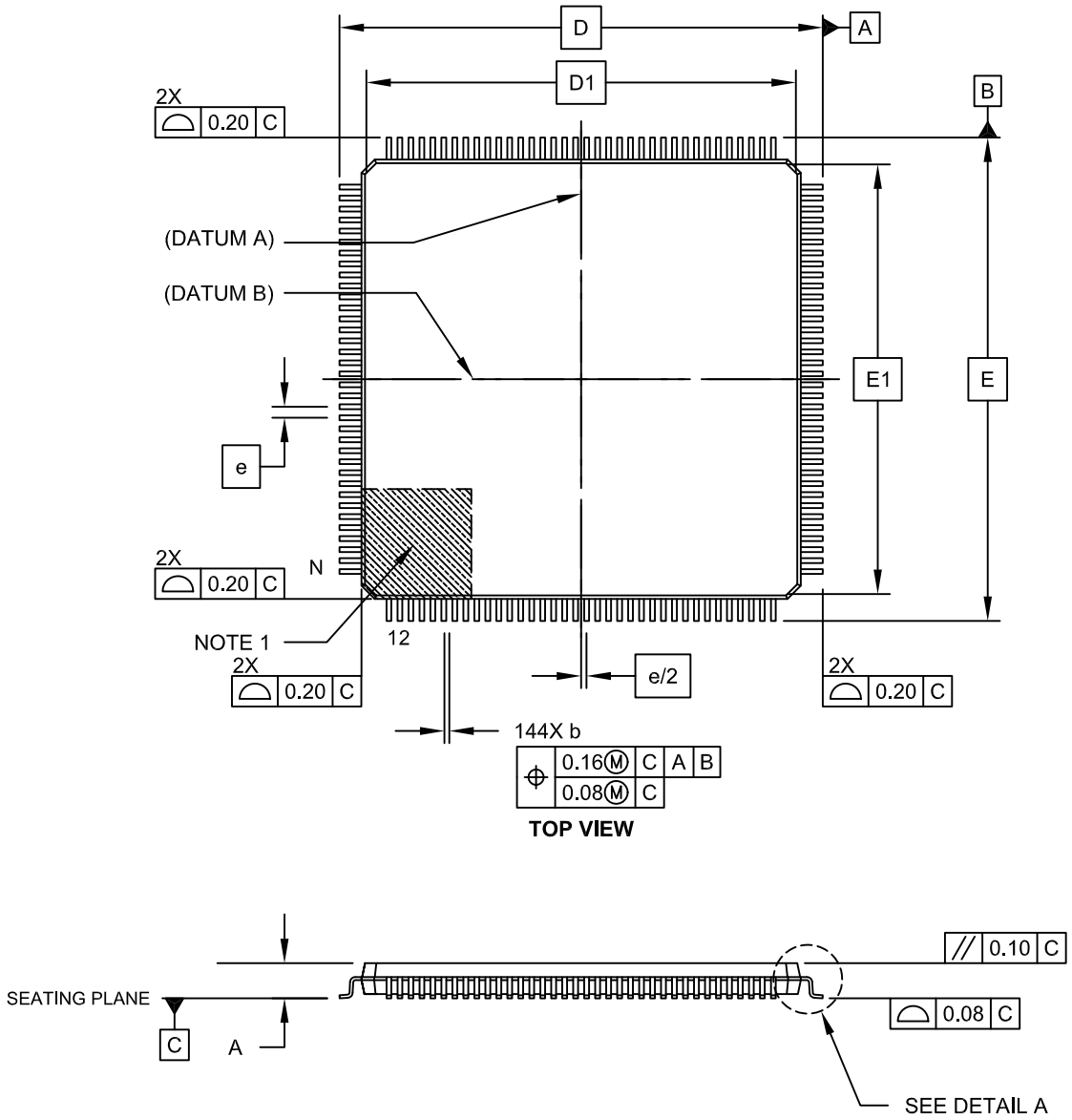
### 144-Lead Plastic Low Profile Quad Flatpack (PL) – 20x20x1.40 mm Body, with 2.00 mm Footprint [LQFP]

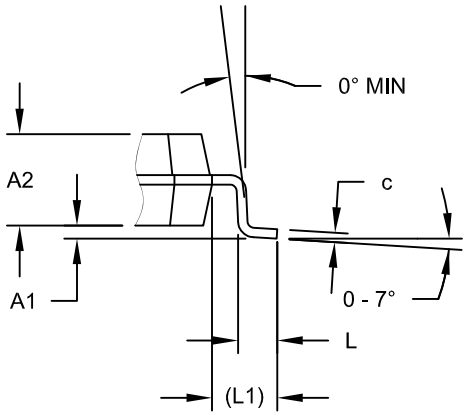
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



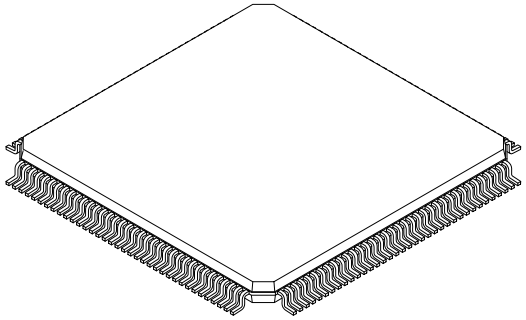

Microchip Technology Drawing C04-044B Sheet 1 of 2

## 144-Lead Plastic Low Profile Quad Flatpack (PL) – 20x20x1.40 mm Body, with 2.00 mm Footprint [LQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**DETAIL A**



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 144 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | - | - | 1.60 |
| Molded Package Height | A2 | 1.35 | 1.40 | 1.45 |
| Standoff | A1 | 0.05 | - | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 (REF) | |
| Overall Width | E | | 22.00 BSC | |
| Overall Length | D | | 22.00 BSC | |
| Molded Body Width | E1 | | 20.00 BSC | |
| Molded Body Length | D1 | | 20.00 BSC | |
| Lead Thickness | c | 0.09 | - | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-044B Sheet 2 of 2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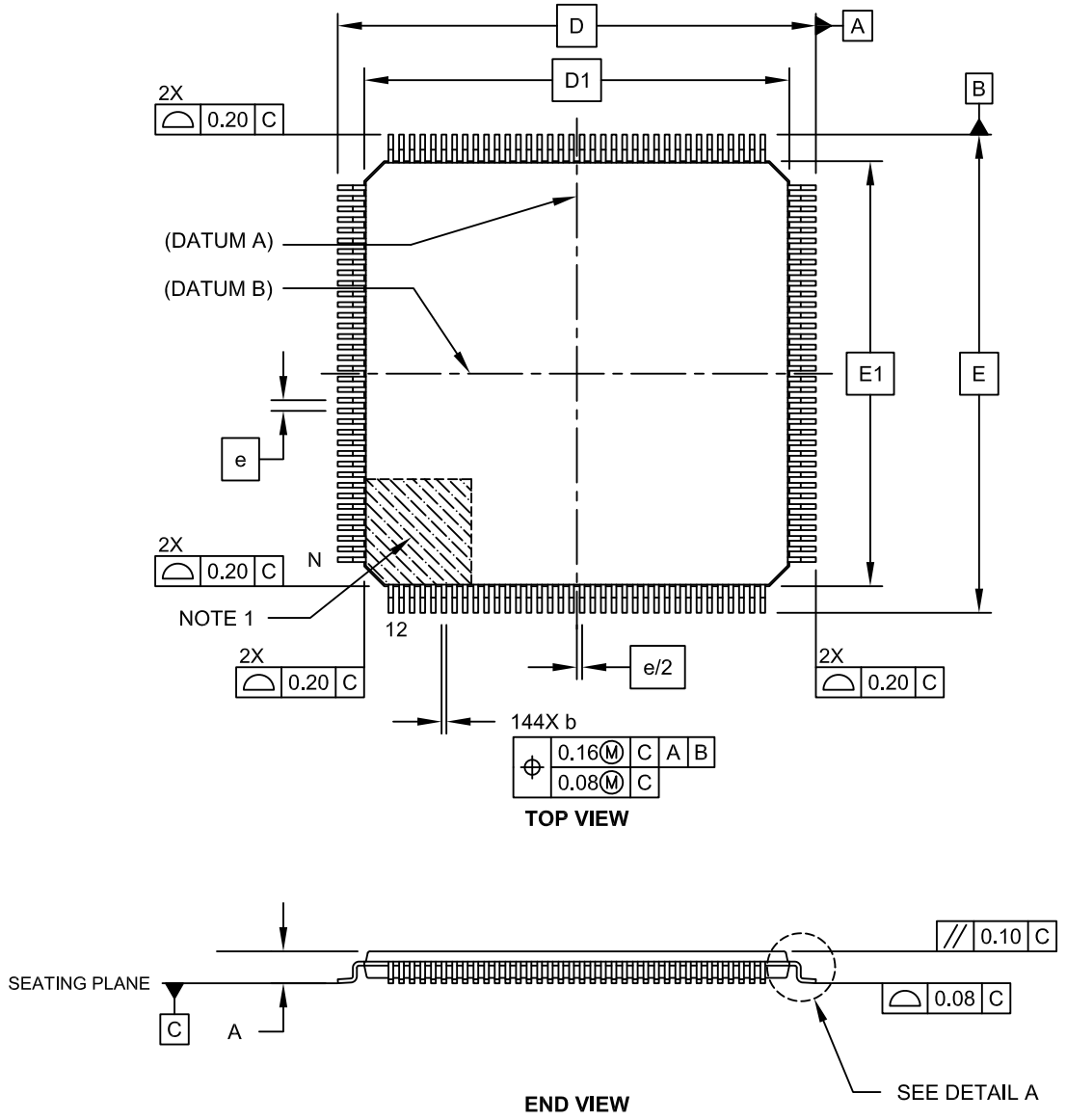
### 144-Lead Plastic Thin Quad Flatpack (PH)-16x16x1mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-155B Sheet 1 of 2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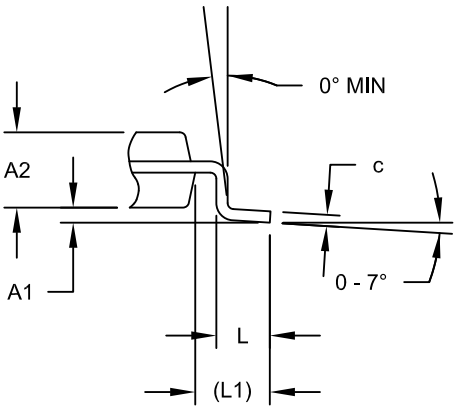
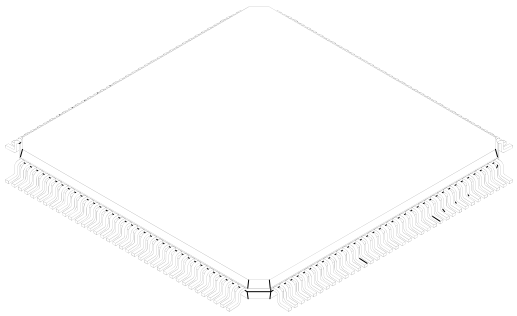
## 144-Lead Plastic Thin Quad Flatpack (PH)-16x16x1mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



**DETAIL A**

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 144 | |
| Lead Pitch | e | | 0.40 BSC | |
| Overall Height | A | - | - | 1.20 |
| Molded PackageThickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | - | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Overall Width | D | | 18.00 BSC | |
| Overall Length | E | | 18.00 BSC | |
| Molded Body Width | D1 | | 16.00 BSC | |
| Molded Body Length | E1 | | 16.00 BSC | |
| Lead Thickness | c | 0.09 | - | 0.20 |
| Lead Width | b | 0.13 | - | 0.23 |

**Notes:**

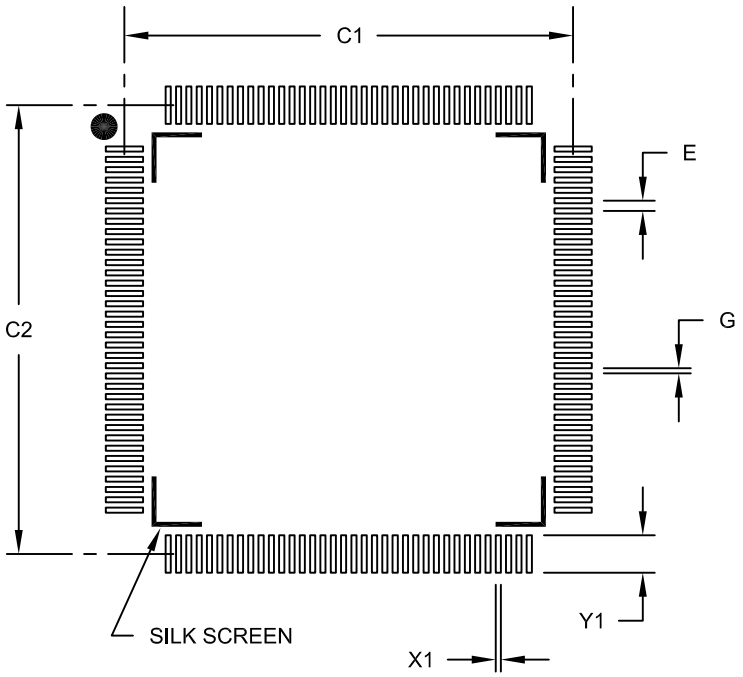
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-155B Sheet 2 of 2

144-Lead Plastic Thin Quad Flat Pack (PH) - 16x16 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.40 BSC | |
| Contact Pad Spacing | C1 | | 17.40 | |
| Contact Pad Spacing | C2 | | 17.40 | |
| Contact Pad Width (X144) | X1 | | | 0.20 |
| Contact Pad Length (X144) | Y1 | | | 1.45 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2155B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# APPENDIX A: REVISION HISTORY

## Revision A (December 2009)

This is the initial released version of this document.

## Revision B (July 2010)

This revision includes minor typographical and formatting changes throughout the data sheet text.

The major changes are referenced by their respective section in Table A-1.

**TABLE A-1: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"High-Performance, 16-bit Digital Signal Controllers and Microcontrollers"** | Removed reference to dual triggers for Motor Control Peripherals.<br>Relocated the VBUSST pin in all pin diagrams (see **"Pin Diagrams"**, Table 2 and Table 3).<br>Added SCK2, SDI2, SDO2 pins in pin location 4,5 and 6 respectively in 64-pin QFN.<br>Added SCK2, SDI2, SDO2 pins in pin location 4,5 and 6 respectively in 64-pin TQFP.<br>Added SCK2, SDI2, SDO2 pins in pin location 10,11 and 12 respectively in 100-pin TQFP.<br>Added SCK2, SDI2, SDO2 pins in Table 2 and Table 3.<br>Moved the RP30 pin to pin location 95, and the RP31 pin to pin location 96 in the 144-pin TQFP and 144-pin LQFP pin diagrams. |
| **Section 1.0 "Device Overview"** | Removed the SCL1 and SDA1 pins from the Pinout I/O Descriptions (see Table 1-1). |
| **Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"** | Removed Section 2.8 "Configuration of Analog and Digital Pins During ICSP Operations" |
| **Section 3.0 "CPU"** | Added Note 4 to the CPU Status Register (SR) in Register 3-1.<br>Added the VAR bit (CORCON<15>) to Register 3-2. |

**TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 4.0 "Memory Organization"** | Added the Write Latch and Auxiliary Interrupt Vector to the Program Memory Map (see Figure 4-1).<br><br>Updated the All Resets value for the DSRPAG and DSWPAG registers in the CPU Core Register Maps (see Table 4-1 and Table 4-2).<br><br>Updated the All Resets value for the INTCON2 register in the Interrupt Controller Register Maps (see Table 4-3 through Table 4-6).<br><br>Updated the All Resets values for all registers in the Output Compare 1 - Output Compare 16 Register Map, with the exception of the OCxTMR and OCxCON1 registers (see Table 4-9).<br><br>Removed the DTM bit (TRGCON1<7> from all PWM Generator # Register Maps (see Table 4-11 through Table 4-17).<br><br>Updated the All Resets value for the QEI1IOC register in the QEI1 Register Map (see Table 4-18).<br><br>Updated the All Resets value for the QEI2IOC register in the QEI1 Register Map (see Table 4-19).<br><br>Added Note 4 to the USB OTG Register Map (see Table 4-25)<br><br>Updated all addresses in the Real-Time Clock and Calendar Register Map (see Table 4-34).<br><br>Removed RPINR22 from Table 4-37 through Table 4-40.<br><br>Updated the All Resets values for all registers in the Peripheral Pin Select Input Register Maps and modified the RPIN37-RPINR43 registers (see Table 4-37 through Table 4-40).<br><br>Added the VREGSF bit (RCON<11>) to the System Control Register Map (see Table 4-43).<br><br>Added the REFOMD bit (PMD4<3>) to the PMD Register Maps (see Table 4-44 through Table 4-47).<br><br>Changed the bit range for CNT from <15:0> to <13:0> for all DMAxCNT registers in the DMAC Register Map (see Table 4-49).<br><br>Updated the All Resets value and removed the ANSC15 and ANSC12 bits in the ANSLEC registers in the PORTC Register Maps (see Table 4-52 and Table 4-53).<br><br>Updated DSxPAG and Page Description of O, Read and U, Read in Table 4-66.<br><br>Added Note to the Table 4-67.<br><br>Updated Arbiter Architecture in Figure 4-8.<br><br>Updated the Unimplemented value and removed the LATG3 and LATG2 bits in the LATG registers and the CNPUG3 and CNPUG2 bits from the CNPUG registers in the PORTG Register Maps (see Table 4-60 and Table 4-61)<br><br>Updated the All Resets value and removed the TRISG3 and TRISG2 bits in the TRISG registers and the ODCG3 and ODCG2 bits from the ODCG registers in the PORTG Register Maps (see Table 4-60 and Table 4-61). |
| **Section 5.0 "Flash Program Memory"** | Updated the NVMOP<3:0> = 1110 definition to Reserved and added Note 6 to the Nonvolatile Memory (NVM) Control Register (see Register 5-1). |
| **Section 6.0 "Resets"** | Added the VREGSF bit (RCON<11>) to the Reset Control Register (see Register 6-1). |


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**TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 7.0 "Interrupt Controller"** | Added the VAR bit (CORCON<15>) to the Core Control Register (see Register 7-2)<br><br>Changed the default POR value for the GIE bit (INTCON2<15) to R/W-1 (see Register 7-4).<br><br>Changed the VECNUM<7:0> = 11111111 pending interrupt vector number to 263 in the Interrupt Control and Status Register (see Register 7-7). |
| **Section 8.0 "Direct Memory Access (DMA)"** | Updated **Section 8.1 "DMAC Registers"**.<br><br>Updated DMA Controller in Figure 8-1.<br><br>Added Note 1 to the DMA Channel x Peripheral Address Register (see Register 8-7).<br><br>Added Note 1 and Note 2 to the DMA Channel x Transfer Count Register (see Register 8-8).<br><br>Updated all RQCOLx bit definitions, changing Peripheral Write to Transfer Request in the DMA Request Collision Status Register (see Register 8-12). |
| **Section 9.0 "Oscillator Configuration"** | Added the Reference Oscillator Control Register (see Register 9-7).<br><br>Added Note 3 and 4 to the CLKDIV Register (see Register 9-2) |
| **Section 10.0 "Power-Saving Features"** | Added the DCIMD and C2MD bits to the Peripheral Module Disable Control Register 1 (see Register 10-1)<br><br>Added the IC6MD, IC5MD, IC4MD, IC3MD, OC8MD, OC7MD, OC6MD, and OC5MD bits to the Peripheral Module Disable Control Register 2 (see Register 10-2)<br><br>Added the T9MD, T8MD, T7MD, and T6MD bits and removed the DSC1MD bit in the Peripheral Module Disable Control Register 3 (see Register 10-3).<br><br>Added the REFOMD bit (PMD4<3>) to the Peripheral Module Disable Control Register 4 (see Register 10-4). |
| **Section 11.0 "I/O Ports"** | Updated the first paragraph of **Section 11.2 "Configuring Analog and Digital Port Pins"**.<br><br>Updated the PWM Fault, Dead-Time Compensation, and Synch Input register numbers of the Selectable Input Sources (see Table 11-2).<br><br>Removed RPINR22 register.<br><br>Bit names and definitions were modified in the following registers:<br>• Peripheral Pin Select Input Register 37 (see Register 11-37)<br>• Peripheral Pin Select Input Register 38 (see Register 11-38)<br>• Peripheral Pin Select Input Register 39 (see Register 11-39)<br>• Peripheral Pin Select Input Register 40 (see Register 11-40)<br>• Peripheral Pin Select Input Register 41 (see Register 11-41)<br>• Peripheral Pin Select Input Register 42 (see Register 11-42)<br>• Peripheral Pin Select Input Register 43 (see Register 11-43) |
| **Section 12.0 "Timer1"** | Added Note in Register 12-1. |
| **Section 14.0 "Input Capture"** | Added Note 1 to the Input Capture Block Diagram (see Figure 14-1). |
| **Section 15.0 "Output Compare"** | Added Note 1 to the Output Compare Module Block Diagram (see Figure 15-1).<br><br>Added Note 2 to the Output Compare x Control Register 2 (see Register 15-2). |
| **Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMU806/810/814 Devices Only)"** | Added Comparator bit values for the CLSRC<4:0> and FLTSRC<4:0> bits in the PWM Fault Current-Limit Control Register (see Register 16-21). |

**TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMU806/810/814 Devices Only)"** | Reordered the bit values for the OUTFNC<1:0> bits and updated the default POR bit value to 'x' for the HOME, INDEX, QEB, and QEA bits in the QEI I/O Control Register (see Register 17-2). |
| **Section 23.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"** | Updated VREFL in the ADC1 and ADC2 Module Block Diagram (see Figure 23-1). |
| **Section 25.0 "Comparator Module"** | Added Note 1 to the Comparator I/O Operating Modes (see Figure 25-1).<br>Removed the CLPWR bit (CMxCON<12>) (see Register 25-2). |
| **Section 29.0 "Special Features"** | Added a new first paragraph to **Section 29.1 "Configuration Bits"** |
| **Section 30.0 "Instruction Set Summary"** | The following instructions have been updated (see Table 30-2):<br>• BRA<br>• CALL<br>• CPBEQ<br>• CPBGT<br>• CPBLT<br>• CPBNE<br>• GOTO<br>• MOVPAG<br>• MUL<br>• RCALL<br>• RETFIE<br>• RETLW<br>• RETURN<br>• TBLRDH<br>• TBLRDL |
| **Section 32.0 "Electrical Characteristics"** | Updated the Typical and Maximum values for DC Characteristics: Operating Current (IDD) (see Table 32-5).<br>Updated the Typical and Maximum values for DC Characteristics: Idle Current (IIDLE) (see Table 32-6).<br>Updated the Maximum values for DC Characteristics: Power-down Current (IPD) (see Table 32-7).<br>Updated the Maximum values for DC Characteristics: Doze Current (IDOZE) (see Table 32-8).<br>Updated the parameter numbers for Internal FRC Accuracy (see Table 32-19).<br>Updated the parameter numbers and the Typical value for parameter F21b for Internal RC Accuracy (see Table 32-20).<br>Updated the Minimum value for PM6 and the Typical and Maximum values for PM7 in Parallel Master Port Read Requirements (see Table 32-52).<br>Added DMA Module Timing Requirements (see Table 32-54). |


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## Revision C (May 2011)

This revision includes minor typographical and formatting changes throughout the data sheet text.

These global changes were implemented:

- All instances of VDDCORE have been removed.
- References to remappable pins have been updated to clarify output-only pins (RPn) versus input/output pins (RPIn).
- The minimum VDD value was changed from 2.7V to 3.0V to adhere to the current BOR specification.

The major changes are referenced by their respective section in Table A-2.

**TABLE A-2: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **High-Performance, 16-bit Digital Signal Controllers and Microcontrollers** | Removed the shading for D+/RG2 and D-/RG3 pin designations in all pin diagrams, as these pins are not 5V tolerant.<br><br>References to remappable pins have been updated to clarify input/output pins (RPn) and input-only pins (RPIn). |
| **Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"** | Add information on the VUSB pin in **Section 2.1 "Basic Connection Requirements"**.<br><br>Updated the title of Section 2.3 to **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"** and modified the first paragraph. |
| **Section 3.0 "CPU"** | Added Note 2 to the Programmer's Model Register Descriptions (see Table 3-1). |
| **Section 4.0 "Memory Organization"** | Added the CANCKS bit (CxCTRL1<11>) to the ECAN1 and ECAN 2 Register Maps (see Table 4-26 and Table 4-29).<br><br>Added the SBOREN bit (RCON<13>) to the System Control Register Map (see Table 4-43).<br><br>Added Note 1 to the PORTG Register maps (see Table 4-60 and Table 4-61).<br><br>Updated the Page Description for DSRPAG = 0x1FF and DSRPAG = 0x200 in Table 4-66.<br><br>Updated the second paragraph of **Section 4.2.9 "EDS Arbitration and Bus Master Priority"**.<br><br>Updated the last note box in **Section 4.2.10 "Software Stack"**. |
| **Section 5.0 "Flash Program Memory"** | Updated the equation formatting in **Section 5.3 "Programming Operations"**.<br><br>Added the Non-Volatile Memory Upper Address (NVMADRU) and Non-Volatile Memory Address (NVMADR) registers (see Register 5-2 and Register 5-3). |
| **Section 6.0 "Resets"** | Added Security Reset to the Reset System Block Diagram (see Figure 6-1).<br><br>Added the SBOREN bit (RCON<13>) and Notes 3 and 4 to the Reset Control register (see Register 6-1). |
| **Section 11.0 "I/O Ports"** | References to remappable pins have been updated to clarify input/output pins (RPn) and input-only pins (RPIn).<br><br>Added the new column, Input/Output, to Input Pin Selection for Selectable Input Sources (see Table 11-2). |
| **Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMU806/810/814 Devices Only)"** | Updated the definition for the INTHLD<31:0> bits (see Register 17-19 and Register 17-20). |

**TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 21.0 "Enhanced CAN (ECAN™) Module"** | Added the CANCKS bit to the ECAN Control Register 1 (CiCTRL1) (see Register 21-1). |
| **Section 22.0 "USB On-The-Go (OTG) Module"** | Removed the USB 3.3V Regulator logic from the USB Interface Diagram (see Figure 22-1). |
| **Section 23.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"** | Updated the ADC Conversion Clock Period Block Diagram (see Figure 23-2). |
| **Section 29.0 "Special Features"** | Updated the last paragraph of **Section 29.1 "Configuration Bits"**<br>Added a note box after the last paragraph of **Section 29.3 "BOR: Brown-out Reset (BOR)"**.<br>Added the RTSP Effect column to the Configuration Bits Description (see Table 29-2). |
| **Section 30.0 "Instruction Set Summary"** | Updated all Status Flags Affected to None for the MOV instruction and added Note 2 (see Table 30-2). |
| **Section 32.0 "Electrical Characteristics"** | Updated the Absolute Maximum Ratings (see page 457).<br>Added Note 1 to the Operating MIPS vs. Voltage (see Table 32-1).<br>Added parameter DI31 (ICNPD) to the I/O Pin Input Specifications (see Table 32-9).<br>Updated the Minimum value for parameter DO26 in the I/O Pin Output Specifications (see Table 32-10).<br>Updated the Minimum value for parameter D132b and the Minimum and Maximum values for parameters D136a, D136b, D137a, D137b, D138a, and D138b in the Program Memory specification (see Table 32-12).<br>Updated the Minimum, Typical, and Maximum values for parameter OS10 (Oscillator Crystal Frequency: SOSC) in the External Clock Timing Requirements (see Table 32-16).<br>Added Note 2 to the PLL Clock Timing Specifications (see Table 32-17).<br>Updated all Timer1 External Clock Timing Requirements (see Table 32-23).<br>Replaced Table 32-34 with Timer2, Timer4, Timer6, Timer8 External Clock Timing Requirements and Timer3, Timer5, Timer7, Timer9 External Clock Timing Requirements (see Table 32-24 and Table 32-25, respectively).<br>Updated the Maximum value for parameter OC15 and the Minimum value for parameter OC20 in the OC/PWM Mode Timing Requirements (see Table 32-29).<br>Updated the Operating Temperature in the ECAN Module I/O Timing Requirements and USB OTG Timing Requirements (see Table 32-51 and Table 32-53, respectively).<br>Updated all SPI specifications (see Figure 32-15 through Figure 32-30 and Table 32-33 through Table 32-48).<br>Removed Note 4 from the DCI Module Timing Requirements (see Table 32-59).<br>Updated the Standard Operating Conditions voltage for the Comparator Specifications (see Table 32-61 through Table 32-64). |


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## Revision D (August 2011)

This revision includes minor typographical and formatting changes throughout the data sheet text.

The Data Converter Interface (DCI) module is available on all dsPIC33EPXXX(GP/MC/MU)806/810/814 and PIC24EPXXX(GP/GU)810/814 devices. References throughout the document have been updated accordingly.

The following pin name changes were implemented throughout the document:

- C1INA renamed to C1IN1+
- C1INB renamed to C1IN2-
- C1INC renamed to C1IN1-
- C1IND renamed to C1IN3-
- C2INA renamed to C2IN1+
- C2INB renamed to C2IN2-
- C2INC renamed to C2IN1-
- C2IND renamed to C2IN3-
- C3INA renamed to C3IN1+
- C3INB renamed to C3IN2-
- C3INC renamed to C3IN1-
- C3IND renamed to C3IN3-

The other major changes are referenced by their respective section in Table A-3.

**TABLE A-3: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **Section 1.0 "Device Overview"** | Added **Section 1.1 "Referenced Sources"**. |
| **Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"** | Updated the Note in **Section 2.1 "Basic Connection Requirements"**. |
| **Section 3.0 "CPU"** | Updated **Section 3.1 "Registers"**. |
| **Section 4.0 "Memory Organization"** | Updated **FIGURE 4-3: "Data Memory Map for dsPIC33EP512MU810/814 Devices with 52 KB RAM"** and **FIGURE 4-5: "Data Memory Map for dsPIC33EP256MU806/810/814 Devices with 28 KB RAM"**.<br><br>Updated the IFS3, IEC3, IPC14, and IPC15 SFRs in the Interrupt Controller Register Map (see Table 4-6).<br><br>Updated the SMPI bits for the AD1CON2 and AD2CON2 SFRs in the ADC1 and ADC2 Register Map (see Table 4-23).<br><br>Updated the All Resets values for the CLKDIV and PLLFBD SFRs and removed the SBOREN bit in the System Control Register Map (see Table 4-43). |
| **Section 6.0 "Resets"** | Removed the SBOREN bit and Notes 3 and 4 from the Reset Control Register (see Register 6-1). |
| **Section 8.0 "Direct Memory Access (DMA)"** | Removed Note 2 from the DMA Channel x IRQ Select Register (see Register 8-2). |
| **Section 9.0 "Oscillator Configuration"** | Updated the PLL Block Diagram (see Figure 9-2).<br><br>Updated the value at PORT and the default designations for the DOZE<2:0>, FRCDIV<2:0>, and PLLPOST<1:0> bits in the Clock Divisor Register and the PLLDIV<8:0> bits in the PLLFBD register (see Register 9-2 and Register 9-3). |
| **Section 23.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"** | Added Note 4 and updated the ADC Buffer names in the ADCx Module Block Diagram (see Figure 23-1).<br><br>Added Note 3 to the ADCx Control Register 1 (see Register 23-1).<br><br>Added the new ADC2 Control Register 2 (see Register 23-3).<br><br>Updated the SMPI<4:0> bit value definitions in the ADC1 Control Register 2 (see Register 23-2). |

**TABLE A-3: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 25.0 "Comparator Module"** | Updated the Comparator I/O Operating Modes diagram (see Figure 25-1).<br><br>Added Note 2 to the Comparator Voltage Reference Control Register (see Register 25-6). |
| **Section 29.0 "Special Features"** | Added Note 3 to the Connections for the On-chip Voltage Regulator (see Figure 29-1). |
| **Section 32.0 "Electrical Characteristics"** | Removed the Voltage on VCAP with respect to VSS from the Absolute Maximum Ratings(1).<br><br>Removed Note 3 and parameter DC18 from the DC Temperature and Voltage Specifications (see Table 32-4).<br><br>Updated the notes in the DC Characteristics: Operating Current (IDD) (see Table 32-5).<br><br>Updated the notes in the DC Characteristics: Idle Current (IIDLE) (see Table 32-6).<br><br>Updated the Typical and Maximum values for parameter DC60c and the notes in the DC Characteristics: Power-down Current (IPD) (see Table 32-7).<br><br>Updated the notes in the DC Characteristics: Doze Current (IDOZE) (see Table 32-8).<br><br>Updated the conditions for parameters DI60a and DI60b (see Table 32-9).<br><br>Updated the conditions for parameter BO10 in the BOR Electrical Characteristics (see Table 32-10).<br><br>Added Note 1 to the Internal Voltage Regulator Specifications (see Table 32-13).<br><br>Updated the Minimum and Maximum values for parameter OS53 in the PLL Clock Timing Specifications (see Table 32-17).<br><br>Updated the Minimum and Maximum values for parameter F21b in the Internal LPRC Accuracy specifications (see Table 32-20).<br><br>Added Note 2 to the ADC Module Specifications (see Table 32-54). |


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## Revision E (August 2011)

This revision includes the following updates to **Section 32.0 "Electrical Characteristics"**:

- The maximum HS value for parameter OS10 was updated (see Table 32-16)
- The OC/PWM Module Timing Characteristics for OCx were updated (see Figure 32-10)
- The Maximum Data Rate values were updated for the SPI1, SPI3, and SPI4 Maximum Data/Clock Rate Summary (see Table 32-33)
- These SPI1, SPI3, and SPI4 Timing Requirements were updated:
  - Maximum value for parameter SP10 and the minimum clock period value for SCKx in Note 3 (see Table 32-34, Table 32-35, and Table 32-36)
  - Maximum value for parameter SP70 and the minimum clock period value for SCKx in Note 3 (see Table 32-38 and Table 32-40)
- The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 32-41)
- These SPI2 Timing Requirements were updated:
  - Maximum value for parameter SP10 and the minimum clock period value for SCKx in Note 3 (see Table 32-42, Table 32-43, and Table 32-44)
  - Maximum value for parameter SP70 and the minimum clock period value for SCKx in Note 3 (see Table 32-45 through Table 32-48)
  - Minimum value for parameters SP40 and SP41 see Table 32-43 through Table 32-48)
- These ADC Module Specifications were updated (see Table 32-54):
  - Minimum value for parameter AD05
  - Maximum value for parameter AD06
  - Minimum value for parameter AD07

## Revision F (February 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

Throughout the document, references to the package formerly known as XBGA where changed to TFBGA.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see **Section 18.1 "SPI Helpful Tips"** and **Section 18.2 "SPI Resources"**. The major changes are referenced by their respective section in Table A-4.

**TABLE A-4: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"16-Bit Microcontrollers and Digital Signal Controllers with High-Speed PWM, USB and Advanced Analog"** | The content on the first page of this section was extensively reworked to provide the reader with the key features and functionality of this device family in an "at-a-glance" format.<br>The following devices were added to the Controller Families table (see Table 1 and the **"Pin Diagrams"** section):<br>• dsPIC33EP512MC806<br>• dsPIC33EP512GP806<br>• PIC24EP512GP806 |
| **Section 2.0 "Guidelines for Getting Started with 16-Bit Digital Signal Controllers and Microcontrollers"** | Added **Section 2.9 "Application Examples"** |
| **Section 3.0 "CPU"** | Updated the Status Register information in the Programmer's Model (see Figure 3-2). |
| **Section 4.0 "Memory Organization"** | Added Interrupt Controller Register Maps (see Table 4-6 and Table 4-7).<br>Added Peripheral Pin Select Output Register Map (see Table 4-39).<br>Added PMD Register Maps (see Table 4-50 and Table 4-51).<br>Added PORTF Register Map (see Table 4-64).<br>Added PORTG Register Map (see Table 4-67).<br>Updated the second note in **Section 4.7 "Bit-Reversed Addressing (dsPIC33EPXXXMU806/810/814 Devices Only)"**. |
| **Section 11.0 "I/O Ports"** | Added RPOR10: Peripheral Pin Select Output Register 10 (see Register 11-54). |
| **Section 14.0 "Input Capture"** | Updated the Input Capture Module Block Diagram (see Figure 14-1). |
| **Section 15.0 "Output Compare"** | Updated the Output Compare Module Block Diagram (see Figure 15-1). |
| **Section 25.0 "Comparator Module"** | Updated the User-programmable Blanking Function Block Diagram (see Figure 25-3).<br>Updated the bit definitions in the Comparator Mask Gating Control Register (see Register 25-4). |
| **Section 29.0 "Special Features"** | Added Note 3 to the Configuration Bits Description (see Table 29-2). |
| **Section 32.0 "Electrical Characteristics"** | Updated the I/O pin Absolute Maximum Ratings.<br>Updated Note 1 in the DC Characteristics: Operating Current (see Table 32-5).<br>Updated Note 1 in the DC Characteristics: Idle Current (see Table 32-6).<br>Updated Note 1 in the DC Characteristics: Power-down Current (see Table 32-7).<br>Updated Note 1 in the DC Characteristics: Doze Current (see Table 32-8).<br>Removed parameters DO16 and DO26, added parameter DO26a, updated parameters DO10 and DO20, and added Note 1 in the DC Characteristics: I/O Pin Output Specifications (see Table 32-10). |


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### Revision G (October 2012)

This revision includes updates to the packaging diagrams in **Section 34.0 "Packaging Information"**. Preliminary has been removed and there are minor text edits throughout the document.

**NOTES:**


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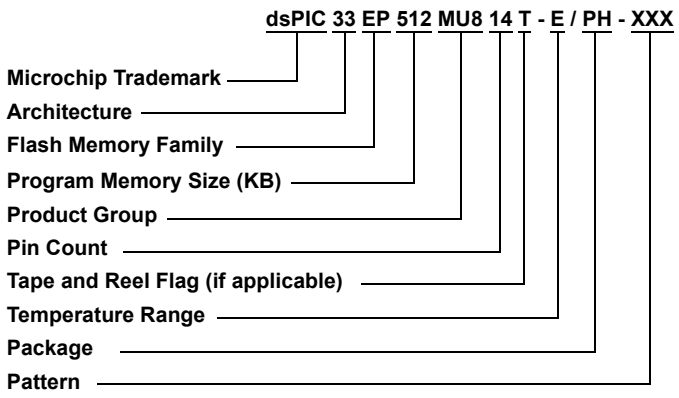


| | | | |
|---|---|---|---|
| **Architecture:** | 33 | = | 16-bit Digital Signal Controller |
| | 24 | = | 16-bit Microcontroller |
| **Flash Memory Family:** | EP | = | Enhanced Performance |
| **Product Group:** | MU8 | = | Motor Control family with USB |
| | GU8 | = | General Purpose family with USB |
| **Pin Count:** | 06 | = | 64-pin |
| | 10 | = | 100-pin, 121-pin |
| | 14 | = | 144-pin |
| **Temperature Range:** | I | = | -40°C to+85°C (Industrial) |
| | E | = | -40°C to+125°C (Extended) |
| **Package:** | PT | = | 10x10 or 12x12 mm TQFP (Thin Quad Flatpack) |
| | PF | = | 14x14 mm TQFP (Thin Quad Flatpack) |
| | MR | = | 9x9 mm QFN (Plastic Quad Flatpack) |
| | BG | = | 10x10 mm TFBGA (Plastic Thin Profile Ball Grid Array ) |
| | PH | = | 16x16 mm TQFP (Thin Quad Flatpack) |
| | PL | = | 20x20 mm LQFP (Low-Profile Quad Flatpack) |

**Examples:**

a) dsPIC33EP512MU814T-E/PH:
Motor Control with USB dsPIC33,
512 KB program memory, 144-pin,
Extended temperature, TQFP package.

**NOTES:**


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