RoHS compliant

Features

- 8 or 12 high current outputs
- R_{ON} = 1.5Ω (typ.) I_{MAX} = 350mA
- Outputs combinable for higher loads
- Digital voltage range VDD 3.3V or 5.0V
- Low standby current < 1µA @50°C
- Low output leakage < 5µA @13V, RT
- SPI interface with diagnostics
- Open load detection
- Short circuit limitation, - detection
- Output clamping for inductive loads typ. >40V
- Thermal overload protection
- -40°C to +125°C operation temperature (QFN)

Applications

- Stepper Motor Driver with Stall Detection
- DC Motor Driver with PWM
- Relay Driver with VBAT- automatically PWM
- LED Driver with 3 logarithmic PWM sources
- Switch Monitoring with pulsed current check and control lamp
- Switch Monitoring with control lamp

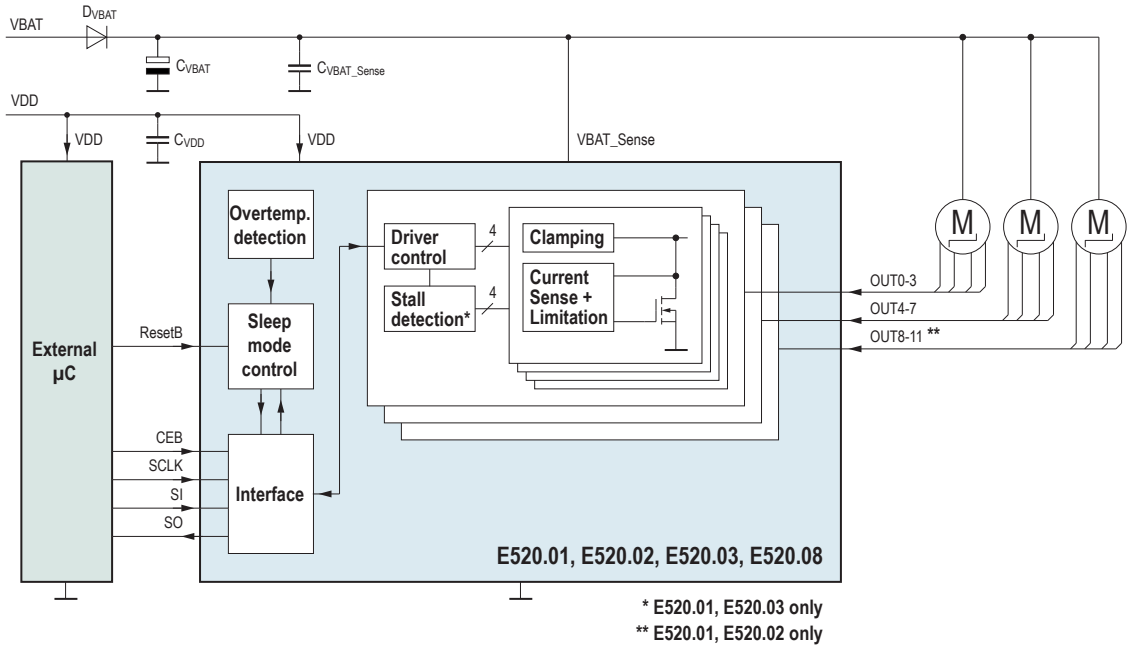
General Description

The IC drives 2 or 3 unipolar stepper motors and provides an optional stall detection for end position detection. For LED dimming a quasi logarithmic duty cycle is following the physiology of the human eye. With 3 PWM sources color LEDs can be driven in 3-color LED mode (245Hz PWM). The Relay PWM mode automatically adjusts the PWM to an effective supply voltage of typ. 11V. All outputs are short circuit and over-temperature protected with error read back capability. Switch monitoring with control lamp combination with only 1 wire and output is possible.

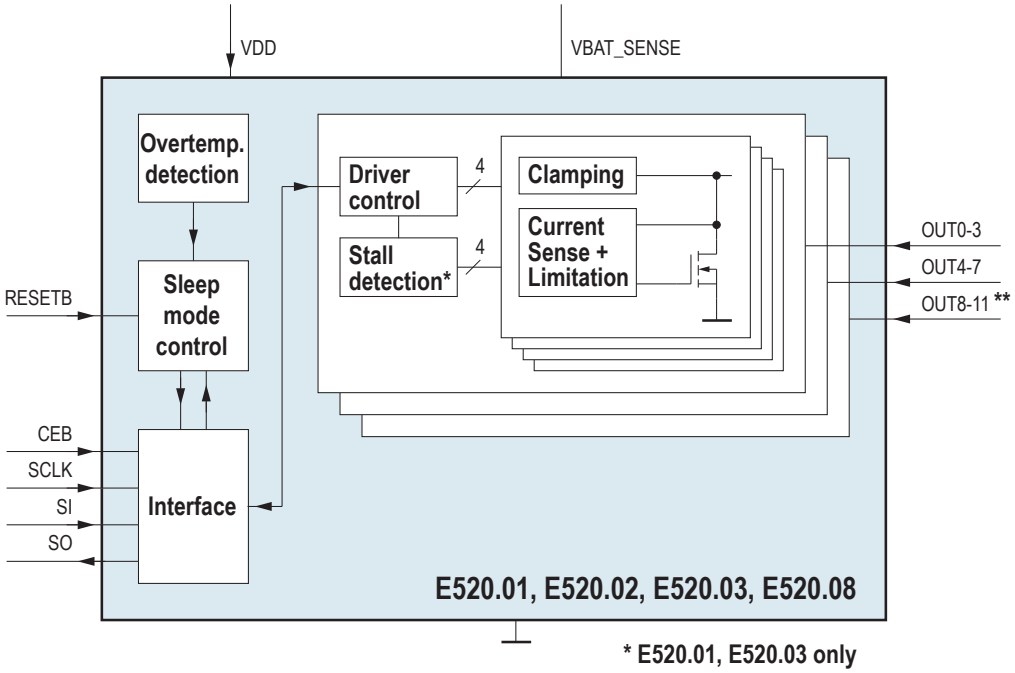
Ordering Information

Product ID	Channels	Stall Detection	Package
E520.01	12	X	QFN32L5, SOIC28
E520.02	12		QFN32L5, SOIC28
E520.03	8	X	QFN32L5 QFN20L5, SOIC20
E520.08	8		QFN32L5 QFN20L5, SOIC20

Typical Application Circuit

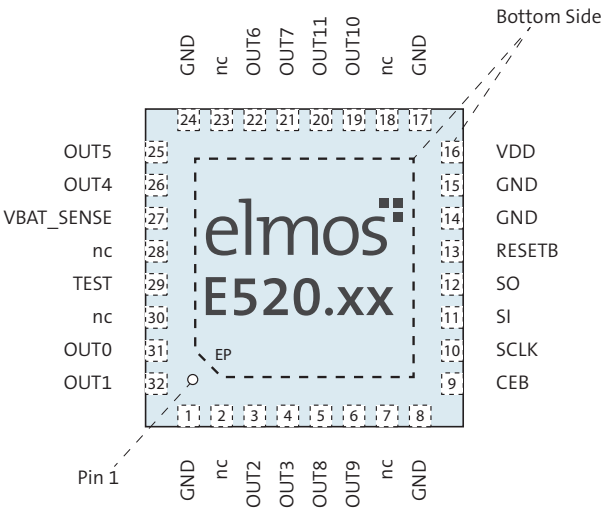


Functional Diagram



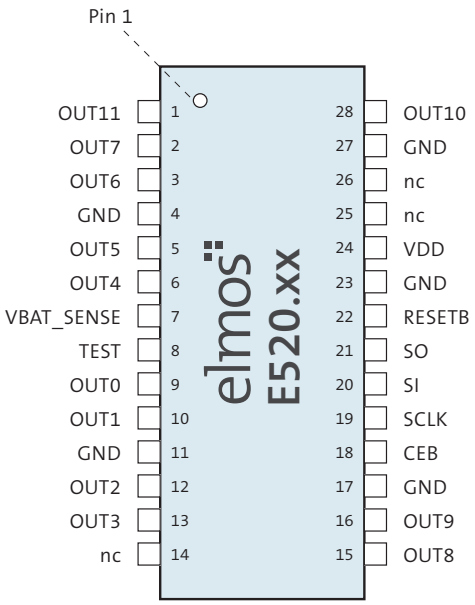
Pin Configuration

Top View Not to Scale



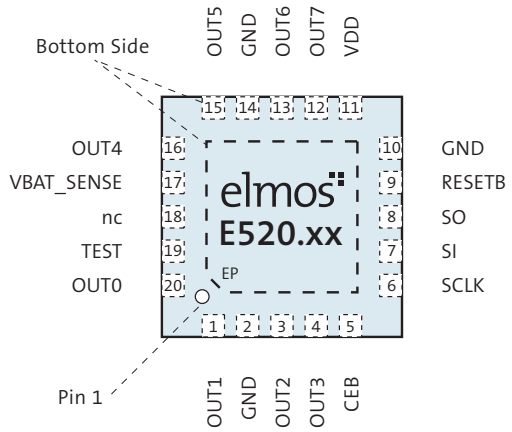
E520.01, E520.02 QFN32L5

Top View Not to Scale



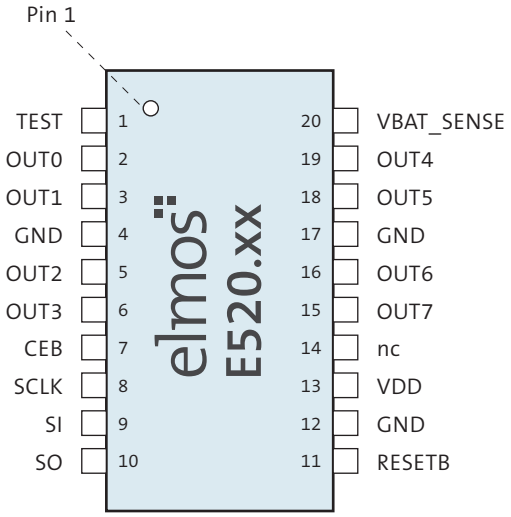
E520.01, E520.02 SOIC28

Top View Not to Scale



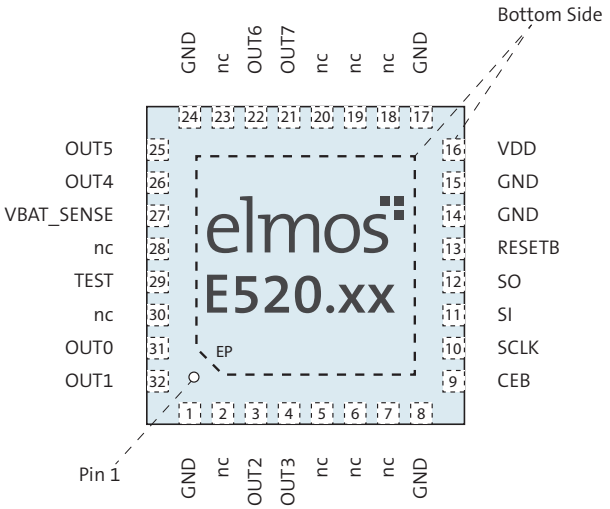
E520.03, E520.08 QFN20L5

Top View Not to Scale



E520.03, E520.08 SOIC20

Top View Not to Scale



E520.03, E520.08 QFN32L5

Pin Description

QFN32L5	QFN20L5	SOIC28	SOIC20	Name	Type [1]	Description
1	2	11	4	GND	S	Common GND pin of driver 0 and driver 1 Common GND pin of driver 2 and driver 3
2	-	14	-	nc		not connected
3	3	12	5	OUT2	O	Low side open drain output driver 2
4	4	13	6	OUT3	O	Low side open drain output driver 3
5	-	15	-	OUT8 [3]	O	Low side open drain output driver 8 [3]
6	-	16	-	OUT9 [3]	O	Low side open drain output driver 9 [3]
7	-	-		nc		not connected
8	-	17	-	GND	S	Common GND pin of driver 8 and driver 9
9	5	18	7	CEB	I	Chip Enable (Output data sampled on falling edge of CEB, input data latched on rising edge)
10	6	19	8	SCLK	I	Serial data input/output clock (Data are clocked by the falling edge of SCLK)
11	7	20	9	SI	I	Serial data input
12	8	21	10	SO	O	Serial data output (High impedance when CE = HIGH)
13	9	22	11	RESETB	I	External reset (pull-down)
14	10	23	12	GND		Ground
15	-	-	-	GND		Ground
16	11	24	13	VDD	S	VDD supply voltage
-	-	25	-	-	O	leave open
		26	-	-	O	leave open
17	-	27	-	GND	S	Common GND pin of driver 10 and driver 11
18	-	-	14	-		not connected
19	-	28	-	OUT10 [3]	O	Low side open drain output driver 10 [3]
20	-	1	-	OUT11 [3]	O	Low side open drain output driver 11 [3]
21	12	2	15	OUT7	O	Low side open drain output driver 7
22	13	3	16	OUT6	O	Low side open drain output driver 6
23		-	-	-		not connected
24	14	4	17	GND	S	Common GND pin of driver 4 and driver 5 Common GND pin of driver 6 and driver 7
25	15	5	18	OUT5	O	Low side open drain output driver 5
26	16	6	19	OUT4	O	Low side open drain output driver 4
27	17	7	20	VBAT_SENSE	I	VBAT Sense Pad (pull down)
28	18	-	-	-		not connected
29	19	8	1	TEST	I	Test mode enable (pull down)
30	-	-	-	-		For application use: Connect to ground
31	20	9	2	OUT0	O	Low side open drain output driver 0
32	1	10	3	OUT1	O	Low side open drain output driver 1
- [2]	- [2]			EP	S	Exposed Die Pad

1) I/O = Input/Output, S= Supply
2) The exposed pad on the bottom side of the QFN is recommended to be connected to GND.
3) For the versions E520.03/08 this pins are not connected.
Note: Pins with identical names have to be connected.

1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages with respect to ground. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

Description	Condition	Symbol	Min	Max	Unit
Logic Supply Voltage		VDD	-0.3	6	V
Transient Output Voltage	Max. 500ms	VOUT	-0.3	42	V
Output Current		IOUT		350	mA
Output Current (transient 500msec)	Schaffner Pulse 2	IOUT		600	mA
Input Voltage	SPI interface pins	VIN	-0.3	VDD+0.3	V
Input Current	SPI interface pins	IIN	-10	10	mA
VBAT_SENSE Input Voltage		VBAT_SENSE	-0.3	42	V
VBAT_SENSE Input Current		IVBAT_SENSE	-10	10	mA
Junction Temperature		TJ	-40	150	°C
Ambient Temperature [1]		TA	-40	125	°C
Storage Temperature		TSTG	-40	150	°C
Thermal Resistance Junction to Ambient QFN32L5 [2]		$R_{TH,JA}$	21	23	°C/W
Thermal Resistance Junction to Ambient QFN20L5 [2]		$R_{TH,JA}$	22	24	°C/W
Thermal Resistance Junction to Ambient SOIC28 [3]		$R_{TH,JA}$	71	87	°C/W
Thermal Resistance Junction to Ambient SOIC20 [3]		$R_{TH,JA}$	76	94	°C/W
Power Dissipation [3] Package QFN32L5	T_A < 85°C	PD_{85}		2800	mW
Power Dissipation [3] Package QFN32L5	T_A < 105°C	PD_{105}		1950	mW
Power Dissipation [3] Package QFN32L5	T_A < 125°C	PD_{125}		1080	mW

Connect pin TEST to GND

1) *The package was qualified at ambient temperatures -40...125°C, for power dissipation < 1W also up to 150°C. If higher ambient temperatures are focused please contact Elmos AG.*
2) *packages according to JEDEC standard JESD-51-6,7.*
3) *packages according to JEDEC standard JESD-51-5.*

2) and 3) *Using same structure on application board will lead to $R_{TH,JA}$ in the specified temperature region. Power dissipation has to be taken into account based on $R_{TH,JA}$ values. Actual thermal performance will depend on die-size, die-pad size, availability of an exposed die-pad and the concentration of hot spots.*
3) *The maximum allowed power dissipation, calculated at TJ,max=150°C is a function of the ambient temperature and the thermal resistance $R_{TH,JA}$. It may be calculated as : Pdmax=(TJ,max-TA)/RTH_JA.*

2 ESD Protection

Description	Condition	Symbol	Min	Max	Unit
ESD HBM Protection at all Pins	1)	$V_{ESD(HBM)}$	-2	2	kV
ESD CDM Protection at all Pins	2)	$V_{ESD(CDM)}$	-500	500	V
ESD CDM Protection at Corner Pins	2)	$V_{ESD(CDM)C}$	-750	750	V

1) According to AEC-Q100-002 (HBM) chip level test
2) According to AEC-Q100-011 (CDM) chip level test

3 Recommended Operating Conditions

Description	Condition	Symbol	Min	Typ	Max	Unit
VDD Supply Voltage Lower Range		VDD,L	3.1	3.3	3.6	V
VDD Supply Voltage Higher Range		VDD,H	4.5	5.0	5.5	V
Output Voltage	Driver off	VOUT	3		25	V
Output Current	Driver on	IOUT			300	mA
Operating Junction Temperature 1)		TJ	-40		150	°C
VBAT_SENSE Input Voltage	LED mode	$V_{BATsense,LED}$	3.0		25.0	V
VBAT_SENSE Input Voltage	Stepper mode	$V_{BATsense,STEPPER}$	7.0		19.0	V
SCLK Duty Cycle		DC_{SCLK}	40%		60%	$T_{H,SCLK} * f_{SCLK}$

1) Operating at junction temperatures close to 150°C significantly reduces the lifetime of the IC. Because of this knowledge of the ambient temperature profile as well as activation profile is essential to calculate estimated lifetime for each individual application.

4 Typical Operating Characteristics

(V_{DD} = 3.1V to 3.6V and 4.5V to 5.5V, T_{AMB} = -40°C to +125°C, unless otherwise noted.
Typical values are at V_{DD} = 3.3V or 5V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Supply Voltages / POR						
VDD Supply Current	active	I_{VDD}			5	mA
VDD Supply Current (Sleep Mode) 1)	RESETB = L V_{OUTx} > 1.0V T_j < 50°C	I_{VDDQ_50}		0.5	1	µA
VDD Supply Current (Sleep Mode) 1)	RESETB = L V_{OUTx} > 1.0V T_j = 125°C	I_{VDDQ_125}			5	µA
Power-On Threshold 1)	V_{DD} rising	$V_{TH,PORB}$		2.7	2.9	V
Power-On-Reset Threshold 1)	V_{DD} falling	$V_{TH,POR}$	2.4	2.6	2.8	V
Power-On-Reset Hysteresis 1)		$V_{HYS,POR}$	30			mV
RESETB LH Delay Time	RESETB	$T_{DEL,RESETB}$	0.31	0.62	0.93	ms
Over Temperature Detection						
Thermal Shut-Off Threshold 1)	T_J rising	$T_{TH,OFF}$	160		200	°C
Thermal Shut-Off Reset Threshold 1)	T_J falling	$T_{TH,ON}$	150		190	°C
Thermal Shut-Off Hysteresis 1)		$T_{TH,HYS}$		20		°C
Digital Control Interface SPI (DC Parameters)						
Low Input Threshold CEB, SI, SCLK		$V_{TL,DIO}$	0.85			V
High Input Threshold CEB, SI, SCLK		$V_{TH,DIO}$			2.45	V
Input Hysteresis CEB, SI, SCLK	1)	$V_{HYS,DIO}$	0.20			V
Input Leakage Current CEB, SI, SCLK	0.0V<V_{IN}<V_{DD}	$I_{LEAK,DIO}$	-1		1	µA
Low Input Threshold RESETB		$V_{TL,RESETB}$	0.20			VDD
High Input Threshold RESETB		$V_{TH,RESETB}$			0.60	VDD
Input Hysteresis RESETB	1)	$V_{HYS,RESETB}$	0.05			VDD
Pull-Down Current RESETB	V_{RESETB}>+3.0V	$I_{PD,RESETB}$	10		50	µA
Passive Pull-Down Resistor RESETB		$R_{PD,RESETB}$		500		kΩ
Low Output Voltage SO CEB=LOW	I_{SO}=+1.6mA	$V_{OL,SO}$			0.40	V
High Output Voltage SO CEB=LOW	I_{SO}=-1.0mA	$V_{OH,SO}$	V_{DD}/V-1.3			V
Tristate Output Leakage Current SO	CEB=HIGH 0.0V < V_{IN} < V_{DD}	$I_{LEAK,SO}$	-5		5	µA
Low Input Threshold TEST		$V_{TL,TEST}$	0.85			V
High Input Threshold TEST	Test Mode	$V_{TH,TEST}$			2.45	V
Pull-Down Current TEST	V_{TEST} > 2.45V	$I_{PD,TEST}$	7		90	µA

1) Not tested in production

Electrical Characteristics (continued)

(V_{DD} = 3.1V to 3.6V and 4.5V to 5.5V, T_{AMB} = -40°C to +125°C, unless otherwise noted.
Typical values are at V_{DD} = 3.3V or 5V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Pull-Down Current TEST (Low Input)	$V_{TEST} > V_{TL,TEST}$	$I_{PD,TEST}$	1			µA
Low Input Threshold VBAT_SENSE		$V_{TL,VBATsense}$	0.85			V
High Input Threshold VBAT_SENSE		$V_{TH,VBATsense}$			2.45	V
Input Hysteresis VBAT_SENSE	1)	$V_{HYS,VBATsense}$	0.20			V
Pull-Down Current VBAT_SENSE	$V_{BATsense} > +3.0V$	$I_{PD,VBATsense}$	10		300	µA
VBAT_SENSE Supply Current (Sleep Mode)	RESETB = L V_{VBAT_SENSE} = 13V V_{OUTx} = 13V T_J < 50°C 1)	$I_{VBATsenseQ}$		2	4	µA
Digital Control Interface SPI (AC Parameters)						
Input Capacitance CEB, SI, SCLK, RESETB, TEST	1)	C_{IN}			5	pF
Marginal Delay SO	1)	$T_{MD,SO}$			0.5	ns/pF
Delay Time between Falling Edge of CEB and Transition of SO from Tristate to Active State CEB↓> SO↑	See SPI Timing Diagram C_{SO} < 20pF 1)	$T_{LSO,ON}$	20		100	ns
Delay Time between Rising Edge of CEB and Transition of SO from Active State to tristate CEB↑ > SO↓	See SPI Timing Diagram C_{SO} < 20pF 1)	$T_{LSO,OFF}$	20		100	ns
Set-Up Time between Falling Edge of CEB and First Rising Edge of SCLK CEB↓ > SCLK↑	See SPI Timing Diagram 1)	T_{LCF}	150			ns
Delay Time Between Rising Edge of SCLK and New Data of SO SCLK↑ > SO↕	See SPI Timing Diagram C_{SO} < 20pF 1)	T_{CSO}	10		60	ns
Set-Up Time of Stable Data on SI before Falling Edge of SCLK SI↕ > SCLK↓	1)	T_{DH}	40			ns
Hold Time of stable Data on SI after Falling Edge of SCLK SCLK↓ > SI↕	1)	T_{LL}	20			ns
Time between Two SPI Protocols CEB↑ > CEB↓	1)	T_{LCR}	1			µs
Hold Time between Falling Edge of SCLK and Rising Edge of CEB SCLK↓ > CEB↑	1)	f_{SCLK}	20			ns
SCLK Clock Frequency	1)	DC_{SCLK}			2	MHz
Recommended Operating Condition: SCLK Duty Cycle	1)		40%		60%	$T_{H,SCLK} * f_{SCLK}$

1) Not tested in production

Electrical Characteristics (continued)

(V_{DD} = 3.1V to 3.6V and 4.5V to 5.5V, T_{AMB} = -40°C to +125°C, unless otherwise noted.
Typical values are at V_{DD} = 3.3V or 5V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Driver Outputs (DC Parameters)						
Short Circuit Output Current OUTx	OUTx = LOW V_{OUTx} = 3.0V t < T_{SCL}	I_{SCL}	350	-	800	mA
Output Clamping Level OUTx	I(OUTx) = 1mA OUTx = HIGH CLMP[1:0] = $X0_b$	V_{CL0}	37		50	V
Output Resistance OUTx	OUTx = LOW I_{OUT} < 200mA T_J = +25°C 1)	$R_{OUT,25C}$	1.2	1.5	1.8	Ω
Output Resistance OUTx	OUTx = LOW I_{OUT} < 200mA T_J = +125°C	$R_{OUT,125C}$	1.8	2.3	2.6	Ω
Output Resistance OUTx	OUTx = LOW I_{OUT} < 200mA T_J = +150°C 1)	$R_{OUT,150C}$	1.9	2.5	3	Ω
Output Leakage Current OUTx (Sleep Mode)	V_{OUTx} = 13V RESETB = LOW OUTx = HIGH T_j < 50°C 1)	$I_{OUTL,50C}$		0.5	1	µA
Output Leakage Current OUTx (Pull-Down Disabled)	V_{OUTx} = 13V RESETB = HIGH PDEx = LOW OUTx = HIGH CLMP[1:0] = $X0_b$ Tj < 50°C 1)	$I_{OUTL,PDOFF,50C}$		3	5	µA
Output leakage current OUTx (Sleep Mode or Pull-Down Disabled)	V_{OUTx} = 25V RESETB = LOW or RESETB = HIGH PDEx = LOW OUTx = HIGH T_j < 125°C 1)	$I_{OUTL,125C}$			10	µA
Low Input Threshold OUTx		$V_{TL,OUT}$	1.5		2.9	V

1) Not tested in production

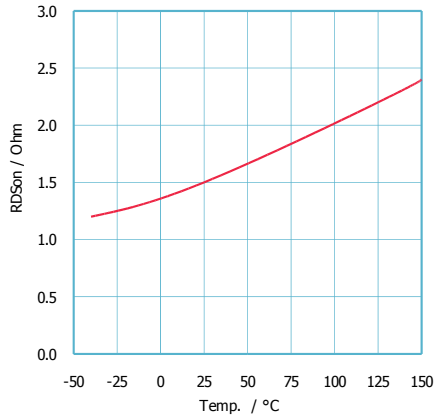
Electrical Characteristics (continued)

(V_{DD} = 3.1V to 3.6V and 4.5V to 5.5V, T_{AMB} = -40°C to +125°C, unless otherwise noted.
Typical values are at V_{DD} = 3.3V or 5V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

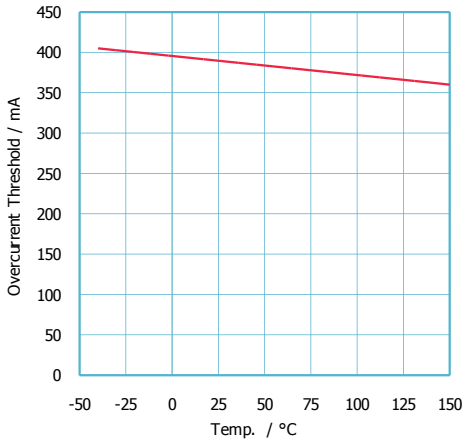
Description	Condition	Symbol	Min	Typ	Max	Unit
Pull-Down Current OUTx	RESETB = HIGH PDEx = HIGH OUTx = HIGH V(OUTX) > 1.5V	$I_{PD,OUT}$	20		300	µA
Driver Outputs (AC Parameters)						
Output Capacitance OUTx	OUTx = HIGH V_{OUT} = 5.0V [1)]	$C_{OUT,5}$		40	60	pF
Output Capacitance OUTx	OUTx = HIGH V_{OUT} = 15.0V [1)]	$C_{OUT,15}$		30	45	pF
Driver Slew Rate of Rising OUTx	R_L = 1kΩ [1)]	dV_{OUT}/dt		5		V/µs
Driver Slew Rate of Falling OUTx	R_L = 1kΩ [1)]	dV_{OUT}/dt		-7		V/µs
Duration of Output Short Circuit Limitation	OUTx = LOW OCC = 0_b $I_{OUT} > I_{SCL}$	T_{SCL0}	18.5	37	55.5	ms
Duration of Output Short Circuit Limitation	OUTx = LOW OCC = 1_b $I_{OUT} > I_{SCL}$	T_{SCL1}	1	2	3	ms
Propagation Delay and Rise Time CEB↑ > OUTx↑	R_L = 1kΩ V_{BAT} = 12.0V V_{OUTx} rising above 90% V_{BAT} threshold [1)]	$T_{N,R}$		13		µs
Propagation Delay and Fall Time CEB↑ > OUTx↓	R_L = 1kΩ V_{BAT} = 12.0V V_{OUTx} falling below 10% V_{BAT} threshold [1)]	$T_{N,F}$		3.5		µs
PWM Frequency	Linear PWM Mode and VBAT Adapted PWM Mode	f_{PWM}	18.75	25	31.3	kHz
PWM Frequency	Logarithmic PWM Mode for LEDs	f_{LED}	180	245	310	Hz

5 Typical Operation Caracteristics

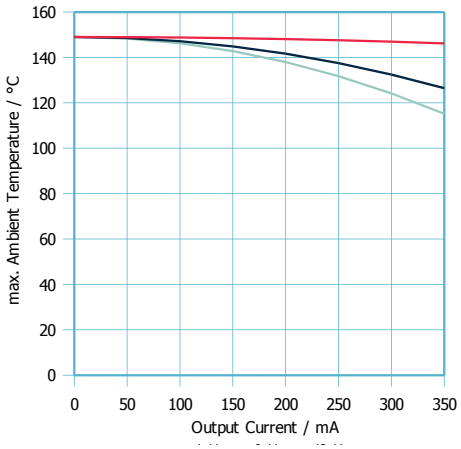
RDSon vs. Temperature



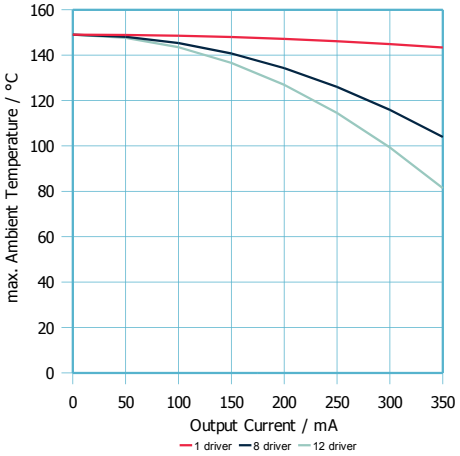
Overcurrent Threshold vs. Temperature



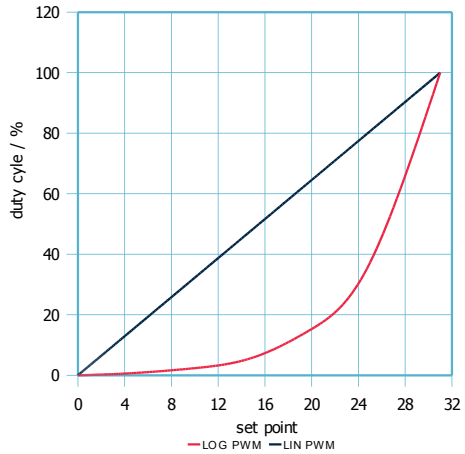
Max. Ambient Temperature vs. Output Current
(RDSon = 2 Ohm, 50% duty cycle, QFN package)
Valid only for DC load



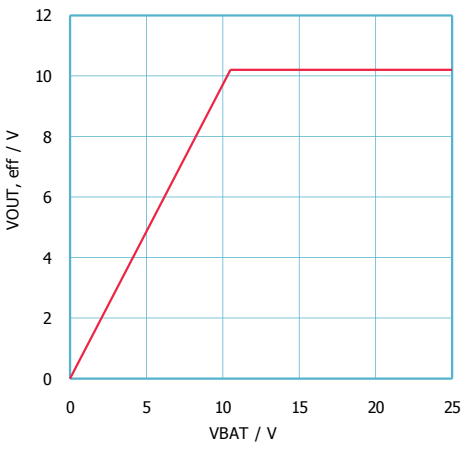
Max. Ambient Temperature vs. Output Current
(RDSon = 2 Ohm, 100% duty cycle, QFN package)



PWM duty cycle vs. set point
logarthmic and linear mode



Adaptive PWM



6 Functional Description

6.1 Supply Voltages / POR

Upon power-up of the supply voltage all data latches and the timers are reset and the output drivers are disabled (OUTx = inactive HIGH). The internal Power-On-Reset is OR'd with the external RESETB input. An analogue low pass filter is added to the RESETB input in order to prevent short spikes on the signal line from triggering a reset event.

After both, internal Power-On-Reset and external RESETB event, have changed to inactive state, the internal reset condition is extended by a time of $T_{DEL,RESETB}$ to allow the circuit to settle properly before normal function is enabled (See timing diagrams)

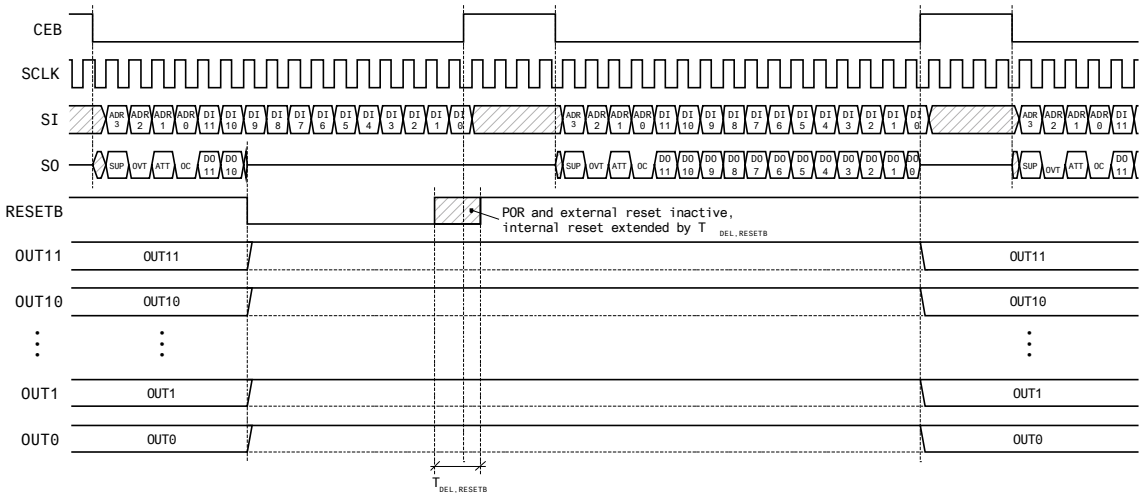


Figure 1. External RESET (Sleep Mode)

6.2 Digital Control Interface

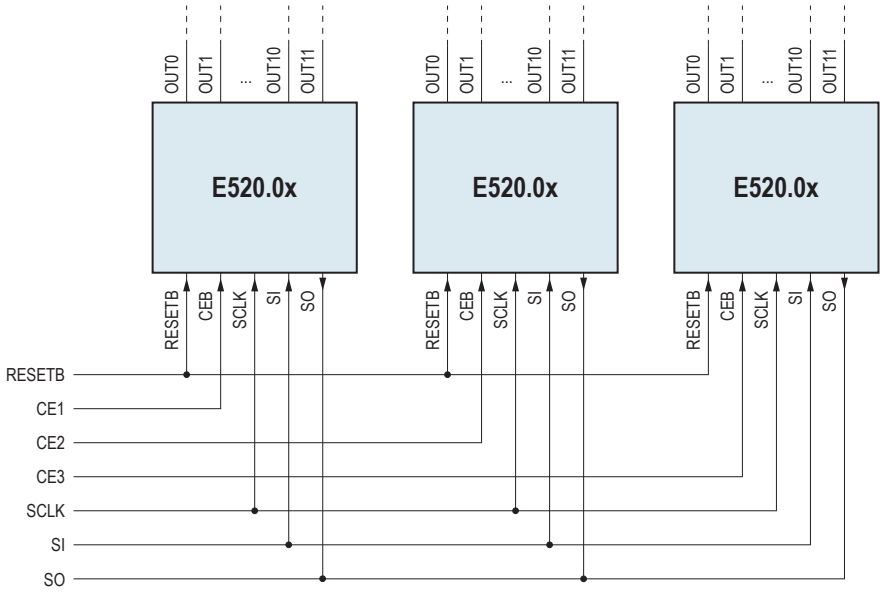


Figure 2. SPI in Parallel Mode

The SI and SO terminals of all devices are tied together. There is an individual chip enable (CEB) line to each device. At most one of these chip enable lines shall be active at any time in order to avoid data bus contention on the SO line. The protocol frame of the SPI consists of 16 bits. It contains an address identifier of 4 bits and 12 data bits for the 12 driver channels or other functions.

The SPI protocol frame is defined as follows:

- On the falling edge of the CEB signal the SO data output is going into low impedance state.
- With each rising edge of the clock signal SCLK the data will be shifted out at SO in "MSB first" order, beginning with four status bits, followed by the data bits DO_{11} down to DO_0.
- With each falling edge of the clock signal SCLK the new input data at SI will be shifted into the SPI register in "MSB first" order, beginning with the address bits ADR3 down to ADR0, followed by the data bits DI_{11} down to DI_0
- On the rising edge of the CEB signal the content of the SPI shift register will be latched and transferred to the output drivers or internal registers, respectively. The SO data output goes back to high impedance state.
- The content of the output data DI[11:0] depends on the submitted address bit.

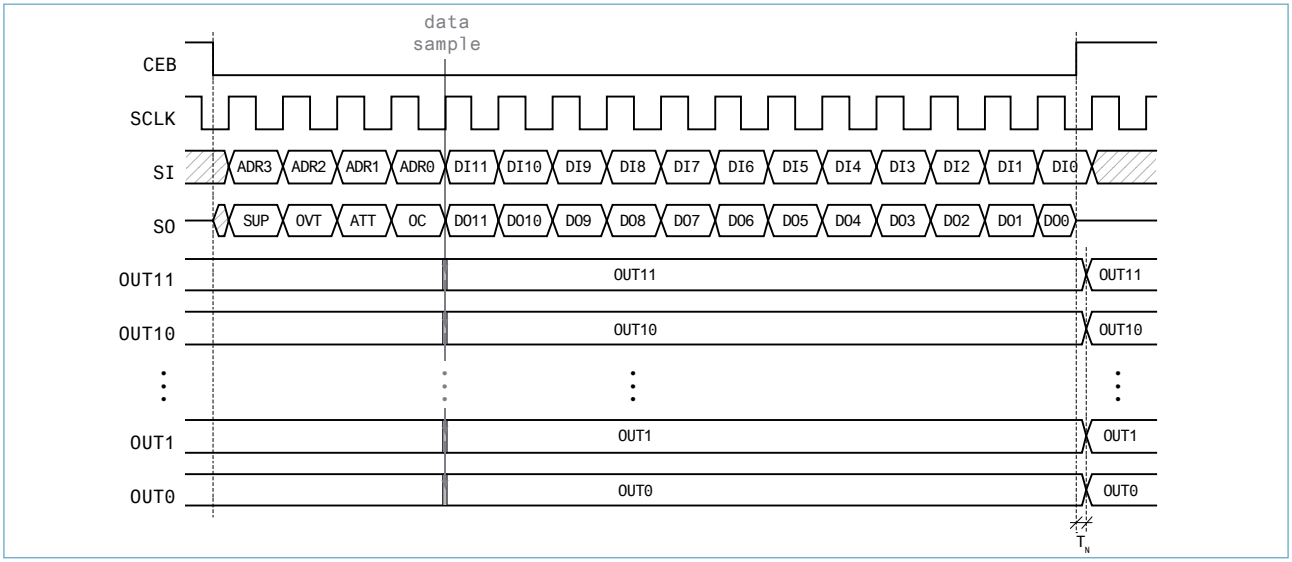


Figure 3. SPI Protocol

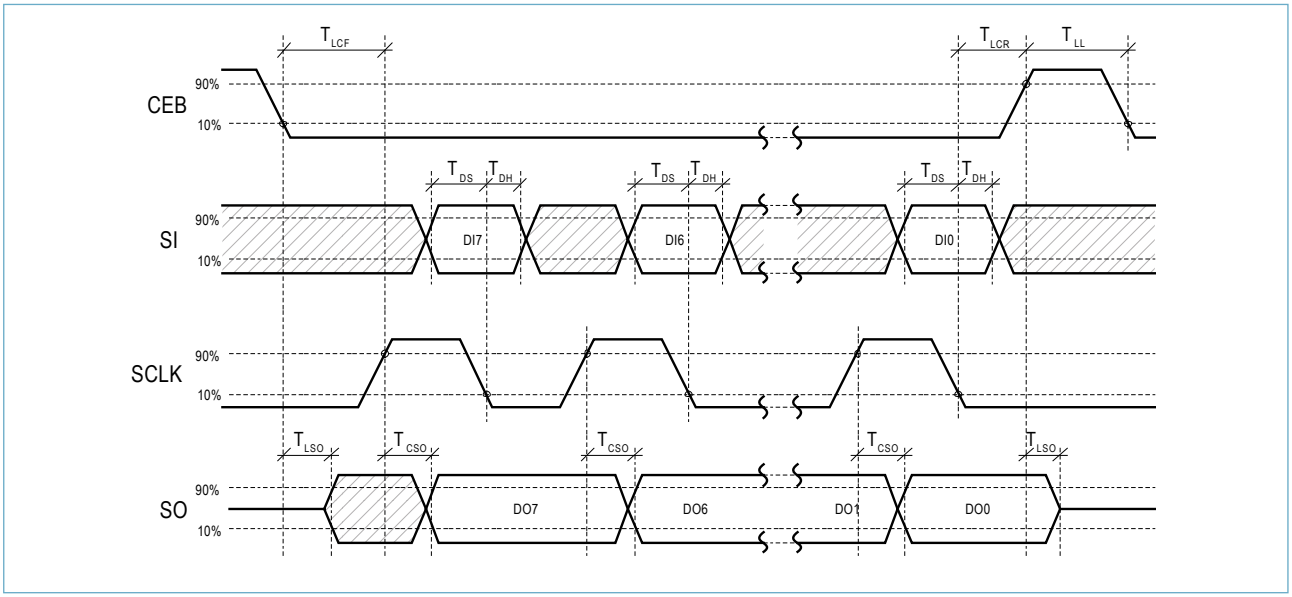


Figure 4. SPI interface Timing Diagram

SPI registers
The following diagram summarises the SPI address and control bits assignments.

Table 1. SPI Register and Control Bit Table

Mode	R/W	ADR3	ADR2	ADR1	ADR0	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
LS driver control	W	0_b	0_b	0_b	0_b	OUT11	OUT10	OUT9	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
	R	SUP	OVT	ATT	OC	STAT11	STAT10	STAT9	STAT8	STAT7	STAT6	STAT5	STAT4	STAT3	STAT2	STAT1	STAT0
	POR	0_b	0_b	0_b	0_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b
Output status	W	0_b	0_b	0_b	1_b	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.
	R	SUP	OVT	ATT	OC	STAT11	STAT10	STAT9	STAT8	STAT7	STAT6	STAT5	STAT4	STAT3	STAT2	STAT1	STAT0
	POR	0_b	0_b	0_b	0_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b
Overcurrent status	W	0_b	0_b	1_b	0_b	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.	res.
	R	SUP	OVT	ATT	OC	OCE11	OCE10	OCE9	OCE8	OCE7	OCE6	OCE5	OCE4	OCE3	OCE2	OCE1	OCE0
	POR	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b
PWM enable	W	0_b	0_b	1_b	1_b	PWE11	PWE10	PWE9	PWE8	PWE7	PWE6	PWE5	PWE4	PWE3	PWE2	PWE1	PWE0
	R	SUP	OVT	ATT	OC	PWE11	PWE10	PWE9	PWE8	PWE7	PWE6	PWE5	PWE4	PWE3	PWE2	PWE1	PWE0
	POR	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b
Relay hold enable	W	0_b	1_b	0_b	0_b	RHE11	RHE10	RHE9	RHE8	RHE7	RHE6	RHE5	RHE4	RHE3	RHE2	RHE1	RHE0
	R	SUP	OVT	ATT	OC	RHE11	RHE10	RHE9	RHE8	RHE7	RHE6	RHE5	RHE4	RHE3	RHE2	RHE1	RHE0
	POR	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b
Pulldown enable	W	0_b	1_b	0_b	1_b	PDE11	PDE10	PDE9	PDE8	PDE7	PDE6	PDE5	PDE4	PDE3	PDE2	PDE1	PDE0
	R	SUP	OVT	ATT	OC	PDE11	PDE10	PDE9	PDE8	PDE7	PDE6	PDE5	PDE4	PDE3	PDE2	PDE1	PDE0
	POR	0_b	0_b	0_b	0_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b	1_b
Configuration and PWM duty cycle	W	0_b	1_b	1_b	0_b	SDS2	SDS1	SDS0	CLMP1	CLMP0	OCC	LOG	PWMA4	PWMA3	PWMA2	PWMA1	PWMA0
	R	SUP	OVT	ATT	OC	SDS2	SDS1	SDS0	CLMP1	CLMP0	OCC	LOG	PWMA4	PWMA3	PWMA2	PWMA1	PWMA0
	POR	0_b	0_b	0_b	0_b	1_b	0_b	0_b	1_b	1_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b
PWM duty cycles	W	0_b	1_b	1_b	1_b	res.	PWMC4	PWMC3	PWMC2	PWMC1	PWMC0	res.	PWMB4	PWMB3	PWMB2	PWMB1	PWMB0
	R	SUP	OVT	ATT	OC	res.	PWMC4	PWMC3	PWMC2	PWMC1	PWMC0	res.	PWMB4	PWMB3	PWMB2	PWMB1	PWMB0
	POR	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b	0_b
Stall detection status and configuration	W	1_b	0_b	0_b	0_b	STOP2	res.	res.	res.	STOP1	res.	res.	res.	STOP0	res.	res.	res.
	R	SUP	OVT	ATT	OC	STOP2	FSW2	STE2	STW2	STOP1	FSW1	STE1	STW1	STOP0	FSW0	STE0	STW0
	POR	0_b	0_b	0_b	0_b	0_b	1_b	0_b	0_b	0_b	1_b	0_b	0_b	0_b	1_b	0_b	0_b

All other addresses are reserved. Write access to any of the reserved addresses will not have any effect, read access will return 0_b. For IC versions only having 8-channels (E520.03 and E520.08) it´s recommended to programm the bits D08-D11 of writable registers to there POR- value (Reset-value). This values can be found in Table 1.

Bits regarding the driver outputs:

OUTx - Output driver latch
0_b corresponds to an active low side driver
1_b corresponds to an inactive low side driver

STATx - Output driver status
0_b corresponds to a low output status
1_b corresponds to a high output status

RHEx - Relay hold mode enable bit
0_b disables $V_{BATsense}$ adapted PWM mode → output state only depends on OUTx
1_b enables $V_{BATsense}$ adapted PWM mode if OUTx = 0_b
PWM frequency fixed to 25kHz, duty cycle adapted to $V_{BATsense}$ voltage level

PWEx - Constant PWM mode enable bit
0_b disables Constant PWM mode → output state only depends on OUTx
1_b enables Constant PWM mode if OUTx = 0_b

PDEx - Enable bit for output pull-down current sources
0_b pull down current switched off
1_b pull down current switched on

CLMP[1:0] - Output clamping
$X0_b$ corresponds to >37V absolute clamping,
01_b corresponds to $V_{BATsense}$ related clamping
11_b refer to chapter output clamping (see Table 2)

OCC - over-current shut-off time configuration bit
0_b corresponds to a time constant of typically 37ms
1_b corresponds to a time constant of typically 2ms

LOG - selection of PWM characteristic
0_b selects Linear PWM mode
1_b selects Logarithmic PWM mode for LED control

PWMA/B/C[4:0] - Constant PWM sources PWMA, PWMB and PWMC
Duty cycles defined by PWMA[4:0], PWMB[4:0] and PWMC[4:0] bits
Counter may be configured to linear or logarithmic mode (via LOG latch)
Relation between output channels and PWM sources PWMA/B/C is fixed by hardware

STOPz - Stall handling bit
0_b has no effect on the motor driver
1_b related motor driver will be stopped if 1_b appears in its STEz flag

STWx - Stall detection warning
0_b no warning accured
1_b indicates potential stall condition (It is recommended that the controller saves the current motor position for later use.)

FSWx - Stepping frequency supervisor
0_b stepping frequency ok
1_b stepping frequency unstable, stall detection automatically disabled

OCEx - Over-current status flag
0_b normal state
1_b over-current detected

STEx - Stall detection indication
0_b no stall indication
1_b stall situation detected

SDSx - Stall detection senitivity
100_b sensitivity default value

6.3 Protection Functions

Supply Control (VBAT_Sense pin)
The flag bit SUP is set if a LOW level has been detected on the VBAT_SENSE input pin The SUP bit is automatically cleared at the end of each SPI frame.

Over-temperature Protection
If the chip temperature exceeds the over-temperature protection threshold $T_{TH,OFF}$, all output drivers are disabled immediately. In contrast to the short circuit protection, the driver latches will not be reset. When the chip temperature decreases below the threshold $T_{TH,ON}$, the previous driver status will be restored without the need for a new SPI protocol.
If a new driver status is transferred to the driver latches during over-temperature condition, this new status will be valid as soon as the chip temperature has decreased below the threshold $T_{TH,ON}$. This also applies if the content of the driver latch is changed by other means, e.g. due to an external reset.

- The flag bit OVT represents the over-temperature status. If an over-temperature condition is present, this bit will be set to HIGH state and all drivers will be disabled.

Short Circuit Protection
When the output current exceeds the value of I_{SCL}, an internal timer is started and the current limitation is activated for the concerned driver. If the current limitation is still active when the timer has expired after the time T_{SCL}, the concerned output is disabled by resetting the related driver latch. After disabling the output the short circuit status is automatically cleared and it is possible to re-activate the outputs by writing 0b bits into the shift register via the serial input SI. In case that the short circuit is still present, the current limitation is again activated and the output is again disabled after the time T_{SCL}. The over-current status flags OCEx of all channels may be read back over the SPI register address 0010_b.

The flag OC is set by the short circuit protection logic and indicates that at least one over-current state bit in the over-current status register at address 0010_b is set. The OC flag is automatically cleared at the end of an SPI frame accessing the over-current status register at address 0010_b with no over-current state present.

The time constant TSCL of the short circuit protection may be selected using the OCC bit, located in the SPI register at address 0110_b.
OCC = 0_b corresponds to a time constant of typically 37ms
OCC = 1_b corresponds to a time constant of typically 2ms
When an output has been disabled due to a short circuit condition (OUTx = inactive HIGH), the related output status bit STATx will set to 1_b in the next SPI protocol. The actual output status is being sampled at the beginning of each protocol when CEB goes low. Polling the output status bits in the serial SPI protocol is the appropriate way to detect if a short circuit condition has been detected. When the output has been enabled by writing a 0_b into the shift register via the serial input SI (OUTx = active LOW) and the related output status bit is found in 1_b state in a subsequent SPI protocol, this indicates that a short circuit condition has occurred.
In the period between detecting an output current level of I_{SCL} and disabling the output after the time T_{SCL}, the output is operating as constant current source. This feature is advantageous when driving loads with a significant inrush current like lamps. By limiting the current, the load is switched on safely. If the load current has settled to a level below I_{SCL} within the time T_{SCL}, the short circuit protection will intentionally not be activated.
In case of very low duty cycles the ON phase of the PWM may become shorter than the settling and latency time of the short circuit detection. Under these conditions the short circuit protection will not be triggered. Due to the low duty cycle the power dissipation and thermal stress of the output driver will also be low under these conditions.

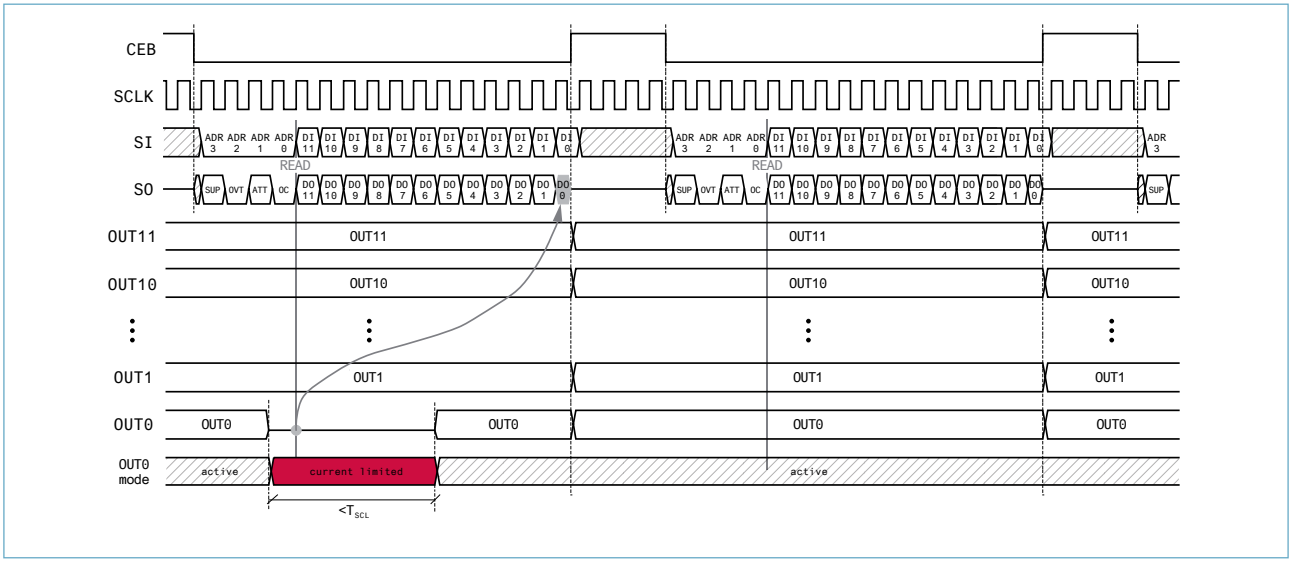


Figure 5. Temporary Short Circuit (e.g. Rush in Current)

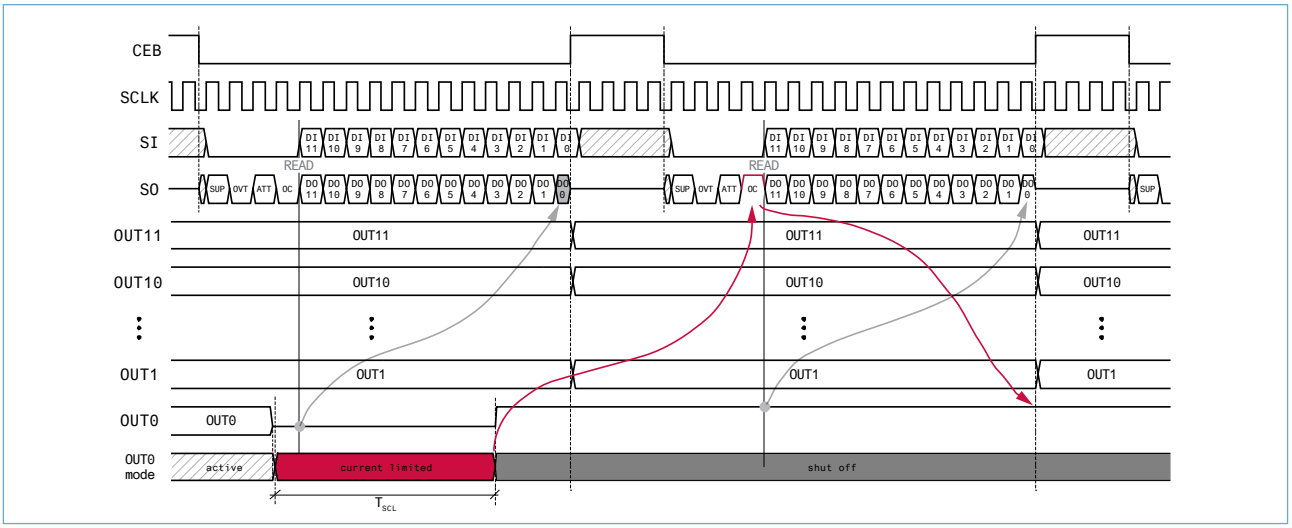


Figure 6. Trigger of Short Circuit Shut-off

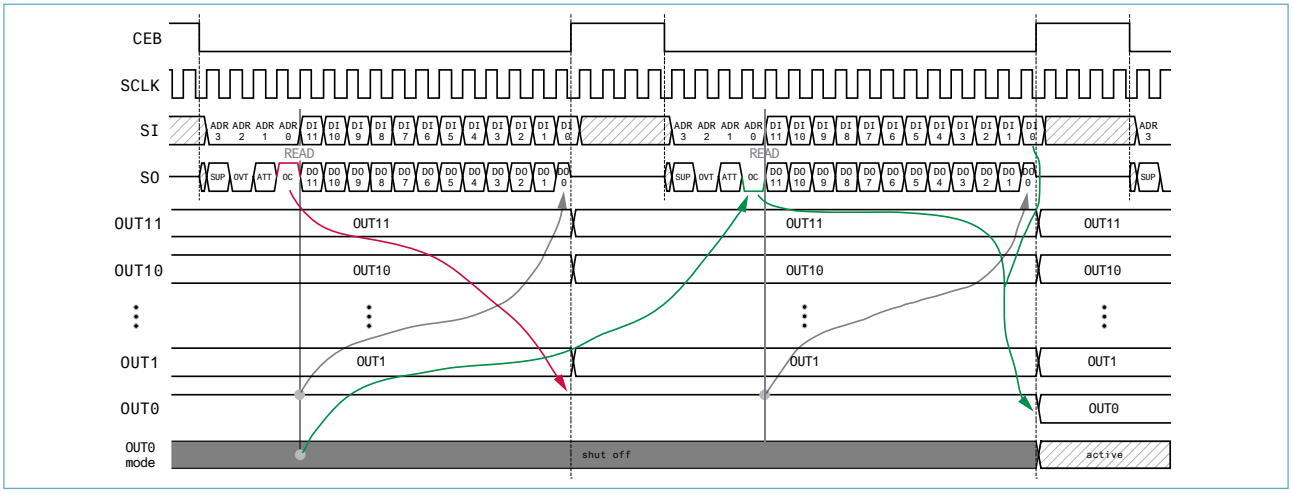


Figure 7. Recovery from Short Circuit Shut-off

Open Load Detection

In order to detect an open load condition, each output is equipped with a pull-down current source of typically 60µA, whose activation/deactivation may be controlled with the PDEx flag in SPI register 0101_b as follows:

PDEx=0_b corresponds to turned-off pull-down current source,

PDEx=1_b corresponds to enabled pull-down current source.

If there is no load connected between the output and the battery supply, the pull-down source will tie the output to ground potential and the related output status flag STATx will be set to 0_b level in the next SPI protocol. The actual output states of all drivers are being sampled after transmission of the 4 address bits Polling the output status flags in the serial SPI protocol is the appropriate way to detect if an open load condition is present.

When the output has been disabled by writing a 1_b bit into the shift register via the serial input SI (OUTx = inactive HIGH) and the related output status flag STATx is found in 0_b state in a subsequent SPI protocol, this indicates that an open load condition is present.

Output Clamping

All driver outputs provide a clamping functionality for inductive loads, which turns on the power transistor as soon as the output voltage of the related channel exceeds a certain voltage level. There is a fixed clamping between 37V and 50V which is permanently active. By default the “stepper motor clamping mode” The following table summarises the possible clamping level configurations:

Table 2. Output Clamping

CLMP[1:0]	PDEx	Clamping Level
$X0_b$	X_b	V_{CL0} typically at >37V
01_b	X_b	V_{CL1} typically at $V_{BATsense}$ or V_{CL0} typically at >37V (whatever is lower)
11_b	0_b	V_{CL1} typically at $V_{BATsense}$ or V_{CL0} typically at >37V (whatever is lower)
11_b	1_b	“stepper motor clamping mode”

Note: *Although the output drivers provide a clamping functionality for inductive loads, an external free wheeling diode to battery voltage level is recommended when using PWM modes with inductive load components in order to reduce power dissipation of the IC. In this case the external clamping level must be lower than the internal clamping level under all supply voltage conditions.*

6.4 Driver Control Modes

The combination of the different control signals is shown in the following simplified schematic and truth table:

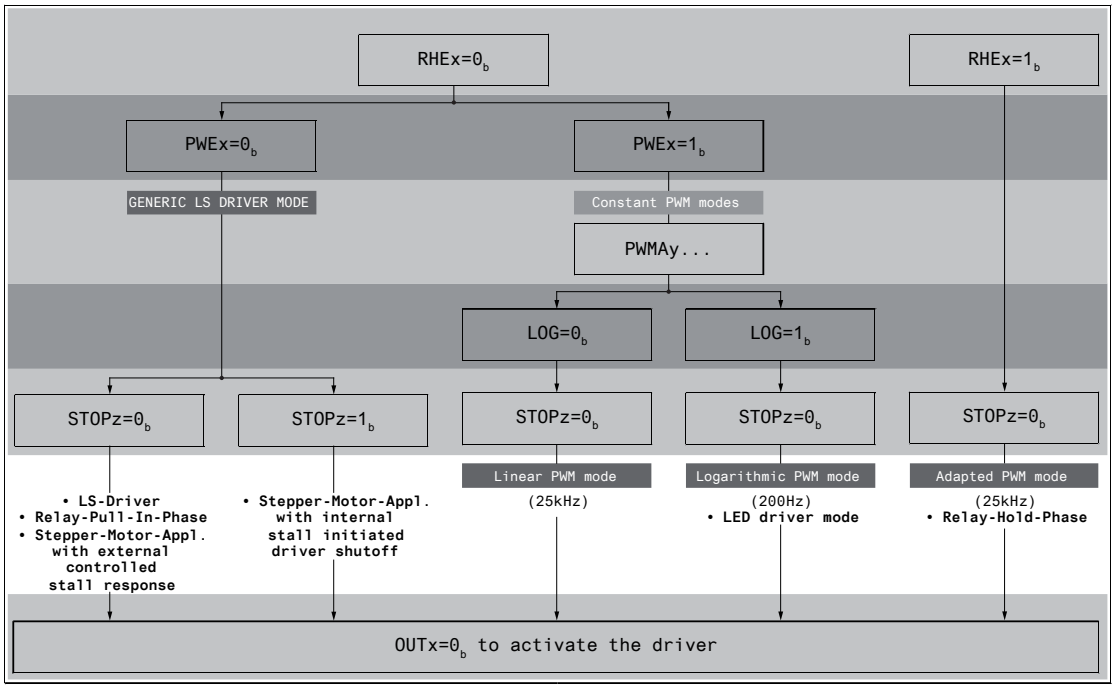


Figure 8. Adjustments for Different Driver Modes

Comments:
x ... [11...0] 12 drivers
y ... [4...0] 5bit adjustment for each PWM source A, B and C (see Table 5)
z ... [2...0] 3 stepper motors (only 2 stepper motors with E520.03 and E520.08)

Note: x=11...0 channel selection for E520.01 and E520.02
x=7...0 channel selection for E520.03 and E520.08
z=2...0 channel selection for 3 stepper motors E520.01 only
z=1...0 channel selection for 2 stepper motors E520.03 only

Table 3. Driver Modes and Applications

OUTx	PWEx	RHEx	LOG	OVT	LSONx	Application
1_b	X	X	X	X	0_b	Driver off
X	X	X	X	1_b	0_b	Over-temperature shut-off
0_b	0_b	0_b	X	0_b	1_b	Driver continously on
0_b	1_b	0_b	0_b	0_b	PWMA/B/C (LIN)	PWM Mode (25kHz linear PWM)
0_b	1_b	0_b	1_b	0_b	PWMA/B/C (LOG)	LED Mode (245Hz logarithmic PWM)
0_b	X	1_b	X	0_b	PWM adapted	Relay Mode (25kHz with duty-cycle adaption to VBAT_SENSE)

6.5 Stepper Motor Connection Scheme

For the proper operation of the stall detection mode a defined assignment between driver channels and the several motors has to be used. The following table lists the connection schemes:

Table 4. Stepper Motor Connection Scheme

Motor pin	Motor 1	Motor 2	Motor 3 [1)]
Coil A, pin 1	OUT0	OUT4	OUT8
Coil A, pin 2	OUT1	OUT5	OUT9
Coil B, pin 1	OUT2	OUT6	OUT10
Coil B, pin 2	OUT3	OUT7	OUT11

1) E520.01/02 only

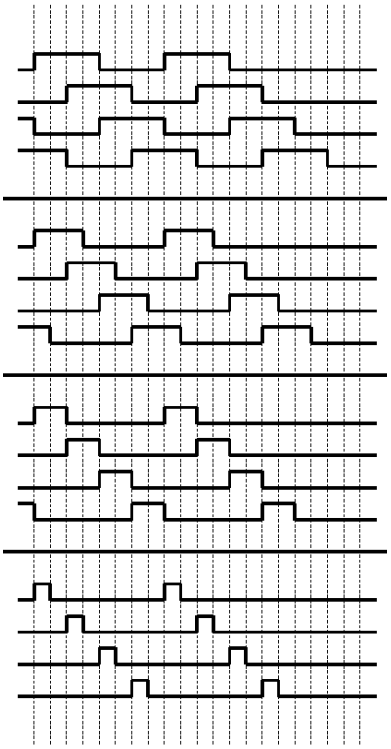
6.6 Enhanced Stall Detection Mode for Stepper Motors

Enhanced stall detection functionality is offered for E520.01 and E520.03 only.

Recommended configurations for stepper motor with stall detection are:

PDEx=1$_b$ in SPI register 0101$_b$ to enable the pull-down current source
OCC=1$_b$ in SPI register 0110$_b$ to set the over-current shut-off time to typ. 2ms
CLMP[1:0]=11$_b$ in SPI register 0110$_b$ stepper motor clamping
SDS=100$_b$ in SPI register 0110$_b$ to set the sensitivity to default values
STOPz=1$_b$ in SPI register 1000$_b$ to stop the motor after a stall detection event

The implemented stall detection works with the following stepping schemes:



full step mode
(2 coils supplied at same time for max. torque)

half step mode

full step mode
also called wave drive
(only 1 coil supplied full time)

full step mode
(only 1 coil supplied reduced time)

Figure 9. Stepping Schemes

Stall Detection

The stall detection logic will generate two status signals for each motor (see *Figure 10*). The first signal indicates a potential stall condition and sets the referred stall warning flag STWx. If STWx is 1_b, it is recommended that the controller saves the current motor position for later use.

The second signal called stall error flag STEx indicates a confirmed stall condition. If STEx is 1_b, the previously saved position should be considered as the actual mechanical position by the controller. This procedure allows to minimise the mismatch between mechanical stop and the position where STEx is set, which is caused by the stall detection filters.
The STWx, STEx and FSWx (see paragraph "Stepping Frequency Supervisor) flags of all stepper motors are cumulated to the ATT flag, which indicates a change of the stall status flags. This cumulated flag will be transmitted in the first section of the SPI return data, independently from the chosen SPI address. The ATT flag, will not be reset automatically. It is cleared every time when the external controller reads the stall status.

If a stall condition has been confirmed and the related flag bit STEx is set, the behaviour of the circuit depends on the configuration of the STOPx control bit, which is located in the SPI register 1000_b.

- If the STOPx bit is 0_b, a confirmed stall condition does not have any effects on the motor drivers. The external controller is in charge to stop the motor movement. If a stall warning or a confirmed stall condition disappears, the related flags STWx or STEx will be automatically cleared by the logic without further acknowledgement by the external micro-controller.
- If the STOPx bit is 1_b, the confirmed stall condition will stop the stalled motor by turning off the related output drivers. In order to recover from this stall condition, the external controller has to interrupt the continuous step frequency, so that the FSWx flag is set by the frequency supervisor. When FSWx is set, the stall detection logic is disabled and the driver outputs can be controlled again.

In order to allow a combined operation of one or more stepper motors and universal low side driver modes, a separate STOPx control bit is available for each motor. On those channel groups not used for stepper motor control, the related STOPx bit shall be set to 0_b to avoid that the stall detection logic interferes with the driver control.

Stepping Frequency Supervisor

Due to the fact that a constant stepping frequency is a mandatory prerequisite for correct stall detection, the IC comprises a stepping frequency supervisor function, which supports the external controller in finding the suitable point in time to enable stall detection.
When a stable stepping frequency (less than 3% deviation in a frequency range from 100 to 400 steps per second) is reached, the FSWx flag is cleared to 0_b and the stall detection is enabled. If the stepping frequency supervisor function has detected a continuous series of 32 step commutations with sufficiently low variation of their stepping period, the FSWx flag will be cleared. If the variation of stepping periods is too large, this flag will be set.

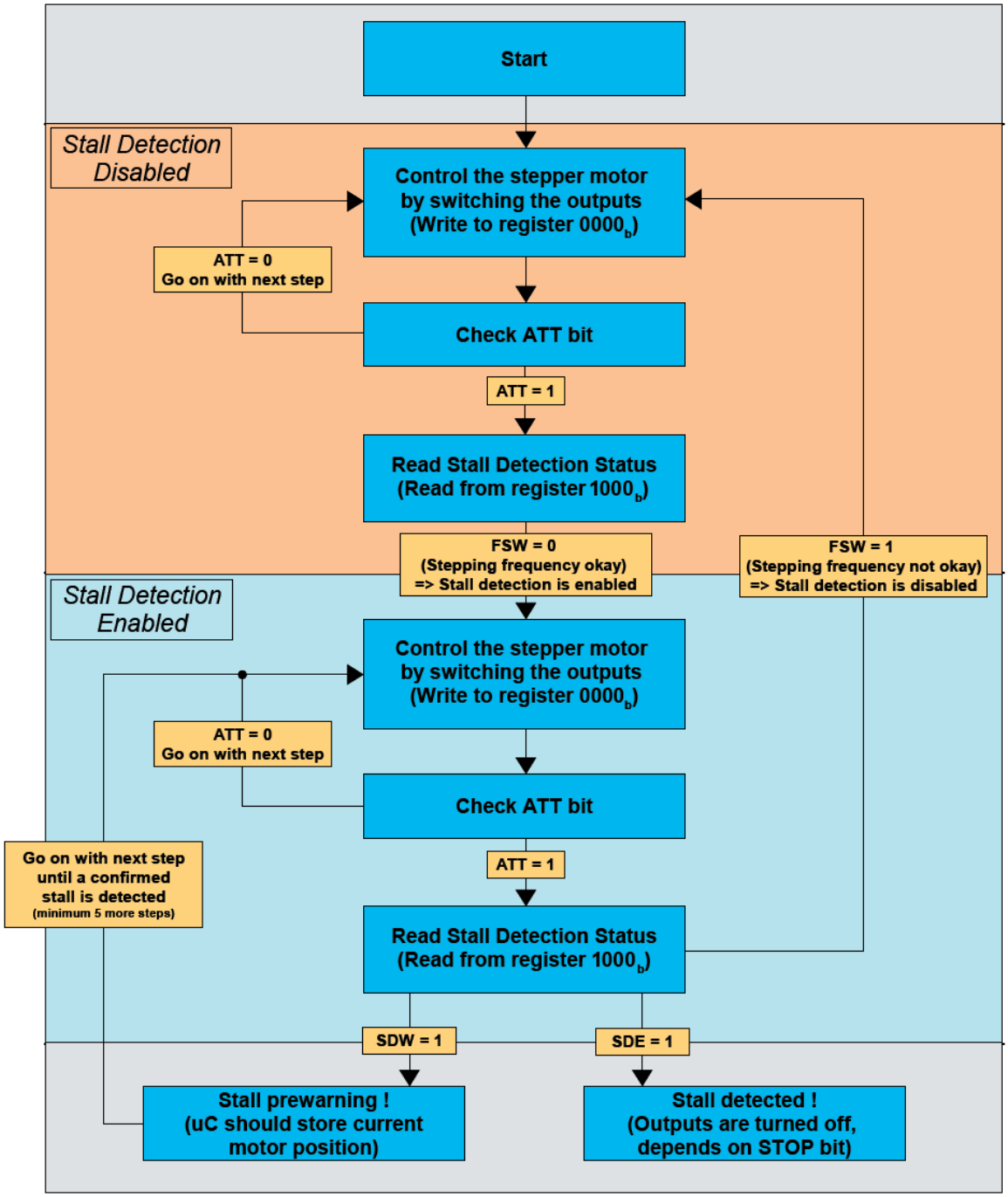


Figure 10. Stall Detection Flowchart

6.7 PWM Output Driving

PWM Source Assignment
Each driver may be controlled only by one out of 3 PWM sources PWMA, PWMB and PWMC. The assignment between the channels and the PWM sources is fixed:

Table 5. PWM Channel Assignment

PWMA	PWMB	PWMC
0	1	2
3	4	5
6	7	8
9	10	11

The pin combination was optimized to drive Three-colour LED applications.
At E520.03 and E520.08 out 8,9,10,11 are not available.
For automotive HVAC systems out 0-7 can be used to drive 2 stepper motors. Out 8,9,10 may be used to drive a 3-color LED for HVAC display illumination.

6.8 Linear PWM Mode

Each of the channels may independently be switched into Linear PWM mode. For this mode three internally clocked PWM sources with the same frequency but independently adjustable duty cycles are implemented.
Recommended configurations for linear pwm mode are:

- PWEx=1_b in SPI register 0011_b to switch the driver into Constant PWM mode PWMAy in SPI register 0110_b, PWMBx and PWMCx in SPI register 0111_b to adjust the duty cycles of PWM sources A, B and C
- LOG=0_b in SPI register 0110_b to select Linear PWM mode

Adjustment of Duty Cycle
In Constant PWM mode 3 PWM sources of the same frequency but several duty cycles are adjustable. These 3 sources A, B and C are independently of each other and may each be adjusted with a resolution of 5 bits.

- PWMX[4:0]=00000_b belongs to 3% duty cycle
- PWMX[4:0]=11111_b belongs to 100% duty cycle (permanently on)

Please note that the effective duty cycle visible on the driver output is additionally affected by propagation delay and slew rates of the power drivers, which guarantee EMC compliant switching behaviour. Duty cycle values stated in this chapter only refer to the digital control signals.

6.9 Smart Relay Driving with $V_{BATsense}$ adapted PWM

The $V_{BATsense}$ adapted PWM mode reduces the power consumption of relays, by driving them with a PWM signal.
There is no need for the external controller to measure the supply voltage and calculate and transfer the optimal PWM duty-cycle to the IC.

The IC itself does this job by measuring the VBAT_SENSE pin.
At low supply voltages the IC drives the relays with 100% duty cycle. At higher-supply voltages the IC automatically limits the effective relay voltage to typ. 11V.

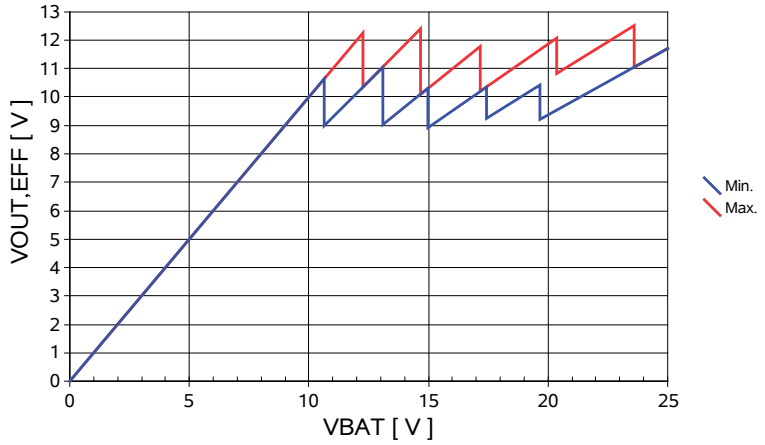


Figure 11. Automatic PWM Generation for Relays

Recommended configurations for relay driver mode are:
- RHEx=1_b in SPI register 0100_b to switch the driver into Adapted PWM mode
- CLMP[1:0]=00_b to use the fixed clamping mode
- OUTx=0_b or 1_b in SPI register 0000_b to activate or deactivate the driver

Comment: If RHEx=1, the states of the PWEx, PWMAy, PWMBy, PWMCy and LOG bits are not relevant for the relevant driver channel. All channels running in $V_{BATsense}$ Adapted PWM Mode are driven with the same frequency (25kHz) and duty cycle.

Relay Pull-In and Hold-Phase
For the Pull-in phase the driver should be driven with
100% duty-cycle (see table below)
After a time the driver may be change to Hold phase by the external controller.

Table 6. Driver Modes

OUTx	RHEx	LS driver mode
1_b	X_b	Permanently off
0_b	0_b	Permanently on in pull-in mode
0_b	1_b	Hold mode with adaptive PWM

Output clamping recommendations
Although the output drivers of the E520.0x IC provide a clamping functionality for inductive loads, an external free wheeling diode to battery voltage level is recommended when using PWM modes with inductive loads.

6.10 Smart LED Driving with Logarithmic PWM Mode

- Duty cycles from 0.1% to 100% can be generated with only 5bit register calculations in the external µC.
- 3 PWM sources for driving 3 - colour – LEDs.

Each LED can be set to constant off, constant on or PWM

PWM frequency is fixed with typically 245Hz. PWM duty cycle is controlled by logarithmic counter characteristic with 5 bit resolution. The logarithmic PWM offers 32 different duty cycle values,.

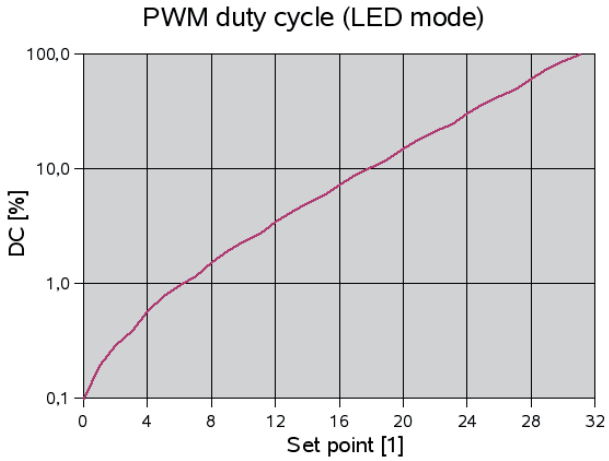


Figure 12. Logarithmic PWM Generation for LEDs with 245 Hz

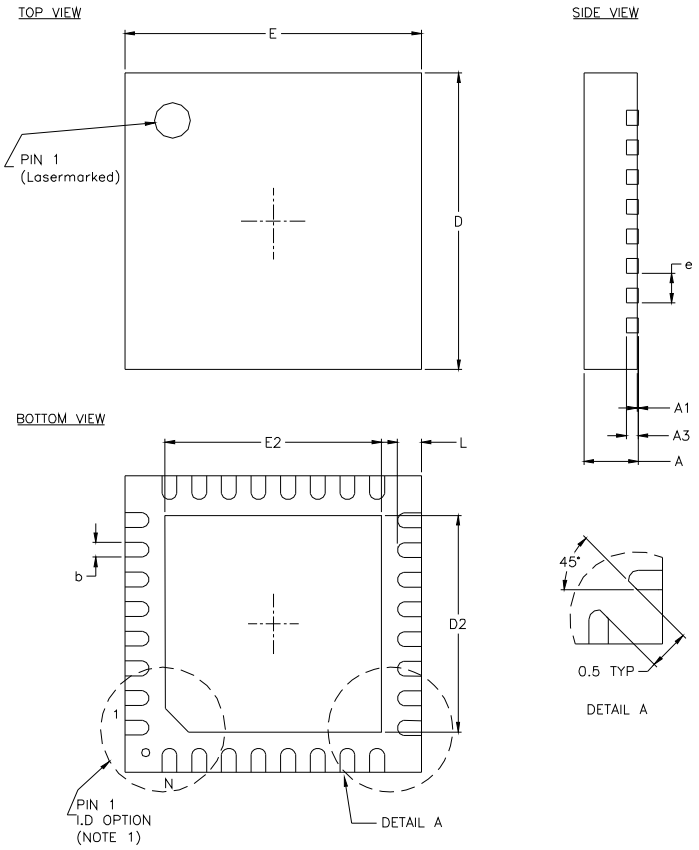
Configurations recommended for LED driver mode:

- RHEx=0_b in SPI register 0100_b to prevent the driver from going into Adapted PWM mode
- PWEx=1_b in SPI register 0011_b to switch the driver into PWM mode.
- PWMAy in SPI register 0110_b, PWMBx and PWMCx in SPI register 0111_b to adjust the duty cycles of PWM sources A, B and C.
- LOG=1_b in SPI register 0110_b to select f_{PWM}=245Hz and logarithmic duty cycle scaling.
- STOPz=0_b in SPI register 1000_b to disable stall detection initiated driver shut-off's,
- OUTx=0_b or 1_b in SPI register 0000_b to activate or deactivate the driver,
- For continuous operation the pull-down current sources should be disabled in order to prevent inactive LEDs from glowing:
  PDEx=0_b in SPI register 0101_b.
- To detect open load conditions the pull-down current sources may be temporarily enabled:
  PDEx=1_b in SPI register 0101_b.
- Either the fixed clamping mode or the "stepper motor clamping mode" may be used:
  CLMP[1:0]=00_b or 11_b in SPI register 0110_b.
- The over-current shut-off may be set to typ. 2ms or typ. 37ms:
  OCC=1_b or 0_b in SPI register 0110_b.

7 Package Information

7.1 QFN32L5

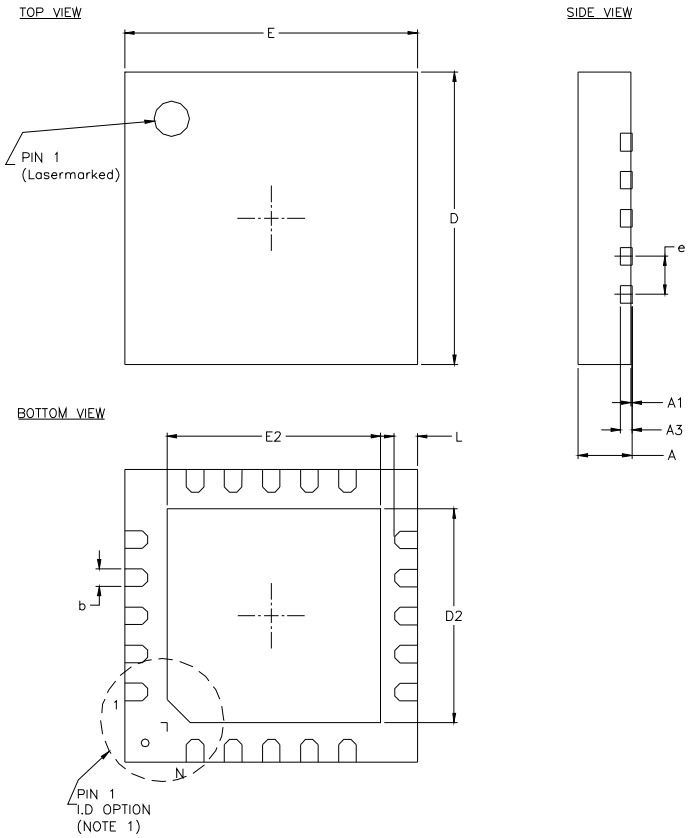
All devices are available in a Pb free, RoHs compliant QFN32L5 plastic package according to JEDEC MO-220 K, variant VHHD-4. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260+5)°C.



Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package Height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand Off	A1	0.00	0.02	0.05	0.000	0.00079	0.002
Thickness of Terminal Leads, Including Lead Finish	A3	--	0.20 REF	--	--	0.0079 REF	--
Width of Terminal Leads	b	0.18	0.25	0.30	0.007	0.010	0.012
Package length / width	D / E	--	5.00 BSC	--	--	0.197 BSC	--
Length / width of exposed pad	D2 / E2	3.50	3.65	3.80	0.138	0.144	0.150
Lead pitch	e	--	0.5 BSC	--	--	0.02 BSC	--
Length of terminal for soldering to substrate	L	0.35	0.40	0.45	0.014	0.016	0.018
Number of terminal positions	N		32			32	

7.2 QFN20L5

E520.03 and E520.08 are available in a Pb free, RoHs compliant package.
Package Outline and Dimensions are not JEDEC conform, compared to the MO-220 K, VHHC-2 this variant has a smaller die pad (2.75mm x 2.75mm).

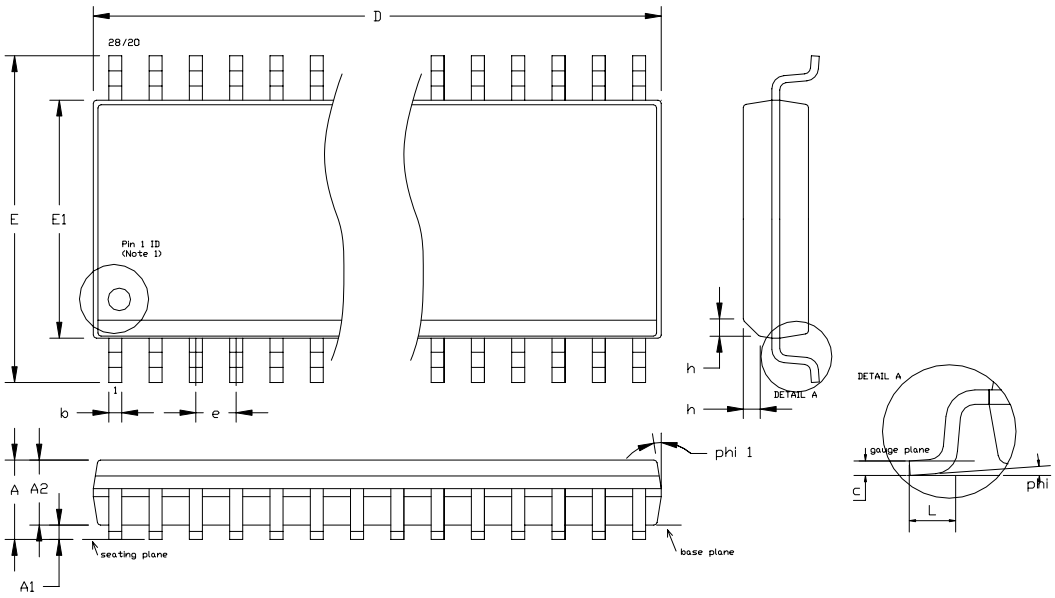


Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package Height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand Off	A1	0.00	0.02	0.05	0.000	0.00079	0.002
Thickness of Terminal Leads, Including Lead Finish	A3	--	0.20 REF	--	--	0.0079 REF	--
Width of Terminal Leads	b	0.25	0.3	0.35	0.010	0.012	0.014
Package Length / Width	D / E	--	5.00 BSC	--	--	0.197 BSC	--
Length / Width of Exposed Pad	D2 / E2	2.60	2.75	2.90	0.102	0.108	0.114
Lead Pitch	e	--	0.65 BSC	--	--	0.026 BSC	--
Length of Terminal for Soldering to Substrate	L	0.35	0.40	0.45	0.014	0.016	0.018
Number of Terminal Positions	N		20			20	

7.3 SOIC20 / SOIC28

E520.03 and E520.08 are available in a Pb free, RoHs compliant SOICW20 plastic package according to JEDEC MS-013-E, variant AE. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260+5)°C.

E520.01 is available in a Pb free, RoHs compliant SOICW28 plastic package according to JEDEC MS-013-E, variant AE. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260+5)°C.



Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package Height	A	--	--	2.65	--	--	0.104
Stand Off	A1	0.10	--	0.30	0.004	--	0.012
Package Body Thickness	A2	2.05	--	--	0.081	--	--
Width of Terminal Leads, Inclusive Lead Finish	b	0.31	--	0.51	0.012	--	0.020
Thickness of Terminal Leads, Inclusive Lead Finish	c	0.20	--	0.33	0.008	--	0.013
Package Length (SOICW28)	D	17.90 BSC			0.705 BSC		
Package Length (SOICW20)	D	12.80 BSC			0.504 BSC		
Package Width	E	10.30 BSC			0.406 BSC		
Package Body Width	E1	7.50 BSC			0.295 BSC		
Lead Pitch	e	1.27 BSC			0.050 BSC		
Length of Terminal for Soldering to Substrate	L	0.4	--	1.27	0.016	--	0.050
Body Chamfer (45°)	h	0.25	--	0.75	0.010	--	0.030
Angle of Lead Mounting Area	phi [°]	0	--	8	0	--	8
Mold Release Angle	phi1 [°]	5	--	15	5	--	15
Number of Terminal Positions	N	20 / 28			20 / 28		

8 Typical Application

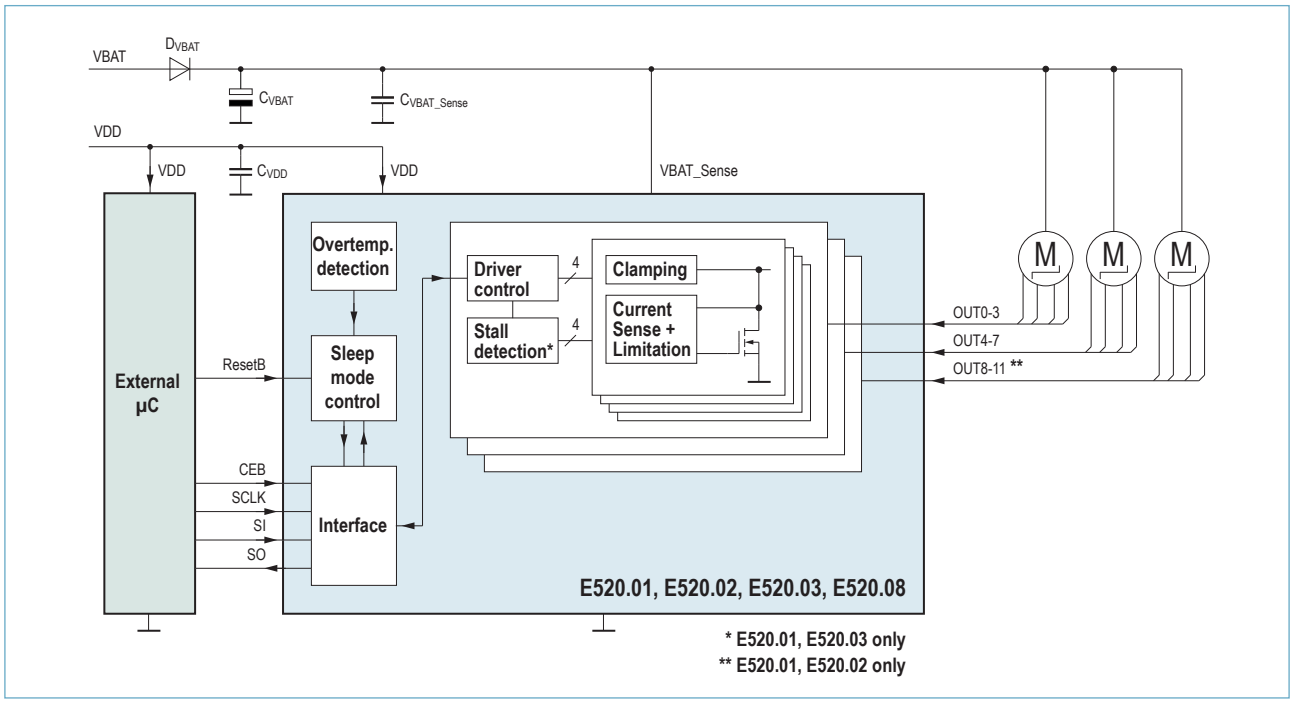


Figure 13. Typical Application Circuit

Table 7. External Components

External Components	Symbol	Typ	Unit
Reverse polarity protection diode	D_{VBAT}	depending on motor load	V
VBAT capacitance	C_{VBAT}	depending on motor load	µF
VDD capacitance	C_{VDD}	100nF ceramic type	nF
VBAT_SENSE capacitance	C_{VBAT_Sense}	100nF ceramic type	nF

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