Triple 150mA Linear LED Controller

E522.80/81/82/83

Preliminary Information - Jun 23, 2015

RoHS compliant

Features

- Three independent Linear Current Drivers (3*150mA)
- Parallel Output Operation for up to 450mA
- Low Power Standby / Sleep Mode
- Thermal Management Option per Channel
- Operating Input Voltage Range 5V to 25V, max. 40V
- External Reference Voltage / Derating Supported
- PWM Dimming (All channels or separate Channels)
- Diagnostic Functionalities (LED Driver Open/Short, IR Config Open/Short, Junction Temperature, Supply Voltage)
- Diagnostic Bus to link ICs
- Selectable “Failure Feedback Mode” or “Single Lamp Behaviour”
- AEC-Q100 Qualification

Applications

- Automotive LED Lighting, Rear Lighting
- Turn Indicator Driver
- Medium Current Interior Lighting
- Industrial LED Applications or RGB Drivers

Ordering Information

Ordering-No.:	$Temp_{Junc}$ Range	Package
E52280A97D	-40°C to +150°C	SOIC16N-EP
E52281A97D	-40°C to +150°C	SOIC16N-EP
E52282A97D	-40°C to +150°C	SOIC16N-EP
E52283A97D	-40°C to +150°C	SOIC16N-EP

General Description

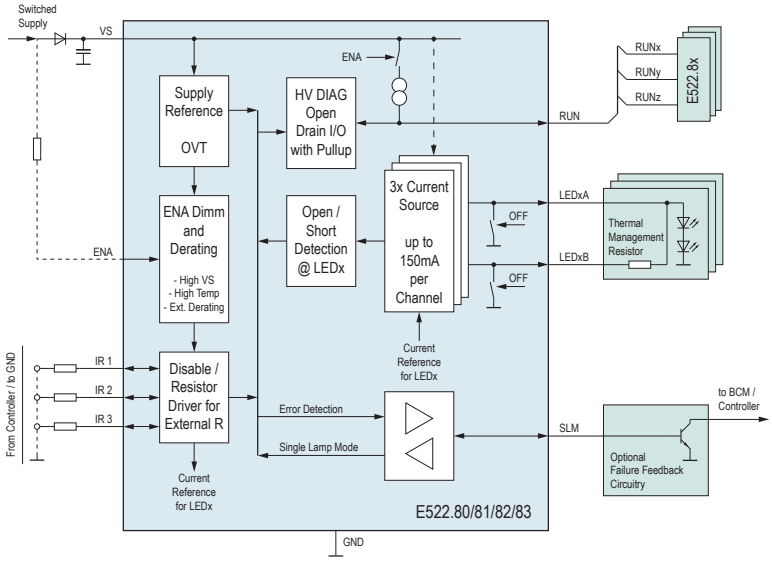
E522.80/81/82/83 family devices provide independent triple linear current controller for LED driving (standalone driver or LED cluster). Diagnostic features are provided to meet automotive requirements, together with a communication interface “RUN” to link ICs to generate more than three channels, supporting individual current configuration and independent digital PWM dimming per channel (e.g. for RGB).

Two external configurable modes of operation allow
- either “Failure Feedback Mode” FFM (operating channels in case of errors, with error signalization)
- or in “Single Lamp Mode” (turning all linked E522.8x´s channels “off” in case of errors)

An intelligent power management system is provided using an external shunt resistor to share power distribution between IC package and external heat sink. Hotspot generation can be avoided by flexible heat spreading on the printed board. Internal derating for reference voltage and over-temperature shutdown for extreme temperatures >180°C protect E522.8x in case of abnormal operation conditions.

A high voltage capable input ENA can be used to either digitally enable or disable E522.8x. In addition, this input may be used as analog reference voltage input to realize e.g. thermal derating.

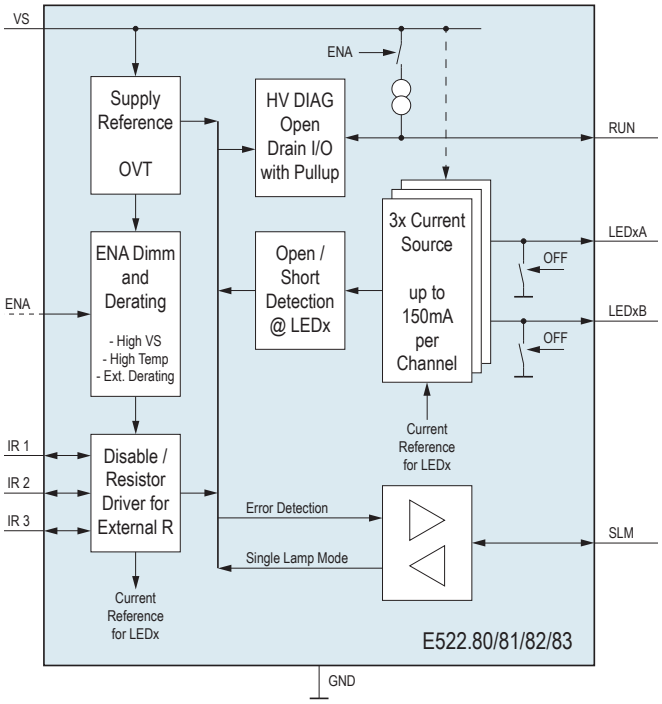
Typical Application Circuit



This document contains information on a pre-production product. Elmos Semiconductor AG reserves the right to change specifications and information herein without notice.

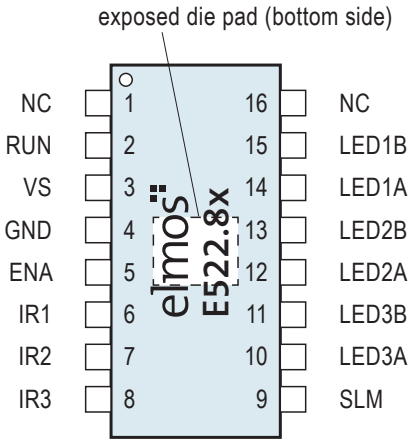
Version	'OPEN' Diagnostic	Package & Current
E522.80	Open Diagnostic at V_{VS} > 7.5V	SOIC16N-EP I_{LED} = 48mA...151mA
E522.81	Open Diagnostic at V_{VS} > 9.0V	SOIC16N-EP I_{LED} = 48mA...151mA
E522.82	Open Diagnostic at V_{VS} > 10.0V	SOIC16N-EP I_{LED} = 48mA...151mA
E522.83	Open Diagnostic at V_{VS} > 15.0V	SOIC16N-EP I_{LED} = 48mA...151mA

Functional Diagram



Pin Configuration

Top View



Note: *Not to scale*

Pin Description

Pin	Name	Type [1)]	Description
1	NC	A_I	Not connected internally
2	RUN	HV_A_IO	RUN Diagnostic Bus Interface to link 522.8x Products
3	VS	HV_S	High-Voltage Supply Input
4	GND	S	Ground Connection
5	ENA	HV_A_I	High-Voltage Enable and optional analog Referencevoltage Input
6	IR1	A_IO	Current Configuration Channel 1, digital Input for Channel 1 dimming
7	IR2	A_IO	Current Configuration Channel 2, digital Input for Channel 2 dimming
8	IR3	A_IO	Current Configuration Channel 3, digital Input for Channel 3 dimming
9	SLM	A_IO	Operating Mode Configuration (“Single Lamp Mode” or “Failure Feedback” Operation)
10	LED3A	HV_A_O	Bypass Output Channel 3, connect to LED directly
11	LED3B	HV_A_O	Priority Output Channel 3, connect to LED via thermal Shunt
12	LED2A	HV_A_O	Bypass Output Channel 2, connect to LED directly
13	LED2B	HV_A_O	Priority Output Channel 2, connect to LED via thermal Shunt
14	LED1A	HV_A_O	Bypass Output Channel 1, connect to LED directly
15	LED1B	HV_A_O	Priority Output Channel 1, connect to LED via thermal Shunt
16	NC	A_I	Not connected internally
-	Exposed Pad		Exposed Pad, Connect to GND for thermal connection

1) A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages referred to VGND. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

No.	Description	Condition	Symbol	Min	Max	Unit
1	VS Pin Voltage		V_{VS}	-0.3	40	V
2	ENA Pin Voltage		V_{ENA}	-0.3	40	V
3	IR1,2,3 Pin Voltage	1)	$V_{IR,x}$	-0.3	5.5	V
4	IR1,2,3 Pin Current		$I_{IR,x}$	-1	1	mA
5	LEDx Current		$I_{LED.x}$	-170	100	mA
6	LEDxA/B Pin Voltage		$V_{LED,x}$	-1	V_{VS}	V
7	RUN Pin Voltage		V_{RUN}	-0.3	V_{VS}	V
8	RUN Pin Current		I_{RUN}	-5	5	mA
9	SLM Pin Voltage		V_{SLM}	-0.3	6.5	V
10	Junction Temperature	Continuous	T_J	-40	150	°C
11	Ambient Temperature	Info Parameter 2)	T_A	-40	125	°C
12	Storage Temperature	Unsoldered Device	T_{ST}	-40	125	°C
13	Power Dissipation	$t_{LIFETIME}$ < 1h	$P_{V,MAX}$		2.5	W
14	Thermal Resistance Junction to Exposed Die Pad	3)	$R_{TH,J-C}$		6	K/W

1) see parameter $V_{IR, CLMP}$ for clamping behaviour

2) consider maximum junction temperature and cooling measures to define ambient operating range

3) Typical thermal resistance to EP is $R_{TH,J-C}$ = 3K/W (not production tested)

2 ESD

No.	Description	Condition	Symbol	Min	Max	Unit
1	ESD HBM Protection at all Pins	1)	$V_{ESD,HBM}$	-2	2	kV
2	ESD CDM Protection at Corner Pins	2)	$V_{ESD,CDM,1}$	-750	750	V
3	ESD CDM Protection at all other Pins	2)	$V_{ESD,CDM,2}$	-500	500	V

1) According to AEC-Q 100-002, Human Body Model, 1.5kΩ resistance, 100pF capacitance.

2) According to AEC-Q 100-011, Charged Device Model, pulse rise time (10% to 90%) <400ps, 1Ω resistance.

3 Recommended Operating Conditions

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Recommended Operating Voltage Range		$V_{VS,OP}$	5	14	25	V
2	Continous Power Dissipation in Package		$P_{V,OP}$			2.2	W
3	VS Capacitance per E522.8x		$C_{VS,OP}$	220	330		nF
4	Nominal Value of Current-Selection Resistor at IR1,2,3 to GND	LED Channel operating [1)]	$R_{IR,x}$	9.53		30	kΩ
5	Capacitance at IRx Pin to drive $R_{IR,x}$		$C_{IR,x}$			100	pF
6	Typical Configured Operating Current per Channel	Sum of LEDxA and LEDxB [1)]	$I_{LED,x}$	48	120	151	mA
7	Dimming Frequency at either ENA or IRx	[2)]	f_{PWM}	50	200	1000	Hz
8	Minimum High / Low pulse- width in case of PWM Dimming		$T_{PULSE,PWM}$	90			µs
9	Total Capacitance for RUN Bus	[3)]	C_{RUN}			1	nF
10	Capacitance at LEDx Driver Outputs	LEDxA and LEDxB	$C_{LED,x}$		6.8	22	nF
11	Inductance at either LEDxA oder LEDxB		$L_{LED,x}$			1	µH

1) If selection interface IR is used with higher resistive values take a reduced accuracy into account. Pay attention to the 'open' state detection limit „IIR,OPEN" for IRx configuration

2) high PWM frequencies need to take into account, that there is an inherent startup delay between rising edge at IRx and current flow, which may influence PWM linearity

3) high capacitance values are possible but lead to additional delay between rising edge at ENA and startup of LEDx Drivers

4 Electrical Characteristics

(V_{VS} = 5V to 25V, T_J= -40°C to 150°C and recommended operating range, unless otherwise noted. Typical values are at V_{VS} = 14V and T_J = 25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
Supply and Bias						
Enable threshold at ENA	V_{ENA} rising	$V_{ENA,ON}$	1.14	1.2	1.26	V
Disable threshold at ENA	V_{ENA} falling	$V_{ENA,OFF}$	1.0	1.06	1.13	V
ENA internal Pulldown Resistor		$R_{ENA,PD}$		500		kΩ
VS undervoltage Release Threshold	VS rising edge	$V_{VS,ERR}$	3.8	4.1	4.4	V
VS undervoltage Hysteresis	VS falling edge	$V_{VS,ERR,HYST}$		440		mV
VS sleep mode Current	V_{VS} = 14V V_{ENA} = 0V $T_J \leq 125°C$	$I_{VS,SLEEP}$		12.5	28	µA
VS current in "Standby Mode"	V_{ENA} > 3V V_{RUN} < 2V No error detected in device [1)]	$I_{VS,STBY,NOM}$		90	140	µA
Average VS Current in "Single Lamp Mode, Counting"	V_{ENA} > 3V "IR Open" error detected by device, SLM open [2)]	$I_{VS,STBY,ERR}$		100	150	µA
Device current consumption (GND pin current)	all channels regulating in saturation, no error detected $I_{LED,x}$ = 120mA	$I_{GND,OP}$		1.4	2.1	mA
Overtemperature Shutdown	T_J rising	$T_{J,OT}$	165	185		°C
Overtemperature Recovery Hysteresis*)	T_J falling	$T_{J,OT,HYST}$		20		°C
Initial Startup Delay of E552.8x after first Power-Up*)	Initial delay after $V_{VS} > V_{VS,ERR}$ $V_{ENA} > V_{ENA,ON}$	t_{START}		30	80	µs
LED Driver						
Current Amplification factor between IRx Input and LEDx Outputs		$A_{I,LEDx/I,IRx}$		960		
Ratio of Current in LEDxB to total configured Current I_{LEDx}	I_{LEDxB} / (I_{LEDxA}+I_{LEDxB}) $V_{VS,LEDxB}$ > 1V	$Q_{B/(A+B)}$	97	99.8		%
LED Current Tolerance (maximum)	R_{IRx} = 9.53kOhm $V_{VS} = V_{ENA}$ = 14V $V_{VS,LEDx}$ > 1V	$I_{LED,MAX}$	-160	-151	-142	mA
LED Current Tolerance (high)	R_{IRx} = 12kOhm $V_{VS} = V_{ENA}$ = 14V $V_{VS,LEDx}$ > 1V	$I_{LED,HIGH}$	-127	-120	-113	mA
LED Current Tolerance (low)	R_{IRx} = 30kOhm $V_{VS} = V_{ENA}$ = 14V $V_{VS,LEDx}$ > 1V	$I_{LED,LOW}$	-54	-48	-42	mA
Drop-Voltage of Bypass Outputs LEDxA for 120mA	I_{LEDxA} = 120mA LEDxB open [1)]	$V_{LEDxA,DROP}$		250	450	mV
Drop-Voltage of Priority Outputs LEDxB for 120mA	I_{LEDxB} = 120mA LEDxA open [1)]	$V_{LEDxB,DROP}$		420		mV
Total pull down Resistance in case of LEDx being turned 'off'	V_{VS} = 14V V_{ENA} = 0V (LEDxA parallel LEDxB)	$R_{LED,PD,OFF}$		10		kΩ

**) Not tested in production*

Notes on table section Supply and Bias

1) See state diagram in chapter „5.4 State Diagram" for details

*2) Please note, that in case of LED or IR shortcircuit the average input current also depends on the configured current and the re-diagnostic dutycycle. Example: In case of a single LED short to GND the current at VS in SLM is typ. approx. 100µA plus 64/5900*I_{LEDx}*

Notes on table section LED Driver

1) Parallel operation of LEDxA/B is possible to reduce Drop-Voltage

Electrical Characteristics (continued)

(V_{VS} = 5V to 25V, T_J= -40°C to 150°C and recommended operating range, unless otherwise noted. Typical values are at V_{VS} = 14V and T_J = 25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
IR Driver						
Internal Nominal Reference to drive R_{IRx}	V_{ENA} > 3.3V $T_J < T_{J,DERATE}$	$V_{REF,NOM}$	1.44	1.5	1.56	V
Internal Reference Derating in case of high V_{VS}	V_{VS} > 29V	$V_{REF,HV}$		0.9		V
Recommended Operating Range for External Reference at ENA [1]	Condition	$V_{REF,EXT}$	0.6		$V_{REF,NOM}$	V
Internal Divider Ratio between ENA and IR in case of external Reference Voltage	1.2V < V_{ENA} < 3V	$N_{ENA,DIV}$		2		
Internal Reference Derating Threshold for high V_{VS}	V_{VS} rising	$V_{VS,DERATE}$	25	27	29	V
Hysteresis for Voltage Derating Threshold	V_{VS} falling	$V_{VS,DERATE,HYST}$		1		V
Starting Junction Temperature for internal Reference Voltage Derating*)	V_{ENA} > 3.3V	$T_{J,DERATE}$	130	139	148	°C
Internal Reference Voltage Derating Slope*)	V_{ENA} > 3.3V $T_J > T_{J,DERATE}$	$dV_{J,DERATE}$		-26.7		mV/K
Disable Threshold at IRx to disable according LED Channel	V_{IR} rising [2]	$V_{IR,DIS}$	1.8	2.4	2.9	V
Hysteresis for IR Disable*)	V_{IR} falling	$V_{IR,DIS,HYST}$		36		mV
Zener Clamping at IRx [3]	I_{IR} = 100µA	$V_{IR,CLMP}$	5.25	6.1	7	V
Pull down Current in IRx Driver for high V_{IR}	V_{IR} = 4V	$I_{IR,PD}$		6		µA
Propagation Delay between Dimming Signal at IR and LED Driver Current Flow*)	V_{ENA} > 3V V_{IR} falling edge [4]	$t_{IR,DEL}$		5		µs
SLM Interface						
Pull down Current in SLM to drive 'low'	Device nominal operation V_{SLM} = 0.7V	$I_{SLM,PD}$		15		µA
Pull up Current in SLM to drive SLM 'high'	Error detected in Device V_{SLM} = 0.7V	$I_{SLM,PU}$		- 250		µA
Threshold to detect Mode of Operation	[1]	$V_{SLM,HIGH}$	1.4	1.5	1.6	V
PWM Frequency at SLM for Failure Signalization in FFM	$V_{SLM} < S_{SLM,HIGH}$ Failure Feedback Mode	$f_{FFM,PWM}$		3.9		kHz

**) Not tested in production*

Notes on table section IR Driver

1) Take 2:1 divider at ENA into account

2) Intended for digital Control with switched GND Potential of RIR,x

3) An unused channel may be disabled by connecting to VS via a suitable Resistor

4) Disable propagation delay of a channel is typ. < 1µs (V_{IR} rising to > $V_{IR,DIS}$)

Notes on table section SLM Interface

1) For "Failure Feedback Mode" connect e.g. bipolar transistor to SLM, otherwise leave open for "Single Lamp Mode"

Electrical Characteristics (continued)

(V_{VS} = 5V to 25V, T_J= -40°C to 150°C and recommended operating range, unless otherwise noted. Typical values are at V_{VS} = 14V and T_J = 25°C. Positive currents flow into the device pins.)

Description	Condition	Symbol	Min	Typ	Max	Unit
RUN Interface and Diagnostics						
RUN Pin Pull up Current to VS	V_{VS} = 14V V_{RUN} = 0V	$I_{RUN,PU}$		- 40		µA
RUN Bus Comparator, High Threshold		$V_{RUN,ENA}$	2.7	3	3.3	V
RUN Bus Comparator, Low Threshold		$V_{RUN,STBY}$	2.25	2.55	2.85	V
Hysteresis for RUN Thresholds	$V_{RUN,ENA}$ - $V_{RUN,STBY}$	$V_{RUN,HYST}$	250	450		mV
RUN State Change Debouncing*)	Rising and falling edge	$t_{RUN,DEL}$		4		µs
RUN Low Level, Nominal	V_{VS} = 14V I_{RUN} = 2mA	$V_{RUN,DRV1}$		0.2	0.8	V
RUN Low Level, low VS or VS Open	VS Pin 'open' I_{RUN} = 2mA T_J < 125°C	$V_{RUN,DRV2}$		1.4	2	V
Current Limitation for RUN driving 'low'	V_{RUN} = 5V	$I_{RUN,LIM}$	10	22		mA
LEDx Short Circuit Detection Threshold	Relative to V_{GND}	$V_{LEDx,SHORT}$	0.9	1	1.1	V
Open Detection Threshold at LEDx, relative to nominal configured current	R_{IRx} = 12kΩ V_{ENA} > 3V [1]	$I_{LEDx,OPEN}$	27.5	37.5	47.5	%
Open Diagnostic Enable Threshold at VS for E522.80	E522.80 [1] V_{VS} rising	$V_{VS,DIAG1}$	7.1	7.5	7.9	V
Open Diagnostic Enable Threshold at VS for E522.81	E522.81 [1] V_{VS} rising	$V_{VS,DIAG2}$	8.55	9	9.45	V
Open Diagnostic Enable Threshold at VS for E522.82	E522.82 [1] V_{VS} rising	$V_{VS,DIAG3}$	9.5	10	10.5	V
Open Diagnostic Enable Threshold at VS for E522.83	E522.83 [1] V_{VS} rising	$V_{VS,DIAG4}$	14.2	15	15.8	V
Open Diagnostic Enable Threshold at VS, Hysteresis	V_{VS} falling	$V_{VS,DIAG,HYST}$		0.5		V
IRx Pin Open Diagnostic Threshold	absolute value	$I_{IR,OPEN}$		9	18	µA
IRx pin short circuit Diagnostic Threshold	absolute value	$I_{IR,SHORT}$	280	380		µA
Error Tolerance after Enabling a Channel	V_{ENA} > $V_{ENA,ON}$ V_{IR} < $V_{IR,DIS}$ [2]	$t_{ERR,DEB1}$		64		µs
Additional Debouncing Time in case of Error Detection during Operation*)	New Error de-tected	$t_{ERR,DEB2}$		4		µs
Re-Diagnosis time out in case of Error Detection	ERR present, E522.8x operated undimmed [3]	$t_{ERR,REDIAG}$	4.1	5.9	9.1	ms

**) Not tested in production*

Notes on table section RUN Interface and Diagnostics

1) threshold is related to nominal current generated at IRx input. This diagnosis is active for VVS voltages higher than VVS,DIAGx

2) start up of a channel is performed within this tolerance time window

3) dimming the erroneous channel resets the according channels re-diagnostic cycle, thus a re-diagnostic is performed with the next enabling of the channel

5 Functional Description

5.1 Overview

E522.80/81/82/83 family devices provide independent triple linear current controller for LED driving, which can optionally be operated in parallel for higher current requirements. These family members support individual current configuration and independent digital PWM dimming per channel (see IR interface).

Various diagnostic features are provided to meet automotive requirements, together with a communication interface named "RUN" to link ICs to generate more than three channels. ICs linked in this way can be operated as a combined cluster of drivers, turning 'on' and 'off' in parallel (e.g. turning all drivers 'off' in case of hardware failures).

Two external configurable modes of operation allow
- either "Failure Feedback Mode" FFM (operating channels in case of errors, with error signalization)
- or in "Single Lamp Mode" (turning all linked E522.8x´s channels "off" in case of errors)

Typical exemplary application topologies are presented in „5.8 Exemplary Application Topologies".
More information on the LEDx drivers and power management can be found in „5.2 LED Driver".
For more details on the configuration and dimming via IRx interface see „5.3 IR Driver".
A detailed overview of functional states is given in „5.4 State Diagram".
Configuration of FFM or Single Lamp Mode is described in „5.5 SLM Interface".
Diagnostic features are located in „5.6 RUN Interface and Diagnostics".

Family members for lower current applications are provided as products E522.84/85/86/87, providing a high degree of functional compatibility to E522.80/81/82/83 at e.g. "RUN" pin. See the according data sheet for more details on these products.

5.2 LED Driver

High side drivers for LEDx provide the current configured by the according IRx pin, reproducing the IIRx with a typical amplification factor of 960:1. In E522.8x there are redundant outputs LEDxA and LEDxB to provide this current. These pins are intended for advanced thermal management (see Typical Application Diagram), sharing IC power with an external power sink as follows:

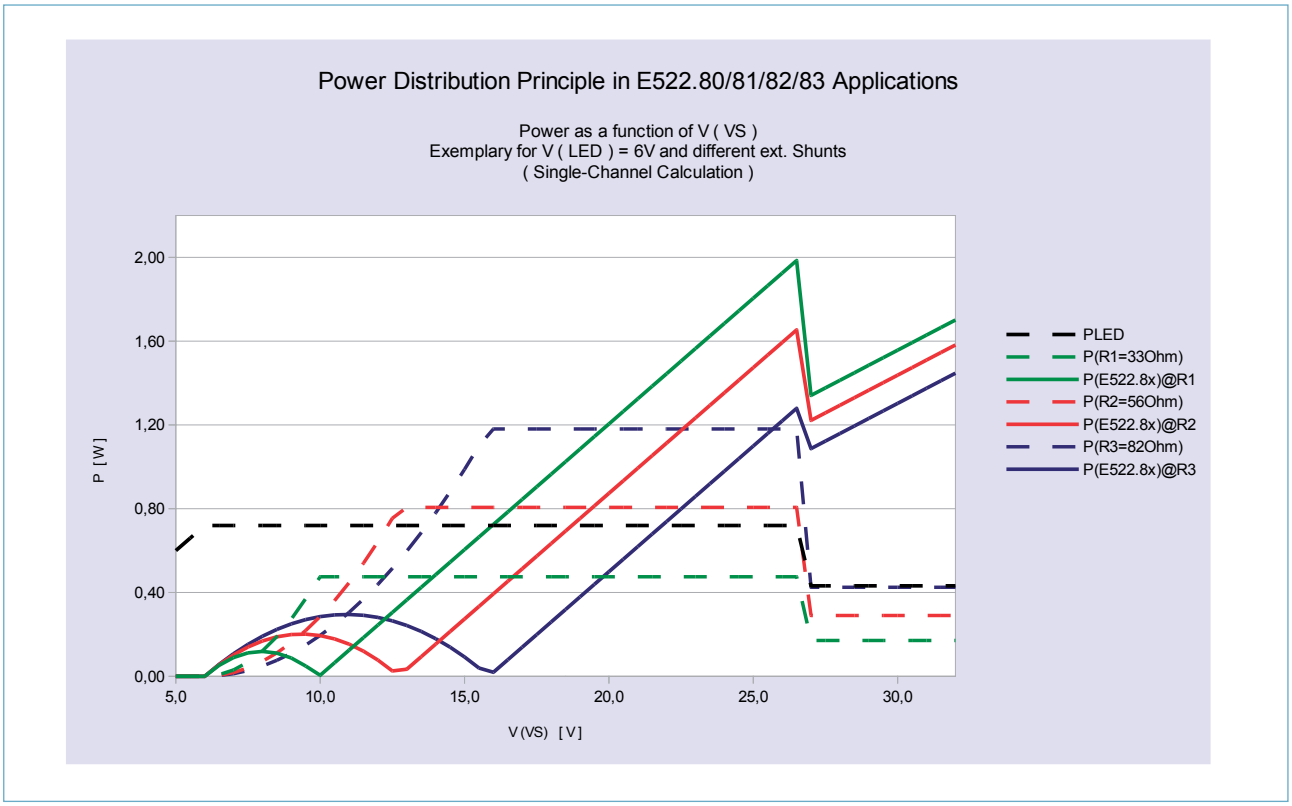


Figure 1. Power Management Example using a Channel of E522.8x at 120mA

To handle the high power that is typically generated in linear LED drivers, the 522.80/81/82/83 device family offers an advanced power distribution feature. The channels current is regulated as a sum of currents in LEDxA and LEDxB. The priority output LEDxB drives the current as long as the voltage headroom allows to. Afterwards the bypass output LEDxA is activated to deliver the remaining current flow.

This distribution of current allows to share some of the linear regulator power with the external Power-Shunt. „Figure 1. Power Management Example using a Channel of E522.8x at 120mA“ shows the basic power generation per channel in (as a function of V_{VS})
- the LED load driven
- the external power shunt, given for exemplary values R1=33Ω, R2=56Ω, R3=82Ω
- the remaining power for this channel in E522.8x

For calculation, this principle offers two points of “zero” power in E522.8x, one for the $V_{VS,Z1} = V_{LED}$ and a second “zero” power point at $V_{VS,Z2} = V_{LED}+I_{LED}*R_{POWERSHUNT}$. Beyond $V_{VS,Z2}$ the power in E522.8x starts to increase linearly as for common linear LED drivers.

At the voltage derating threshold $V_{VS,DERATE}$ the internal reference is reduced to 60% of nominal, thus the overall system power is reduced as shown to avoid excessive heat generation in case of e.g. load dump pulses.

5.3 IR Driver

The interface IRx is used to configure the current in the according LEDxA/B channel. By connecting the IRx input to GND potential, the current flow in IRx is multiplied to LEDxA/B by a factor of typical 960:1.

Digital dimming can be applied to IRx by setting $V_{IRx} > V_{IR,DIS}$. A simple option to control the current is to switch the GND connection of R_{IRx} by a micro controller port, thus ‘low’ level drives the current into IRx, the high level disables the according channel.

Various factors influence the reference voltage driven to IR as an output. Details are illustrated in Figure 2.
In nominal case (typical junction temperature, $V_{ENA} > 3V$) the internal reference is used. The lowest reference applied to the amplifier shown in Figure 2 is used to regulate V_{IR}.

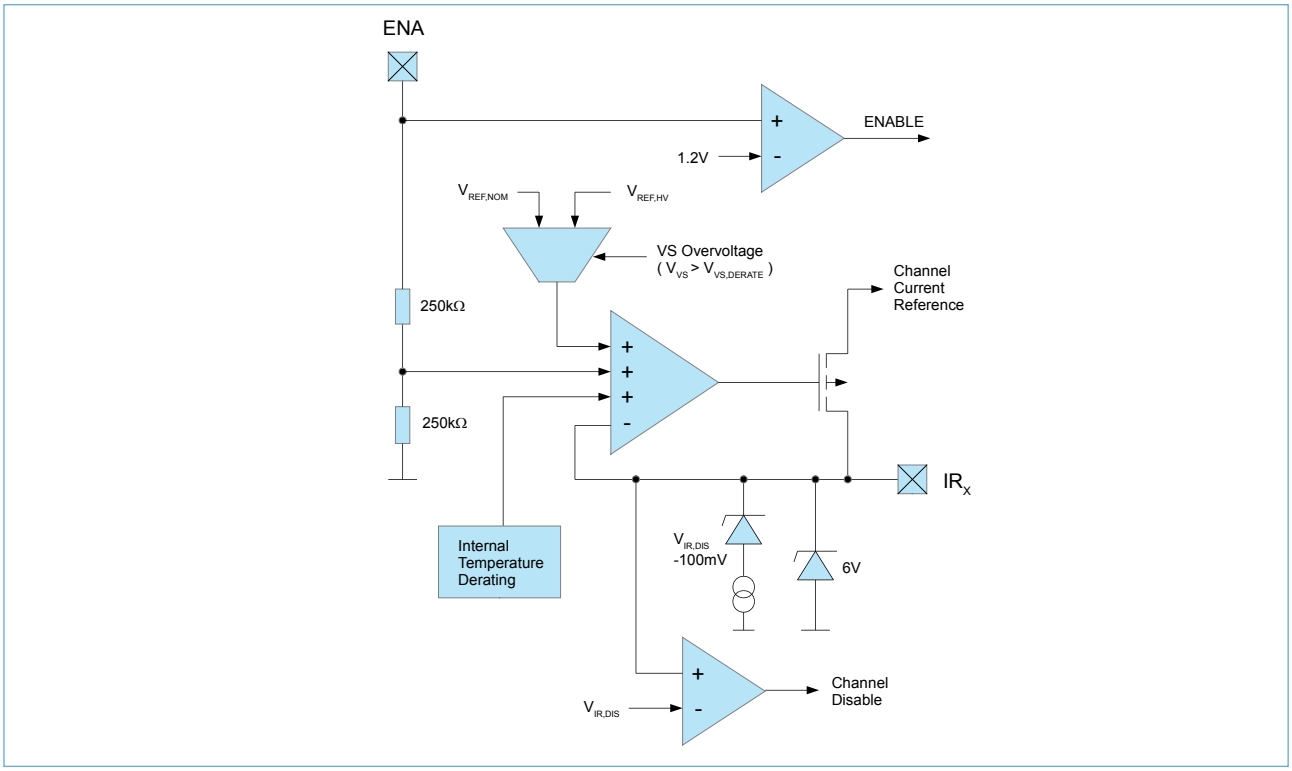


Figure 2. IR Reference Generation

In case that less than three current drivers are needed, the internal clamping as shown in „Figure 2. IR Reference Generation“ allows to connect this input to e.g. VS directly by a resistor of typ. 100kΩ.
Note that this resistor will contribute to the overall sleep mode or standby current of the application.

Connecting the IRx inputs statically to other supply voltages $V_{SUPPLY} > V_{IR,DIS}$ is also possible to effectively disable the according channel. Please note, that the maximum supply voltage to turn IRx 'off' may be restricted by the clamping voltage at this pin, see parameter „VIR,CLMP“.

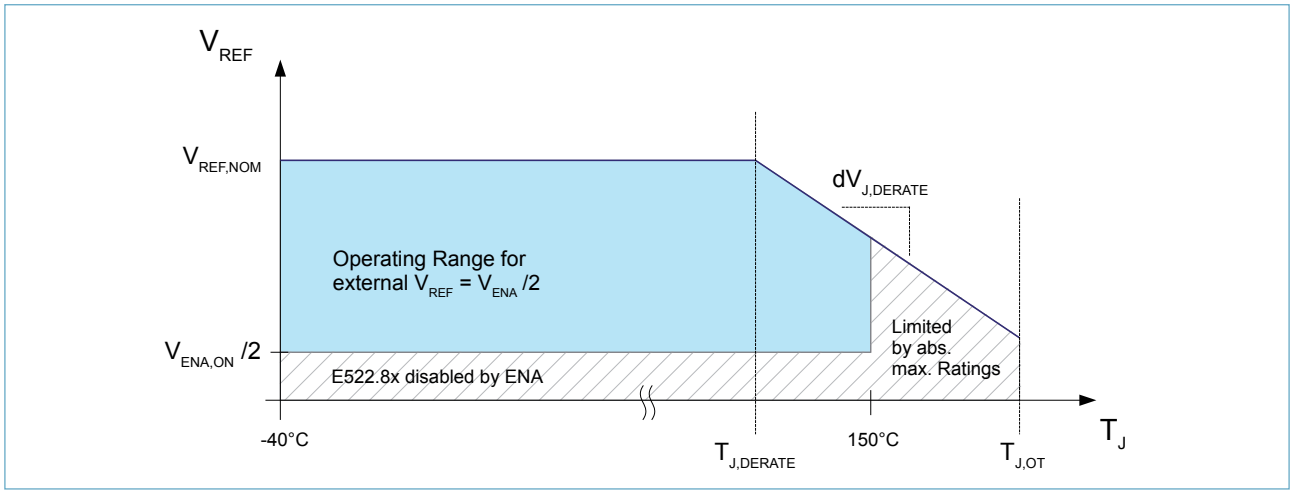


Figure 3. Principle of Internal Temperature Derating

The internal reference derating function implemented is rather tolerant to allow external configuration of derating by the user. It typically starts to derate the internal reference at T_J = 138°C, falling with typ. -26.7mV/K beyond this temperature. The range of operating E522.8x with external reference or external derating is shown in „Figure 3. Principle of Internal Temperature Derating“.

To realize an external derating function and shut down, it is possible to use e.g. a temperature dependent resistor divider at ENA. In the range of typically 3V down to $V_{ENA,OFF}$ the voltage VENA/2 is used to drive V_{IR}. Falling below $V_{ENA,OFF}$ disables E522.8x, restarting with $V_{ENA,ON}$.

5.4 State Diagram

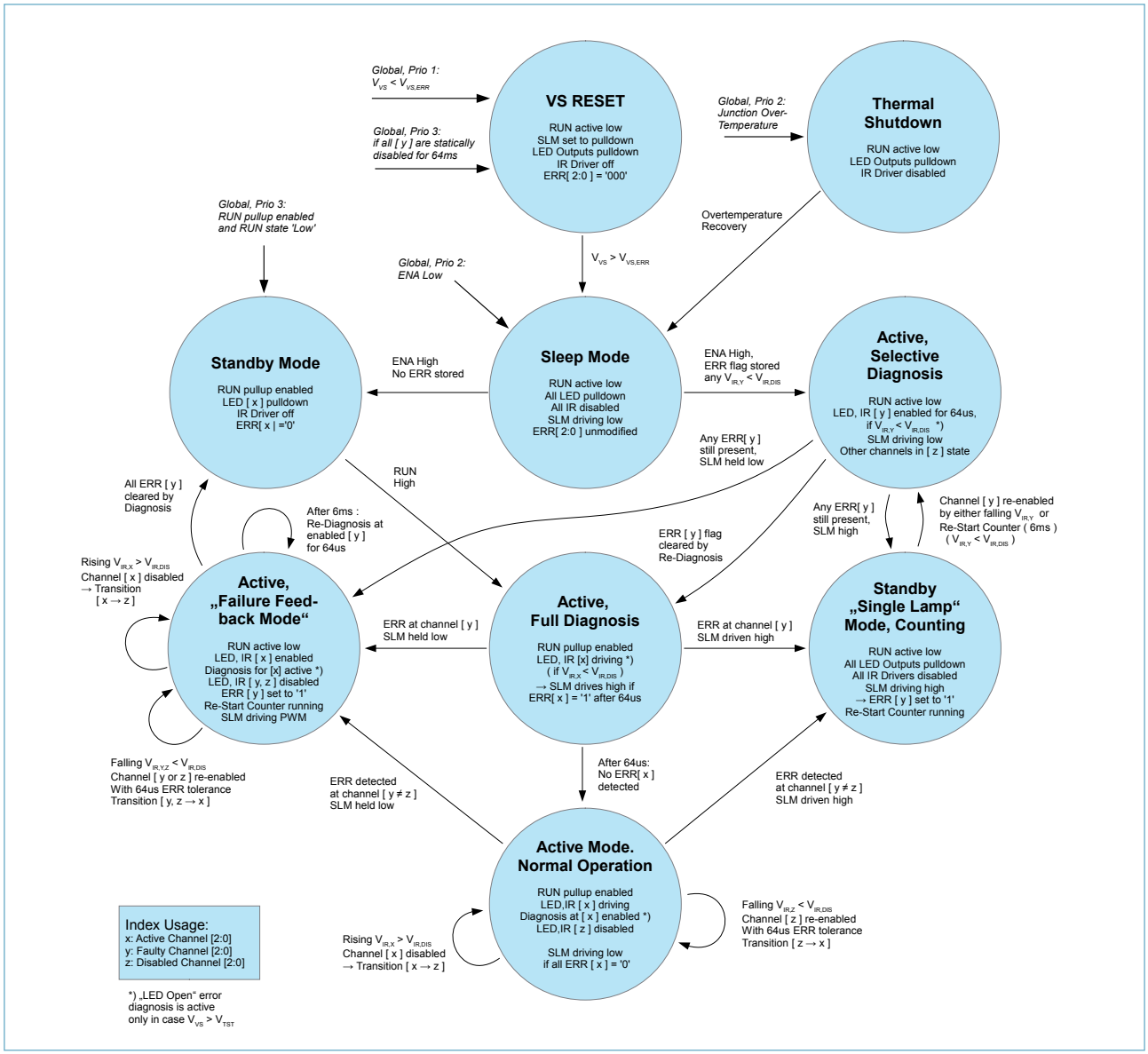


Figure 4. State Diagram E522.80/81/82/83

5.5 SLM Interface

The pin SLM ("Single Lamp Mode") can be used to distinguish between single lamp behaviour or failure feedback mode (FFM). The basic setup of this pin is shown in „Figure 5. SLM Configuration".

Single Lamp Mode is characterized by switching all channels 'off' in case of a single failure on any channel. This behavior allows a network of LEDs to behave in a comparable manner to single bulb lamp. Other E522.8x devices should be connected by RUN to each other to allow switching other ICs to standby mode as well.
To operate E522.8x in this way, the pin SLM has to be left open, thus the voltage level V_{SLM} exceeds $V_{SLM,HIGH}$.

Failure Feedback Mode (FFM) is used to provide status feedback to some external circuitry, e.g. a microcontroller or a body control module. In this mode of operation a failing channel can be indicated, thus the other channels are not affected by the error detection and remain operated. This mode can as well be used in case of applications for which the diagnostics of channels must not affect other channels.

To use E522.8x in this way, it is recommended to use a bipolar external device and connect its base to SLM (a direct connection of SLM pin to GND is possible as well if channels shall be made independent of eachother). The threshold VSLM,HIGH is high enough to detect SLM as being held low by the base-emitter voltage of the external bipolar device. Other E522.8x in the application can share the same bipolar base to reduce device count (wired-OR).

Note, that RUN is switched to low in this case as well, thus a direct connection to other E522.8x is not recommended in FFM. (Remark: FFM can also be achieved by connecting SLM directly to GND).

More detailed information on the behavior of E522.80/81/82/83 can be found in the statediagram in „Figure 4. State Diagram E522.80/81/82/83".

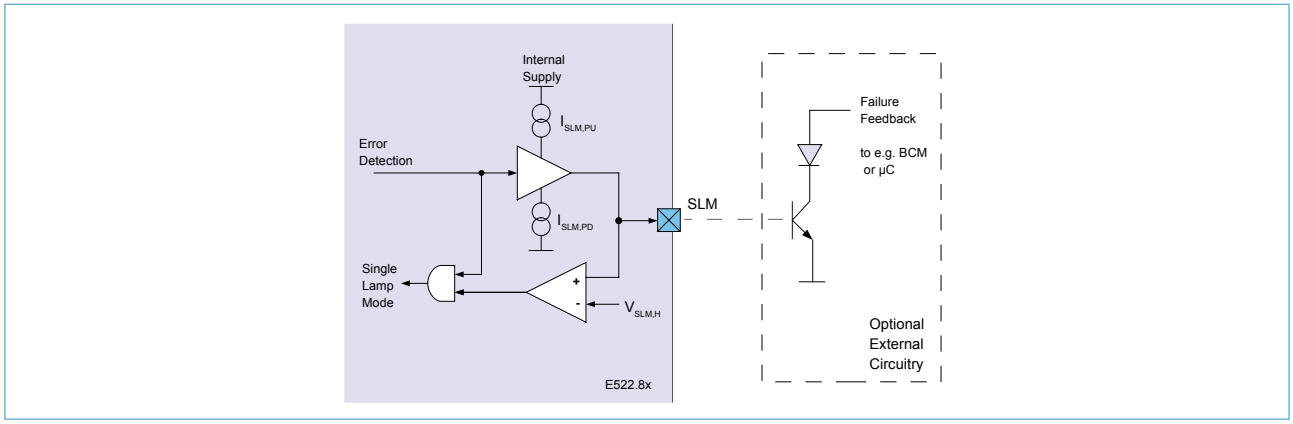


Figure 5. SLM Configuration

During "Failure Feedback Mode" a 4 bit pulse-width modulated (PWM) signal is provided at the SLM output to determine which channels are failing. This protocol is repeated typically every 256µs (typ. 16µs bit-time), representing the actual ERR[2:0] state at the start of the PWM cycle.

The falling edge at SLM between typ. 56.3% and 93.8% represents the ERR[2:0] register status (only for enabled channels - disabled channels or channels without failure are treated as '0' in this PWM, see table below. Remark, a potential failure flag remains stored internally for re-diagnosis)

Note, that if all channels are disabled by IR dimming, SLM provides a static 'high' level (all ERR[2:0] entries are blanked by dimming). If the 'off' condition at IR is applied to a channel for typical >64ms, the according entry in ERR[2:0] register is reseted, see also chapter „5.6 RUN Interface and Diagnostics".

For physical layer implementation, make sure the output level is limited to avoid detection of SLM operating mode, e.g. by using an external NPN bipolar transistor per E522.8x („Figure 5. SLM Configuration").

Table 1. PWM Dutycycle Reference Table

PWM Dutycycle	ERR[2], channel LEDx3	ERR[1], channel LEDx2	ERR[0], channel LEDx1
100%	'0'	'0'	'0'
93.8%	'0'	'0'	'1'
87.5%	'0'	'1'	'0'
81.3%	'0'	'1'	'1'
75.0%	'1'	'0'	'0'
68.8%	'1'	'0'	'1'
62.5%	'1'	'1'	'0'
56.3%	'1'	'1'	'1'

Digital '0' represents either correct operation at LEDx or disabled channels ($V_{IR,x} > V_{IR,DIS}$)

Example A: PWM in case of channel LEDx2 failure detection (all channels enabled):
ERR[2:0] = '010' (no failures blanked by dimming at IRx)
=> PWM Dutycycle of 87.5%

Example B: PWM in case of channel LEDx2 & LEDx3 failure detection (channel LEDx2 disabled):
ERR[2:0] = '110' (failure at channel 2 is blanked by dimming, thus the relevant register value becomes '100')
=> PWM Dutycycle of 75.0%

5.6 RUN Interface and Diagnostics

Diagnostic features provided in E522.8x include the monitoring of

- High resistive IRx drivers for each channel (e.g. in case of 'open' connection for any of the connected devices)
- Short-circuit at IRx drivers to GND for each channel
- Short circuit of LEDxA/B to GND for each channel (checking for a static threshold of $V_{LEDx,SHORT}$)
- Open LEDxA connections for each channel (E522.8x family members provide different thresholds of VVS to enable this monitor, thus avoiding wrong 'OPEN' error detection in case V_{VS} is smaller than the forward voltage of the LEDs (V_{LED})
- Internal junction overtemperature (disabling all channels)
- V_{VS} voltage monitoring for undervoltage (providing defined behavior for slow supply ramping)

The driver "OPEN" detection is relative to the actual current configured at IRx. This detection is active if the supply V_{VS} is higher than $V_{VS,DIAGx}$, which is a family member specific threshold.

If a defect at any of the channels is detected, it is stored for selective re-diagnosis. Dimming at either ENA or V_{IR} does not delete this information. A diagnosis cycle showing removal of the erroneous conditions, VS under-voltage or permanent disable of all failing channels via IR input (see below) resets the stored flag(s) to '0'.

Erroneous channels can be deactivated and removed from state consideration by setting the according $V_{IR,y} > V_{IR,DIS}$. Once the disable request exceeds a length of typ. 64ms (in any mode other than 'Sleep Mode' or 'VS Reset'), the channel will no longer be considered for SLM or FFM state. In this way, e.g. a SLM application may be re-enabled (without the erroneous channel). For details see statediagram, global transitions into VS_RESET state.

Re-diagnosis in case of continuous operation is performed on a regular time-basis of $t_{ERR,REDIAG}$ to allow replacement of defect loads / LEDs for such applications.

A loss of VS connection for a single E522.8x is propagated via RUN being set to low, as well as for ENA being 'low' (e.g. in case of 'OPEN' failure at ENA).

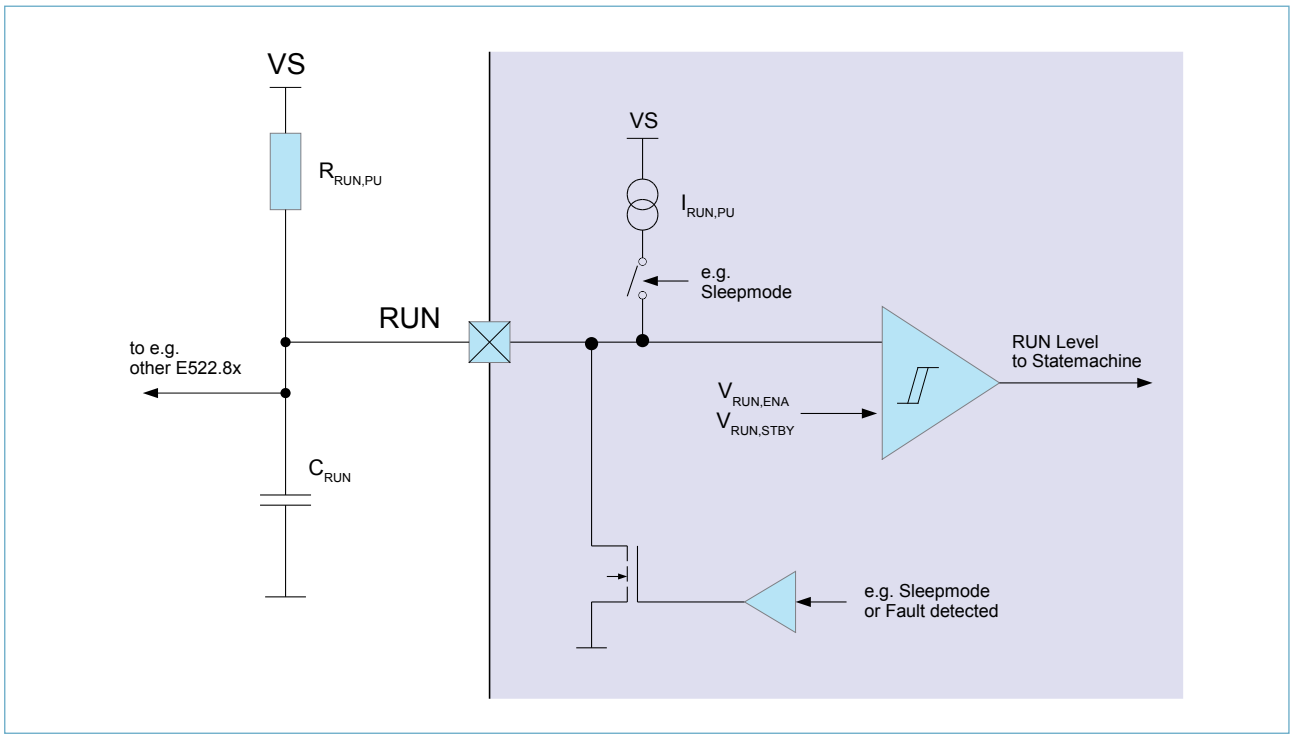


Figure 6. RUN Interface

The basic structure of the RUN interface is shown in Figure 6. Please note, that the purpose of the RUN bus is to form a direct connection to other family members E522.8x or local circuitry, preferably on the same PCB. In that case or if RUN is unused, the components C_{RUN} and $R_{RUN,PU}$ may be omitted. They are recommended to protect the bus for additional requirements (e.g. EMC). The interface itself is not suitable for usage in a wiring harness without adequate protective measures.

The limits for usable values for C_{RUN} and $R_{RUN,PU}$ are given by the tolerable delay at startup or from standby together with the current limitation for the RUN interface (see „RUN Interface and Diagnostics“). Furthermore, $R_{RUN,PU}$ can contribute to sleepmode current consumption due to RUN being driven active low in this case.

5.7 Typical Performance Figures

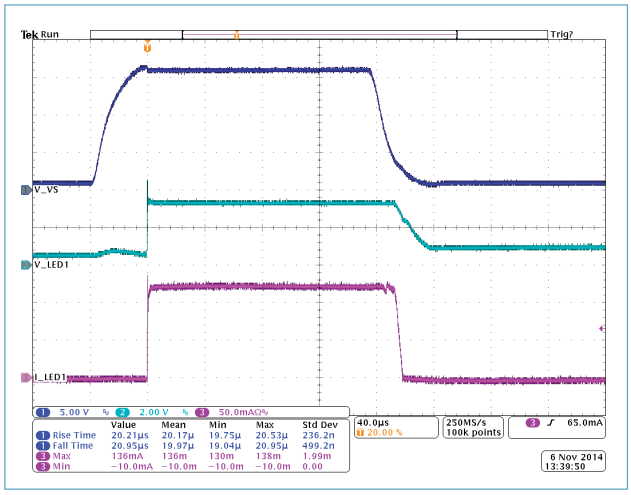


Figure 7. Fast Supply Step (Startup)

Typical Startup from unsupplied to 16V, Delay to deliver current is <40µs.
Dark-Blue: VS-Supply, Bright-Blue: LED voltage, Purple: Current Probe for LED current

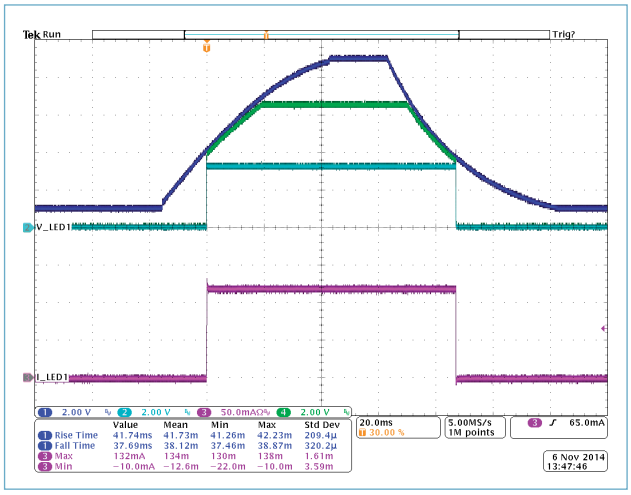


Figure 8. Slow Supply Ramping

Ramping of Supply in >20ms. Green and bright-blue channels show the primary and secondary LED driver outputs, dark-blue is the supply voltage at VS. Purple Curve is the according current probed.

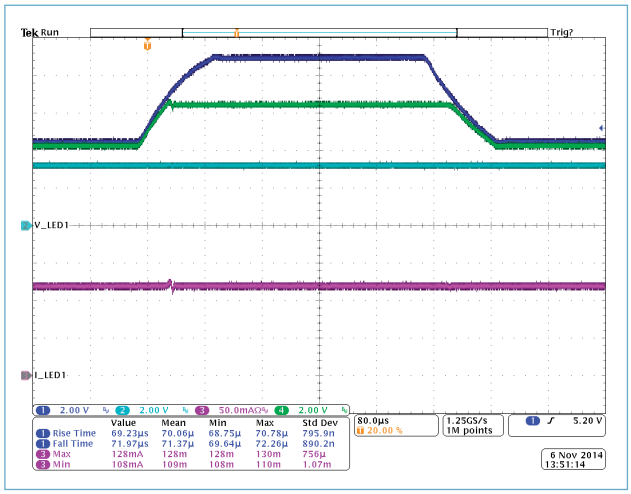


Figure 9. Fast Channel Switch-Over LEDA & LEDB

Switch-over between primary and bypass channel.
Dark-Blue: Supply at VS, Green: LED primary driver, Bright-Blue: Bypass Driver (LED Voltage), Purple: LED Current

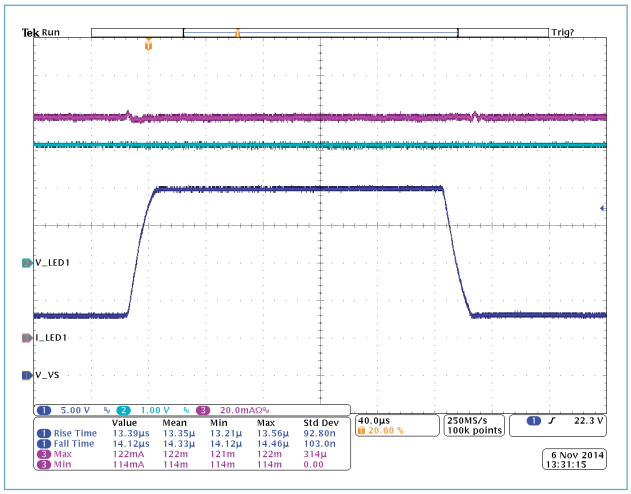


Figure 10. Very fast VS Stepresponse (8V to 25V)

Very steep rising and falling VS Supply,
8V to 25V at VS, Risetime approx. 14µs.
Purple Channel: LED Current
Bright-Blue Channel: LED Voltage
Dark-Blue Channel: VS Supply Voltage (Step)

5.8 Exemplary Application Topologies

This chapter provides various exemplary Application topologies and use-cases for E522.80/81/82/83. From basic setup to full automotive setup there are typical options given, which of course can be combined to more complex systems. Please make sure, that examples taken from this chapter fulfil your application requirements.

5.8.1 Basic Application Topology

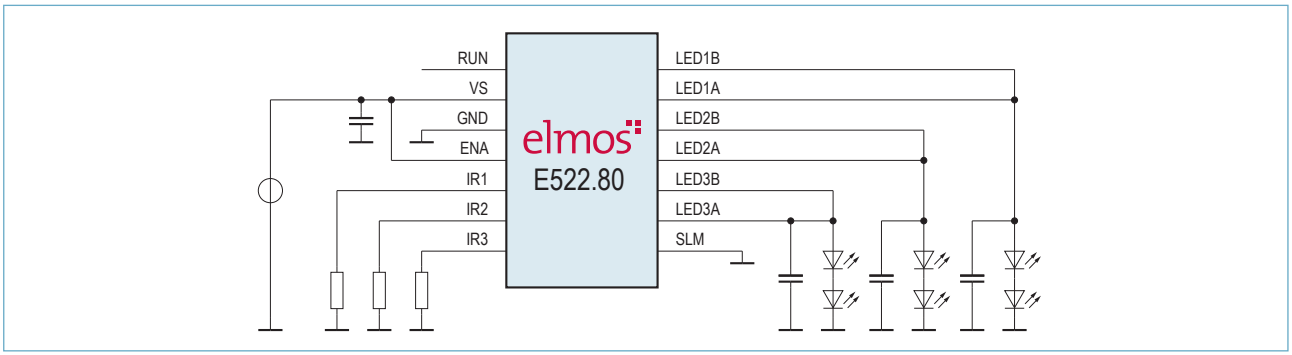


Figure 11. Basic Topology

This is an exemplary basic implementation using E522.80/81/82/83 Family members. The basic features are

- Permanent operation of all LED strings
- Individual current configuration for each LED String
- Channels diagnostic does not interfere between channels (FFM mode used - see SLM pin and RUN pin open)
- Capacitors at the LED loads are used to improve PSRR of the circuit

5.8.2 Basic µC RGB Setup

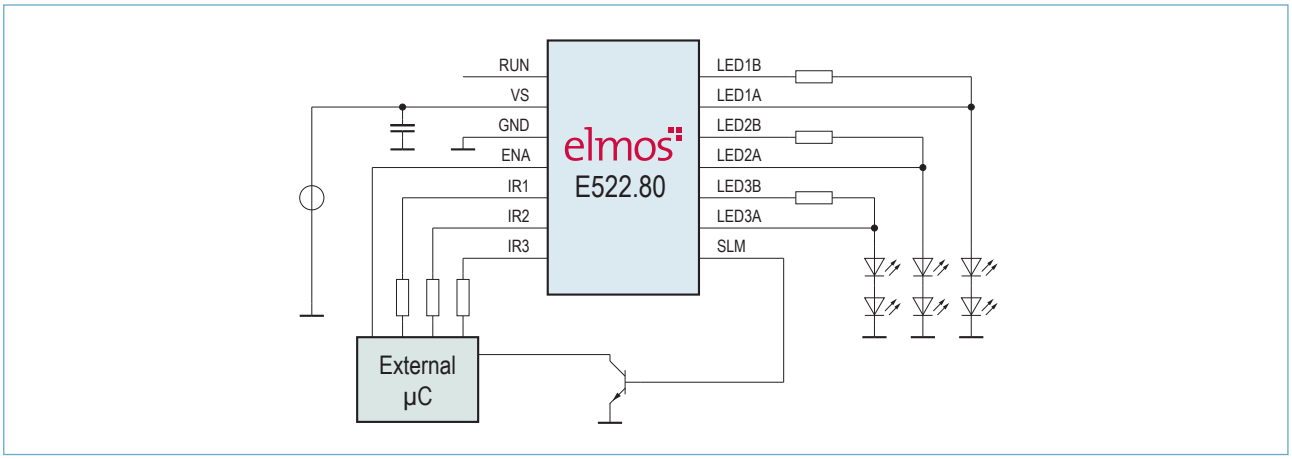


Figure 12. RGB µC Topology

RGB driving is possible using the individual current configuration per channel of the LEDs via IR. An additional µController drives the resistors to GND (enable of channel) or to its supply (disable of channel).

- External controller provides colour mixtures by dimming at either IR1,2,3 or ENA
- Optionally, instead of digital signals, an analog reference can be generated by the controllers DAC to the ENA pin (with respect to the input impedance of ENA)
- Diagnostic feedback is provided from SLM by failure-feedback mode, indicating potential issues for a channel via PWM signal. In this way e.g. redundancy can be build for the colours, compensating a single channel fail with another LED string

Hint: Make sure, that the voltage drop across the controller ports is low to make sure, that reference current remains accurate.

5.8.3 Six Channel Cluster and Supply-Dimming

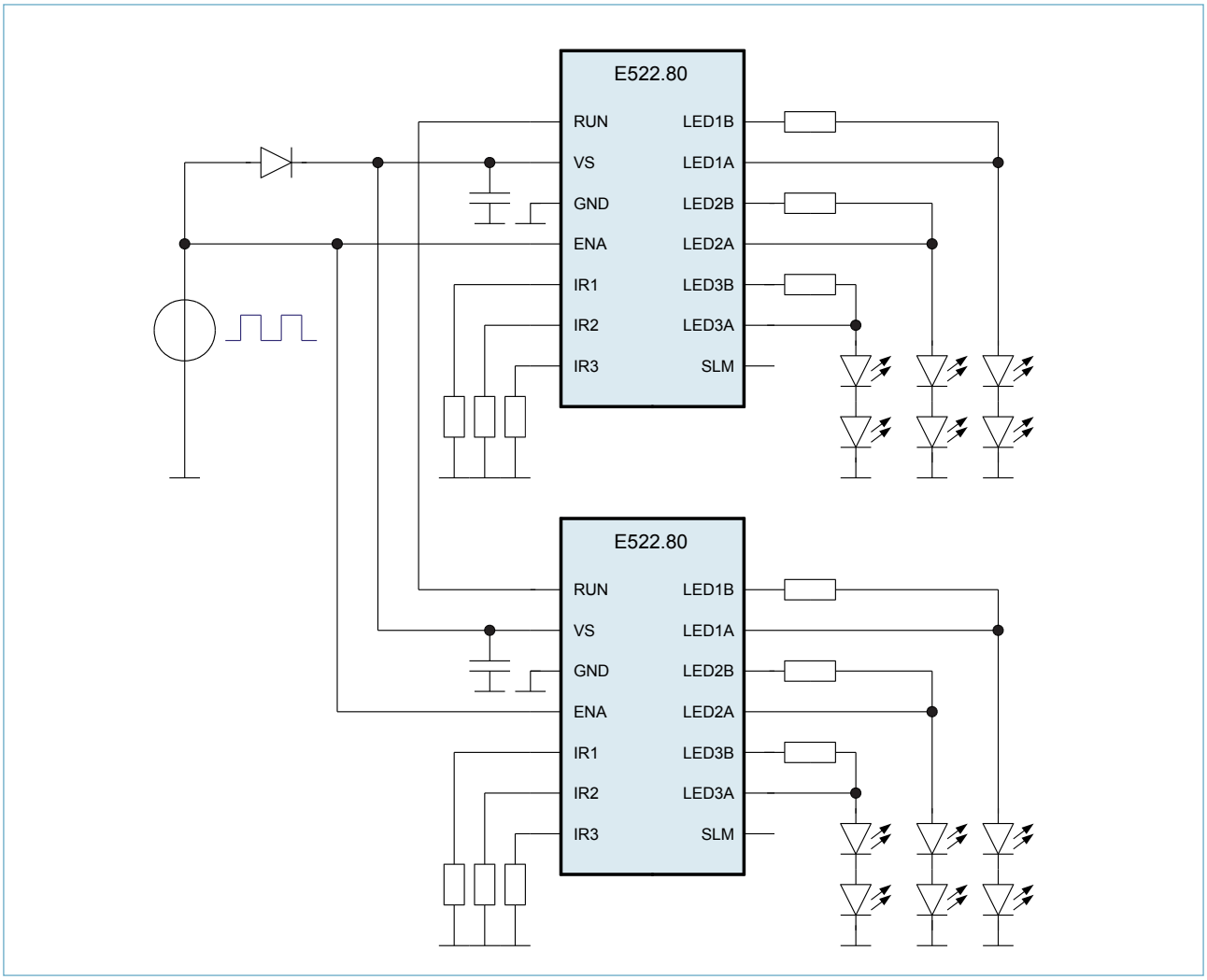


Figure 13. Six Channel Cluster in SLM

This Application is a six-channel cluster, that makes use of the following product features:

- Digital Dimming via supply line is possible. ICs remain powered by reverse polarity protection and input capacitors, consuming only very low sleep mode currents.
- Single-Lamp Mode (SLM) is configured, deactivating all LEDs in case of a single channel failure on any LED Output. RUN connection is used to propagate the information between ICs, immitating the failing behaviour of a bulb if necessary.
- Thermal management resistors are applied to distribute the power on the PCB

5.8.4 Thermal Management and Parallel Operation

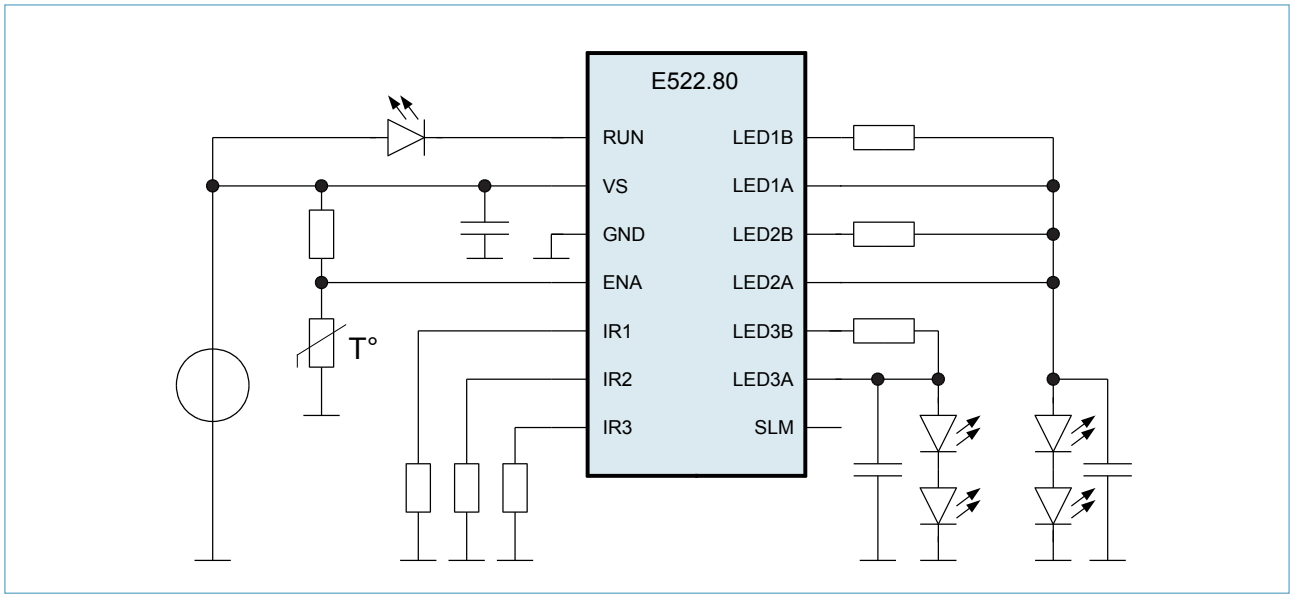


Figure 14. Thermal Application Topology

In this setup more thermal handling options are presented:

- Thermal shunts at LEDxB are used for power-distribution on the PCB
- Temperature depending divider at ENA provides derating, if the divided voltage falls below the internal reference of E522.8x
- Parallel operation of two channels to increase output current
- A fail-indicator LED is connected to RUN, which may be useful e.g. to identify defect PCBs
- Capacitors parallel to loads improve PSRR and thus the lifetime of the LEDs in case of e.g. ESD events

5.8.5 Automotive Cluster Application

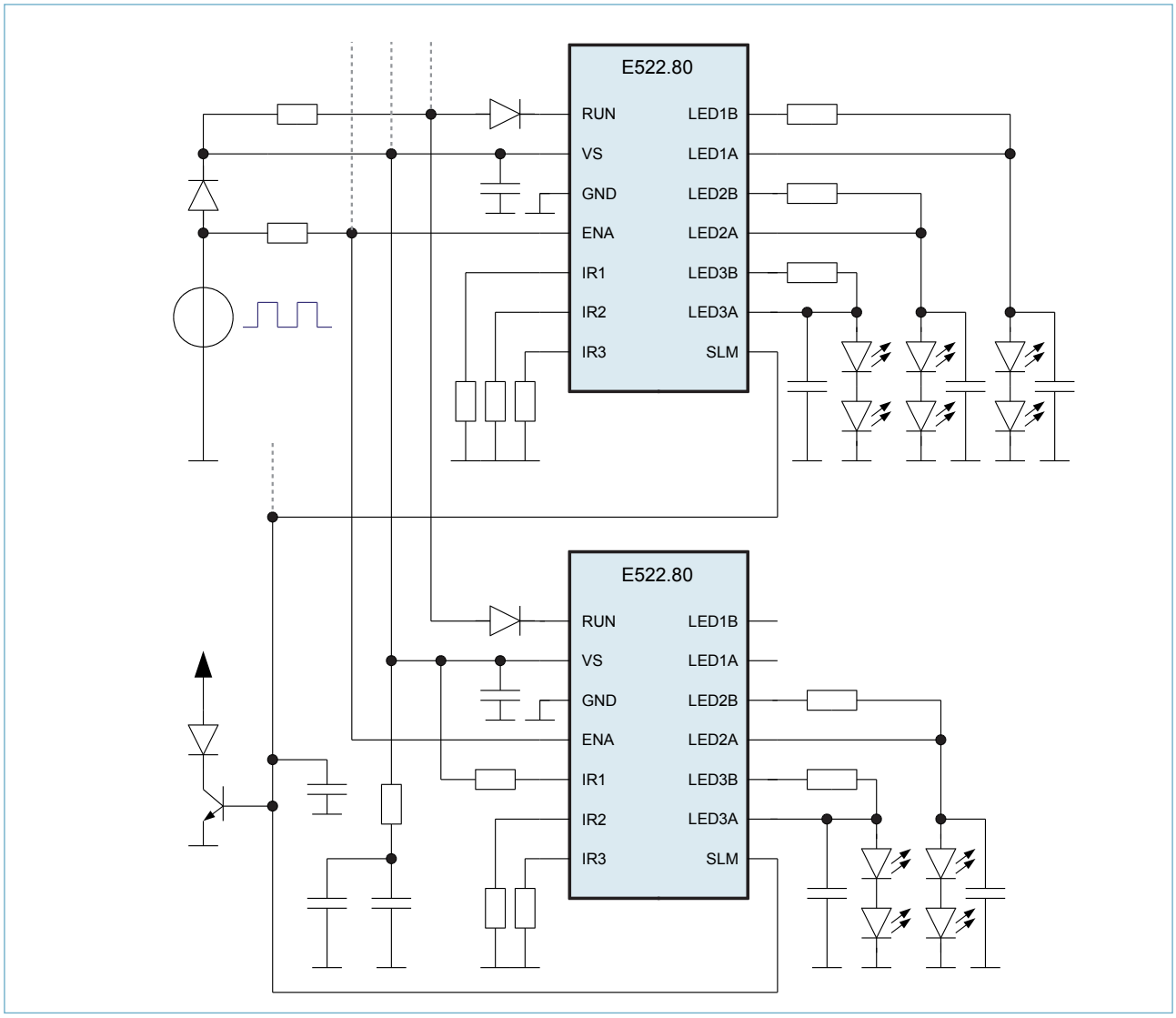


Figure 15. Automotive Cluster Application

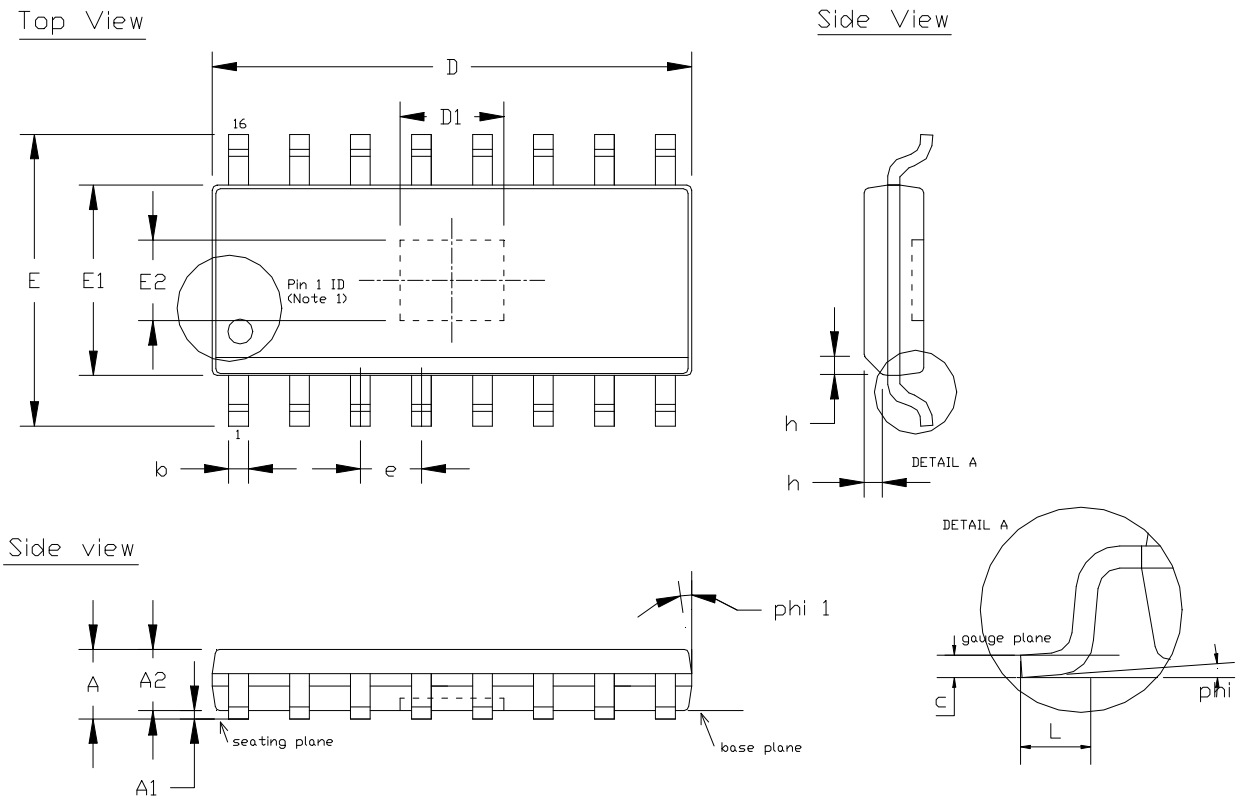
The application shows additional elements, that are typically useful for an automotive environment. Further elements may be necessary (e.g. input protection or suppressor diodes as required).

Features of this setup are:

- Digital dimming via battery line, e.g. from control modules highside driver
- RUN diode-Or bus for failure indication, making use of central bus pull-up resistor to VS. Hint: Take the resistor into account for sleep mode current consumption (ENA 'low' leads to active-low RUN state for all disabled ICs)
- If the RUN diagnostic bus drawn is not used by means of e.g. a local controller, it can be omitted for FFM (leave RUN pins just open)
- FFM (Failure-Feedback Mode): SLM is shared by more than one IC, driving a potential feedback path to the control module. In this mode a failure is reported, the cluster remains active
- Exemplary single-channel deactivation via IR Resistor to VS at lower IC
- Various protective devices added for automotive environment, like e.g. damping R-C network for inductive supply line
- Topology can be extended by further devices of the E522.8x family to build larger clusters

6 Package Reference

All devices are available in a Pb free, RoHs compliant SOIC16N-EP plastic package according to JEDEC MS-012-F, variant BC. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260+5)°C.



Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package height	A	--	--	1.75	--	--	0.067
Stand off	A1	0.00	--	0.15	0.000	--	0.006
Package body thickness	A2	1.25	--	--	0.049	--	--
Width of terminal leads, inclusive lead finish	b	0.31	--	0.51	0.012	--	0.020
Thickness of terminal leads, inclusive lead finish	c	0.10	--	0.25	0.004	--	0.010
Package length	D		9.90 BSC			0.390 BSC	
Exposed pad length	D1	2.290	2.540	2.800	0.090	0.100	0.110
Package width	E		6.00 BSC			0.236 BSC	
Package body width	E1		3.90 BSC			0.154 BSC	
Exposed pad width	E2	1.780	2.030	2.290	0.070	0.080	0.090
Lead pitch	e		1.27 BSC			0.050 BSC	
Length of terminal for soldering to substrate	L	0.4	--	1.27	0.016	--	0.050
body chamfer (45°)	h	0.25	--	0.50	0.010	--	0.020
Angle of lead mounting area	phi [°]	0	--	8	0	--	8
mold release angle	phi1 [°]	5	--	15	5	--	15
Number of terminal positions	N		16			16	

Note: the mm values are valid, the inch values contains rounding errors

7 Functional Safety

The development of this product is based on a process according to an ISO/TS16949 certified quality management system. Functional safety requirements according to ISO 26262 have not been submitted to Elmos and therefore have not been considered for the development of this product.

8 Record of Revision

Chapter	Revision	Change and Reason for Change	Date	Released Elmos
-	.00	Initial revision	Nov 26, 2014	DHOE/ZOE
6	.01	Drawing and dimensions revised	Jun 23, 2015	DHOE/ZOE
-	.01	Product classification changed from advanced product information to preliminary information	Jun 23, 2015	DHOE/ZOE
-	.01	Adapted to the specification	Jun 23, 2015	ASU/ZOE

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