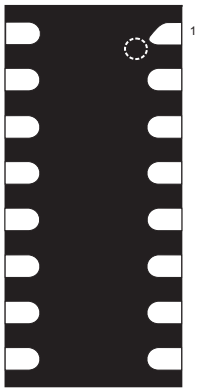
ECMF06-6AM16

Common mode filter with ESD protection for MIPI D-PHY and MDDI interface

Datasheet – production data



Micro QFN-16 L:
1.35 x 3.3 mm

Features

- Very large differential bandwidth: higher than 6 GHz
- High common mode attenuation:
  - -24 dB at 900 MHz
  - -20 dB between 800 MHz and 2.2 GHz
- Very low PCB space consumption
- Thin package: 0.55 mm max
- Lead-free package
- High reduction of parasitic elements through integration

Complies with the following standards:

- IEC 61000-4-2 level 4:
  - ±15 kV (air discharge)
  - ±8 kV (contact discharge)

Applications

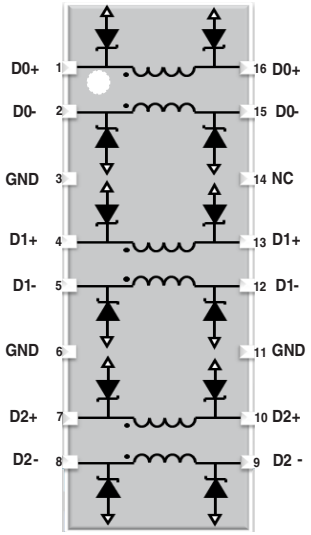
- Mobile phones
- Notebook, laptop
- Portable devices

Description

The ECMF06-6AM16 is a highly integrated common mode filter designed to suppress EMI/RFI common mode noise on high speed differential serial buses like MIPI D-PHY or MDDI.

The ECMF06-6AM16 can protect and filter 3 differential lanes.

Figure 1. Pin configuration (top view)



This is information on a product in full production. www.st.com

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	10 30	kV
I_{DC}	Maximum DC current		100	mA
T_{op}	Operating temperature		-40 to +85	°C
T_j	Maximum junction temperature		125	°C
T_{stg}	Storage temperature range		- 55 to +150	°C

Figure 2. Electrical characteristics (definitions)

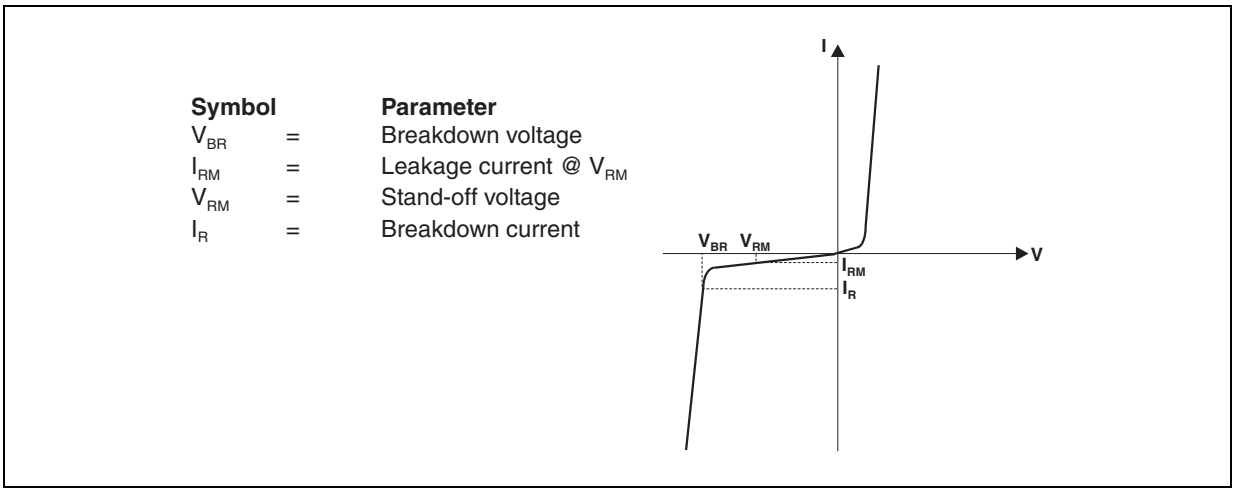


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6			V
I_{RM}	V_{RM} = 3 V per line			100	nA
R_{DC}	DC serial resistance		2.7	4	Ω

Table 3. Pin description

Pin name	Description	Pin name	Description	Pin name	Description	Pin name	Description
1	D0+ DSI receiver	5	D1- DSI receiver	9	D2- DSI transmitter	13	D1+ DSI transmitter
2	D0- DSI receiver	6	GND DSI receiver	10	D2+ DSI transmitter	14	NC DSI transmitter
3	GND DSI receiver	7	D2+ DSI receiver	11	GND DSI transmitter	15	D0- DSI transmitter
4	D1+ DSI receiver	8	D2- DSI receiver	12	D1- DSI transmitter	16	D0+ DSI transmitter

Figure 3. SDD21 differential attenuation measurement ($Z_{0\ diff}$ = 100 Ω)

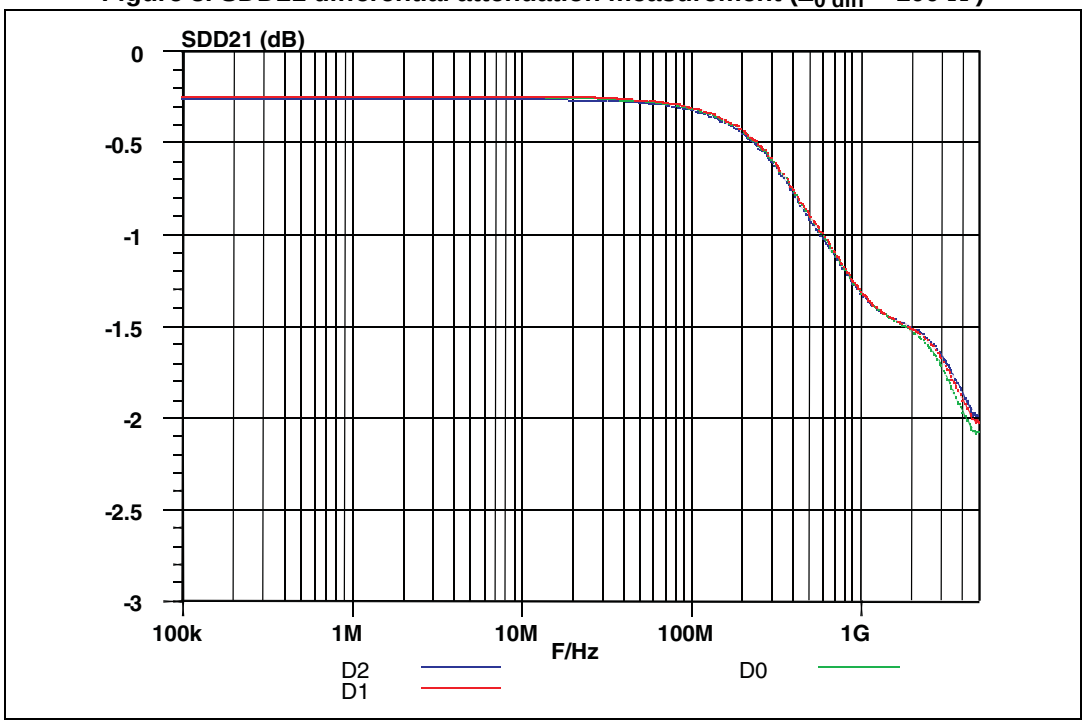


Figure 4. SCC21 common mode attenuation measurement ($Z_{0\ com}$ = 50 Ω)

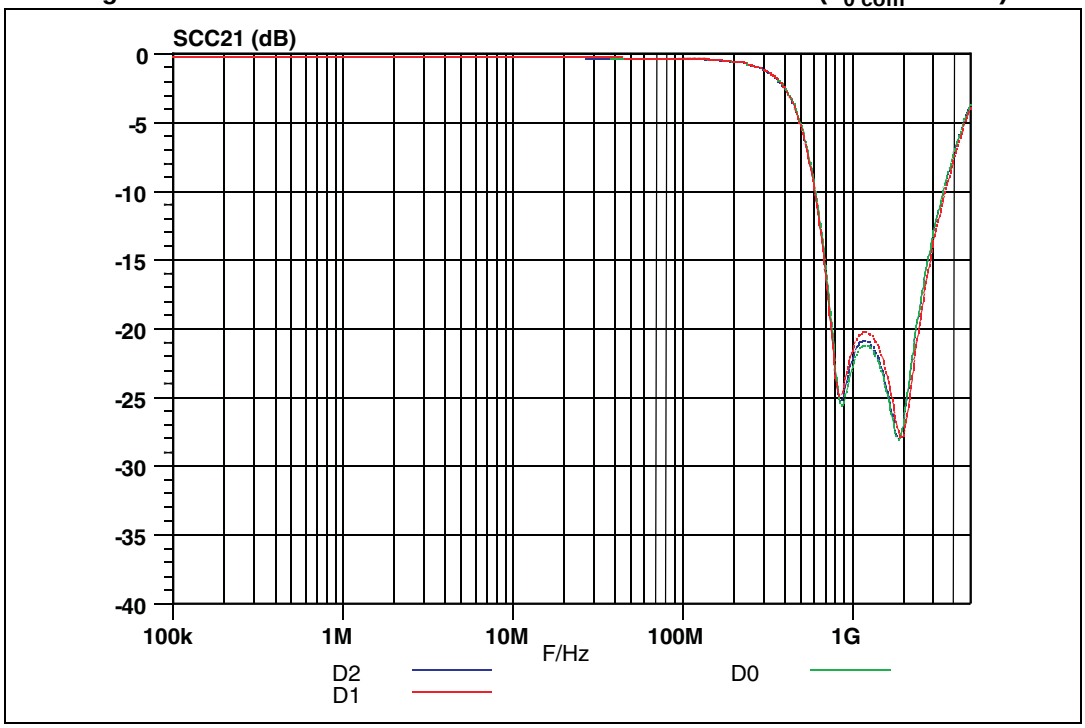


Figure 5. SDD11 differential return loss measurement ($Z_{0\ diff}$ = 100 Ω)

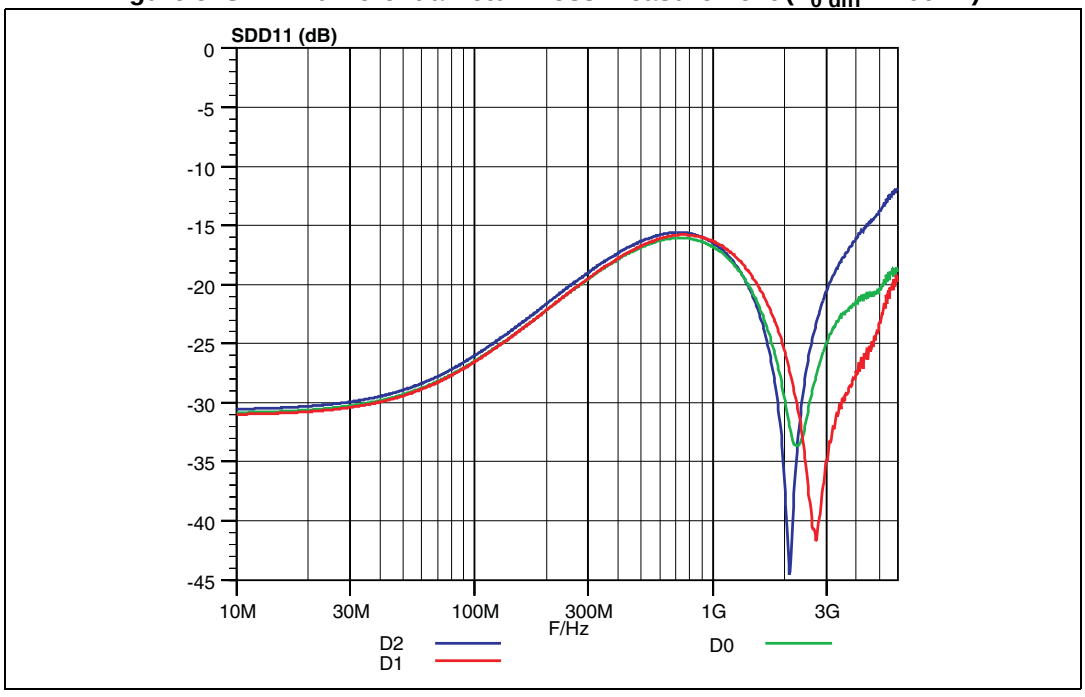


Figure 6. SDD22 differential attenuation measurement ($Z_{0\ diff}$ = 100 Ω)

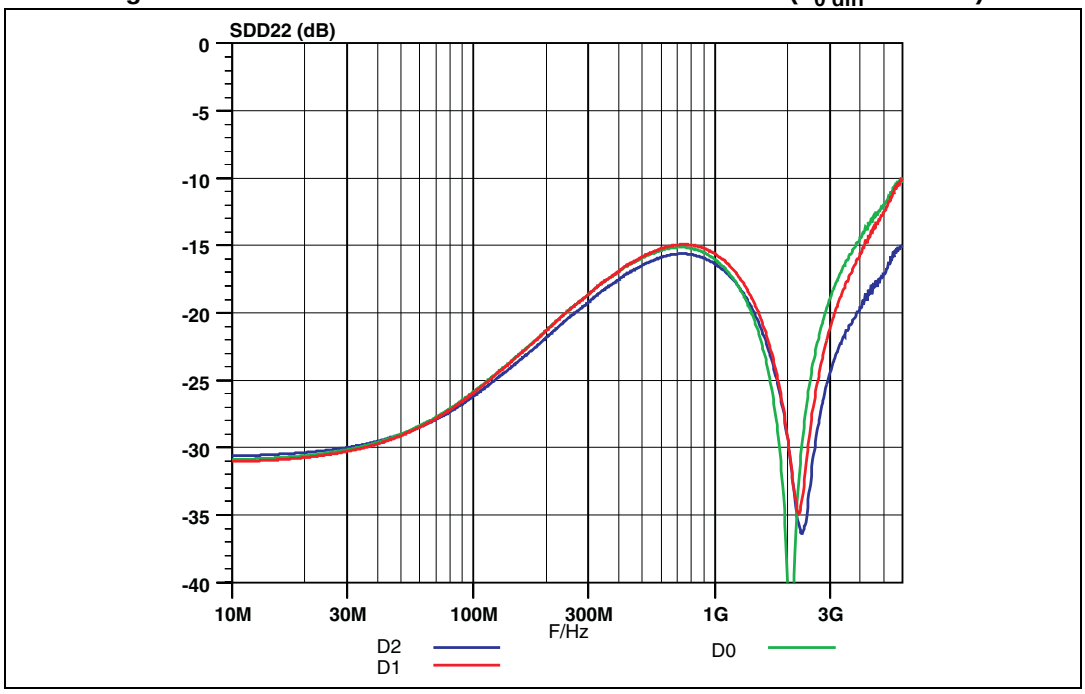


Figure 7. SDDxx inter-lane differential cross-coupling measurement ($Z_{0\ diff}$ = 100 Ω)

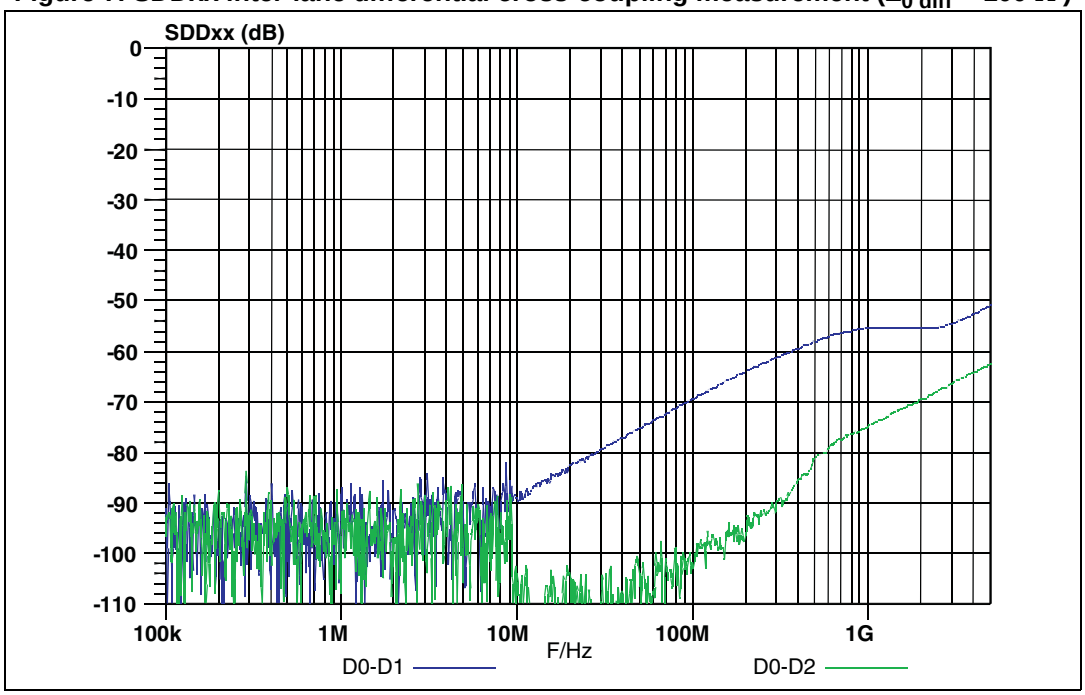


Figure 8. SCCxx inter-lane common-mode cross-coupling measurement ($Z_{0\ diff}$ = 100 Ω)

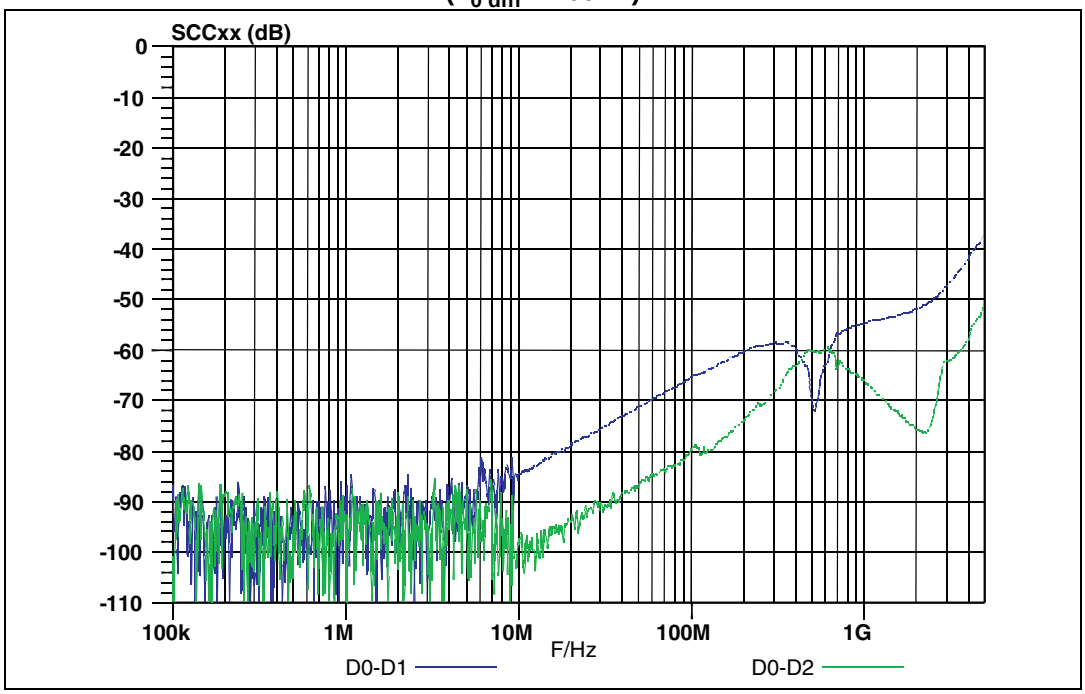


Figure 9. MIPI D-PHY low power mode test setup

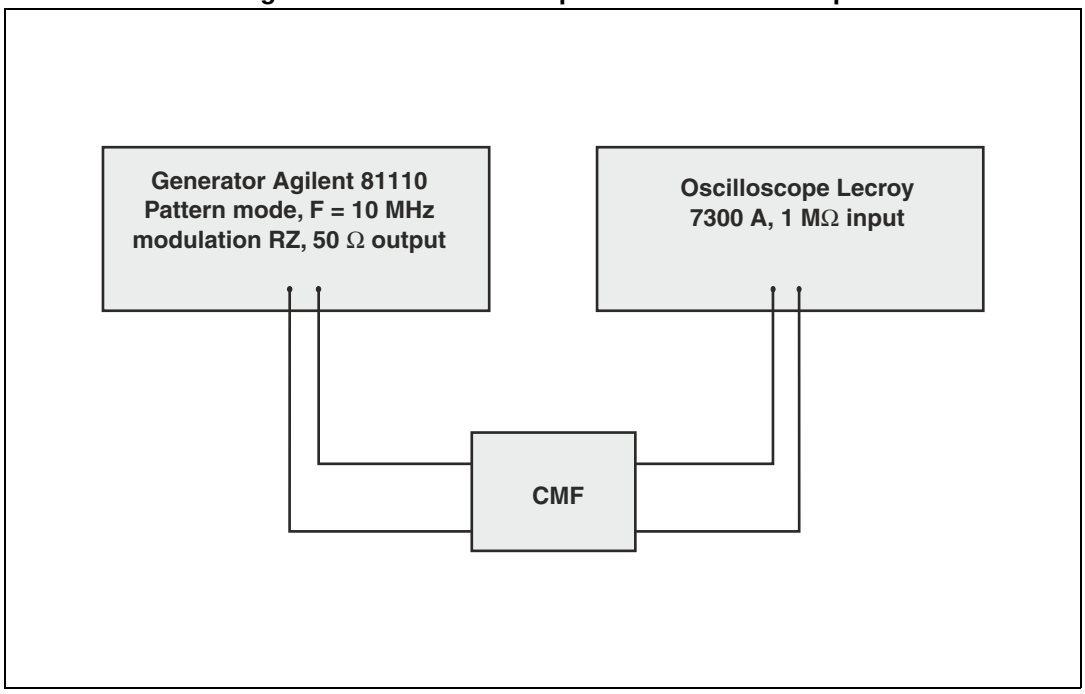


Figure 10. Low power pulse response - see *Figure 9* for test setup

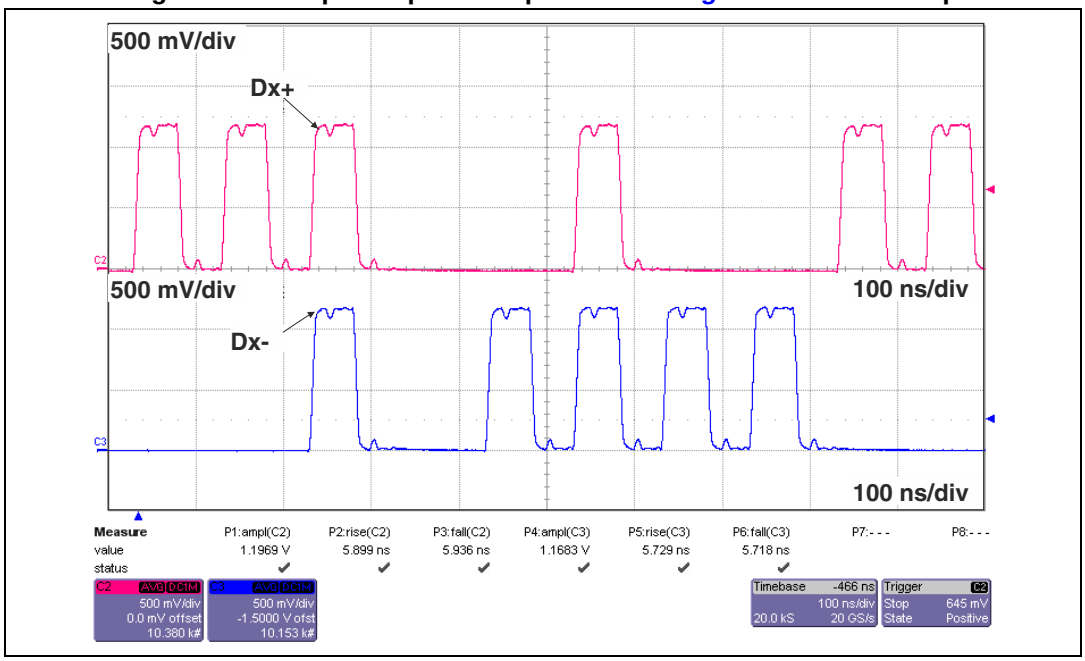


Figure 11. ESD response to IEC61000-4-2 (+8 kV contact discharge) - see *Figure 13* for test set-up

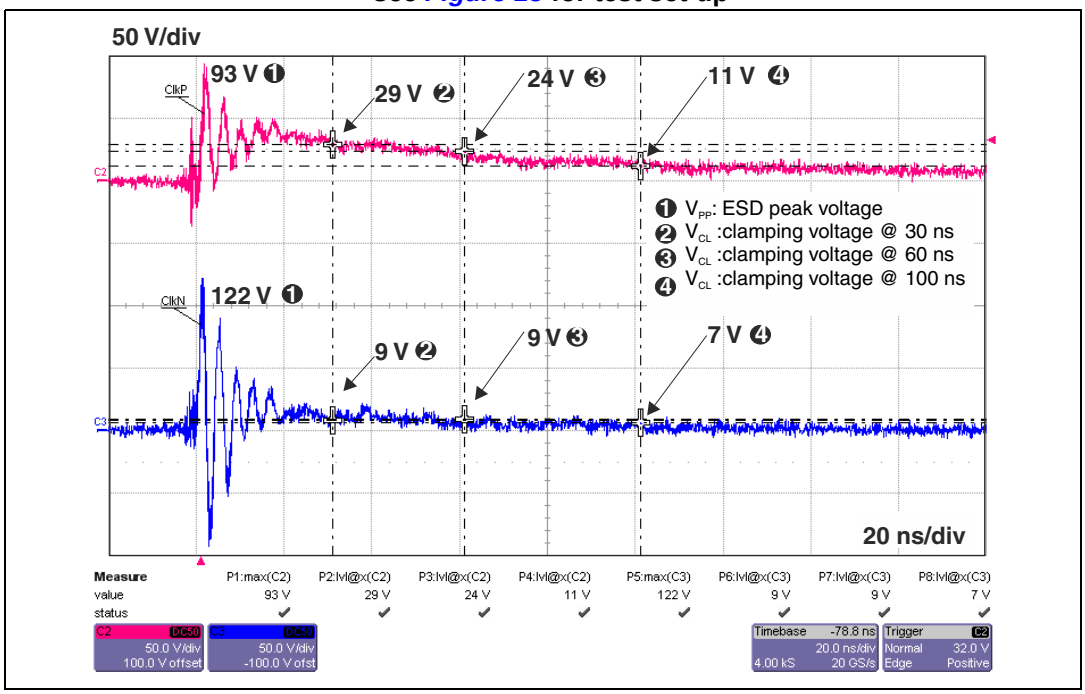


Figure 12. ESD response to IEC61000-4-2 (-8 kV contact discharge) - see *Figure 13* for test set-up

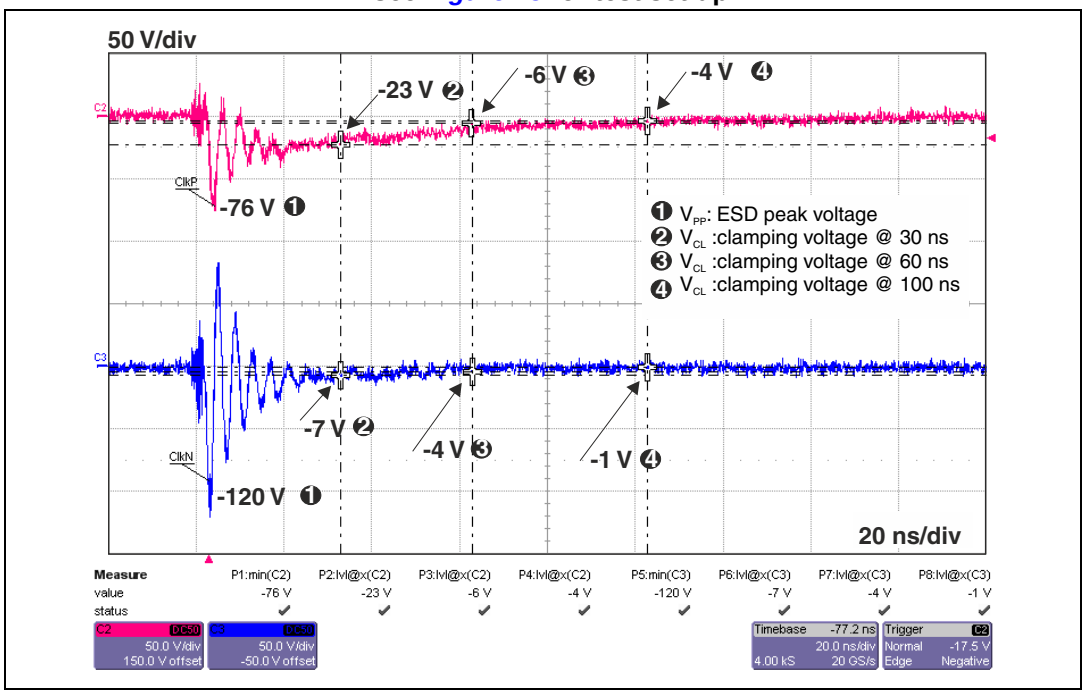
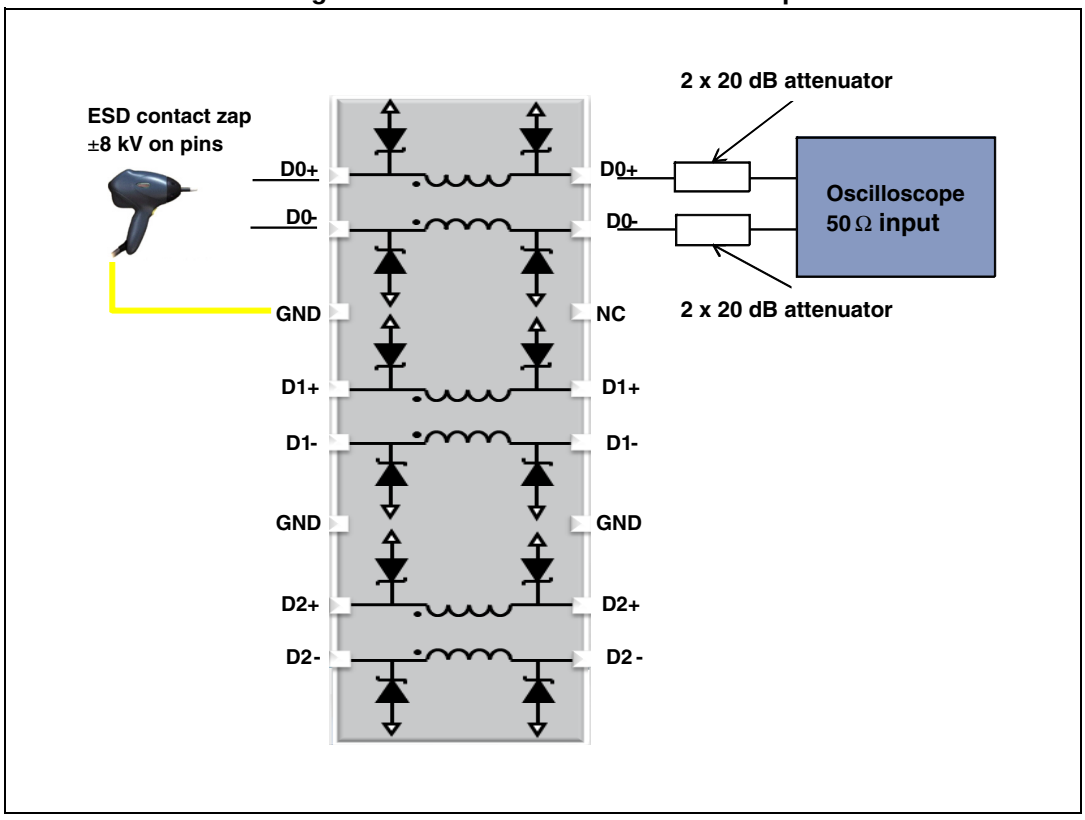
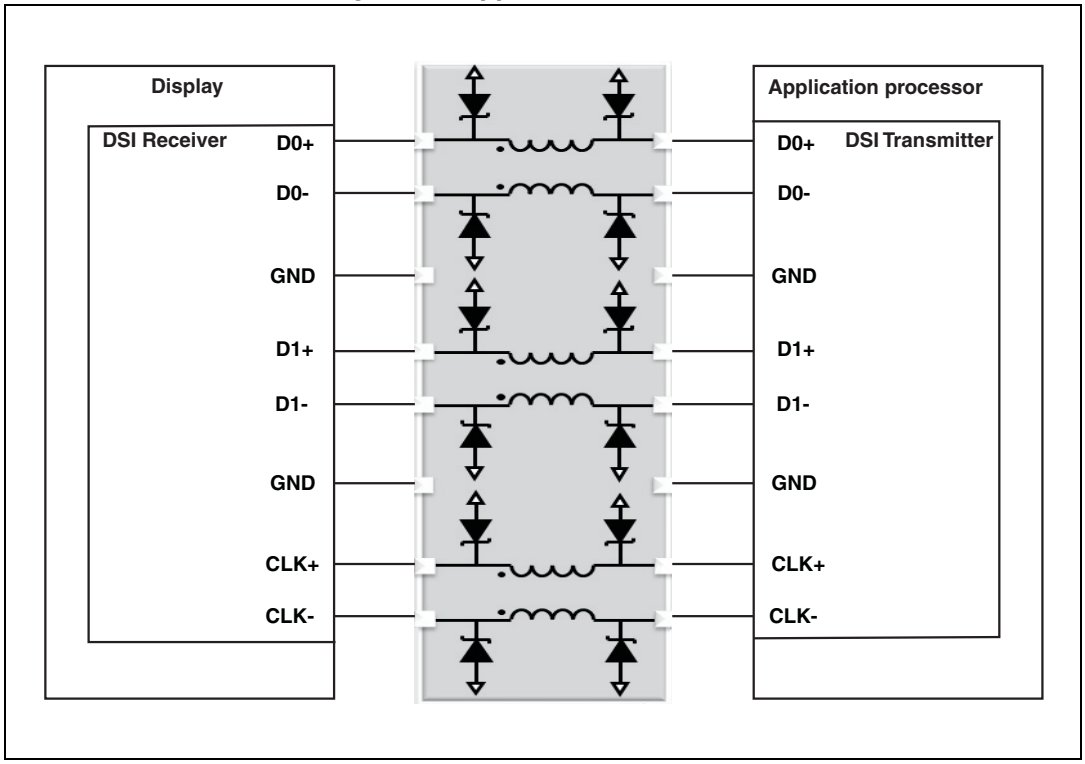


Figure 13. ESD measurement test set-up



2 Application information

Figure 14. Application information



3 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

Figure 15. Micro QFN 3.3 x 1.35 16L package dimension definitions

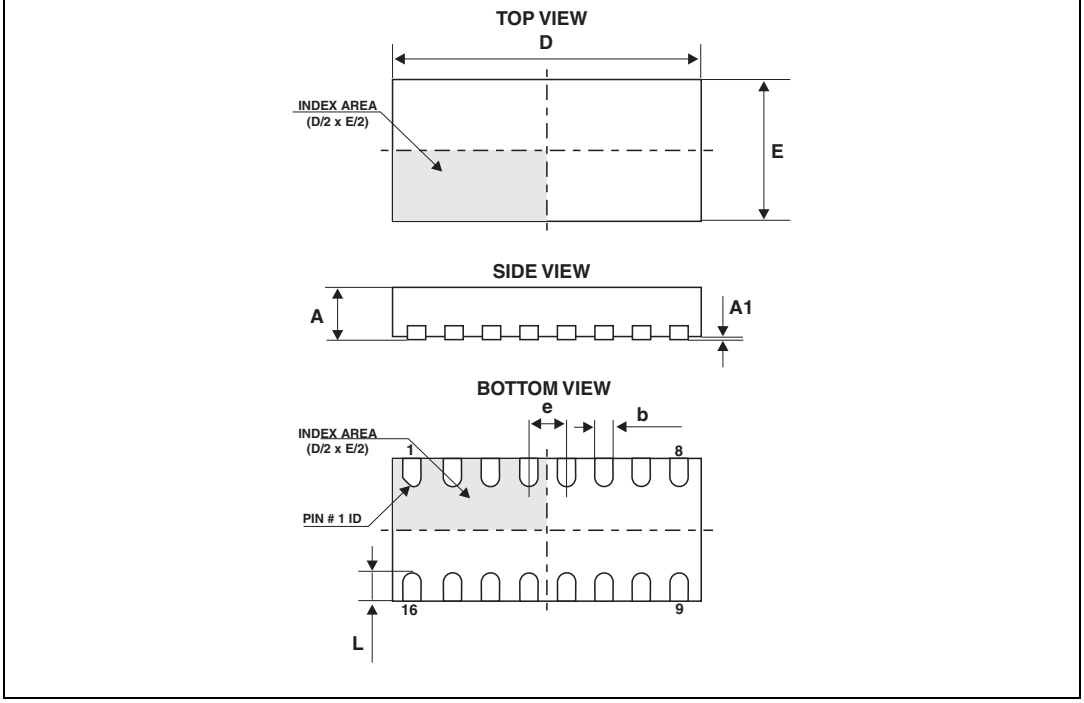


Table 4. Micro QFN 3.3 x 1.35 16L package dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.00	0.0008	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D	3.25	3.30	3.35	0.128	0.130	0.132
E	1.30	1.35	1.40	0.051	0.053	0.055
e	0.35	0.40	0.45	0.014	0.016	0.018
L	0.30	0.40	0.50	0.118	0.016	0.020

Figure 16. Footprint

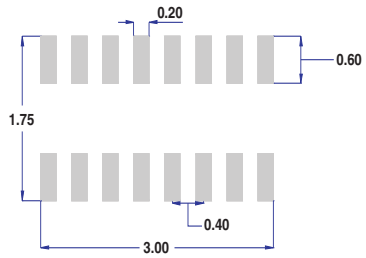
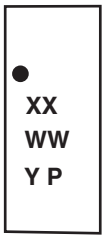
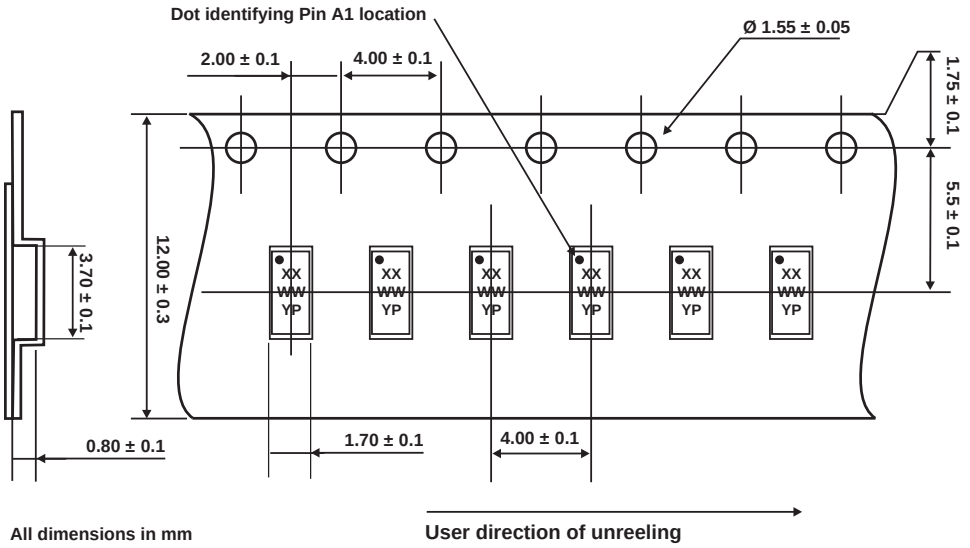


Figure 17. Marking



Dot: Pin 1
XX: Marking
WW: Assembly week
Y: Assembly year
P: Assembly plant

Figure 18. Tape and reel specifications

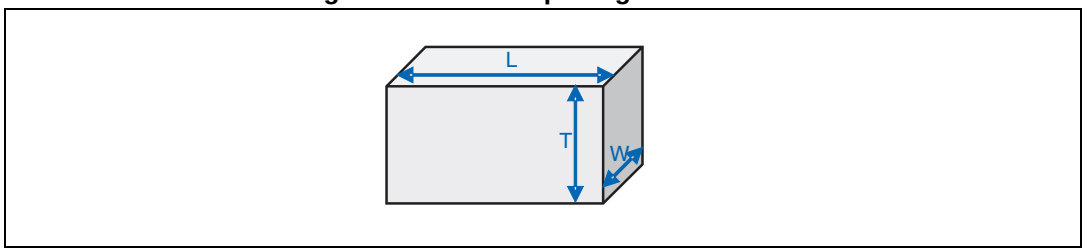


4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 19. Stencil opening dimensions



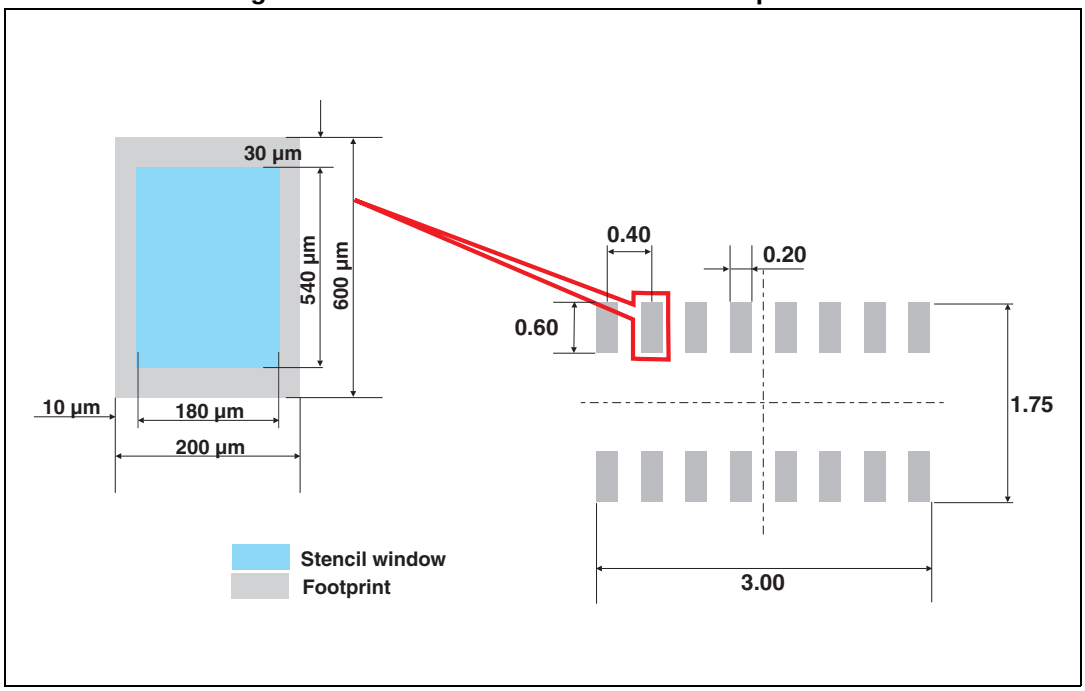
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 20. Recommended stencil window position



4.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

4.3 Placement

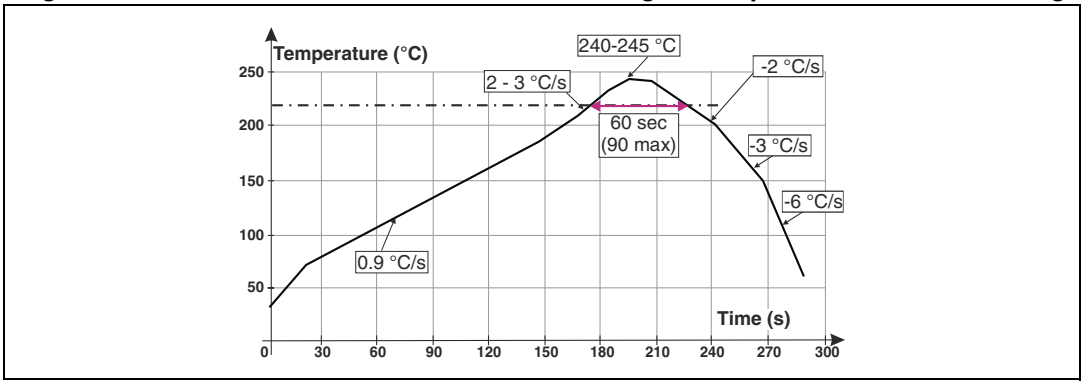
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 21. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Figure 22. Ordering information scheme

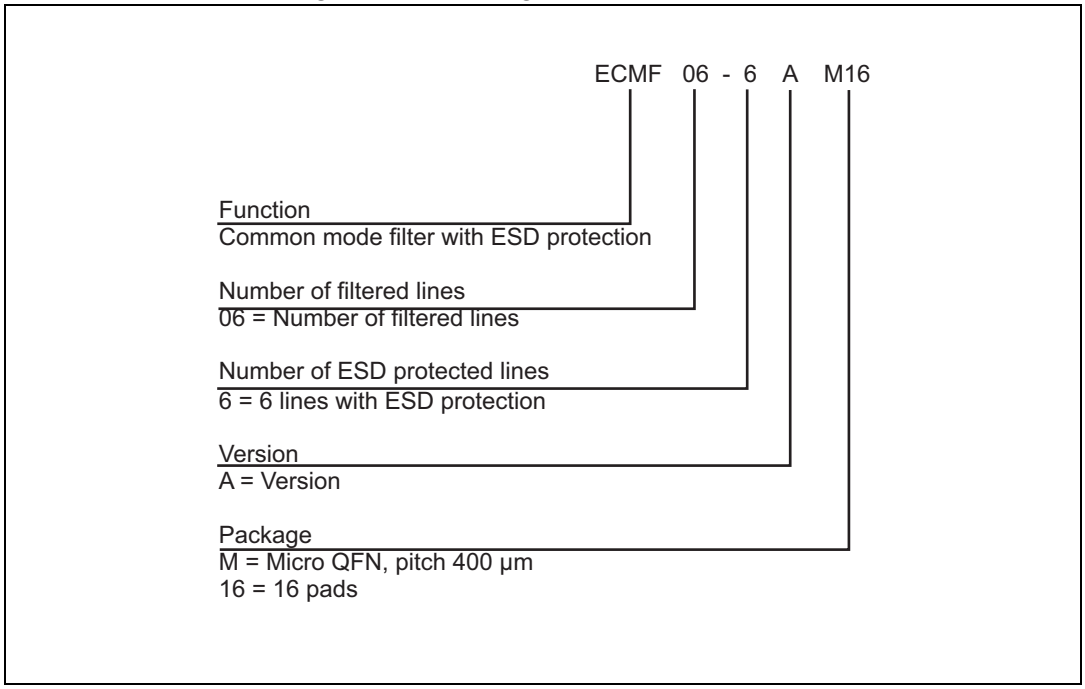


Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ECMF06-6AM16	KF	Micro QFN-16L	6.3 mg	3000	Tape and reel

For the latest information on available order codes see the product pages on www.st.com.

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
14-Feb-2012	1	Initial release.
04-Oct-2012	2	Inserted *Table 3* and updated *Figure 1* to add A1 marker.
26-may-2014	3	Updated *Figure 21*, *Figure 22*, *Figure 22* and document reformatted.

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