

- ▶ Low Voltage PECL
- ▶ 7 x 5 mm Footprint
- ▶ Low Jitter
- ▶ Pb Free/RoHS Compliant

ECS-PEC25/PEC33

SMD PECL OSCILLATOR

ECS-PEC25 (2.5V) and ECS-PEC33 (3.3V) miniature SMD PECL oscillators. Ideal for low jitter applications.

OPERATING CONDITIONS / ELECTRICAL CHARACTERISTICS

PARAMETERS	CONDITIONS	ECS-PEC25 (+2.5V)			ECS-PEC33 (+3.3V)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Frequency Range		40.0		300.0	40.0		300.0	MHz
Operating Temperature	Standard	0		+70	0		+70	°C
	Extended (N Option)	-40		+85	-40		+85	°C
Storage Temperature		-50		+125	-50		+125	°C
Supply Voltage	VDD	+2.375	+2.5	+2.625	+3.135	+3.3	+3.465	VDC
Frequency Stability *	Option A			± 100			± 100	ppm
	Option B			± 50			± 50	ppm
	Option C			± 25			± 25	ppm
Input Current	Pin 1 open or VIH			90			90	mA
Stand-by Current	Pin 1 = VIL			30			30	μA
Output Symmetry	@ 50% VDD level			40/60			45/55	%
Rise and Fall Times	20% VDD to 80% level			1			1	ns
"0" level	VOL			+1.195			+1.745	VDC
"1" level	VOH	+1.415			+2.215			VDC
Output Load	50Ω into VDD -2V							
Disable delay time				200			200	ns
Enable/Startup time				10			10	ms
RMS Jitter	12 KHz to 20 MHz band			1			1	ps
Aging				± 5			± 5	ppm

DIMENSIONS (mm)

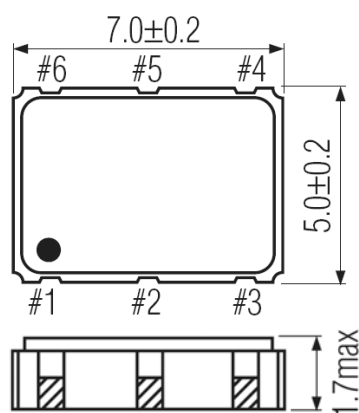


Figure 1) Top, Side and Bottom views

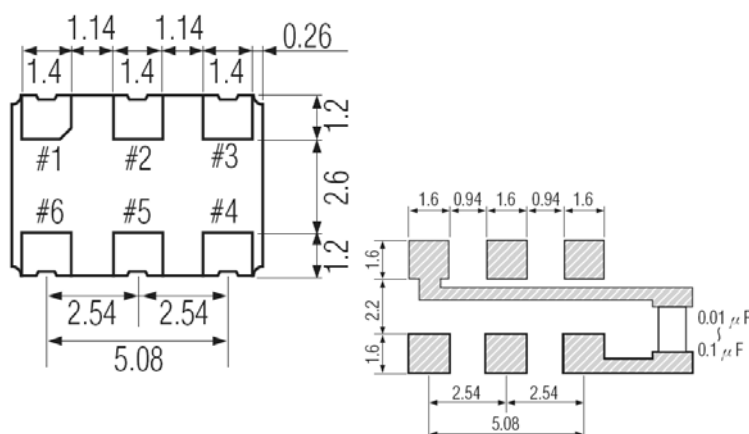


Figure 2) Suggested Land Pattern

Pin Connections

Pin #1	Tri-State
Pin #2	N.C.
Pin #3	Ground
Pin #4	Output
Pin #5	C-Output
Pin #6	VDD

Tri-State Control Voltage

Pad 1	Pad 4 & 5
Open	Oscillation
VIH 70% VDD Min	Oscillation
VIL 30% VDD Max	No Oscillation

Note: Internal crystal oscillation to be halted (Pin #1=VIL)

PART NUMBERING GUIDE: Example ECS-PEC33-1000-B-N

ECS - Series - Frequency Abbreviation - Stability - Temperature

PEC25 = +2.5V
PEC33 = +3.3V

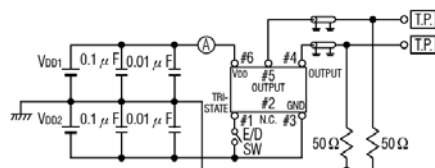
1000 = 100.000 MHz
See Frequency Abbreviations (Pg 2)

A = ± 100 ppm
B = ± 50 ppm
C = ± 25 ppm

Blank = 0 ~ +70°C
M = -20 ~ +70°C
N = -40 ~ +85°C

Frequency Abbreviations

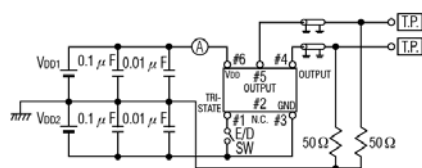
FREQUENCY MHz	CODE
100.000	1000
106.250	1062.5
125.000	1250
155.520	1555.2
156.250	1562.5



Termination : 50 Ω impedance matching

VDD	VDD1	VDD2
+3.3V	+2.0V	-1.3V
+2.5V	+2.0V	-0.5V

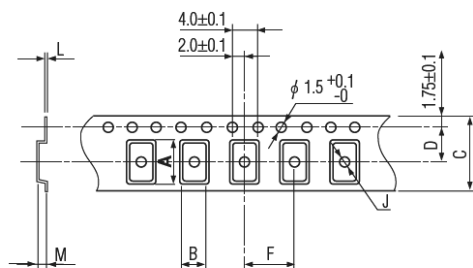
Figure 1) Test Circuit (1)



Termination : 50 Ω impedance matching

VDD	VDD1	VDD2
+3.3V	+2.0V	-1.3V
+2.5V	+2.0V	-0.5V

Figure 2) Test Circuit (2)



A	B	C	D	F	J	L	M	Reel Dia.	Qty/Reel
7.5	5.5	16.0	7.5	8.0	2.0	0.3	2.2	245	1000pcs

Figure 3) Pocket Tape Dimensions

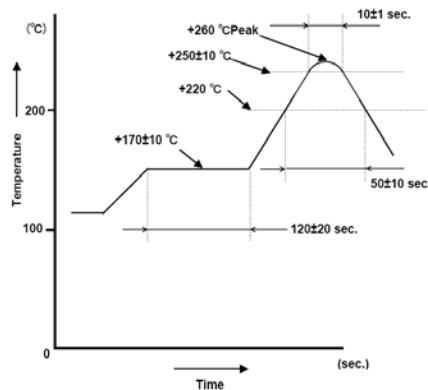
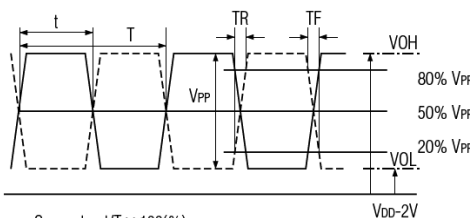


Figure 4) Suggested Reflow Profile

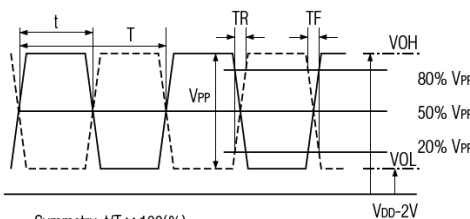
Termination : 50 Ω impedance matching



Symmetry= $t/T \times 100(\%)$

Figure 5) Output Waveform (1)

Termination : 50 Ω impedance matching



Symmetry= $t/T \times 100(\%)$

Figure 6) Output Waveform (2)

Package Data	
Item	Description
Lid	Metal
Base	Ceramic
Sealing	Seam
Terminal	Tungsten (metalized)
Plating	Gold/Nickel (Surface)/(Under)
RoHS	Compliant (Pb Free)