

400MHz Slew Enhanced VFAs

The EL5x02 and EL5x03 families represent high-speed VFAs based on a CFA amplifier architecture. This gives the typical high slew rate benefits of a CFA family along with the stability and ease of use associated with the VFA type architecture. With slew rates of 3500V/ μ s, this family of devices enables the use of voltage feedback amplifiers in a space where the only alternative has been current feedback amplifiers. This family will also be available in single, dual, and triple versions, with 200MHz, 400MHz, and 750MHz versions. These are all available in single, dual, and triple versions.

Both families operate on single 5V or $\pm$ 5V supplies from minimum supply current. EL5x02 also features an output enable function, which can be used to put the output in to a high-impedance mode. This enables the outputs of multiple amplifiers to be tied together for use in multiplexing applications.

Typical applications for these families will include cable driving, filtering, A-to-D and D-to-A buffering, multiplexing and summing within video, communications, and instrumentation designs.

Features

- Operates off 3V, 5V, or $\pm$ 5V applications
- Power-down to 0 μ A (EL5x02)
- -3dB bandwidth = 400MHz
- $\pm$ 0.1dB bandwidth = 50MHz
- Low supply current = 5mA
- Slew rate = 3500V/ μ s
- Low offset voltage = 5mV max
- Output current = 140mA
- A_{VOL} = 2000
- Diff gain/phase = 0.01%/0.01°
- Pb-Free plus anneal available (RoHS compliant)

Applications

- Video amplifiers
- PCMCIA applications
- A/D drivers
- Line drivers
- Portable computers
- High speed communications
- RGB applications
- Broadcast equipment
- Active filtering

Ordering Information

PART NUMBER	PART MARKING	PACKAGE	TAPE & REEL	PKG. DWG. #
EL5102IS	5102IS	8 Ld SOIC	-	MDP0027
EL5102IS-T7	5102IS	8 Ld SOIC	7"	MDP0027
EL5102IS-T13	5102IS	8 Ld SOIC	13"	MDP0027
EL5102ISZ (See Note)	5102ISZ	8 Ld SOIC (Pb-free)	-	MDP0027
EL5102ISZ-T7 (See Note)	5102ISZ	8 Ld SOIC (Pb-free)	7"	MDP0027
EL5102ISZ-T13 (See Note)	5102ISZ	8 Ld SOIC (Pb-free)	13"	MDP0027
EL5102IW-T7	q	6 Ld SOT-23	7" (3K pcs)	MDP0038
EL5102IW-T7A	q	6 Ld SOT-23	7" (250 pcs)	MDP0038
EL5102IWZ-T7 (See Note)	BBSA	6 Ld SOT-23 (Pb-free)	7" (3K pcs)	MDP0038
EL5102IWZ-T7A (See Note)	BBSA	6 Ld SOT-23 (Pb-free)	7" (250 pcs)	MDP0038
EL5103IC-T7	B	5 Ld SC-70	7" (3K pcs)	P5.049
EL5103IC-T7A	B	5 Ld SC-70	7" (250 pcs)	P5.049
EL5103IW-T7	g	5 Ld SOT-23	7" (3K pcs)	MDP0038
EL5103IWZ-T7	BBTA	5 Ld SOT-23 (Pb-free)	7" (3K pcs)	MDP0038
EL5103IWZ-T7A	BBTA	5 Ld SOT-23 (Pb-free)	7" (250 pcs)	MDP0038
EL5202IY	BRAAA	10 Ld MSOP	-	MDP0043
EL5202IY-T7	BRAAA	10 Ld MSOP	7"	MDP0043
EL5202IY-T13	BRAAA	10 Ld MSOP	13"	MDP0043
EL5202IYZ (See Note)	BAAAD	10 Ld MSOP (Pb-free)	-	MDP0043
EL5202IYZ-T7 (See Note)	BAAAD	10 Ld MSOP (Pb-free)	7"	MDP0043
EL5202IYZ-T13 (See Note)	BAAAD	10 Ld MSOP (Pb-free)	13"	MDP0043
EL5203IS	5203IS	8 Ld SOIC	-	MDP0027
EL5203IS-T7	5203IS	8 Ld SOIC	7"	MDP0027
EL5203IS-T13	5203IS	8 Ld SOIC	13"	MDP0027
EL5203ISZ (See Note)	5203ISZ	8 Ld SOIC (Pb-free)	-	MDP0027

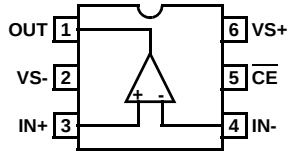
Ordering Information (Continued)

PART NUMBER	PART MARKING	PACKAGE	TAPE & REEL	PKG. DWG. #
EL5203ISZ-T7 (See Note)	5203ISZ	8 Ld SOIC (Pb-free)	7"	MDP0027
EL5203ISZ-T13 (See Note)	5203ISZ	8 Ld SOIC (Pb-free)	13"	MDP0027
EL5203IY	BSAAA	8 Ld MSOP	-	MDP0043
EL5203IY-T7	BSAAA	8 Ld MSOP	7"	MDP0043
EL5203IY-T13	BSAAA	8 Ld MSOP	13"	MDP0043
EL5203IYZ (See Note)	BAAAE	8 Ld MSOP (Pb-free)	-	MDP0043
EL5203IYZ-T7 (See Note)	BAAAE	8 Ld MSOP (Pb-free)	7"	MDP0043
EL5203IYZ-T13 (See Note)	BAAAE	8 Ld MSOP (Pb-free)	13"	MDP0043
EL5302IU	5302IU	16 Ld QSOP	-	MDP0040
EL5302IU-T7	5302IU	16 Ld QSOP	7"	MDP0040
EL5302IU-T13	5302IU	16 Ld QSOP	13"	MDP0040
EL5302IUZ (See Note)	5302IUZ	16 Ld QSOP (Pb-free)	-	MDP0040
EL5302IUZ-T7 (See Note)	5302IUZ	16 Ld QSOP (Pb-free)	7"	MDP0040
EL5302IUZ-T13 (See Note)	5302IUZ	16 Ld QSOP (Pb-free)	13"	MDP0040

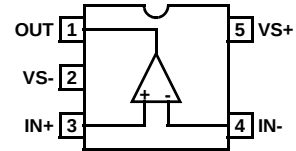
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020

Pinouts

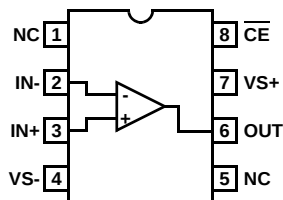
EL5102
(6 LD SOT-23)
TOP VIEW



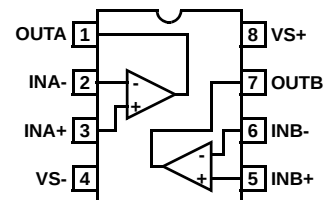
EL5103
(5 LD SOT-23)
TOP VIEW



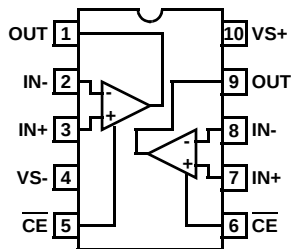
EL5102
(8 LD SOIC)
TOP VIEW



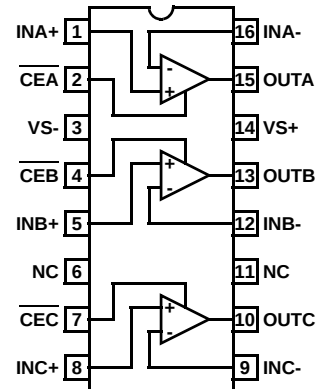
EL5203
(8 LD SOIC, MSOP)
TOP VIEW



EL5202
(10 LD MSOP)
TOP VIEW



EL5302
(16 LD QSOP)
TOP VIEW



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage between V_{S+} and GND 13.2V
 Maximum Supply Slewrate between V_{S+} and V_{S-} 1V/ μs
 Input Voltage $\pm V_S$
 Differential Input Voltage $\pm 4\text{V}$
 Maximum Continuous Output Current 80mA

Maximum Current into I_{N+} , I_{N-} , $\overline{\text{CE}}$ $\pm 5\text{mA}$
 Power Dissipation See Curves
 Storage Temperature Range -65°C to $+150^\circ\text{C}$
 Ambient Operating Temperature Range -40°C to $+85^\circ\text{C}$
 Operating Junction Temperature 150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications $V_{S+} = +5\text{V}$, $V_{S-} = -5\text{V}$, $T_A = 25^\circ\text{C}$, $R_L = 500\Omega$, $V_{\text{ENABLE}} = +5\text{V}$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Offset Voltage	EL5102, EL5103, EL5202, EL5203		1	5	mV
		EL5302		2	8	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		10		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$V_{IN} = 0\text{V}$	-12	2	12	μA
I_{OS}	Input Offset Current	$V_{IN} = 0\text{V}$	-8	1	8	μA
TCI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		50		$\text{nA}/^\circ\text{C}$
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.75\text{V}$ to $\pm 5.25\text{V}$	-70	-80		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = -3\text{V}$ to 3.0V	-60	-80		dB
CMIR	Common Mode Input Range	Guaranteed by CMRR test	-3	± 3.3	3	V
R_{IN}	Input Resistance	Common mode	200	400		$\text{k}\Omega$
C_{IN}	Input Capacitance	SO package		1		pF
$I_{S,ON}$	Supply Current - Enabled per amplifier		4.6	5.2	5.8	mA
$I_{S,OFF}$	Supply Current - Shut-down per amplifier	V_{S+}	+1	0	+25	μA
		V_{S-}	-25	7	-1	μA
AVOL	Open Loop Gain	$V_{OUT} = \pm 2.5\text{V}$, $R_L = 1\text{k}\Omega$ to GND	58	66		dB
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 150\Omega$ to GND		60		dB
V_{OUT}	Output Voltage Swing	$R_L = 1\text{k}\Omega$ to GND	± 3.5	± 3.9		V
		$R_L = 150\Omega$ to GND	± 3.4	± 3.7		V
I_{OUT}	Output Current	$A_V = 1$, $R_L = 10\Omega$ to 0V	± 80	± 150		mA
$V_{\overline{\text{CE}}-ON}$	$\overline{\text{CE}}$ Pin Voltage for Power-up		$(V_{S+})-5$		$(V_{S+})-3$	V
$V_{\overline{\text{CE}}-OFF}$	$\overline{\text{CE}}$ Pin Voltage for Shut-down		$(V_{S+})-1$		V_{S+}	V
I_{EN-ON}	Pin Current - Enabled	$\overline{\text{CE}} = 0\text{V}$	-1	0	+1	μA
I_{EN-OFF}	Pin Current - Disabled	$\overline{\text{CE}} = +5\text{V}$	1	14	25	μA

Closed Loop AC Electrical Specifications $V_{S+} = +5V$, $V_{S-} = -5V$, $T_A = 25^{\circ}C$, $V_{ENABLE} = +5V$, $A_V = +1$, $R_F = 0\Omega$, $R_L = 150\Omega$ to GND pin, unless otherwise specified. (Note 1)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
BW	-3dB Bandwidth ($V_{OUT} = 400mV_{P-P}$)	$A_V = 1$, $R_F = 0\Omega$		400		MHz
SR	Slew Rate	$A_V = +2$, $R_L = 100\Omega$, $V_{OUT} = -3V$ to $+3V$	1100	2200	5000	V/ μ s
		$R_L = 500\Omega$, $V_{OUT} = -3V$ to $+3V$		4000		V/ μ s
t_R, t_F	Rise Time, Fall Time	$\pm 0.1V$ step		2.8		ns
OS	Overshoot	$\pm 0.1V$ step		10		%
t_S	0.1% Settling Time	$V_S = \pm 5V$, $R_L = 500\Omega$, $A_V = 1$, $V_{OUT} = \pm 3V$		20		ns
dG	Differential Gain (Note 2)	$A_V = 2$, $R_F = 1k\Omega$		0.01		%
dP	Differential Phase (Note 2)	$A_V = 2$, $R_F = 1k\Omega$		0.01		°
e_N	Input Noise Voltage	$f = 10kHz$		12		nV/ $\sqrt{Hz}$
i_N	Input Noise Current	$f = 10kHz$		11		pA/ $\sqrt{Hz}$
t_{DIS}	Disable Time (Note 3)			50		ns
t_{EN}	Enable Time (Note 3)			25		ns

NOTES:

1. All AC tests are performed on a "warmed up" part, except slew rate, which is pulse tested.
2. Standard NTSC signal = $286mV_{P-P}$, $f = 3.58MHz$, as V_{IN} is swept from $0.6V$ to $1.314V$. R_L is DC coupled.
3. Disable/Enable time is defined as the time from when the logic signal is applied to the ENABLE pin to when the supply current has reached half its final value.

Typical Performance Curves

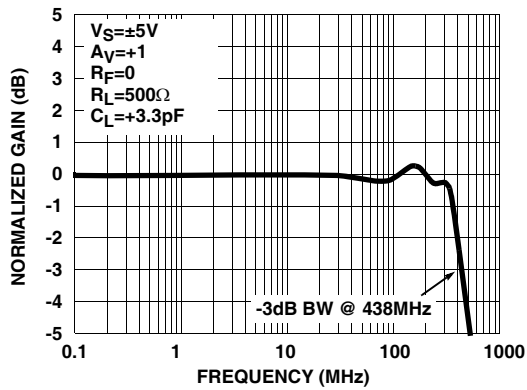


FIGURE 1. GAIN vs FREQUENCY (-3dB BANDWIDTH)

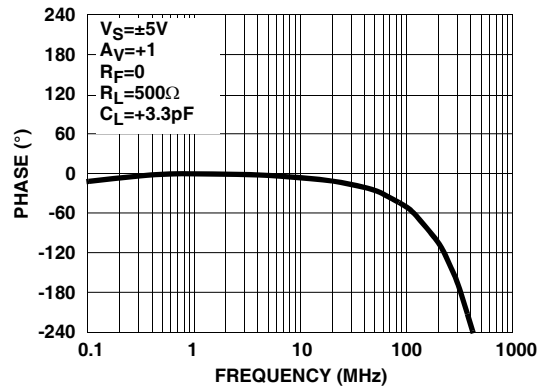


FIGURE 2. PHASE vs FREQUENCY

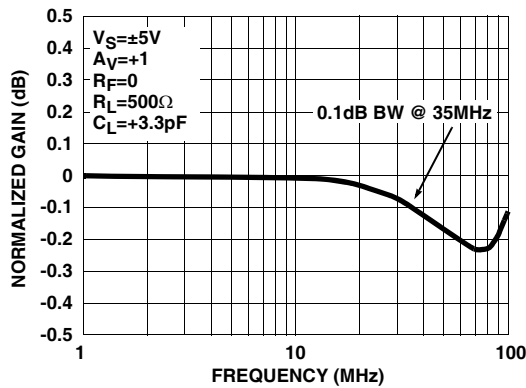


FIGURE 3. 0.1dB BANDWIDTH

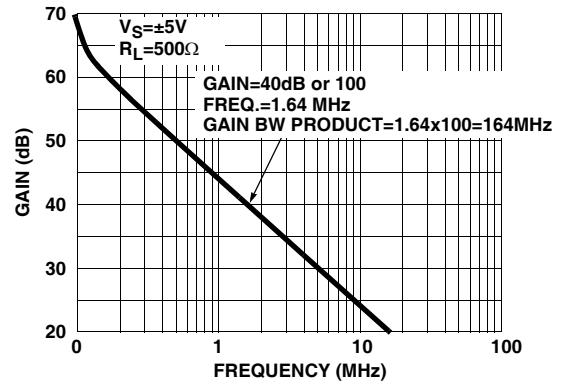


FIGURE 4. GAIN BANDWIDTH PRODUCT

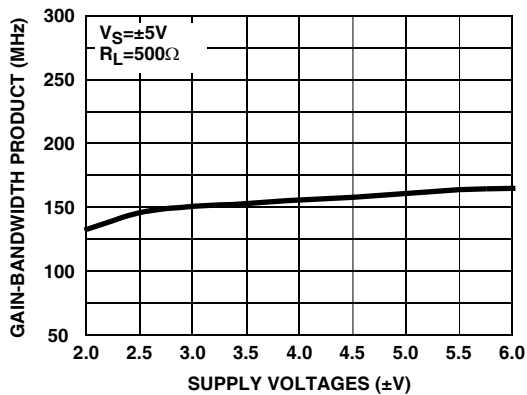


FIGURE 5. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGES

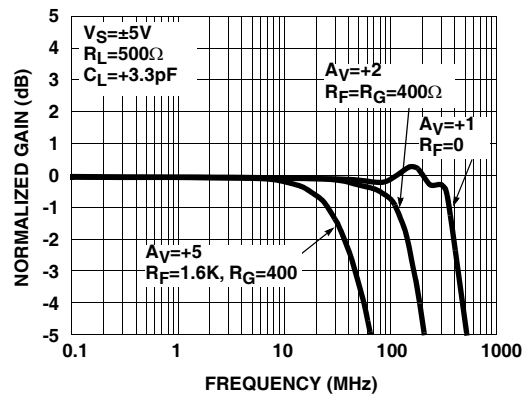


FIGURE 6. GAIN vs FREQUENCY FOR VARIOUS $+A_V$

Typical Performance Curves (Continued)

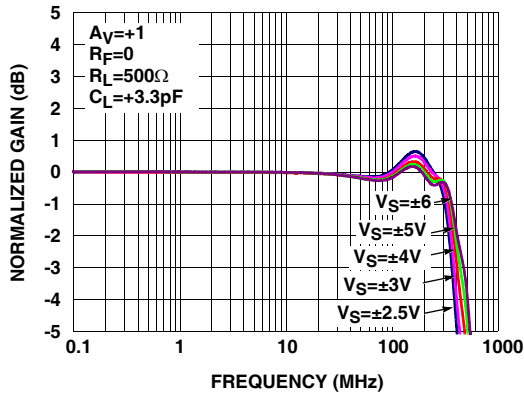


FIGURE 7. GAIN vs FREQUENCY FOR VARIOUS $\pm V_S$

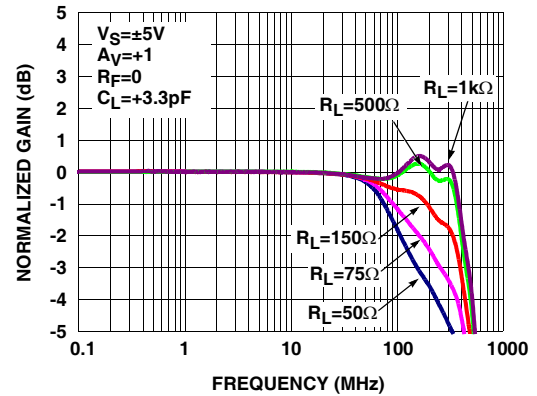


FIGURE 8. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} ($A_V = +1$)

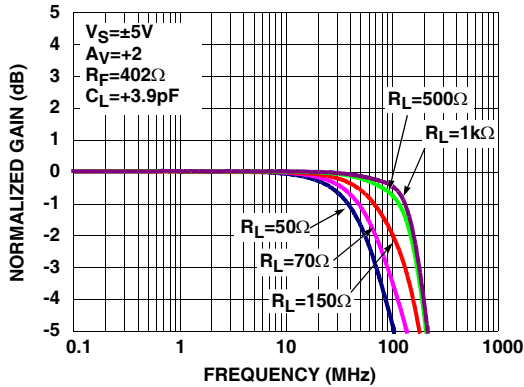


FIGURE 9. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} ($A_V = +2$)

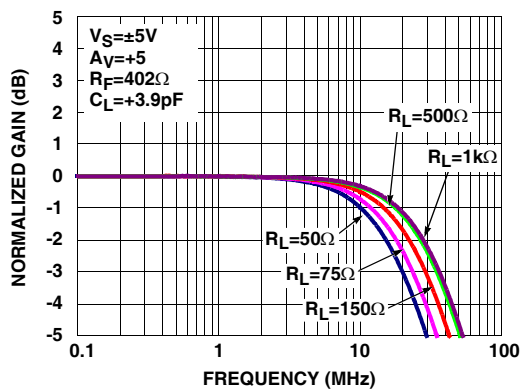


FIGURE 10. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} ($A_V = +5$)

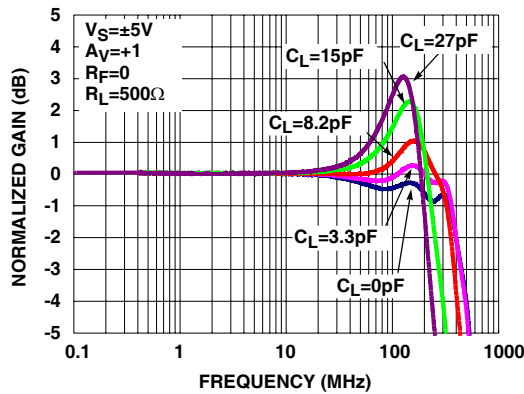


FIGURE 11. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} ($A_V = +1$)

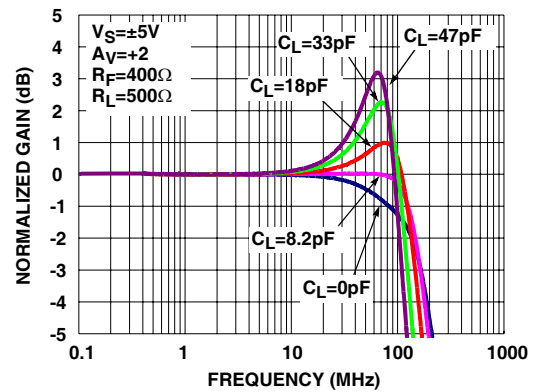


FIGURE 12. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} ($A_V = +2$)

Typical Performance Curves (Continued)

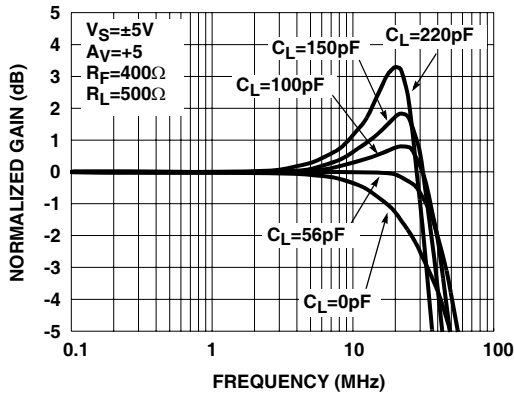


FIGURE 13. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} ($A_V = +5$)

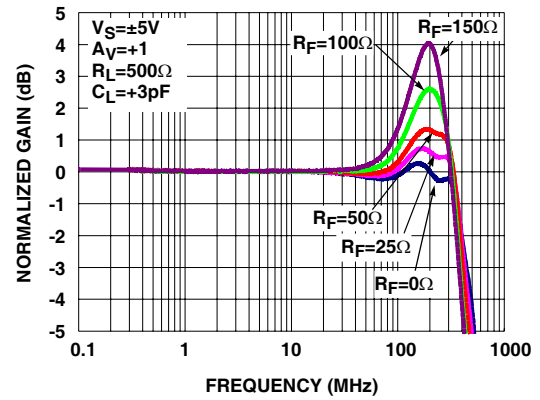


FIGURE 14. GAIN vs FREQUENCY FOR VARIOUS R_F ($A_V = +1$)

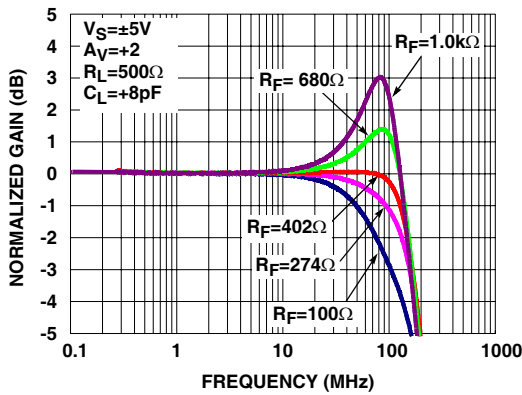


FIGURE 15. GAIN vs FREQUENCY FOR VARIOUS R_F ($A_V = +2$)

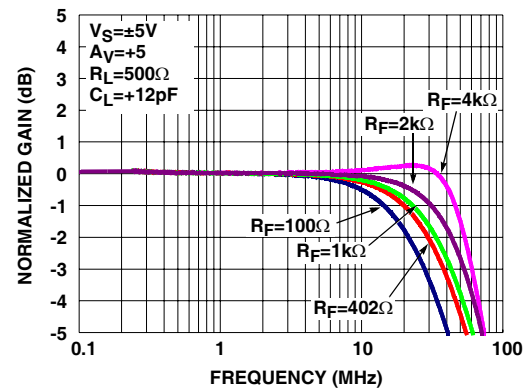


FIGURE 16. GAIN vs FREQUENCY FOR VARIOUS R_F ($A_V = +5$)

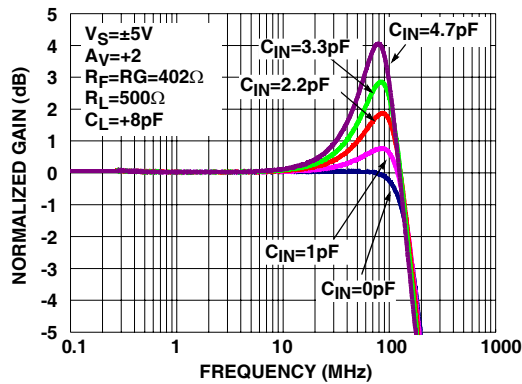


FIGURE 17. GAIN vs FREQUENCY FOR VARIOUS $C_{IN(-)}$ ($A_V = +2$)

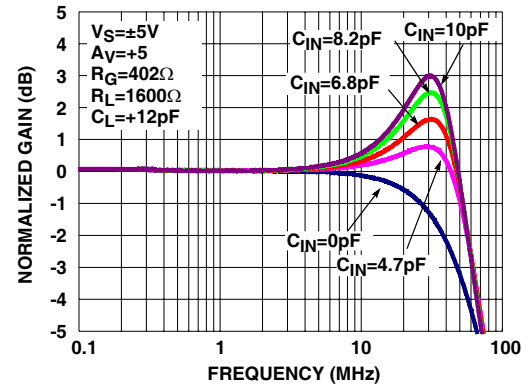


FIGURE 18. GAIN vs FREQUENCY FOR VARIOUS $C_{IN(-)}$ ($A_V = +5$)

Typical Performance Curves (Continued)

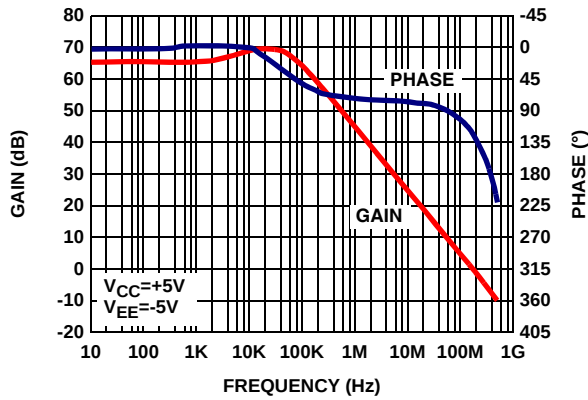


FIGURE 19. OPEN LOOP GAIN AND PHASE vs FREQUENCY

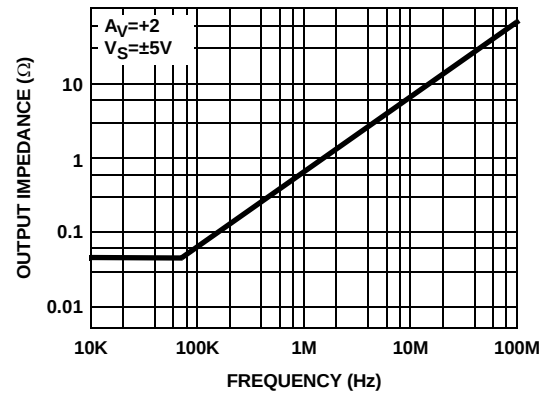


FIGURE 20. OUTPUT IMPEDANCE/PHASE vs FREQUENCY

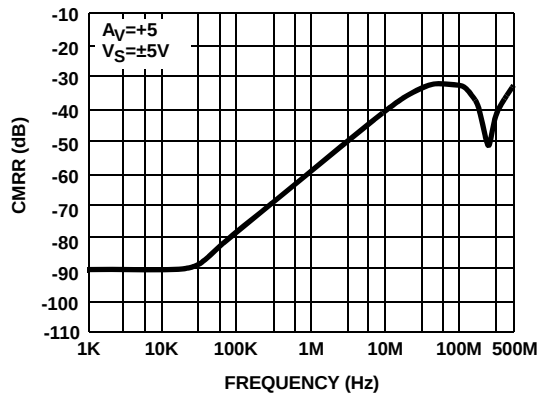


FIGURE 21. CMRR vs FREQUENCY

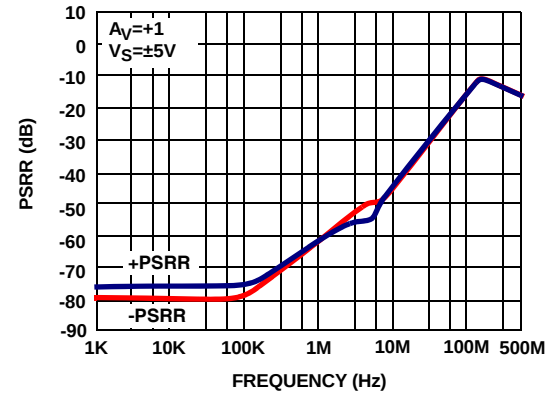


FIGURE 22. PSRR vs FREQUENCY

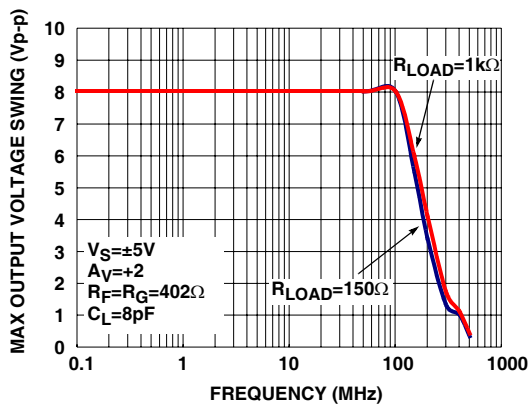


FIGURE 23. MAX OUTPUT VOLTAGE SWING vs FREQUENCY

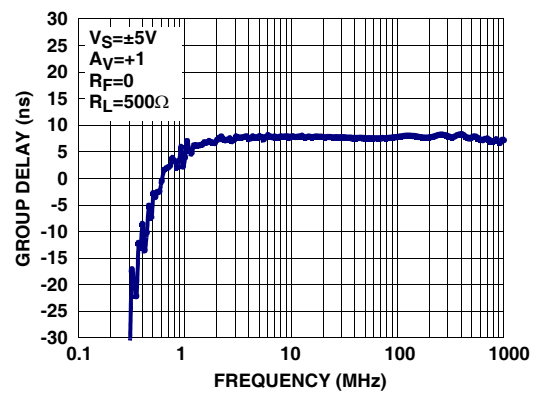


FIGURE 24. GROUP DELAY vs FREQUENCY

Typical Performance Curves (Continued)

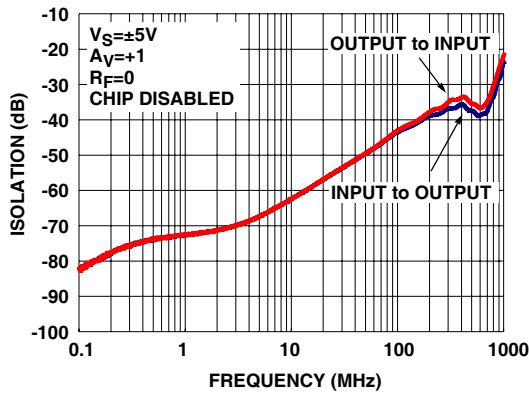


FIGURE 25. INPUT AND OUTPUT ISOLATION

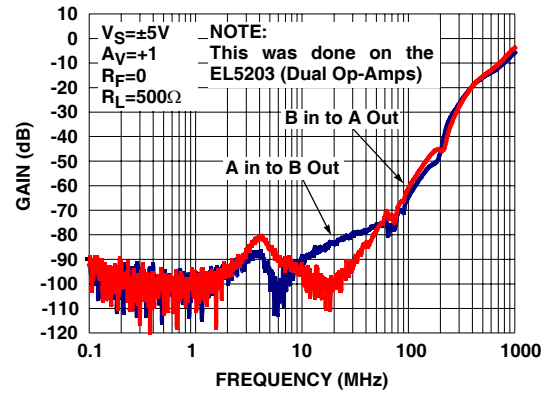


FIGURE 26. CHANNEL TO CHANNEL ISOLATION

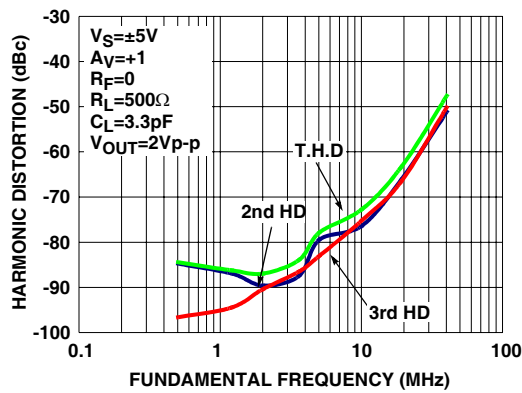


FIGURE 27. HARMONIC DISTORTION vs FREQUENCY

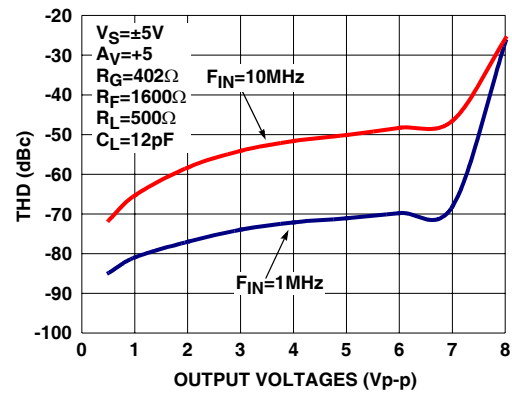


FIGURE 28. TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGES

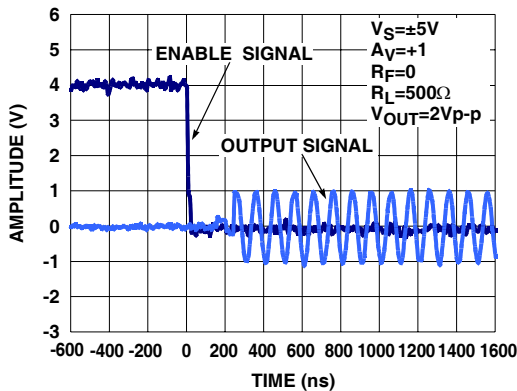


FIGURE 29. TURN-ON TIME

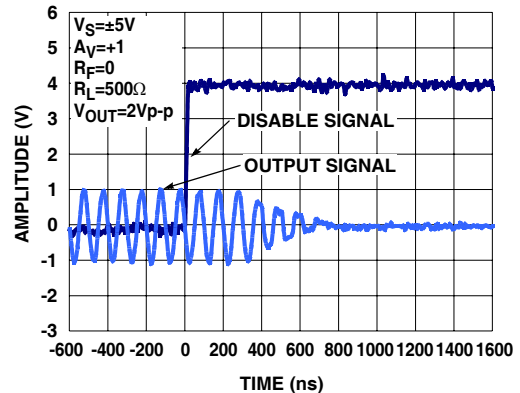


FIGURE 30. TURN-OFF TIME

Typical Performance Curves (Continued)

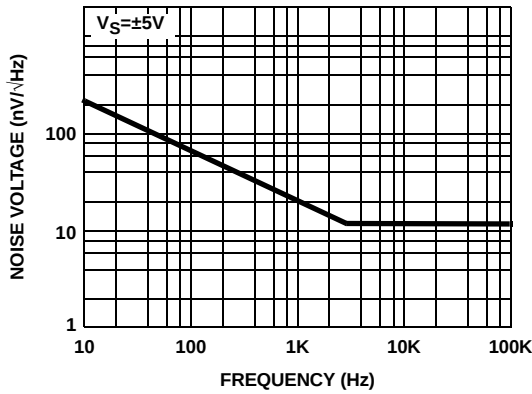


FIGURE 31. EQUIVALENT NOISE VOLTAGE vs FREQUENCY

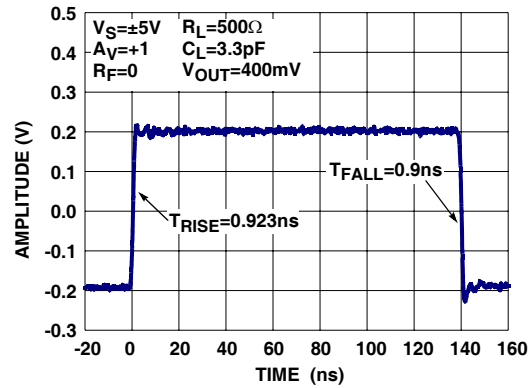


FIGURE 32. SMALL SIGNAL STEP RESPONSE_RISE AND FALL TIME

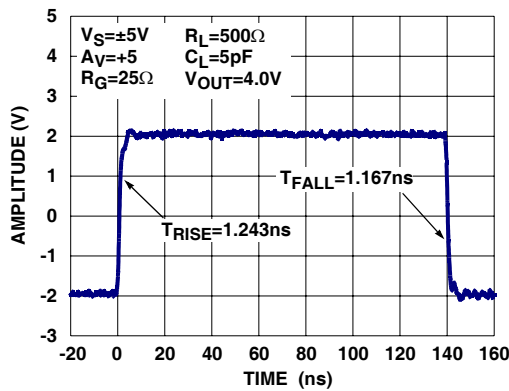


FIGURE 33. LARGE SIGNAL STEP RESPONSE_RISE AND FALL TIME

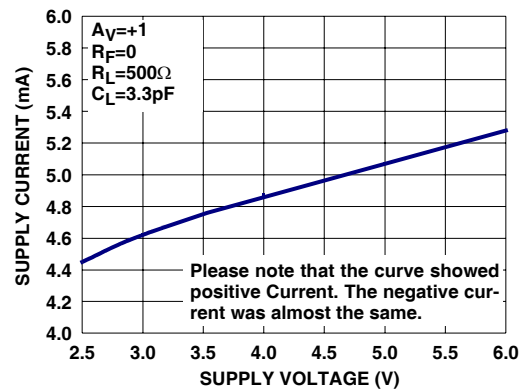


FIGURE 34. SUPPLY CURRENT vs SUPPLY VOLTAGE

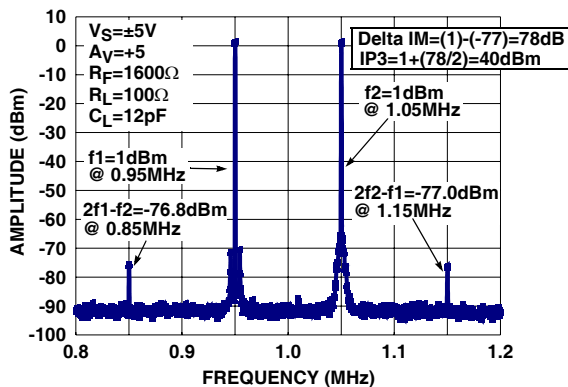


FIGURE 35. THIRD ORDER IMD INTERCEPT (IP3)

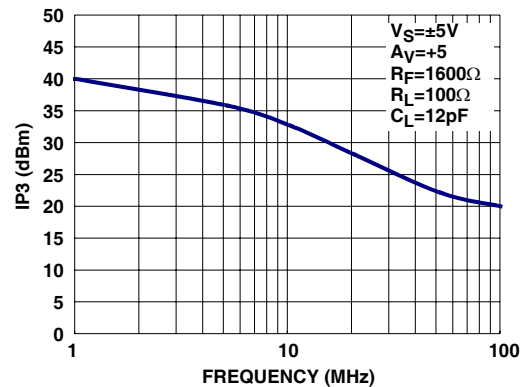


FIGURE 36. THIRD ORDER IMD INTERCEPT vs FREQUENCY

Typical Performance Curves (Continued)

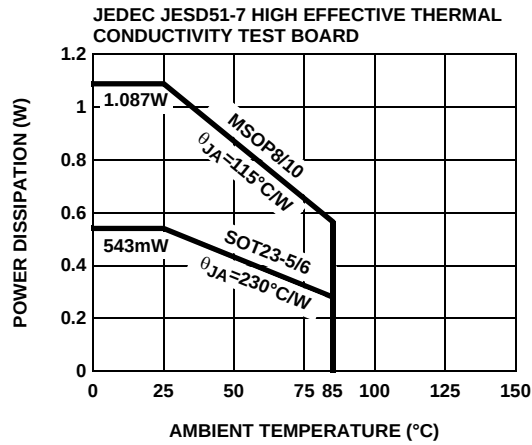


FIGURE 37. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

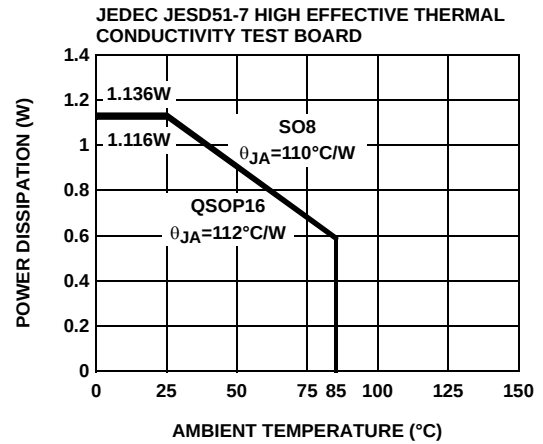


FIGURE 38. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

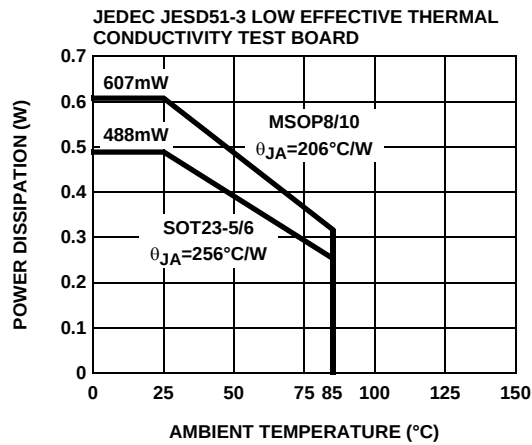


FIGURE 39. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

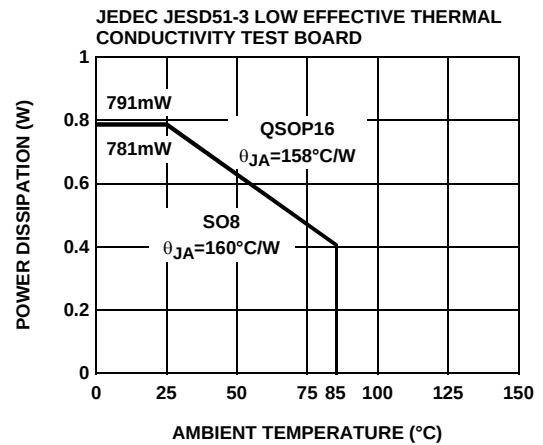
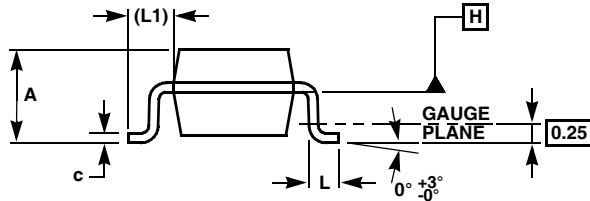
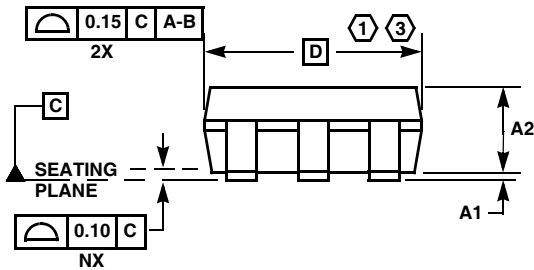
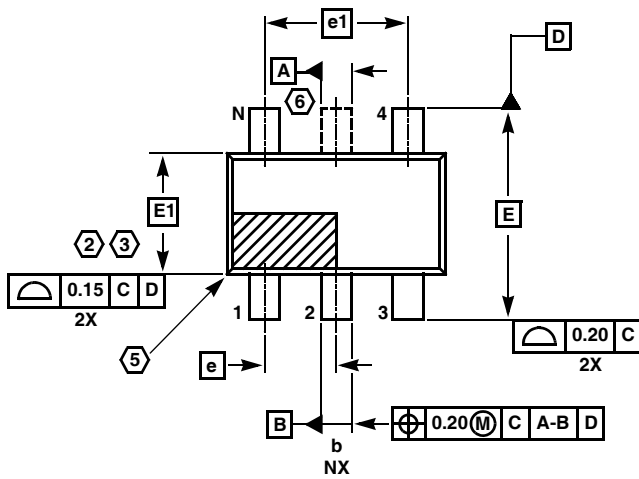


FIGURE 40. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

SOT-23 Package Family



MDP0038

SOT-23 PACKAGE FAMILY

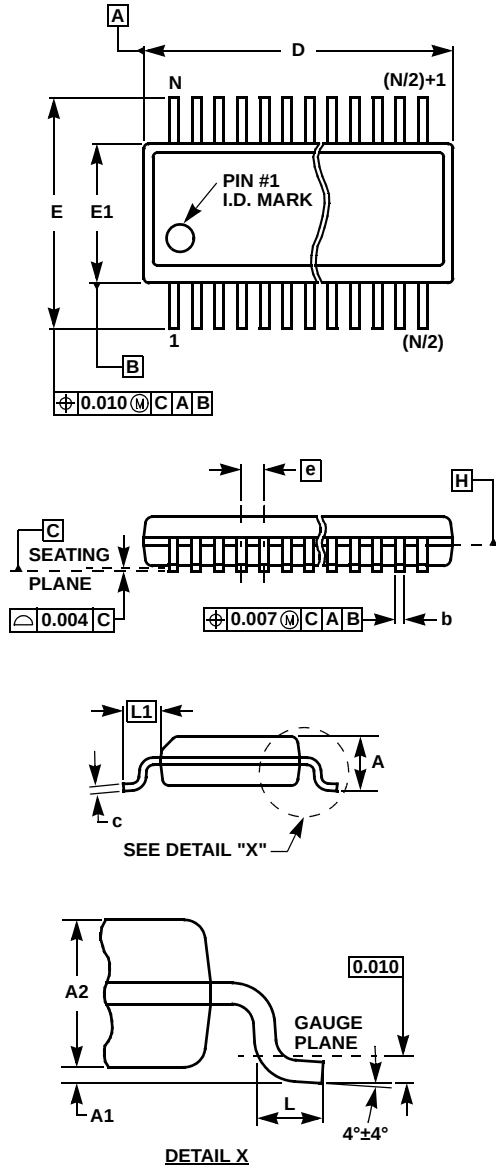
SYMBOL	SOT23-5	SOT23-6	TOLERANCE
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. E 3/00

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

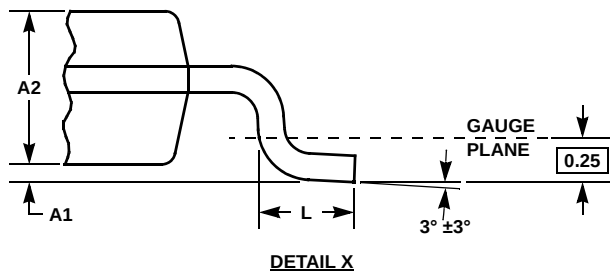
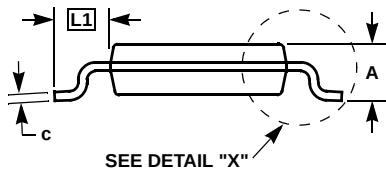
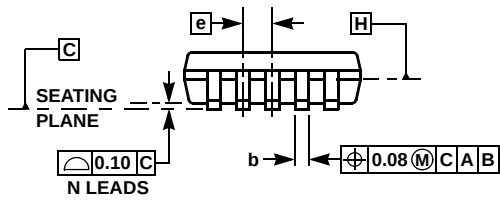
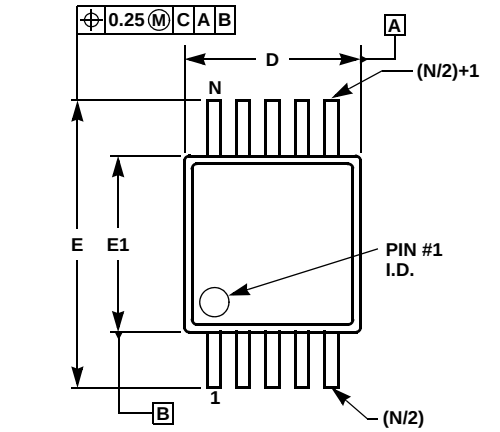
SYMBOL	QSOP16	QSOP24	QSOP28	TOLERANCE	NOTES
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. E 3/01

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

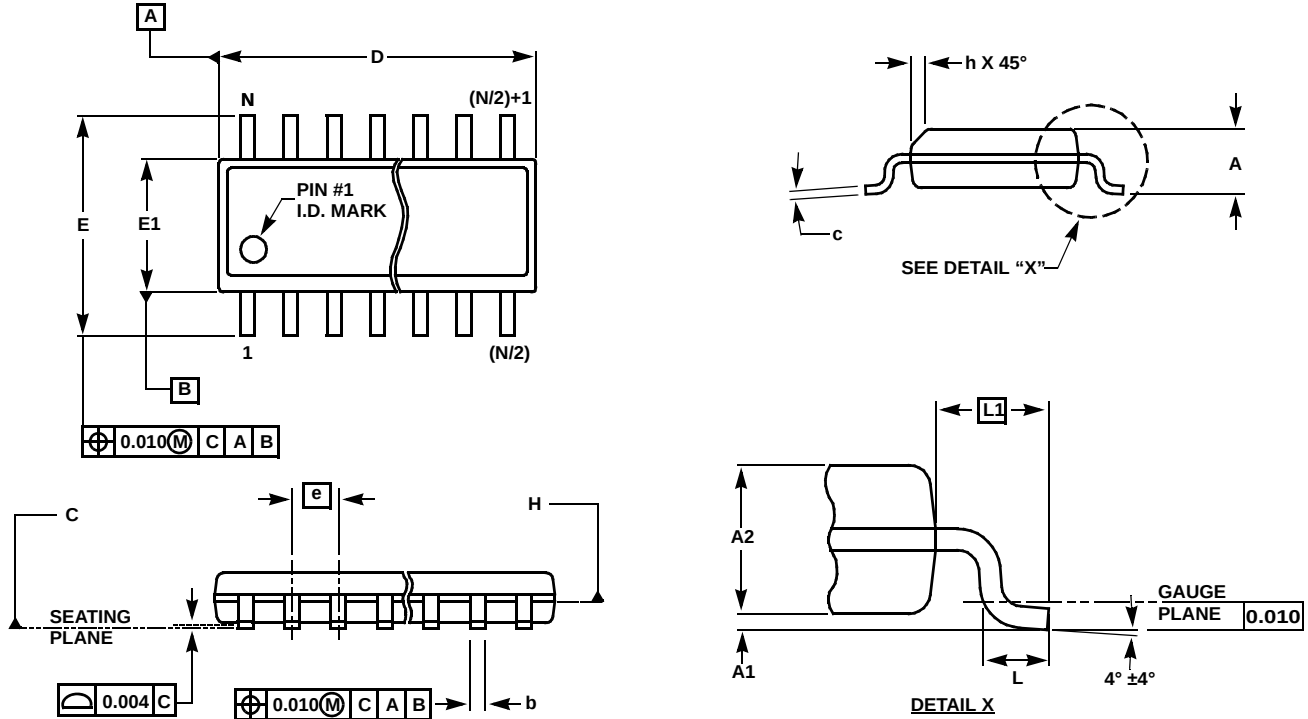
SYMBOL	MSOP8	MSOP10	TOLERANCE	NOTES
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. C 6/99

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

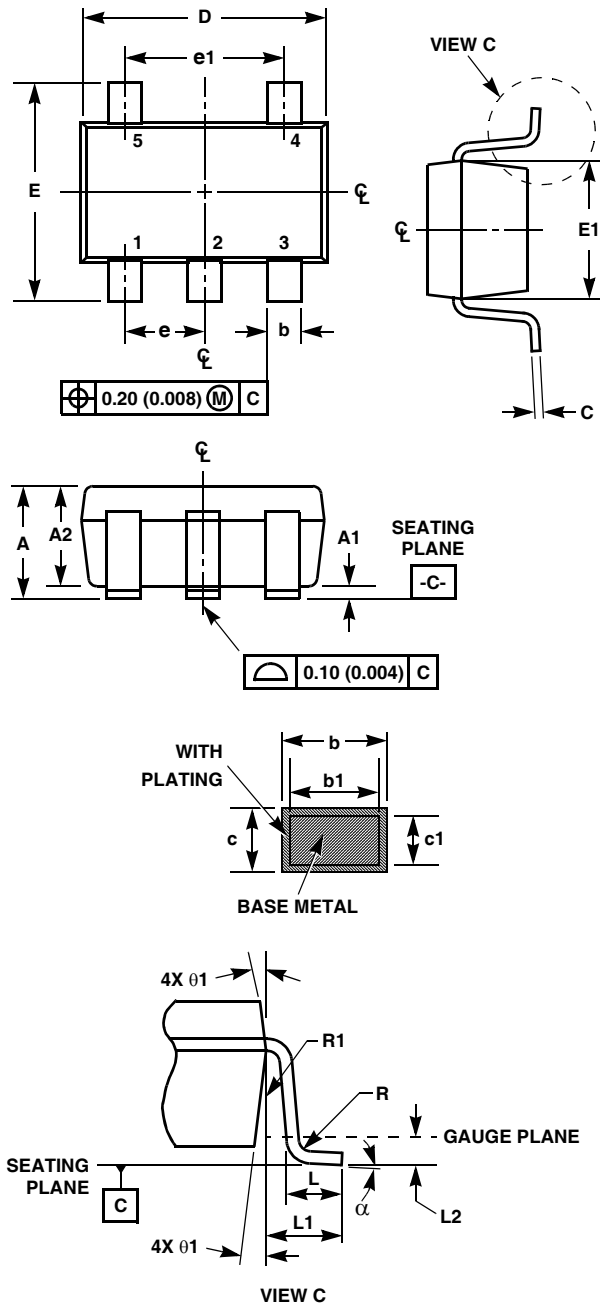
SYMBOL	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. L 2/01

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Small Outline Transistor Plastic Packages (SC70-5)



P5.049

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	-
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		-
α	0°	8°	0°	8°	-
N	5		5		5
R	0.004	-	0.10	-	-
R1	0.004	0.010	0.15	0.25	-

Rev. 2 9/03

NOTES:

1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. "N" is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.

Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com