

Electrical Characteristics

Operating Conditions

When Cyclone® III devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Cyclone III devices, system designers must consider the operating requirements within this document. Cyclone III devices are offered in both commercial and industrial grades. Commercial devices are offered in -6 (fastest), -7, and -8 speed grades.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone III devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Conditions beyond those listed in [Table 1-1](#) may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device. All parameters representing voltages are measured with respect to ground.

Symbol	Parameter	Min	Max	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	-0.5	1.8	V
V _{CCIO}	Supply voltage for output buffers	-0.5	3.9	V
V _{CCA}	Supply (analog) voltage for PLL regulator	-0.5	3.75	V
V _{CCD_PLL}	Supply (digital) voltage for PLL	-0.5	1.8	V
V _I	DC input voltage	-0.5	3.95	V
I _{OUT}	DC output current, per pin	-25	40	mA
V _{ESDHBM}	Electrostatic discharge voltage using the human body model	NA	±2000	V
V _{ESDCDM}	Electrostatic discharge voltage using the charged device model	NA	±500	V
T _{STG}	Storage temperature	-65	150	°C
T _J	Operating junction temperature	-40	125	°C

Note to Table 1-1:

- (1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

Maximum Allowed Overshoot/Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in [Table 1-2](#) and undershoot to -2.0 V for input currents less than 100 mA and for periods shorter than 20 ns.

[Table 1-2](#) lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as percentage of high-time over the lifetime of the device.

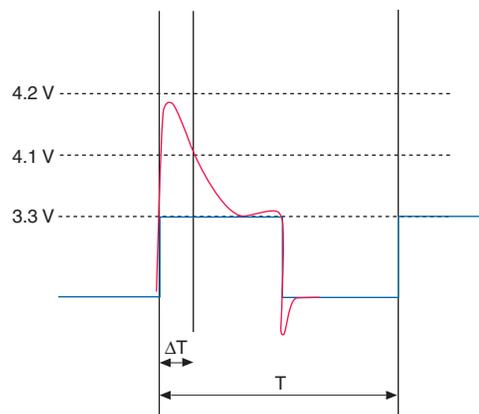
A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.2 V can only be at 4.2 V for 10.74% over the lifetime of the device; for device lifetime of 10 years, this amounts to 10.74/10ths of a year. [Figure 1–1](#) shows the way to determine the overshoot duration.

Symbol	Parameter	Condition	Overshoot Duration as % of High Time	Unit
Vi	AC Input Voltage	$V_I = 3.95 \text{ V}$	100	%
		$V_I = 4.0 \text{ V}$	95.67	%
		$V_I = 4.05 \text{ V}$	55.24	%
		$V_I = 4.10 \text{ V}$	31.97	%
		$V_I = 4.15 \text{ V}$	18.52	%
		$V_I = 4.20 \text{ V}$	10.74	%
		$V_I = 4.25 \text{ V}$	6.23	%
		$V_I = 4.30 \text{ V}$	3.62	%
		$V_I = 4.35 \text{ V}$	2.1	%
		$V_I = 4.40 \text{ V}$	1.22	%
		$V_I = 4.45 \text{ V}$	0.71	%
		$V_I = 4.50 \text{ V}$	0.41	%
		$V_I = 4.60 \text{ V}$	0.14	%
		$V_I = 4.70 \text{ V}$	0.047	%

Note to Table 1–2:

- (1) [Figure 1–1](#) shows the methodology to determine the overshoot duration. In the example in [Figure 1–1](#), overshoot voltage is shown in red and is present on the Cyclone III input pin at over 4.1 V but below 4.2 V. From [Table 1–1](#), for an overshoot of 4.1 V the percentage of high time for the overshoot can be as high as 31.97% over a 10-year period. Percentage of high time is calculated as $(\Delta T)/T \times 100$. This 10-year period assumes the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations where the device is in an idle state, lifetimes are increased.

Figure 1–1. Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone III devices. The steady-state voltage and current values expected from Cyclone III devices are provided in [Table 1-3](#). All supplies must be strictly monotonic without plateaus.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCINT} (3)	Supply voltage for internal logic and input buffers	—	1.15	1.2	1.25	V
V_{CCIO} (3)	Supply voltage for output buffers, 3.3-V operation	—	3.15	3.3	3.45	V
	Supply voltage for output buffers, 3.0-V operation	—	2.85	3	3.15	V
	Supply voltage for output buffers, 2.5-V operation	—	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	—	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	—	1.425	1.5	1.575	V
	Supply voltage for output buffers, 1.2-V operation	—	1.14	1.2	1.26	V
V_{CCA} (3)	Supply (analog) voltage for PLL regulator	—	2.375	2.5	2.625	V
V_{CCD_PLL} (3)	Supply (digital) voltage for PLL	—	1.15	1.2	1.25	V
V_I	Input voltage	—	-0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	-40	—	100	°C
t_{RAMP}	Power supply ramptime	Standard POR (4)	50 μ s	—	50 ms	—
		Fast POR (5)	50 μ s	—	3 ms	—

Notes to Table 1-3:

- (1) V_{CCIO} for all I/O banks should be powered up during device operation. All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.
- (2) V_{CCD_PLL} must always be connected to V_{CCINT} through a decoupling capacitor and ferrite bead.
- (3) The V_{CC} must rise monotonically.
- (4) POR time for Standard POR ranges between 50 – 200 ms. All supplies must be up and stable within 50 ms.
- (5) POR time for Fast POR ranges between 3 – 9 ms. All supplies must be up and stable within 3 ms.

DC Characteristics

This section lists the I/O leakage currents, pin capacitance, on chip termination tolerance and and bus hold specifications for Cyclone III devices.

Supply Current

Standby current is the current the device draws after the device is configured with no inputs/outputs toggling and no activity in the device. Since these currents vary largely with resources used, use the Excel-based Early Power Estimator to get supply current estimates for your design. [Table 1-4](#) lists I/O pin leakage current for Cyclone III devices.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input Pin Leakage Current	$V_I = V_{CCIO_MAX}$ to 0 V	-10	—	10	μ A
I_{OZ}	Tri-stated I/O Pin Leakage Current	$V_O = V_{CCIO_MAX}$ to 0 V	-10	—	10	μ A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CCINT0}	V_{CCINT} supply current (standby)	$V_I =$ ground, no load, no toggling inputs, $T_J = 25C$	EP3C5	1.7	(3)	mA
			EP3C10	1.7		mA
			EP3C16	3.0		mA
			EP3C25	3.5		mA
			EP3C40	4.3		mA
			EP3C55	5.2		mA
			EP3C80	6.5		mA
			EP3C120	8.4		mA
I_{CCA0}	V_{CCA} supply current (standby)	$V_I =$ ground, no load, no toggling inputs, $T_J = 25C$	EP3C5	11.3	(3)	mA
			EP3C10	11.3		mA
			EP3C16	11.4		mA
			EP3C25	18.4		mA
			EP3C40	18.6		mA
			EP3C55	18.7		mA
			EP3C80	18.9		mA
			EP3C120	19.2		mA
I_{CCD_PLL0}	V_{CCD_PLL} supply current (standby)	$V_I =$ ground, no load, no toggling inputs, $T_J = 25C$	EP3C5	4.1	(3)	mA
			EP3C10	4.1		mA
			EP3C16	8.2		mA
			EP3C25	8.2		mA
			EP3C40	8.2		mA
			EP3C55	8.2		mA
			EP3C80	8.2		mA
			EP3C120	8.2		mA
I_{CCIO0}	V_{CCIO} supply current (standby)	$V_I =$ ground, no load, no toggling inputs, $T_J = 25C$	EP3C5	0.6	(3)	mA
			EP3C10	0.6		mA
			EP3C16	0.9		mA
			EP3C25	0.9		mA
			EP3C40	1.3		mA
			EP3C55	1.3		mA
			EP3C80	1.3		mA
			EP3C120	1.2		mA

Notes to Table 1–4:

- (1) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).
- (2) 10 μA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.
- (3) Maximum values depend on the actual T_J and design utilization. Refer to the Excel-based PowerPlay Early Power Estimator (available at www.altera.com/support/devices/estimator/cy3-estimator/cy3-power_estimator.html) or the Quartus II PowerPlay Power Analyzer feature for maximum values. Refer to the “Power Consumption” on page 1–11” for more information.

Bus Hold

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode. Table 1-5 lists bus hold specifications for Cyclone III devices. Also listed are the input pin capacitances and on-chip termination tolerance specifications.

Table 1-5. Cyclone III Bus Hold Parameter *Note (1)*

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN} > V_{IL}$ (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	μ A
Bus-hold high, sustaining current	$V_{IN} < V_{IL}$ (minimum)	-8	—	-12	—	-30	—	-50	—	-70	—	-70	—	μ A
Bus-hold low, overdrive current	$0\text{ V} < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	μ A
Bus-hold high, overdrive current	$0\text{ V} < V_{IN} < V_{CCIO}$	—	-125	—	-175	—	-200	—	-300	—	-500	—	-500	μ A
Bus-hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Note to Table 1-5:

(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

On-Chip Termination (OCT) Specifications

Table 1-6 lists variation of uncalibrated OCT across process, temperature, and voltage.

Table 1-6. Uncalibrated On-Chip Series Termination Specifications						Preliminary
Symbol	V_{CCIO} (V)	Resistance Tolerance				Unit
		Commercial		Industrial		
		Min	Max	Min	Max	
Series Termination without calibration	3.0	-30	+30	(1)	(1)	%
	2.5	-30	+30	(1)	(1)	%
	1.8	-30	+30	(1)	(1)	%
	1.5	-30	+30	(1)	(1)	%
	1.2	-40	+40	(1)	(1)	%

Note to Table 1-6:

(1) Pending silicon characterization.

OCT calibration is automatically performed at power up for OCT enabled I/Os.

Table 1-7 lists the OCT calibration accuracy at power up.

Table 1-7. On-Chip Series Termination Power-up Calibration Specifications				Preliminary
Symbol	V_{CCIO} (V)	Calibration Accuracy		Unit
		Commercial Max	Industrial Max	
Series Termination with power-up calibration	3.0	±10%	(1)	%
	2.5	±10%	(1)	%
	1.8	±10%	(1)	%
	1.5	±10%	(1)	%
	1.2	±10%	(1)	%

Note to Table 1-7:

- (1) Pending silicon characterization.

Table 1-8 lists the percentage change of the OCT resistance with voltage and temperature. Use Table 1-8 and Equation 1-1 to determine OCT variation after power-up calibration.

Table 1-8. On-Chip Termination Variation After Power-up Calibration		
Nominal Voltage	dR/dT (%ΔOhm/°C)	dR/dmV (%ΔOhm/mV)
3.0	0.262	-0.026
2.5	0.234	-0.039
1.8	0.219	-0.086
1.5	0.199	-0.136
1.2	0.161	-0.288

Note to Table 1-8:

- (1) This table is needed to calculate the final OCT resistance with the variation of temperature and voltage.

Equation 1-1. Notes (1), (2), (3), (4), (5), (6), (7), (8), (9), (10), (11), (12)

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dmV \text{ — (1)}$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT \text{ — (2)}$$

$$\text{For } \Delta R_x < 0; MF_x = 1 / (|\Delta R_x| / 100 + 1) \text{ — (3)}$$

$$\text{For } \Delta R_x > 0; MF_x = \Delta R_x / 100 + 1 \text{ — (4)}$$

$$MF = MF_V \times MF_T \text{ — (5)}$$

$$R_{\text{final}} = R_{\text{initial}} \times MF \text{ — (6)}$$

Notes to Equation 1-1:

- (1) ΔR_V is variation of resistance with voltage.
- (2) ΔR_T is variation of resistance with temperature.
- (3) dR/dT is the percentage change of resistance with temperature.
- (4) dR/dmV is the percentage change of resistance with voltage.
- (5) V_2 is final voltage.
- (6) V_1 is the initial voltage.
- (7) T_2 is the final temperature.
- (8) T_1 is the initial temperature.
- (9) MF is multiplication factor.
- (10) R_{final} is final resistance.
- (11) R_{initial} is initial resistance.
- (12) Subscript x refers to both v and T.

For example, to calculate the change of 50 Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V,

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$$

$$\Delta R_T = (85 - 25) \times 0.262 = 15.72$$

Since ΔR_V is negative,

$$MF_V = 1 / (3.83/100 + 1) = 0.963$$

Since ΔR_T is positive,

$$MF_T = 15.72/100 + 1 = 1.157$$

$$MF = 0.963 \times 1.157 = 1.114$$

$$R_{\text{final}} = 50 \times 1.114 = \underline{55.71 \Omega}$$

Pin Capacitance

Table 1-9 shows the Cyclone III device family pin capacitance.

Table 1-9. Cyclone III Device Pin Capacitance Note (1) (Part 1 of 2)				Preliminary
Symbol	Parameter	Typical – QFP	Typical – FBGA	Unit
C_{IOTB}	Input capacitance on top/bottom I/O pins	7	6	pF
C_{IOLR}	Input capacitance on left/right I/O pins	6	5	pF
$C_{LVDSLRL}$	Input capacitance on left/right I/O pins with Dedicated LVDS output	8	7	pF
C_{VREFLR}	Input capacitance on left/right I/O pins with V_{REF}	21	21	pF
C_{VREFTB}	Input capacitance on top/bottom I/O pins with V_{REF}	23 (2)	23 (2)	pF
C_{CLKTB}	Input capacitance on top/bottom dedicated clock input pins	7	6	pF

Table 1–9. Cyclone III Device Pin Capacitance <i>Note (1) (Part 2 of 2)</i>				Preliminary
Symbol	Parameter	Typical – QFP	Typical – FBGA	Unit
C _{CLKLR}	Input capacitance on left/right dedicated clock input pins	6	5	pF

Notes to Table 1–9:

- (1) Pending silicon characterization.
- (2) C_{VREFTB} for EP3C25 is 30 pF.

Internal Weak Pull-up and Weak Pull-down Resistor

Table 1–10 lists the weak pull-up and pull-down resistor values for Cyclone III devices.

Table 1–10. Cyclone III Internal Weak Pull-Up/Weak Pull-Down Resistor <i>Note (1)</i>						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{CONF_PU} (2)	Value of I/O pin pull-up resistor before and during configuration	V _I = 0 V, V _{CCIO} = 3.3 V ± 5% (3), (4)	7	25	41	KΩ
		V _I = 0 V, V _{CCIO} = 3.0 V ± 5% (3), (4)	7	28	47	KΩ
		V _I = 0 V, V _{CCIO} = 2.5 V ± 5% (3), (4)	8	35	61	KΩ
		V _I = 0 V, V _{CCIO} = 1.8 V ± 5% (3), (4)	10	57	108	KΩ
		V _I = 0 V, V _{CCIO} = 1.5 V ± 5% (3), (4)	13	82	163	KΩ
		V _I = 0 V, V _{CCIO} = 1.2 V ± 5% (3), (4)	19	143	351	KΩ
R _{CONF_PD} (2)	Value of I/O pin pull-down resistor before and during configuration	V _I = 0 V, V _{CCIO} = 3.3 V ± 5% (3), (4)	6	19	30	KΩ
		V _I = 0 V, V _{CCIO} = 3.0 V ± 5% (3), (4)	6	22	36	KΩ
		V _I = 0 V, V _{CCIO} = 2.5 V ± 5% (3), (4)	6	25	43	KΩ
		V _I = 0 V, V _{CCIO} = 1.8 V ± 5% (3), (4)	7	35	71	KΩ
		V _I = 0 V, V _{CCIO} = 1.5 V ± 5% (3), (4)	8	50	112	KΩ

Notes to Table 1–10:

- (1) All I/O pins have an option to enable weak pull-up except configuration, test and JTAG pin. Weak pull-down feature is only available for JTAG TCK.
- (2) R_{CONF} values are based on characterization. R_{CONF} = V_{CCIO}/I_{RCONF}. R_{CONF} values may be different if V_I value is not 0 V. V_I refers to the input voltage at the I/O pin.
- (3) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) Minimum condition at –40°C and high V_{CC}, typical condition at 25°C and nominal V_{CC} and maximum condition at 125°C and low V_{CC} for R_{CONF} values.

Hot Socketing

Table 1–11 lists the hot-socketing specifications for Cyclone III devices.

Table 1–11. Cyclone III Hot Socketing Specifications		
Symbol	Parameter	Maximum
I _{IOPIN(DC)}	DC current per I/O pin	300 μA
I _{IOPIN(AC)}	AC current per I/O pin	8 mA (1)

Note to Table 1–11:

- (1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |I_{IOPIN}| = C dv/dt, where C is I/O pin capacitance and dv/dt is the slew rate.

I/O Standard Specifications

The following tables list input voltage sensitivities (V_{IH} and V_{IL}), and output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Cyclone III devices. Tables 1–12 to 1–17 show the Cyclone III device family I/O standard specifications. Refer to “Single-ended Voltage referenced I/O Standard” in “Glossary” for voltage referenced receiver input waveform and explanation of terms used in Table 1–12.

Table 1–12. Single-Ended I/O Standard Specifications Note (1)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (3) (mA)	I_{OH} (3) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTTL (2)	3.15	3.3	3.45	—	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS (2)	3.15	3.3	3.45	—	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	–2
3.0-V LVTTTL (2)	2.85	3.0	3.15	–0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	–4
3.0-V LVCMOS (2)	2.85	3.0	3.15	–0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCIO} - 0.2$	0.1	–0.1
2.5-V LVTTTL and LVCMOS (2)	2.375	2.5	2.625	–0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.2	2.1	0.1	–0.1
								0.4	2.0	1	–1
								0.7	1.7	2	–2
1.8-V LVTTTL and LVCMOS	1.71	1.8	1.89	–0.3	$0.35 * V_{CCIO}$	$0.65 * V_{CCIO}$	2.25	0.45	$V_{CCIO} - 0.45$	2	–2
1.5-V LVCMOS	1.425	1.5	1.575	–0.3	$0.35 * V_{CCIO}$	$0.65 * V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 * V_{CCIO}$	$0.75 * V_{CCIO}$	2	–2
1.2-V LVCMOS	1.14	1.2	1.26	–0.3	$0.35 * V_{CCIO}$	$0.65 * V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 * V_{CCIO}$	$0.75 * V_{CCIO}$	2	–2
PCI and PCI-X	2.85	3.0	3.15	—	$0.3 * V_{CCIO}$	$0.5 * V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 * V_{CCIO}$	$0.9 * V_{CCIO}$	1.5	–0.5

Notes to Table 1–12:

- (1) AC load $CL = 10$ pF.
- (2) For more detail of interfacing Cyclone III devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O standards, refer to AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTTL and LVCMOS I/O Systems.
- (3) Specified I_{OL} and I_{OH} are valid with lowest current strength setting available for respective I/O standards. I_{OL} and I_{OH} values correspond to the selected current strength settings value. For example, current drive characteristics for 3.3-V LVTTTL with 8 mA current strength setting are 8 mA (I_{OL}) and –8 mA (I_{OH}) at 0.45 V (V_{OL}) and 2.4 V (V_{OH}), respectively.

Refer to “Glossary” for explanation of terms used in Table 1–13.

Table 1–13. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V) (3)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	$0.48 * V_{CCIO}$ (1)	$0.5 * V_{CCIO}$ (1)	$0.52 * V_{CCIO}$ (1)	—	$0.5 * V_{CCIO}$	—
				$0.47 * V_{CCIO}$ (2)	$0.5 * V_{CCIO}$ (2)	$0.53 * V_{CCIO}$ (2)			

Notes to Table 1–13:

- (1) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.
- (2) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.
- (3) V_{TT} of transmitting device must track V_{REF} of the receiving device.

Table 1–14. Single-Ended SSTL and HSTL I/O Standards Signal Specifications

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	$V_{REF} - 0.18$	$V_{REF} + 0.18$	—	—	$V_{REF} - 0.35$	$V_{REF} + 0.35$	—	$V_{TT} - 0.57$	$V_{TT} + 0.57$	8.1	-8.1
SSTL-2 Class II	—	$V_{REF} - 0.18$	$V_{REF} + 0.18$	—	—	$V_{REF} - 0.35$	$V_{REF} + 0.35$	—	$V_{TT} - 0.76$	$V_{TT} + 0.76$	16.4	-16.4
SSTL-18 Class I	—	$V_{REF} - 0.125$	$V_{REF} + 0.125$	—	—	$V_{REF} - 0.25$	$V_{REF} + 0.25$	—	$V_{TT} - 0.475$	$V_{TT} + 0.475$	6.7	-6.7
SSTL-18 Class II	—	$V_{REF} - 0.125$	$V_{REF} + 0.125$	—	—	$V_{REF} - 0.25$	$V_{REF} + 0.25$	—	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	—	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	-0.24	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.24$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	-0.24	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.24$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	14	-14



For more illustrations of receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*.

Table 1–15. Differential SSTL I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			$V_{Swing(DC)}$ (V)		$V_{X(DC)}$ (V)			$V_{Swing(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.7	V_{CCIO}	(1)	—	(1)
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	V_{CCIO}	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	V_{CCIO}	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$

Note to Table 1–15:

(1) Pending silicon characterization.

Table 1–16. Differential HSTL I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	$0.48 * V_{CCIO}$	—	$0.52 * V_{CCIO}$	$0.48 * V_{CCIO}$	—	$0.52 * V_{CCIO}$	0.3	$0.48 * V_{CCIO}$

Refer to “Transmitter Output Waveform” in “Glossary” for an explanation of terms used in Table 1–17.

Table 1–17. Differential I/O Standard Specifications

I/O Standard	V _{CCIO} (V)			V _{TH} (mV)			V _{IN} (V)			V _{OD} (mV) (1)			V _{OS} (V) (1)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (Row I/Os) (2)	2.375	2.5	2.625	-100	V _{CM} = 1.25V	100	0	D _{MAX} ≤ 500 Mbps	1.85	247	—	600	1.125	1.25	1.375
							0.5	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.85						
							1	D _{MAX} > 700 Mbps	1.6						
LVPECL (Column I/Os) (2)	2.375	2.5	2.625	-100	V _{CM} = 1.25V	100	0	D _{MAX} ≤ 500 Mbps	1.85	247	—	600	1.125	1.25	1.375
							0.5	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.85						
							1	D _{MAX} > 700 Mbps	1.6						
LVDS (Row I/Os)	2.375	2.5	2.625	-100	V _{CM} = 1.25V	100	0	D _{MAX} ≤ 500 Mbps	1.85	247	—	600	1.125	1.25	1.375
							0.5	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.85						
							1	D _{MAX} > 700 Mbps	1.6						
LVDS (Column I/Os)	2.375	2.5	2.625	-100	V _{CM} = 1.25V	100	0	D _{MAX} ≤ 500 Mbps	1.85	247	—	600	1.125	1.25	1.375
							0.5	500 Mbps ≤ D _{MAX} ≤ 700 Mbps	1.85						
							1	D _{MAX} > 700 Mbps	1.6						
mini-LVDS (Row I/Os) (3)	2.375	2.5	2.625	—	—	—	—	—	—	300	—	600	1.0	1.2	1.4
mini-LVDS (Column I/Os) (3)	2.375	2.5	2.625	—	—	—	—	—	—	300	—	600	1.0	1.2	1.4
RSDS® (Row I/Os) (3) (4)	2.375	2.5	2.625	—	—	—	—	—	—	100	200	600	0.5	1.2	1.5
RSDS (Column I/Os) (3)	2.375	2.5	2.625	—	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS® (Row I/Os) (3) (4)	2.375	2.5	2.625	—	—	—	—	—	—	100	200	600	0.5	1.2	1.4
PPDS (Column I/Os) (3)	2.375	2.5	2.625	—	—	—	—	—	—	100	200	600	0.5	1.2	1.4

Notes to Table 1–17:

- (1) R_L range : 90 ≤ R_L ≤ 110 Ω
- (2) LVPECL input standard is only supported at clock input. Output standard is not supported.
- (3) Mini-LVDS, RSDS and PPDS standards are only supported at output pins of Cyclone III devices.
- (4) RSDS and PPDS are registered trademarks of National Semiconductor.

Power Consumption

Altera offers two ways to estimate power for a design: the Excel-based Early Power Estimator and the Quartus® II **PowerPlay Power Analyzer** feature.

The interactive Excel-based Early Power Estimator is typically used prior to designing the device in order to get a magnitude estimate of the device power. The Quartus II **PowerPlay Power Analyzer** provides better quality estimates based on the specifics of the design after place-and-route is complete. The **PowerPlay Power Analyzer** can apply a combination of user-entered, simulation-derived, and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.



For more information on power estimation tools, refer to the *Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of the Cyclone III core and periphery blocks for commercial grade devices.

These characteristics can be designated as *Preliminary* or *Final*. Each designation is defined below.

Preliminary	Final
Preliminary characteristics are created using simulation results, process data, and other known parameters.	Final numbers are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage and junction temperature conditions.

The upper-right hand corner of a table shows the designation as *Preliminary* or *Final*.

Core Performance Specifications

Clock Tree Specifications

Table 1–18 lists the clock tree specifications for Cyclone III devices.

Device	Performance			Unit
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	
EP3C5	500	(2)	(2)	MHz
EP3C10	500	(2)	(2)	MHz
EP3C16	500	(2)	(2)	MHz
EP3C25	500	(2)	(2)	MHz
EP3C40	500	(2)	(2)	MHz
EP3C55	500	(2)	(2)	MHz
EP3C80	500	(2)	(2)	MHz
EP3C120	(1)	437.5	(2)	MHz

Notes to Table 1–18:

- (1) EP3C120 offered in –7 and –8 speed grades only.
- (2) Pending silicon characterization.

PLL Specifications

Table 1–19 describes the Cyclone III PLL specifications when operating in both the commercial junction temperature range (0°C to 85°C) and the industrial junction temperature range (–40°C to 100°C). For more information on PLL Block, refer to “PLL Block” in “Glossary”.

Symbol	Parameter	Min	Typ	Max	Unit
f_{iN} (1)	Input clock frequency (–6 speed grade)	5	—	472.5	MHz
	Input clock frequency (–7 speed grade)	5	—	472.5	MHz
	Input clock frequency (–8 speed grade)	5	—	472.5	MHz
f_{iNPFD}	PFD input frequency (–6 speed grade)	5	—	325	MHz
	PFD input frequency (–7 speed grade)	5	—	325	MHz
	PFD input frequency (–8 speed grade)	5	—	325	MHz

Symbol	Parameter	Min	Typ	Max	Unit
f_{VCO}	PLL internal VCO operating range	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER}$	Input clock period jitter	—	200	—	ps
f_{OUT_EXT} (external clock output) (1)	PLL output frequency (–6 speed grade)	5	—	472.5	MHz
	PLL output frequency (–7 speed grade)	5	—	472.5	MHz
	PLL output frequency (–8 speed grade)	5	—	472.5	MHz
f_{OUT} (to global clock)	PLL output frequency (–6 speed grade)	5	—	472.5	MHz
	PLL output frequency (–7 speed grade)	5	—	450	MHz
	PLL output frequency (–8 speed grade)	5	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	100 (2)	μ s
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
$t_{OUTJITTE\ R_DEDCLK}$	Dedicated clock output period jitter	—	—	300	ps
$t_{OUTJITTE\ R_IO}$	Regular I/O period jitter	—	—	(4)	ps
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	± 60	ps
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 (3)	—	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz

Notes to Table 1–19:

- (1) This parameter is limited in Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) For extended temperature devices, the maximum lock time is 500 μ s.
- (3) With 100 MHz scanclk frequency.
- (4) Pending silicon characterization.
- (5) V_{CCD_PLL} should always be connected to V_{CCINT} through decoupling capacitor and ferrite bead.

Embedded Multiplier Specifications

Table 1–20 describes the Cyclone III embedded multiplier specifications.

Mode	Resources Used	Performance			Unit
	Number of Multipliers	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	
9×9-bit multiplier	1	260	223	180	MHz
18×18-bit multiplier	1	260	223	180	MHz

Memory Block Specifications

Table 1–21 describes the Cyclone III M9K Memory block specifications.

Table 1–21. Cyclone III Memory Block Performance Specifications <i>Note (1)</i>					Preliminary
Memory	Mode	Resources Used		Performance	
		LEs	M9K Memory	–6 Speed Grade	Unit
M9K Block	FIFO 256×36	47	1	311	MHz
	Single-port 256×36	0	1	311	MHz
	Simple dual-port 256×36 CLK	0	1	311	MHz
	True dual port 512×18 single CLK	0	1	311	MHz

Note to Table 1–21:

(1) Values for device speed grade –7 and –8 will be available after characterization.

Configuration and JTAG Specifications

Table 1–22 lists the Cyclone III Configuration Mode Specifications.

Table 1–22. Cyclone III Configuration Mode Specifications			Preliminary
Programming Mode	DCLK F_{max}	Unit	
Passive Serial (PS)	133	MHz	
Fast Passive Parallel (FPP) <i>(1)</i>	100	MHz	

Note to Table 1–22:

(1) EP3C25 and smaller family members support 133 MHz.

Table 1–23 lists the Cyclone III Active Configuration Mode Specifications.

Table 1–23. Cyclone III Active Configuration Mode Specifications			Preliminary
Programming Mode	DCLK Range	Unit	
Active Parallel (AP)	20 – 40	MHz	
Active Serial (AS)	20 – 40	MHz	

Table 1–24 shows the JTAG timing parameters and values for Cyclone III. For more information, refer to “JTAG Waveform” in “Glossary”.

Table 1–24. Cyclone III JTAG Timing Parameters (Part 1 of 2)					Preliminary
Symbol	Parameter	Min	Max	Unit	
t_{JCP}	TCK clock period	40	—	ns	
t_{JCH}	TCK clock high time	20	—	ns	
t_{JCL}	TCK clock low time	20	—	ns	
t_{JPSU_TDI}	JTAG port setup time for TDI <i>(1)</i>	1	—	ns	
t_{JPSU_TMS}	JTAG port setup time for TMS <i>(1)</i>	3	—	ns	
t_{JPH}	JTAG port hold time	10	—	ns	
t_{JPCO}	JTAG port clock to output <i>(1)</i>	—	15	ns	

Symbol	Parameter	Min	Max	Unit
t_{JPZX}	JTAG port high impedance to valid output (1)	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance (1)	—	15	ns
t_{JSSU}	Capture register setup time (1)	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Note to Table 1–24:

(1) The specification is shown for 3.3 V, 3.0 V and 2.5 V LVTTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVCMOS, the JTAG port clock to output time is 16 ns.

Periphery Performance

High-Speed I/O Specification

Tables 1–25 through 1–30 show the high-speed I/O timing for Cyclone III devices. Refer to “Glossary” for definitions of high-speed timing specifications.

Symbol	Modes	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	x10	10	—	180	10	—	155.5	10	—	155.5	MHz
	x8	10	—	180	10	—	155.5	10	—	155.5	MHz
	x7	10	—	180	10	—	155.5	10	—	155.5	MHz
	x4	10	—	180	10	—	155.5	10	—	155.5	MHz
	x2	10	—	180	10	—	155.5	10	—	155.5	MHz
	x1	10	—	360	10	—	311	10	—	311	MHz
Device operation in Mbps	x10	100	—	360	100	—	311	100	—	311	Mbps
	x8	80	—	360	80	—	311	80	—	311	Mbps
	x7	70	—	360	70	—	311	70	—	311	Mbps
	x4	40	—	360	40	—	311	40	—	311	Mbps
	x2	20	—	360	20	—	311	20	—	311	Mbps
	x1	10	—	360	10	—	311	10	—	311	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500 (1)	—	—	500 (1)	—	—	500 (1)	ps
t_{RISE}	20 – 80%, $C_{LOAD} = 5$ pF	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, $C_{LOAD} = 5$ pF	—	500	—	—	500	—	—	500	—	ps

Table 1–25. RSDS Transmitter Timing Specification Notes (3), (4) (Part 2 of 2)

Symbol	Modes	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{LOCK}	—	—	—	(2)	—	—	(2)	—	—	(2)	ms

Notes to Table 1–25:

- (1) Preliminary, pending silicon characterization.
- (2) Pending silicon characterization.
- (3) Applicable for both dedicated and three-resistor RSDS transmitter.
- (4) Dedicated RSDS transmitter is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6). Three-resistor RSDS transmitter is supported at the output pin of all I/O banks.

Table 1–26. Single-Resistor RSDS Transmitter Timing Specification Note (3)

Symbol	Modes	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	x10	10	—	85	10	—	85	10	—	85	MHz
	x8	10	—	85	10	—	85	10	—	85	MHz
	x7	10	—	85	10	—	85	10	—	85	MHz
	x4	10	—	85	10	—	85	10	—	85	MHz
	x2	10	—	85	10	—	85	10	—	85	MHz
	x1	10	—	170	10	—	170	10	—	170	MHz
Device operation in Mbps	x10	100	—	170	100	—	170	100	—	170	Mbps
	x8	80	—	170	80	—	170	80	—	170	Mbps
	x7	70	—	170	70	—	170	70	—	170	Mbps
	x4	40	—	170	40	—	170	40	—	170	Mbps
	x2	20	—	170	20	—	170	20	—	170	Mbps
	x1	10	—	170	10	—	170	10	—	170	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500 (1)	—	—	500 (1)	—	—	550 (1)	ps
t_{RISE}	20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, $C_{\text{LOAD}} = 5 \text{ pF}$	—	500	—	—	500	—	—	500	—	ps
t_{LOCK}	—	—	—	(2)	—	—	(2)	—	—	(2)	ms

Notes to Table 1–26:

- (1) Preliminary, pending silicon characterization.
- (2) Pending silicon characterization.
- (3) Single-resistor RSDS transmitter is supported at the output pin of all I/O banks.

Symbol	Modes	–6 Speed Grade			–7 Speed Grade			–8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK} (input clock frequency)	×10	10	—	200	10	—	155.5	10	—	155.5	MHz
	×8	10	—	200	10	—	155.5	10	—	155.5	MHz
	×7	10	—	200	10	—	155.5	10	—	155.5	MHz
	×4	10	—	200	10	—	155.5	10	—	155.5	MHz
	×2	10	—	200	10	—	155.5	10	—	155.5	MHz
	×1	10	—	400	10	—	311	10	—	311	MHz
Device operation in Mbps	×10	100	—	400	100	—	311	100	—	311	Mbps
	×8	80	—	400	80	—	311	80	—	311	Mbps
	×7	70	—	400	70	—	311	70	—	311	Mbps
	×4	40	—	400	40	—	311	40	—	311	Mbps
	×2	20	—	400	20	—	311	20	—	311	Mbps
	×1	10	—	400	10	—	311	10	—	311	Mbps
t _{DUTY}	—	45	—	55	45	—	55	45	—	55	%
T _{CCS}	—	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500 (1)	—	—	500 (1)	—	—	550 (1)	ps
t _{RISE}	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{FALL}	20 – 80%, C _{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	ps
t _{LOCK}	—	—	—	(2)	—	—	(2)	—	—	(2)	ms

Notes to Table 1–27:

- (1) Preliminary, pending silicon characterization.
- (2) Pending silicon characterization.
- (3) Applicable for both dedicated and three-resistor mini-LVDS transmitter.
- (4) Dedicated mini-LVDS transmitter is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6). Three-resistor mini-LVDS transmitter is supported at the output pin of all I/O banks.

Symbol	Modes	–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
f _{HCLK} (input clock frequency)	×10	10	420	10	370	10	320	MHz
	×8	10	420	10	370	10	320	MHz
	×7	10	420	10	370	10	320	MHz
	×4	10	420	10	370	10	320	MHz
	×2	10	420	10	370	10	320	MHz
	×1	10	420	10	402.5	10	402.5	MHz

Symbol	Modes	–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
HSIODR	×10	100	840	100	740	100	640	Mbps
	×8	80	840	80	740	80	640	Mbps
	×7	70	840	70	740	70	640	Mbps
	×4	40	840	40	740	40	640	Mbps
	×2	20	840	20	740	20	640	Mbps
	×1	10	420	10	402.5	10	402.5	Mbps
t _{DUTY}	—	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500 (1)	—	500 (1)	—	550 (1)	ps
t _{LOCK}	—	—	(2)	—	(2)	—	(2)	ms

Notes to Table 1–28:

- (1) Preliminary, pending silicon characterization.
(2) Pending silicon characterization.
(3) Dedicated LVDS transmitter is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6).

Symbol	Modes	–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
f _{HCLK} (input clock frequency)	×10	10	320	10	320	10	275	MHz
	×8	10	320	10	320	10	275	MHz
	×7	10	320	10	320	10	275	MHz
	×4	10	320	10	320	10	275	MHz
	×2	10	320	10	320	10	275	MHz
	×1	10	402.5	10	402.5	10	402.5	MHz
HSIODR	×10	100	640	100	640	100	550	Mbps
	×8	80	640	80	640	80	550	Mbps
	×7	70	640	70	640	70	550	Mbps
	×4	40	640	40	640	40	550	Mbps
	×2	20	640	20	640	20	550	Mbps
	×1	10	402.5	10	402.5	10	402.5	Mbps
t _{DUTY}	—	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500 (1)	—	500 (1)	—	550 (1)	ps
t _{LOCK}	—	—	(2)	—	(2)	—	(2)	ms

Notes to Table 1–29:

- (1) Preliminary, pending silicon characterization.
(2) Pending silicon characterization.
(3) Three-Resistor LVDS transmitter is supported at output pin of all I/O banks.

Symbol	Modes	–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
f _{HSCLK} (input clock frequency)	x10	10	437.5	10	370	10	320	MHz
	x8	10	437.5	10	370	10	320	MHz
	x7	10	437.5	10	370	10	320	MHz
	x4	10	437.5	10	370	10	320	MHz
	x2	10	437.5	10	370	10	320	MHz
	x1	10	437.5	10	402.5	10	402.5	MHz
HSIODR	x10	100	875	100	740	100	640	Mbps
	x8	80	875	80	740	80	640	Mbps
	x7	70	875	70	740	70	640	Mbps
	x4	40	875	40	740	40	640	Mbps
	x2	20	875	20	740	20	640	Mbps
	x1	10	437.5	10	402.5	10	402.5	Mbps
SW	—	—	400	—	400	—	400	ps
Input jitter tolerance	—	—	500 (1)	—	500 (1)	—	550 (1)	ps
t _{LOCK}	—	—	(2)	—	(2)	—	(2)	ms

Notes to Table 1–30:

- (1) Preliminary, pending silicon characterization.
- (2) Pending silicon characterization.
- (3) Dedicated LVDS receiver is supported at all banks.

External Memory Interface Specifications

Cyclone III devices support external memory interfaces up to 200 MHz. Cyclone III external memory interfaces are auto-calibrating and easy to implement. Tables 1–31 through 1–35 list the External Memory Interface Specifications for the Cyclone III device family.

Use Tables 1–31 through 1–35 for memory interface timing analysis.

Memory Standard	I/O Standard	Commercial					
		–6 Speed Grade (MHz)		–7 Speed Grade (MHz)		–8 Speed Grade (MHz)	
		Column I/Os	Row I/Os	Column I/Os	Row I/Os	Column I/Os	Row I/Os
DDR2 SDRAM (2)	SSTL-18 Class I	200	167	167	150	167	133
	SSTL-18 Class II	133	125	125	(3)	(3)	(3)
DDR SDRAM (2)	SSTL-2 Class I	167	150	150	133	133	125
	SSTL-2 Class II	133	125	125	100	100	(3)
QDR II SRAM (4)	1.8-V HSTL Class I	167	150	150	133	133	125
	1.8-V HSTL Class II	125	125	100	100	100	100

Notes to Table 1–31:

- (1) These numbers are preliminary until characterization is final.
- (2) The values apply for interfaces with both modules and components.
- (3) Support will be evaluated after characterization.
- (4) QDR II SRAM also supports the 1.5-V HSTL I/O standard. However, Altera recommends using the 1.8-V HSTL I/O standard for maximum performance because of the higher I/O Current Strength.
- (5) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os.

Memory Standard	Commercial					
	–6 Speed Grade (MHz)		–7 Speed Grade (MHz)		–8 Speed Grade (MHz)	
	Column I/Os	Row I/Os	Column I/Os	Row I/Os	Column I/Os	Row I/Os
DDR2 SDRAM (2)	166	166	150	150	133	133
DDR SDRAM (2)	166	166	150	150	133	133

Notes to Table 1–32:

- (1) These numbers are preliminary until characterization is final.
- (2) The values apply for interfaces with both modules and components.
- (3) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os.

Memory Standards	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Unit
	Column I/Os		Row I/Os		Column I/Os		Row I/Os		Column I/Os		Row I/Os		
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	
DDR2 SDRAM	620	620	745	745	755	755	840	840	790	790	945	945	ps
DDR SDRAM	595	595	730	730	728	728	843	843	850	850	975	975	ps
QDR II SRAM	695	695	780	780	790	790	885	885	895	895	970	970	ps

Note to Table 1–33:

(1) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os.

Memory Standards	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Unit
	Column I/Os		Row I/Os		Column I/Os		Row I/Os		Column I/Os		Row I/Os		
	Lead	Lag	Lead	Lag	Lead	Lag	Lead	Lag	Lead	Lag	Lead	Lag	
DDR2 SDRAM	585	585	645	645	595	595	650	650	595	595	660	660	ps
DDR SDRAM	610	610	670	670	620	620	680	680	630	630	685	685	ps
QDR II SRAM	670	670	725	725	675	675	735	735	685	685	740	740	ps

Note to Table 1–34:

(1) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os.

Name	Description	Max	Unit
$t_{\text{OUTFULLJITTER}}$	Half-period jitter (PLL driving DDIO outputs)	(1)	ps

Note to Table 1–35:

(1) Pending silicon characterization.

DCD Specifications

Table 1–36 lists the worst case duty cycle distortion for Cyclone III devices. Detailed information on duty cycle distortion will be published after characterization.

Symbol	–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	40	60	%

Notes to Table 1–36:

- (1) Preliminary DCD specification applies to clock outputs from PLLs, global clock tree and IOE driving dedicated and general purpose I/O pins.
- (2) Detailed DCD specification pending silicon characterization.

I/O Timing

Timing Model

The DirectDrive™ technology and MultiTrack™ interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Cyclone III device densities and speed grades. This section describes and specifies the performance of I/Os and internal timing.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

 The timing numbers listed in the tables of this section are extracted from the Quartus II software version 7.2.

Preliminary, Correlated, and Final Timing

Timing models can have either preliminary, correlated, or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. [Table 1–37](#) shows the status of the Cyclone III device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Correlated numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Final timing numbers are based on complete correlation to actual devices and addressing any minor deviations from the correlated timing model. When the timing models are final, all or most of the Cyclone III family devices have been completely characterized and no further changes to the timing model are expected.

Table 1–37. Cyclone III Device Timing Model Status

Device	Preliminary	Correlated	Final
EP3C5	✓	—	—
EP3C10	✓	—	—
EP3C16	✓	—	—
EP3C25	✓	—	—
EP3C40	✓	—	—
EP3C55	✓	—	—
EP3C80	✓	—	—
EP3C120	✓	—	—

I/O Timing Measurement Methodology

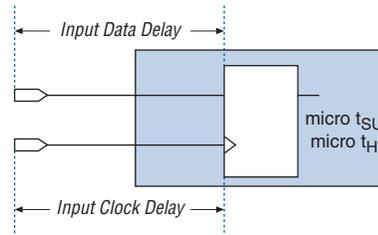
Altera characterizes timing delays at the worst-case process, minimum voltage, and maximum temperature for input register setup time (t_{SU}) and hold time (t_H). The Quartus II software uses the following equations to calculate t_{SU} and t_H timing for Cyclone III devices input signals:

$$t_{SU} = + \text{data delay from input pin to input register} \\ + \text{micro setup time of the input register} \\ - \text{clock delay from input pin to input register}$$

$$t_H = - \text{data delay from input pin to input register} \\ + \text{micro hold time of the input register} \\ + \text{clock delay from input pin to input register}$$

Figure 1–2 shows the setup and hold timing diagram for input registers.

Figure 1–2. Input Register Setup and Hold Timing Diagram



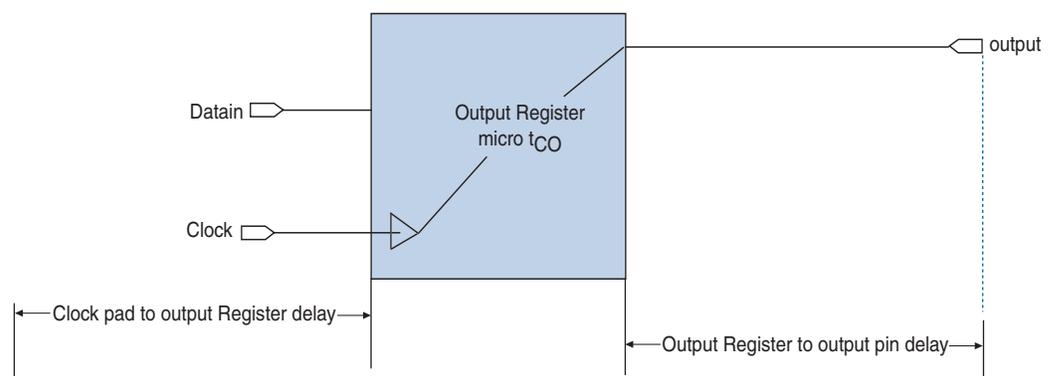
For output timing, different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 1–38. Use the following equations to calculate clock pin to output pin timing for Cyclone III devices.

t_{CO} from clock pin to I/O pin =

- + delay from clock pad to I/O output register
- + IOE output register clock-to-output delay
- + delay from output register to output pin

Figure 1–3. Output Register Clock to Output Timing Diagram



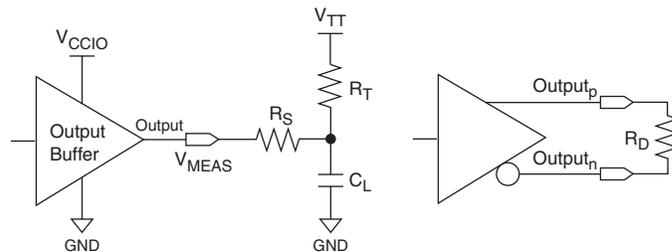
Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 1–38.
2. Record the time to V_{MEAS} .

3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions shown in Table 1–38 using the above equation. Figure 1–4 shows the model of the circuit that is represented by the output timing of the Quartus II software.

Figure 1–4. Output Delay Timing Reporting Setup Modeled by Quartus II Software Notes (1), (2)



Notes to Figure 1–4:

- (1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay must be accounted for with IBIS model simulations.
- (2) V_{CCINT} is 1.10 V unless otherwise specified.

Figure 1–5 and Figure 1–6 show the I/O interface with single and multiple external output resistors.

Figure 1–5. I/O Interface with Single External Output Resistor

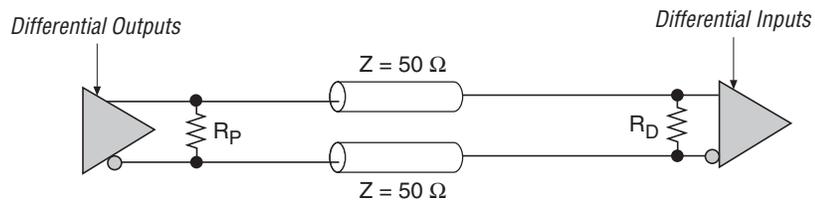
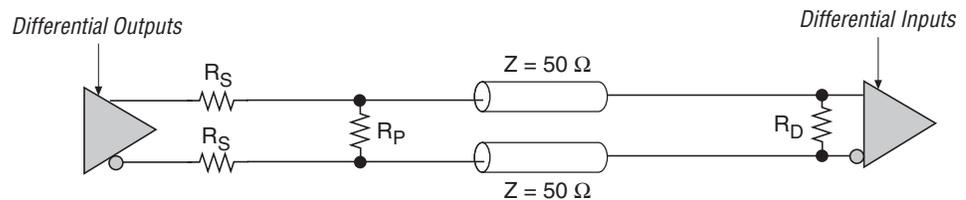


Figure 1–6. I/O Interface with Three External Output Resistor Network



I/O Standard	Loading and Termination							Measurement Point
	R_S (Ω)	R_T (Ω)	R_D (Ω)	R_P (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
3.3-V LVTTTL	—	—	—	—	3.085	—	0	1.5425
3.3-V LVCMOS	—	—	—	—	3.085	—	0	1.5425
3.0-V LVTTTL	—	—	—	—	2.80	—	0	1.40
3.0-V LVCMOS	—	—	—	—	2.80	—	0	1.40
2.5-V LVTTTL/LVCMOS	—	—	—	—	2.325	—	0	1.1625
1.8-V LVTTTL/LVCMOS	—	—	—	—	1.66	—	0	0.83
1.5-V LVCMOS	—	—	—	—	1.375	—	0	0.6875
1.2-V LVCMOS	—	—	—	—	1.10	—	0	0.55
3.0-V PCI	—	—	—	—	2.80	—	10	1.40
3.0-V PCI-X	—	—	—	—	2.80	—	10	1.40
SSTL-2 Class I	25	50	—	—	2.325	1.1625	0	1.1625
SSTL-2 Class II	25	25	—	—	2.325	1.1625	0	1.1625
SSTL-18 Class I	25	50	—	—	1.66	0.83	0	0.83
SSTL-18 Class II	25	25	—	—	1.66	0.83	0	0.83
1.8-V HSTL Class I	50	50	—	—	1.66	0.83	0	0.83
1.8-V HSTL Class II	25	25	—	—	1.66	0.83	0	0.83
1.5-V HSTL Class I	50	50	—	—	1.375	0.6875	0	0.6875
1.5-V HSTL Class II	—	25	—	—	1.375	0.6875	0	0.6875
1.2-V HSTL Class I	—	50	—	—	1.10	0.55	0	0.55
1.2-V HSTL Class II	—	25 (50 50)	—	—	1.10	0.55	0	0.55
LVDS	—	—	100	—	2.325	—	0	1.1625
LVDS_E_3R	120 (6)	—	100	170 (6)	2.325	—	0	1.1625
mini-LVDS	—	—	100	—	2.325	—	0	1.1625
mini-LVDS_E_3R	120 (6)	—	100	170 (6)	2.325	—	0	1.1625
PPDS	—	—	100	—	2.325	—	0	1.1625
PPDS_E_3R	120 (6)	—	100	170 (6)	2.325	—	0	1.1625
RSDS	—	—	100	—	2.325	—	0	1.1625
RSDS_E_1R	—	—	100	100 (6)	2.325	—	0	1.1625
RSDS_E_3R	120 (6)	—	100	170 (6)	2.325	—	0	1.1625

Notes to Table 1–38:

- (1) Input measurement point at internal node is $0.5 \times V_{CCINT}$.
- (2) Output measuring point for V_{MEAS} at buffer output is $0.5 \times V_{CCIO}$.
- (3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.
- (4) Less than 50-mV ripple on V_{CCIO} . $V_{CCINT} = 1.10$ V with less than 30-mV ripple.
- (5) The interface has to use external termination R_T . The termination voltage V_{TT} may either be supplied by an independent power supply or created through a Thevenin equivalent circuit.
- (6) Pending silicon characterization.

I/O Default Capacitive Loading

Refer to [Table 1–39](#) for default capacitive loading of different I/O standards.

<i>Table 1–39. Default Loading of Different I/O Standards for Cyclone III Devices</i>		Preliminary
I/O Standard	Capacitive Load	Unit
3.3-V LVTTTL	0	pF
3.3-V LVCMOS	0	pF
3.0-V LVTTTL	0	pF
3.0-V LVCMOS	0	pF
2.5-V LVTTTL/LVCMOS	0	pF
1.8-V LVTTTL/LVCMOS	0	pF
1.5-V LVCMOS	0	pF
1.2-V LVCMOS	0	pF
3.0-V PCI	10	pF
3.0-V PCI-X	10	pF
SSTL-2 Class I	0	pF
SSTL-2 Class II	0	pF
SSTL-18 Class I	0	pF
SSTL-18 Class II	0	pF
1.8-V HSTL Class I	0	pF
1.8-V HSTL Class II	0	pF
1.5-V HSTL Class I	0	pF
1.5-V HSTL Class II	0	pF
1.2-V HSTL Class I	0	pF
1.2-V HSTL Class II	0	pF
Differential SSTL-2 Class I	0	pF
Differential SSTL-2 Class II	0	pF
Differential SSTL-18 Class I	0	pF
Differential SSTL-18 Class II	0	pF
1.2-V Differential HSTL Class I	0	pF
1.2-V Differential HSTL Class II	0	pF
1.5-V Differential HSTL Class I	0	pF
1.5-V Differential HSTL Class II	0	pF
1.8-V Differential HSTL Class I	0	pF
1.8-V Differential HSTL Class II	0	pF
LVDS	0	pF
LVDS_E_3R	0	pF
mini-LVDS	0	pF
mini-LVDS_E_3R	0	pF
PPDS	0	pF
PPDS_E_3R	0	pF
RSDS	0	pF
RSDS_E_1R	0	pF
RSDS_E_3R	0	pF

Maximum Input and Output Clock Toggle Rate

The maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Table 1–40 specifies the maximum input clock toggle rates. Table 1–41 specifies the maximum output clock toggle rates at 0 pF load. Table 1–42 specifies the derating factors for the output clock toggle rate for a non 0 pF load.

To calculate the output toggle rate for a non 0 pF load, use this formula:

The toggle rate for a non 0 pF load

$$= 1000 / (1000 / \text{toggle rate at 0 pF load} + \text{derating factor} * \text{load value in pF} / 1000)$$

For example, the output toggle rate at 0 pF load for SSTL-18 Class II 16 μ A I/O standard is 260 MHz on a –6 device clock output pin. The derating factor is 26 ps/pF. For a 10 pF load the toggle rate is calculated as:

$$1000 / (1000/260 + 26 \times 10 / 1000) = 243 \text{ (MHz)}$$

Tables 1–40 through 1–42 show the I/O toggle rates for Cyclone III devices.

Table 1–40. Maximum Input Toggle Rate on Cyclone III Devices (Part 1 of 2)									Preliminary
I/O Standard	Maximum Input Toggle Rate on CIII Devices (MHz)								
	Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.3-V LVTTTL	250	237	225	250	237	225	250	237	225
3.3-V LVCMOS	250	237	225	250	237	225	250	237	225
3.0-V LVTTTL	250	237	225	250	237	225	250	237	225
3.0-V LVCMOS	250	237	225	250	237	225	250	237	225
2.5V	250	237	225	250	237	225	250	237	225
1.8V	250	237	225	250	237	225	250	237	225
1.5V	250	237	225	250	237	225	250	237	225
1.2V	200	190	180	200	190	180	200	190	180
SSTL-2 Class I	250	237	225	250	237	225	250	237	225
SSTL-2 Class II	250	237	225	250	237	225	250	237	225
SSTL-18 Class I	300	285	270	300	285	270	300	285	270
SSTL-18 Class II	300	285	270	300	285	270	300	285	270
1.8-V HSTL Class I	300	285	270	300	285	270	300	285	270
1.8-V HSTL Class II	300	285	270	300	285	270	300	285	270
1.5-V HSTL Class I	300	285	270	300	285	270	300	285	270
1.5-V HSTL Class II	300	285	270	300	285	270	300	285	270
1.2-V HSTL Class I	200	190	180	200	190	180	200	190	180
1.2-V HSTL Class II	200	190	180	(1)	(1)	(1)	200	190	180
3.0-V PCI	250	237	225	250	237	225	250	237	225

I/O Standard	Maximum Input Toggle Rate on CIII Devices (MHz)								
	Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.0-V PCI-X	250	237	225	250	237	225	250	237	225
DIFFERENTIAL 2.5-V SSTL Class I	(2)	(2)	(2)	(2)	(2)	(2)	250	237	225
DIFFERENTIAL 2.5-V SSTL Class II	(2)	(2)	(2)	(2)	(2)	(2)	250	237	225
DIFFERENTIAL 1.8-V SSTL Class I	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
DIFFERENTIAL 1.8-V SSTL Class II	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
DIFFERENTIAL 1.8-V HSTL Class I	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
DIFFERENTIAL 1.8-V HSTL Class II	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
DIFFERENTIAL 1.5-V HSTL Class I	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
DIFFERENTIAL 1.5-V HSTL Class II	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
DIFFERENTIAL 1.2-V HSTL Class I	(2)	(2)	(2)	(2)	(2)	(2)	200	190	180
DIFFERENTIAL 1.2-V HSTL Class II	(2)	(2)	(2)	(2)	(2)	(2)	200	190	180
LVPECL	(3)	(3)	(3)	(3)	(3)	(3)	437.5	370	320
LVDS	437.5	370	320	437.5	370	320	437.5	370	320

Notes to Table 1–40:

- (1) The 1.2 V_HSTL_CLASS_II is only supported on column I/O pins.
- (2) Input differential standard is only supported on GCLK pin.
- (3) Input LVPECL is only supported on GCLK pin.

I/O Standard	Maximum Output Toggle Rate on CIII Devices (MHz)									
	Current Strength (mA) or OCT Setting	Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.3-V LVTTTL	4	250	237	225	250	237	225	250	237	225
	8	250	237	225	250	237	225	250	237	225
3.3-V LVCMOS	2	250	237	225	250	237	225	250	237	225
3.0-V LVTTTL	4	250	237	225	250	237	225	250	237	225
	8	250	237	225	250	237	225	250	237	225
	12	250	237	225	250	237	225	250	237	225
	16	250	237	225	250	237	225	250	237	225
3.0-V LVCMOS	4	250	237	225	250	237	225	250	237	225
	8	250	237	225	250	237	225	250	237	225
	12	250	237	225	250	237	225	250	237	225
	16	250	237	225	250	237	225	250	237	225

Table 1–41. Maximum Output Toggle Rate on Cyclone III Devices (Part 2 of 4)										Preliminary
I/O Standard	Maximum Output Toggle Rate on CIII Devices (MHz)									
	Current Strength (mA) or OCT Setting	Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
2.5V	4	250	237	225	250	237	225	250	237	225
	8	250	237	225	250	237	225	250	237	225
	12	250	237	225	250	237	225	250	237	225
	16	250	237	225	250	237	225	250	237	225
1.8V	2	250	237	225	250	237	225	250	237	225
	4	250	237	225	250	237	225	250	237	225
	6	250	237	225	250	237	225	250	237	225
	8	250	237	225	250	237	225	250	237	225
	10	250	237	225	250	237	225	250	237	225
	12	250	237	225	250	237	225	250	237	225
	16	250	237	225	250	237	225	250	237	225
1.5V	2	250	237	225	250	237	225	250	237	225
	4	250	237	225	250	237	225	250	237	225
	6	250	237	225	250	237	225	250	237	225
	8	250	237	225	250	237	225	250	237	225
	10	250	237	225	250	237	225	250	237	225
	12	250	237	225	250	237	225	250	237	225
	16	250	237	225	250	237	225	250	237	225
1.2V	2	250	237	225	250	237	225	250	237	225
	4	250	237	225	250	237	225	250	237	225
	6	250	237	225	250	237	225	250	237	225
	8	250	237	225	250	237	225	250	237	225
	10	250	237	225	250	237	225	250	237	225
	12	250	237	225	(1)	(1)	(1)	250	237	225
SSTL-2 Class I	8	250	237	225	250	237	225	250	237	225
	12	250	237	225	250	237	225	250	237	225
SSTL-2 Class II	16	250	237	225	250	237	225	250	237	225
SSTL-18 Class I	8	300	285	270	300	285	270	300	285	270
	10	300	285	270	300	285	270	300	285	270
	12	300	285	270	300	285	270	300	285	270
SSTL-18 Class II	12	300	285	270	300	285	270	300	285	270
	16	300	285	270	300	285	270	300	285	270
1.8-V HSTL Class I	8	300	285	270	300	285	270	300	285	270
	10	300	285	270	300	285	270	300	285	270
	12	300	285	270	300	285	270	300	285	270
1.8-V HSTL Class II	16	300	285	270	300	285	270	300	285	270
1.5-V HSTL Class I	8	300	285	270	300	285	270	300	285	270
	10	300	285	270	300	285	270	300	285	270
	12	300	285	270	300	285	270	300	285	270
1.5-V HSTL Class II	16	300	285	270	300	285	270	300	285	270

Table 1–41. Maximum Output Toggle Rate on Cyclone III Devices (Part 3 of 4)

I/O Standard	Maximum Output Toggle Rate on CIII Devices (MHz)									
	Current Strength (mA) or OCT Setting	Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
1.2-V HSTL Class I	8	250	237	225	250	237	225	250	237	225
	10	250	237	225	250	237	225	250	237	225
	12	250	237	225	(1)	(1)	(1)	250	237	225
1.2-V HSTL Class II	14	250	237	225	(1)	(1)	(1)	250	237	225
3.0-V PCI	—	250	237	225	250	237	225	250	237	225
3.0-V PCI-X	—	250	237	225	250	237	225	250	237	225
DIFFERENTIAL 2.5-V SSTL Class I	8	(2)	(2)	(2)	(2)	(2)	(2)	250	237	225
	12	(2)	(2)	(2)	(2)	(2)	(2)	250	237	225
DIFFERENTIAL 2.5-V SSTL Class II	16	(2)	(2)	(2)	(2)	(2)	(2)	250	237	225
DIFFERENTIAL 1.8-V SSTL Class I	8	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
	10	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
	12	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
DIFFERENTIAL 1.8-V HSTL Class I	8	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
	10	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
	12	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
DIFFERENTIAL 1.5-V HSTL Class I	8	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
	10	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
	12	(2)	(2)	(2)	(2)	(2)	(2)	300	285	270
DIFFERENTIAL 1.2-V HSTL Class I	8	(2)	(2)	(2)	(2)	(2)	(2)	250	237	225
	10	(2)	(2)	(2)	(2)	(2)	(2)	250	237	225
	12	(2)	(2)	(2)	(2)	(2)	(2)	250	237	225
LVDS	—	(4)	(4)	(4)	420	370	320	(4)	(4)	(4)
LVDS_E_3R	—	320	320	275	320	320	275	320	320	275
mini-LVDS	—	(3)	(3)	(3)	200	155.5	155.5	(4)	(4)	(4)
mini-LVDS_E_3R	—	200	155.5	155.5	200	155.5	155.5	200	155.5	155.5
PPDS	—	(3)	(3)	(3)	220	155.5	155.5	(4)	(4)	(4)
PPDS_E_3R	—	220	155.5	155.5	220	155.5	155.5	220	155.5	155.5
RSDS	—	(3)	(3)	(3)	180	155.5	155.5	(4)	(4)	(4)
RSDS_E_1R	—	85	85	85	85	85	85	85	85	85
RSDS_E_3R	—	180	155.5	155.5	180	155.5	155.5	180	155.5	155.5
3.0-V LVTTTL	OCT 25 OHM	250	237	225	250	237	225	250	237	225
	OCT 50 OHM	250	237	225	250	237	225	250	237	225
2.5V	OCT 25 OHM	250	237	225	250	237	225	250	237	225
	OCT 50 OHM	250	237	225	250	237	225	250	237	225

I/O Standard	Maximum Output Toggle Rate on CIII Devices (MHz)									
	Current Strength (mA) or OCT Setting	Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
1.8V	OCT 25 OHM	250	237	225	250	237	225	250	237	225
	OCT 50 OHM	250	237	225	250	237	225	250	237	225
1.5V	OCT 25 OHM	250	237	225	250	237	225	250	237	225
	OCT 50 OHM	250	237	225	250	237	225	250	237	225
1.2V	OCT 25 OHM	250	237	225	(5)	(5)	(5)	250	237	225
	OCT 50 OHM	250	237	225	250	237	225	250	237	225

Notes to Table 1–41:

- (1) The 1.2 V (12 mA) and 1.2 V_HSTL_CLASS_I / II (12 mA and 14 mA respectively) are only supported on column I/O pins.
- (2) Output differential standard is only supported on PLLCLKOUT pin.
- (3) Dedicated differential standards are supported at row I/O pins.
- (4) Output dedicated LVDS is only supported on row I/O pins. Input dedicated LVDS is supported at all I/O pins.
- (5) The 1.2-V output standard with 25-Ω output termination is only supported at column and PLLCLKOUT pin.

I/O Standard	Current Strength (mA) or OCT Setting	Maximum Output Clock Toggle Rate Derating Factors (ps/pf)					
		Column I/O Pins			Row I/O Pins		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.3-V LVTTTL	4	438	438	438	337	337	337
	8	305	305	305	267	267	267
3.3-V LVCMOS	2	298	298	298	300	300	300
3.0-V LVTTTL	4	438	438	438	438	438	438
	8	305	305	305	305	305	305
	12	138	138	138	138	138	138
	16	145	145	145	145	145	145
3.0-V LVCMOS	4	298	298	298	298	298	298
	8	189	189	189	189	189	189
	12	42	42	42	42	42	42
	16	87	87	87	87	87	87

Table 1–42. Maximum Output Toggle Rate Derating Factors on Cyclone III Devices (Part 2 of 3)		Preliminary					
I/O Standard	Current Strength (mA) or OCT Setting	Maximum Output Clock Toggle Rate Derating Factors (ps/pf)					
		Column I/O Pins			Row I/O Pins		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
2.5V	4	228	228	228	269	269	269
	8	173	173	173	190	190	190
	12	118	118	118	118	118	118
	16	64	64	64	64	64	64
1.8V	2	452	452	452	331	331	331
	4	320	320	320	244	244	244
	6	227	227	227	178	178	178
	8	37	37	37	58	58	58
	10	41	41	41	46	46	46
	12	6	6	6	12	12	12
	16	6	6	6	12	12	12
1.5V	2	738	738	738	539	539	539
	4	499	499	499	299	299	299
	6	260	260	260	59	59	59
	8	21	21	21	21	21	21
	10	21	21	21	21	21	21
	12	21	21	21	21	21	21
	16	21	21	21	21	21	21
1.2V	2	738	738	738	539	539	539
	4	499	499	499	299	299	299
	6	260	260	260	59	59	59
	8	21	21	21	21	21	21
	10	21	21	21	21	21	21
	12	21	21	21	(1)	(1)	(1)
SSTL-2 Class I	8	46	46	46	24	24	24
	12	66	66	66	23	23	23
SSTL-2 Class II	16	41	41	41	15	15	15
SSTL-18 Class I	8	19	19	19	46	46	46
	10	19	19	19	23	23	23
	12	19	19	19	19	19	19
SSTL-18 Class II	12	30	30	30	30	30	30
	16	30	30	30	30	30	30
1.8-V HSTL Class I	8	26	26	26	59	59	59
	10	46	46	46	64	64	64
	12	66	66	66	70	70	70
1.8-V HSTL Class II	16	62	62	62	62	62	62

I/O Standard	Current Strength (mA) or OCT Setting	Maximum Output Clock Toggle Rate Derating Factors (ps/pf)					
		Column I/O Pins			Row I/O Pins		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
1.5-V HSTL Class I	8	39	39	39	27	27	27
	10	41	41	41	41	41	41
	12	42	42	42	42	42	42
1.5-V HSTL Class II	16	18	18	18	18	18	18
1.2-V HSTL Class I	8	39	39	39	27	27	27
	10	41	41	41	41	41	41
	12	42	42	42	(1)	(1)	(1)
1.2-V HSTL Class II	14	18	18	18	(1)	(1)	(1)
3.0-V PCI	—	98	98	98	98	98	98
3.0-V PCI-X	—	98	98	98	98	98	98
LVDS	—	(3)	(3)	(3)	10	10	10
LVDS_E_3R	—	11	11	11	11	11	11
mini-LVDS	—	(2)	(2)	(2)	10	10	10
mini-LVDS_E_3R	—	11	11	11	11	11	11
PPDS	—	(2)	(2)	(2)	10	10	10
PPDS_E_3R	—	11	11	11	11	11	11
RSDS	—	(2)	(2)	(2)	10	10	10
RSDS_E_1R	—	11	11	11	11	11	11
RSDS_E_3R	—	11	11	11	11	11	11
3.0-V LVTTTL	OCT 25 OHM	305	305	305	305	305	305
	OCT 50 OHM	305	305	305	305	305	305
2.5V	OCT 25 OHM	173	173	173	190	190	190
	OCT 50 OHM	173	173	173	190	190	190
1.8V	OCT 25 OHM	37	37	37	58	58	58
	OCT 50 OHM	37	37	37	58	58	58
1.5V	OCT 25 OHM	21	21	21	21	21	21
	OCT 50 OHM	21	21	21	21	21	21
1.2V	OCT 25 OHM	21	21	21	(4)	(4)	(4)
	OCT 50 OHM	21	21	21	21	21	21

Notes to Table 1–42:

- (1) The 1.2 V (12 mA) and 1.2 V_HSTL_CLASS_I /II (12 mA and 14 mA, respectively) are only supported on column I/O pins.
- (2) Dedicated differential standards are supported at row I/O pins.
- (3) Output dedicated LVDS is only supported on row I/O pins. Input dedicated LVDS is supported at all I/O pins.
- (4) The 1.2-V output standard with 25-Ω output termination is only supported at column and PLLCLKOUT pin.

IOE Programmable Delay

Tables 1–43 and 1–44 show IOE programmable delay for Cyclone III devices.

Table 1–43. Cyclone III IOE Programmable Delay on Column Pins Notes (1), (2)

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.313	0	2.141	0	2.282	0	2.409	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.467	0	2.355	0	2.473	0	2.59	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.559	0	0.96	0	1.054	0	1.151	ns

Notes to Table 1–43:

- (1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting “0” as available in the Quartus II software.
- (3) The fast model timing parameter is for commercial devices.

Table 1–44. Cyclone III IOE Programmable Delay on Row Pins Notes (1), (2)

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.312	0	2.13	0	2.271	0	2.373	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.476	0	2.367	0	2.487	0	2.609	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.595	0	1.022	0	1.124	0	1.226	ns

Notes to Table 1–44:

- (1) The incremental values for the settings are generally linear. For exact values of each setting use the latest version of the Quartus II software.
- (2) The minimum and maximum offset timing numbers are in reference to setting “0” as available in the Quartus II software.
- (3) The fast model timing parameter is for commercial devices.

Typical Design Performance

User I/O Pin Timing Parameters

Tables 1–45 through 1–92 show user I/O pin timing for Cyclone III devices. I/O buffer t_{SU} , t_H and t_{CO} are reported for the cases when clock is driven by global clock and a PLL.

The 12 mA programmable current strength for 1.2 V and 1.2-V HSTL Class I I/O standard is not supported at row I/Os. The 1.2-V HSTL Class II standard is only supported at column I/Os. PCI and PCI-X do not support programmable current strength.



For more information about programmable current strength, refer to the *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*.

Dedicated LVDS, mini-LVDS, PPDS, and RSDS I/O standards are supported at row I/Os. External resistor networks are required if the differential standards are used as output pins at column banks. LVDS I/O standard is supported at both input and output pins. PPDS, RSDS, and mini-LVDS standards are only supported at output pins.



For more information about the differential I/O interface, refer to the *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*.

EP3C5 I/O Timing Parameters

Tables 1–45 through 1–50 show the maximum I/O timing parameters for EP3C5 devices.

Table 1–45. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

I/O Standard	Drive Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	1.171	1.206	1.220	ns
			t_H	–0.901	–0.901	–0.879	ns
		GCLK PLL	t_{SU}	3.191	3.412	3.612	ns
			t_H	–2.921	–3.107	–3.271	ns
	8 mA	GCLK	t_{SU}	1.171	1.206	1.220	ns
			t_H	–0.901	–0.901	–0.879	ns
		GCLK PLL	t_{SU}	3.191	3.412	3.612	ns
			t_H	–2.921	–3.107	–3.271	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.171	1.206	1.220	ns
			t_H	–0.901	–0.901	–0.879	ns
		GCLK PLL	t_{SU}	3.191	3.412	3.612	ns
			t_H	–2.921	–3.107	–3.271	ns
3.0-V LVTTTL	4 mA	GCLK	t_{SU}	1.171	1.206	1.220	ns
			t_H	–0.901	–0.901	–0.879	ns
		GCLK PLL	t_{SU}	3.191	3.412	3.612	ns
			t_H	–2.921	–3.107	–3.271	ns
	8 mA	GCLK	t_{SU}	1.171	1.206	1.220	ns
			t_H	–0.901	–0.901	–0.879	ns
		GCLK PLL	t_{SU}	3.191	3.412	3.612	ns
			t_H	–2.921	–3.107	–3.271	ns
	12 mA	GCLK	t_{SU}	1.171	1.206	1.220	ns
			t_H	–0.901	–0.901	–0.879	ns
		GCLK PLL	t_{SU}	3.191	3.412	3.612	ns
			t_H	–2.921	–3.107	–3.271	ns
	16 mA	GCLK	t_{SU}	1.171	1.206	1.220	ns
			t_H	–0.901	–0.901	–0.879	ns
		GCLK PLL	t_{SU}	3.191	3.412	3.612	ns
			t_H	–2.921	–3.107	–3.271	ns

Table 1–45. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Drive Strength	Clock	Parameter	–6	–7	–8	Unit		
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.171	1.206	1.220	ns		
			t_H	–0.901	–0.901	–0.879	ns		
		GCLK PLL	t_{SU}	3.191	3.412	3.612	ns		
			t_H	–2.921	–3.107	–3.271	ns		
		8 mA	GCLK	t_{SU}	1.171	1.206	1.220	ns	
				t_H	–0.901	–0.901	–0.879	ns	
	GCLK PLL		t_{SU}	3.191	3.412	3.612	ns		
			t_H	–2.921	–3.107	–3.271	ns		
	12 mA	GCLK	t_{SU}	1.171	1.206	1.220	ns		
			t_H	–0.901	–0.901	–0.879	ns		
		GCLK PLL	t_{SU}	3.191	3.412	3.612	ns		
			t_H	–2.921	–3.107	–3.271	ns		
	16 mA	GCLK	t_{SU}	1.171	1.206	1.220	ns		
			t_H	–0.901	–0.901	–0.879	ns		
		GCLK PLL	t_{SU}	3.191	3.412	3.612	ns		
			t_H	–2.921	–3.107	–3.271	ns		
	2.5V	4 mA	GCLK	t_{SU}	1.114	1.161	1.188	ns	
				t_H	–0.844	–0.857	–0.848	ns	
			GCLK PLL	t_{SU}	3.134	3.367	3.580	ns	
				t_H	–2.864	–3.063	–3.240	ns	
			8 mA	GCLK	t_{SU}	1.114	1.161	1.188	ns
					t_H	–0.844	–0.857	–0.848	ns
		GCLK PLL		t_{SU}	3.134	3.367	3.580	ns	
				t_H	–2.864	–3.063	–3.240	ns	
12 mA		GCLK	t_{SU}	1.114	1.161	1.188	ns		
			t_H	–0.844	–0.857	–0.848	ns		
		GCLK PLL	t_{SU}	3.134	3.367	3.580	ns		
			t_H	–2.864	–3.063	–3.240	ns		
16 mA		GCLK	t_{SU}	1.114	1.161	1.188	ns		
			t_H	–0.844	–0.857	–0.848	ns		
		GCLK PLL	t_{SU}	3.134	3.367	3.580	ns		
			t_H	–2.864	–3.063	–3.240	ns		

Table 1–45. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Drive Strength	Clock	Parameter	–6	–7	–8	Unit
1.8V	2 mA	GCLK	t_{SU}	1.049	1.122	1.175	ns
			t_H	–0.781	–0.819	–0.834	ns
		GCLK PLL	t_{SU}	3.069	3.328	3.567	ns
			t_H	–2.801	–3.025	–3.226	ns
	4 mA	GCLK	t_{SU}	1.049	1.122	1.175	ns
			t_H	–0.781	–0.819	–0.834	ns
		GCLK PLL	t_{SU}	3.069	3.328	3.567	ns
			t_H	–2.801	–3.025	–3.226	ns
	6 mA	GCLK	t_{SU}	1.049	1.122	1.175	ns
			t_H	–0.781	–0.819	–0.834	ns
		GCLK PLL	t_{SU}	3.069	3.328	3.567	ns
			t_H	–2.801	–3.025	–3.226	ns
	8 mA	GCLK	t_{SU}	1.049	1.122	1.175	ns
			t_H	–0.781	–0.819	–0.834	ns
		GCLK PLL	t_{SU}	3.069	3.328	3.567	ns
			t_H	–2.801	–3.025	–3.226	ns
	10 mA	GCLK	t_{SU}	1.049	1.122	1.175	ns
			t_H	–0.781	–0.819	–0.834	ns
		GCLK PLL	t_{SU}	3.069	3.328	3.567	ns
			t_H	–2.801	–3.025	–3.226	ns
	12 mA	GCLK	t_{SU}	1.049	1.122	1.175	ns
			t_H	–0.781	–0.819	–0.834	ns
		GCLK PLL	t_{SU}	3.069	3.328	3.567	ns
			t_H	–2.801	–3.025	–3.226	ns
	16 mA	GCLK	t_{SU}	1.049	1.122	1.175	ns
			t_H	–0.781	–0.819	–0.834	ns
		GCLK PLL	t_{SU}	3.069	3.328	3.567	ns
			t_H	–2.801	–3.025	–3.226	ns

Table 1–45. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Drive Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	1.118	1.214	1.292	ns
			t_H	–0.848	–0.909	–0.949	ns
		GCLK PLL	t_{SU}	3.138	3.420	3.684	ns
			t_H	–2.868	–3.115	–3.341	ns
	4 mA	GCLK	t_{SU}	1.118	1.214	1.292	ns
			t_H	–0.848	–0.909	–0.949	ns
		GCLK PLL	t_{SU}	3.138	3.420	3.684	ns
			t_H	–2.868	–3.115	–3.341	ns
	6 mA	GCLK	t_{SU}	1.118	1.214	1.292	ns
			t_H	–0.848	–0.909	–0.949	ns
		GCLK PLL	t_{SU}	3.138	3.420	3.684	ns
			t_H	–2.868	–3.115	–3.341	ns
	8 mA	GCLK	t_{SU}	1.118	1.214	1.292	ns
			t_H	–0.848	–0.909	–0.949	ns
		GCLK PLL	t_{SU}	3.138	3.420	3.684	ns
			t_H	–2.868	–3.115	–3.341	ns
	10 mA	GCLK	t_{SU}	1.118	1.214	1.292	ns
			t_H	–0.848	–0.909	–0.949	ns
		GCLK PLL	t_{SU}	3.138	3.420	3.684	ns
			t_H	–2.868	–3.115	–3.341	ns
	12 mA	GCLK	t_{SU}	1.118	1.214	1.292	ns
			t_H	–0.848	–0.909	–0.949	ns
		GCLK PLL	t_{SU}	3.138	3.420	3.684	ns
			t_H	–2.868	–3.115	–3.341	ns
	16 mA	GCLK	t_{SU}	1.118	1.214	1.292	ns
			t_H	–0.848	–0.909	–0.949	ns
		GCLK PLL	t_{SU}	3.138	3.420	3.684	ns
			t_H	–2.868	–3.115	–3.341	ns

Table 1–45. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Drive Strength	Clock	Parameter	–6	–7	–8	Unit	
1.2V	2 mA	GCLK	t_{SU}	1.270	1.394	1.498	ns	
			t_H	–0.998	–1.085	–1.151	ns	
		GCLK PLL	t_{SU}	3.290	3.600	3.890	ns	
			t_H	–3.018	–3.291	–3.543	ns	
		4 mA	GCLK	t_{SU}	1.270	1.394	1.498	ns
				t_H	–0.998	–1.085	–1.151	ns
	GCLK PLL		t_{SU}	3.290	3.600	3.890	ns	
			t_H	–3.018	–3.291	–3.543	ns	
	6 mA	GCLK	t_{SU}	1.270	1.394	1.498	ns	
			t_H	–0.998	–1.085	–1.151	ns	
		GCLK PLL	t_{SU}	3.290	3.600	3.890	ns	
			t_H	–3.018	–3.291	–3.543	ns	
	8 mA	GCLK	t_{SU}	1.270	1.394	1.498	ns	
			t_H	–0.998	–1.085	–1.151	ns	
		GCLK PLL	t_{SU}	3.290	3.600	3.890	ns	
			t_H	–3.018	–3.291	–3.543	ns	
	10 mA	GCLK	t_{SU}	1.270	1.394	1.498	ns	
			t_H	–0.998	–1.085	–1.151	ns	
		GCLK PLL	t_{SU}	3.290	3.600	3.890	ns	
			t_H	–3.018	–3.291	–3.543	ns	
	12 mA	GCLK	t_{SU}	1.270	1.394	1.498	ns	
			t_H	–0.998	–1.085	–1.151	ns	
		GCLK PLL	t_{SU}	3.290	3.600	3.890	ns	
			t_H	–3.018	–3.291	–3.543	ns	
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.095	1.171	1.229	ns	
			t_H	–0.825	–0.867	–0.887	ns	
		GCLK PLL	t_{SU}	3.131	3.393	3.637	ns	
			t_H	–2.861	–3.089	–3.295	ns	
	12 mA	GCLK	t_{SU}	1.095	1.171	1.229	ns	
			t_H	–0.825	–0.867	–0.887	ns	
		GCLK PLL	t_{SU}	3.131	3.393	3.637	ns	
			t_H	–2.861	–3.089	–3.295	ns	
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.095	1.171	1.229	ns	
			t_H	–0.825	–0.867	–0.887	ns	
		GCLK PLL	t_{SU}	3.131	3.393	3.637	ns	
			t_H	–2.861	–3.089	–3.295	ns	

Table 1–45. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Drive Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.156	1.260	1.344	ns
			t_H	–0.886	–0.954	–1.000	ns
		GCLK PLL	t_{SU}	3.192	3.482	3.752	ns
			t_H	–2.922	–3.176	–3.408	ns
	10 mA	GCLK	t_{SU}	1.156	1.260	1.344	ns
			t_H	–0.886	–0.954	–1.000	ns
		GCLK PLL	t_{SU}	3.192	3.482	3.752	ns
			t_H	–2.922	–3.176	–3.408	ns
	12 mA	GCLK	t_{SU}	1.156	1.260	1.344	ns
			t_H	–0.886	–0.954	–1.000	ns
		GCLK PLL	t_{SU}	3.192	3.482	3.752	ns
			t_H	–2.922	–3.176	–3.408	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.156	1.260	1.344	ns
			t_H	–0.886	–0.954	–1.000	ns
		GCLK PLL	t_{SU}	3.192	3.482	3.752	ns
			t_H	–2.922	–3.176	–3.408	ns
	16 mA	GCLK	t_{SU}	1.156	1.260	1.344	ns
			t_H	–0.886	–0.954	–1.000	ns
		GCLK PLL	t_{SU}	3.192	3.482	3.752	ns
			t_H	–2.922	–3.176	–3.408	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.156	1.260	1.344	ns
			t_H	–0.886	–0.954	–1.000	ns
		GCLK PLL	t_{SU}	3.192	3.482	3.752	ns
			t_H	–2.922	–3.176	–3.408	ns
	10 mA	GCLK	t_{SU}	1.156	1.260	1.344	ns
			t_H	–0.886	–0.954	–1.000	ns
		GCLK PLL	t_{SU}	3.192	3.482	3.752	ns
			t_H	–2.922	–3.176	–3.408	ns
	12 mA	GCLK	t_{SU}	1.156	1.260	1.344	ns
			t_H	–0.886	–0.954	–1.000	ns
		GCLK PLL	t_{SU}	3.192	3.482	3.752	ns
			t_H	–2.922	–3.176	–3.408	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.156	1.260	1.344	ns
			t_H	–0.886	–0.954	–1.000	ns
		GCLK PLL	t_{SU}	3.192	3.482	3.752	ns
			t_H	–2.922	–3.176	–3.408	ns

Table 1–45. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Drive Strength	Clock	Parameter	–6	–7	–8	Unit	
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.112	1.220	1.310	ns	
			t_H	–0.842	–0.915	–0.967	ns	
		GCLK PLL	t_{SU}	3.148	3.442	3.718	ns	
			t_H	–2.878	–3.137	–3.375	ns	
		10 mA	GCLK	t_{SU}	1.112	1.220	1.310	ns
				t_H	–0.842	–0.915	–0.967	ns
	GCLK PLL		t_{SU}	3.148	3.442	3.718	ns	
			t_H	–2.878	–3.137	–3.375	ns	
	12 mA	GCLK	t_{SU}	1.112	1.220	1.310	ns	
			t_H	–0.842	–0.915	–0.967	ns	
		GCLK PLL	t_{SU}	3.148	3.442	3.718	ns	
			t_H	–2.878	–3.137	–3.375	ns	
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.112	1.220	1.310	ns	
			t_H	–0.842	–0.915	–0.967	ns	
		GCLK PLL	t_{SU}	3.148	3.442	3.718	ns	
			t_H	–2.878	–3.137	–3.375	ns	
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.244	1.379	1.494	ns	
			t_H	–0.972	–1.070	–1.147	ns	
		GCLK PLL	t_{SU}	3.280	3.601	3.902	ns	
			t_H	–3.008	–3.292	–3.555	ns	
	10 mA	GCLK	t_{SU}	1.244	1.379	1.494	ns	
			t_H	–0.972	–1.070	–1.147	ns	
		GCLK PLL	t_{SU}	3.280	3.601	3.902	ns	
			t_H	–3.008	–3.292	–3.555	ns	
	12 mA	GCLK	t_{SU}	1.244	1.379	1.494	ns	
			t_H	–0.972	–1.070	–1.147	ns	
		GCLK PLL	t_{SU}	3.280	3.601	3.902	ns	
			t_H	–3.008	–3.292	–3.555	ns	
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	1.244	1.379	1.494	ns	
			t_H	–0.972	–1.070	–1.147	ns	
		GCLK PLL	t_{SU}	3.280	3.601	3.902	ns	
			t_H	–3.008	–3.292	–3.555	ns	
3.0-V PCI	—	GCLK	t_{SU}	1.167	1.202	1.215	ns	
			t_H	–0.897	–0.897	–0.874	ns	
		GCLK PLL	t_{SU}	3.187	3.408	3.607	ns	
			t_H	–2.917	–3.103	–3.266	ns	
3.0-V PCI-X	—	GCLK	t_{SU}	1.167	1.202	1.215	ns	
			t_H	–0.897	–0.897	–0.874	ns	
		GCLK PLL	t_{SU}	3.187	3.408	3.607	ns	
			t_H	–2.917	–3.103	–3.266	ns	

Table 1–46. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit		
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.176	1.223	1.233	ns		
			t_H	–0.907	–0.918	–0.891	ns		
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns		
			t_H	–2.925	–3.113	–3.282	ns		
	8 mA	GCLK	t_{SU}	1.176	1.223	1.233	ns		
			t_H	–0.907	–0.918	–0.891	ns		
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns		
			t_H	–2.925	–3.113	–3.282	ns		
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.176	1.223	1.233	ns		
			t_H	–0.907	–0.918	–0.891	ns		
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns		
			t_H	–2.925	–3.113	–3.282	ns		
		3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.176	1.223	1.233	ns
					t_H	–0.907	–0.918	–0.891	ns
GCLK PLL	t_{SU}			3.194	3.418	3.624	ns		
	t_H			–2.925	–3.113	–3.282	ns		
8 mA	GCLK		t_{SU}	1.176	1.223	1.233	ns		
			t_H	–0.907	–0.918	–0.891	ns		
	GCLK PLL		t_{SU}	3.194	3.418	3.624	ns		
			t_H	–2.925	–3.113	–3.282	ns		
12 mA	GCLK		t_{SU}	1.176	1.223	1.233	ns		
			t_H	–0.907	–0.918	–0.891	ns		
	GCLK PLL		t_{SU}	3.194	3.418	3.624	ns		
			t_H	–2.925	–3.113	–3.282	ns		
16 mA	GCLK	t_{SU}	1.176	1.223	1.233	ns			
		t_H	–0.907	–0.918	–0.891	ns			
	GCLK PLL	t_{SU}	3.194	3.418	3.624	ns			
		t_H	–2.925	–3.113	–3.282	ns			

Table 1–46. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.176	1.223	1.233	ns
			t_H	–0.907	–0.918	–0.891	ns
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns
			t_H	–2.925	–3.113	–3.282	ns
	8 mA	GCLK	t_{SU}	1.176	1.223	1.233	ns
			t_H	–0.907	–0.918	–0.891	ns
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns
			t_H	–2.925	–3.113	–3.282	ns
	12 mA	GCLK	t_{SU}	1.176	1.223	1.233	ns
			t_H	–0.907	–0.918	–0.891	ns
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns
			t_H	–2.925	–3.113	–3.282	ns
	16 mA	GCLK	t_{SU}	1.176	1.223	1.233	ns
			t_H	–0.907	–0.918	–0.891	ns
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns
			t_H	–2.925	–3.113	–3.282	ns
2.5V	4 mA	GCLK	t_{SU}	1.119	1.179	1.204	ns
			t_H	–0.850	–0.875	–0.863	ns
		GCLK PLL	t_{SU}	3.137	3.374	3.595	ns
			t_H	–2.868	–3.070	–3.254	ns
	8 mA	GCLK	t_{SU}	1.119	1.179	1.204	ns
			t_H	–0.850	–0.875	–0.863	ns
		GCLK PLL	t_{SU}	3.137	3.374	3.595	ns
			t_H	–2.868	–3.070	–3.254	ns
	12 mA	GCLK	t_{SU}	1.119	1.179	1.204	ns
			t_H	–0.850	–0.875	–0.863	ns
		GCLK PLL	t_{SU}	3.137	3.374	3.595	ns
			t_H	–2.868	–3.070	–3.254	ns
	16 mA	GCLK	t_{SU}	1.119	1.179	1.204	ns
			t_H	–0.850	–0.875	–0.863	ns
		GCLK PLL	t_{SU}	3.137	3.374	3.595	ns
			t_H	–2.868	–3.070	–3.254	ns

Table 1–46. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	-6	-7	-8	Unit
1.8V	2 mA	GCLK	t_{SU}	1.055	1.140	1.190	ns
			t_H	-0.788	-0.837	-0.848	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns
	4 mA	GCLK	t_{SU}	1.055	1.140	1.190	ns
			t_H	-0.788	-0.837	-0.848	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns
	6 mA	GCLK	t_{SU}	1.055	1.140	1.190	ns
			t_H	-0.788	-0.837	-0.848	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns
	8 mA	GCLK	t_{SU}	1.055	1.140	1.190	ns
			t_H	-0.788	-0.837	-0.848	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns
	10 mA	GCLK	t_{SU}	1.055	1.140	1.190	ns
			t_H	-0.788	-0.837	-0.848	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns
	12 mA	GCLK	t_{SU}	1.055	1.140	1.190	ns
			t_H	-0.788	-0.837	-0.848	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns
	16 mA	GCLK	t_{SU}	1.055	1.140	1.190	ns
			t_H	-0.788	-0.837	-0.848	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns

Table 1–46. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	1.124	1.233	1.308	ns
			t_H	–0.855	–0.928	–0.965	ns
		GCLK PLL	t_{SU}	3.132	3.418	3.689	ns
			t_H	–2.863	–3.113	–3.346	ns
	4 mA	GCLK	t_{SU}	1.124	1.233	1.308	ns
			t_H	–0.855	–0.928	–0.965	ns
		GCLK PLL	t_{SU}	3.132	3.418	3.689	ns
			t_H	–2.863	–3.113	–3.346	ns
	6 mA	GCLK	t_{SU}	1.124	1.233	1.308	ns
			t_H	–0.855	–0.928	–0.965	ns
		GCLK PLL	t_{SU}	3.132	3.418	3.689	ns
			t_H	–2.863	–3.113	–3.346	ns
	8 mA	GCLK	t_{SU}	1.124	1.233	1.308	ns
			t_H	–0.855	–0.928	–0.965	ns
		GCLK PLL	t_{SU}	3.132	3.418	3.689	ns
			t_H	–2.863	–3.113	–3.346	ns
	10 mA	GCLK	t_{SU}	1.124	1.233	1.308	ns
			t_H	–0.855	–0.928	–0.965	ns
		GCLK PLL	t_{SU}	3.132	3.418	3.689	ns
			t_H	–2.863	–3.113	–3.346	ns
	12 mA	GCLK	t_{SU}	1.124	1.233	1.308	ns
			t_H	–0.855	–0.928	–0.965	ns
		GCLK PLL	t_{SU}	3.132	3.418	3.689	ns
			t_H	–2.863	–3.113	–3.346	ns
16 mA	GCLK	t_{SU}	1.124	1.233	1.308	ns	
		t_H	–0.855	–0.928	–0.965	ns	
	GCLK PLL	t_{SU}	3.132	3.418	3.689	ns	
		t_H	–2.863	–3.113	–3.346	ns	

Table 1–46. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.2V	2 mA	GCLK	t_{SU}	1.277	1.413	1.515	ns	
			t_H	–1.006	–1.104	–1.167	ns	
		GCLK PLL	t_{SU}	3.285	3.598	3.896	ns	
			t_H	–3.014	–3.289	–3.548	ns	
	4 mA	GCLK	t_{SU}	1.277	1.413	1.515	ns	
			t_H	–1.006	–1.104	–1.167	ns	
		GCLK PLL	t_{SU}	3.285	3.598	3.896	ns	
			t_H	–3.014	–3.289	–3.548	ns	
	6 mA	GCLK	t_{SU}	1.277	1.413	1.515	ns	
			t_H	–1.006	–1.104	–1.167	ns	
		GCLK PLL	t_{SU}	3.285	3.598	3.896	ns	
			t_H	–3.014	–3.289	–3.548	ns	
	8 mA	GCLK	t_{SU}	1.277	1.413	1.515	ns	
			t_H	–1.006	–1.104	–1.167	ns	
		GCLK PLL	t_{SU}	3.285	3.598	3.896	ns	
			t_H	–3.014	–3.289	–3.548	ns	
	10 mA	GCLK	t_{SU}	1.277	1.413	1.515	ns	
			t_H	–1.006	–1.104	–1.167	ns	
		GCLK PLL	t_{SU}	3.285	3.598	3.896	ns	
			t_H	–3.014	–3.289	–3.548	ns	
	SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.112	1.192	1.256	ns
				t_H	–0.843	–0.887	–0.913	ns
			GCLK PLL	t_{SU}	3.127	3.393	3.643	ns
				t_H	–2.858	–3.088	–3.300	ns
12 mA		GCLK	t_{SU}	1.112	1.192	1.256	ns	
			t_H	–0.843	–0.887	–0.913	ns	
		GCLK PLL	t_{SU}	3.127	3.393	3.643	ns	
			t_H	–2.858	–3.088	–3.300	ns	
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.112	1.192	1.256	ns	
			t_H	–0.843	–0.887	–0.913	ns	
		GCLK PLL	t_{SU}	3.127	3.393	3.643	ns	
			t_H	–2.858	–3.088	–3.300	ns	

Table 1–46. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit		
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.174	1.281	1.373	ns		
			t_H	–0.905	–0.975	–1.028	ns		
		GCLK PLL	t_{SU}	3.179	3.472	3.750	ns		
			t_H	–2.910	–3.166	–3.405	ns		
		10 mA	GCLK	t_{SU}	1.174	1.281	1.373	ns	
				t_H	–0.905	–0.975	–1.028	ns	
	GCLK PLL		t_{SU}	3.179	3.472	3.750	ns		
			t_H	–2.910	–3.166	–3.405	ns		
	12 mA	GCLK	t_{SU}	1.174	1.281	1.373	ns		
			t_H	–0.905	–0.975	–1.028	ns		
		GCLK PLL	t_{SU}	3.179	3.472	3.750	ns		
			t_H	–2.910	–3.166	–3.405	ns		
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.174	1.281	1.373	ns		
			t_H	–0.905	–0.975	–1.028	ns		
		GCLK PLL	t_{SU}	3.179	3.472	3.750	ns		
			t_H	–2.910	–3.166	–3.405	ns		
	16 mA	GCLK	t_{SU}	1.174	1.281	1.373	ns		
			t_H	–0.905	–0.975	–1.028	ns		
		GCLK PLL	t_{SU}	3.179	3.472	3.750	ns		
			t_H	–2.910	–3.166	–3.405	ns		
		1.8-V HSTL Class I	8mA	GCLK	t_{SU}	1.174	1.281	1.373	ns
					t_H	–0.905	–0.975	–1.028	ns
GCLK PLL	t_{SU}			3.179	3.472	3.750	ns		
	t_H			–2.910	–3.166	–3.405	ns		
10 mA	GCLK		t_{SU}	1.174	1.281	1.373	ns		
			t_H	–0.905	–0.975	–1.028	ns		
	GCLK PLL		t_{SU}	3.179	3.472	3.750	ns		
			t_H	–2.910	–3.166	–3.405	ns		
12 mA	GCLK		t_{SU}	1.174	1.281	1.373	ns		
			t_H	–0.905	–0.975	–1.028	ns		
	GCLK PLL		t_{SU}	3.179	3.472	3.750	ns		
			t_H	–2.910	–3.166	–3.405	ns		
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.174	1.281	1.373	ns		
			t_H	–0.905	–0.975	–1.028	ns		
		GCLK PLL	t_{SU}	3.179	3.472	3.750	ns		
			t_H	–2.910	–3.166	–3.405	ns		

Table 1–46. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.129	1.240	1.336	ns	
			t_H	–0.860	–0.935	–0.992	ns	
		GCLK PLL	t_{SU}	3.134	3.431	3.713	ns	
			t_H	–2.865	–3.126	–3.369	ns	
		10 mA	GCLK	t_{SU}	1.129	1.240	1.336	ns
				t_H	–0.860	–0.935	–0.992	ns
	GCLK PLL	t_{SU}	3.134	3.431	3.713	ns		
		t_H	–2.865	–3.126	–3.369	ns		
	12 mA	GCLK	t_{SU}	1.129	1.240	1.336	ns	
			t_H	–0.860	–0.935	–0.992	ns	
		GCLK PLL	t_{SU}	3.134	3.431	3.713	ns	
			t_H	–2.865	–3.126	–3.369	ns	
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.129	1.240	1.336	ns	
			t_H	–0.860	–0.935	–0.992	ns	
		GCLK PLL	t_{SU}	3.134	3.431	3.713	ns	
			t_H	–2.865	–3.126	–3.369	ns	
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.260	1.398	1.521	ns	
			t_H	–0.989	–1.089	–1.174	ns	
		GCLK PLL	t_{SU}	3.265	3.589	3.898	ns	
			t_H	–2.994	–3.280	–3.551	ns	
	10 mA	GCLK	t_{SU}	1.260	1.398	1.521	ns	
			t_H	–0.989	–1.089	–1.174	ns	
		GCLK PLL	t_{SU}	3.265	3.589	3.898	ns	
			t_H	–2.994	–3.280	–3.551	ns	
3.0-V PCI	—	GCLK	t_{SU}	1.172	1.219	1.229	ns	
			t_H	–0.903	–0.914	–0.887	ns	
		GCLK PLL	t_{SU}	3.190	3.414	3.620	ns	
			t_H	–2.921	–3.109	–3.278	ns	
3.0-V PCI-X	—	GCLK	t_{SU}	1.172	1.219	1.229	ns	
			t_H	–0.903	–0.914	–0.887	ns	
		GCLK PLL	t_{SU}	3.190	3.414	3.620	ns	
			t_H	–2.921	–3.109	–3.278	ns	

Table 1–47. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
3.3-V LVTTTL	4 mA	GCLK	t_{CO}	8.985	5.616	6.133	ns	
		GCLK PLL	t_{CO}	3.137	3.421	3.752	ns	
	8 mA	GCLK	t_{CO}	6.559	5.147	5.641	ns	
		GCLK PLL	t_{CO}	2.688	2.952	3.260	ns	
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	7.338	5.238	5.737	ns	
		GCLK PLL	t_{CO}	2.774	3.043	3.356	ns	
3.0-V LVTTTL	4 mA	GCLK	t_{CO}	7.761	5.320	5.828	ns	
		GCLK PLL	t_{CO}	2.868	3.125	3.447	ns	
	8 mA	GCLK	t_{CO}	6.201	5.060	5.546	ns	
		GCLK PLL	t_{CO}	2.610	2.865	3.165	ns	
	12 mA	GCLK	t_{CO}	5.553	4.938	5.425	ns	
		GCLK PLL	t_{CO}	2.486	2.743	3.044	ns	
	16 mA	GCLK	t_{CO}	5.193	4.873	5.346	ns	
		GCLK PLL	t_{CO}	2.436	2.678	2.965	ns	
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	6.199	5.059	5.545	ns	
		GCLK PLL	t_{CO}	2.608	2.864	3.164	ns	
	8 mA	GCLK	t_{CO}	5.222	4.877	5.361	ns	
		GCLK PLL	t_{CO}	2.439	2.682	2.980	ns	
	12 mA	GCLK	t_{CO}	4.910	4.836	5.310	ns	
		GCLK PLL	t_{CO}	2.398	2.641	2.929	ns	
	16 mA	GCLK	t_{CO}	4.733	4.817	5.291	ns	
		GCLK PLL	t_{CO}	2.378	2.622	2.910	ns	
	2.5V	4 mA	GCLK	t_{CO}	7.945	5.458	5.974	ns
			GCLK PLL	t_{CO}	2.990	3.263	3.593	ns
8 mA		GCLK	t_{CO}	6.327	5.181	5.684	ns	
		GCLK PLL	t_{CO}	2.718	2.986	3.303	ns	
12 mA		GCLK	t_{CO}	5.679	5.059	5.560	ns	
		GCLK PLL	t_{CO}	2.600	2.864	3.179	ns	
16 mA		GCLK	t_{CO}	5.371	5.003	5.500	ns	
		GCLK PLL	t_{CO}	2.548	2.808	3.119	ns	

Table 1–47. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t_{CO}	12.204	6.766	7.439	ns	
		GCLK PLL	t_{CO}	4.163	4.571	5.058	ns	
	4 mA	GCLK	t_{CO}	8.798	6.180	6.827	ns	
		GCLK PLL	t_{CO}	3.589	3.985	4.446	ns	
	6 mA	GCLK	t_{CO}	7.468	5.875	6.486	ns	
		GCLK PLL	t_{CO}	3.319	3.680	4.105	ns	
	8 mA	GCLK	t_{CO}	6.807	5.759	6.357	ns	
		GCLK PLL	t_{CO}	3.205	3.564	3.976	ns	
	10 mA	GCLK	t_{CO}	6.459	5.693	6.293	ns	
		GCLK PLL	t_{CO}	3.142	3.498	3.912	ns	
	12 mA	GCLK	t_{CO}	6.151	5.612	6.199	ns	
		GCLK PLL	t_{CO}	3.077	3.417	3.818	ns	
	16 mA	GCLK	t_{CO}	5.833	5.558	6.136	ns	
		GCLK PLL	t_{CO}	3.023	3.363	3.755	ns	
	1.5V	2 mA	GCLK	t_{CO}	11.568	7.334	8.189	ns
			GCLK PLL	t_{CO}	4.571	5.139	5.808	ns
		4 mA	GCLK	t_{CO}	8.497	6.671	7.429	ns
			GCLK PLL	t_{CO}	4.000	4.476	5.048	ns
6 mA		GCLK	t_{CO}	7.476	6.461	7.206	ns	
		GCLK PLL	t_{CO}	3.803	4.266	4.825	ns	
8 mA		GCLK	t_{CO}	6.947	6.325	7.036	ns	
		GCLK PLL	t_{CO}	3.685	4.130	4.655	ns	
10 mA		GCLK	t_{CO}	6.630	6.255	6.969	ns	
		GCLK PLL	t_{CO}	3.618	4.060	4.588	ns	
12 mA		GCLK	t_{CO}	6.430	6.206	6.909	ns	
		GCLK PLL	t_{CO}	3.582	4.011	4.528	ns	
16 mA		GCLK	t_{CO}	6.090	6.080	6.751	ns	
		GCLK PLL	t_{CO}	3.464	3.885	4.370	ns	
1.2V		2 mA	GCLK	t_{CO}	11.760	8.699	9.923	ns
			GCLK PLL	t_{CO}	5.647	6.504	7.542	ns
		4 mA	GCLK	t_{CO}	9.137	8.122	9.252	ns
			GCLK PLL	t_{CO}	5.148	5.927	6.871	ns
	6 mA	GCLK	t_{CO}	8.318	7.908	8.998	ns	
		GCLK PLL	t_{CO}	4.967	5.713	6.617	ns	
	8 mA	GCLK	t_{CO}	7.910	7.815	8.892	ns	
		GCLK PLL	t_{CO}	4.884	5.620	6.511	ns	
	10 mA	GCLK	t_{CO}	7.574	7.631	8.650	ns	
		GCLK PLL	t_{CO}	4.739	5.436	6.269	ns	
	12 mA	GCLK	t_{CO}	7.418	7.603	8.622	ns	
		GCLK PLL	t_{CO}	4.713	5.408	6.241	ns	

Table 1–47. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.646	5.089	5.580	ns
		GCLK PLL	t_{CO}	2.609	2.866	3.162	ns
	12 mA	GCLK	t_{CO}	4.611	5.053	5.543	ns
		GCLK PLL	t_{CO}	2.574	2.830	3.125	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.554	4.991	5.476	ns
		GCLK PLL	t_{CO}	2.517	2.768	3.058	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.050	5.563	6.132	ns
		GCLK PLL	t_{CO}	3.013	3.340	3.714	ns
	10 mA	GCLK	t_{CO}	5.019	5.525	6.086	ns
		GCLK PLL	t_{CO}	2.982	3.302	3.668	ns
	12 mA	GCLK	t_{CO}	5.004	5.510	6.068	ns
		GCLK PLL	t_{CO}	2.967	3.287	3.650	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	4.991	5.495	6.055	ns
		GCLK PLL	t_{CO}	2.954	3.272	3.637	ns
	16 mA	GCLK	t_{CO}	4.972	5.476	6.035	ns
		GCLK PLL	t_{CO}	2.935	3.253	3.617	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.031	5.535	6.094	ns
		GCLK PLL	t_{CO}	2.994	3.312	3.676	ns
	10 mA	GCLK	t_{CO}	5.022	5.528	6.091	ns
		GCLK PLL	t_{CO}	2.985	3.305	3.673	ns
	12 mA	GCLK	t_{CO}	5.001	5.503	6.060	ns
		GCLK PLL	t_{CO}	2.964	3.280	3.642	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	4.973	5.470	6.024	ns
		GCLK PLL	t_{CO}	2.936	3.247	3.606	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.536	6.130	6.801	ns
		GCLK PLL	t_{CO}	3.499	3.907	4.383	ns
	10 mA	GCLK	t_{CO}	5.523	6.111	6.776	ns
		GCLK PLL	t_{CO}	3.486	3.888	4.358	ns
	12 mA	GCLK	t_{CO}	5.514	6.105	6.772	ns
		GCLK PLL	t_{CO}	3.477	3.882	4.354	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.471	6.052	6.708	ns
		GCLK PLL	t_{CO}	3.434	3.829	4.290	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.707	7.570	8.579	ns
		GCLK PLL	t_{CO}	4.670	5.347	6.161	ns
	10 mA	GCLK	t_{CO}	6.629	7.464	8.424	ns
		GCLK PLL	t_{CO}	4.592	5.241	6.006	ns
	12 mA	GCLK	t_{CO}	6.627	7.464	8.428	ns
		GCLK PLL	t_{CO}	4.590	5.241	6.010	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.570	7.393	8.347	ns
		GCLK PLL	t_{CO}	4.533	5.170	5.929	ns

Table 1–47. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V PCI	—	GCLK	t_{CO}	5.112	5.147	5.629	ns
		GCLK PLL	t_{CO}	2.700	2.952	3.248	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.112	5.147	5.629	ns
		GCLK PLL	t_{CO}	2.700	2.952	3.248	ns

Table 1–48. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{CO}	8.926	9.613	10.351	ns
		GCLK PLL	t_{CO}	6.907	3.366	3.688	ns
	8 mA	GCLK	t_{CO}	6.518	7.029	7.624	ns
		GCLK PLL	t_{CO}	4.499	2.902	3.206	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	7.298	7.845	8.408	ns
		GCLK PLL	t_{CO}	5.279	2.989	3.297	ns
3.0-V LVTTTL	4 mA	GCLK	t_{CO}	7.730	8.290	8.898	ns
		GCLK PLL	t_{CO}	5.711	3.087	3.388	ns
	8 mA	GCLK	t_{CO}	6.174	6.678	7.252	ns
		GCLK PLL	t_{CO}	4.155	2.832	3.127	ns
	12 mA	GCLK	t_{CO}	5.527	6.025	6.557	ns
		GCLK PLL	t_{CO}	3.508	2.706	3.000	ns
	16 mA	GCLK	t_{CO}	5.172	5.627	6.135	ns
		GCLK PLL	t_{CO}	3.153	2.652	2.933	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	6.172	6.676	7.250	ns
		GCLK PLL	t_{CO}	4.153	2.831	3.125	ns
	8 mA	GCLK	t_{CO}	5.201	5.661	6.178	ns
		GCLK PLL	t_{CO}	3.182	2.654	2.936	ns
	12 mA	GCLK	t_{CO}	4.891	5.340	5.828	ns
		GCLK PLL	t_{CO}	2.872	2.614	2.897	ns
	16 mA	GCLK	t_{CO}	4.717	5.158	5.649	ns
		GCLK PLL	t_{CO}	2.698	2.594	2.877	ns
2.5V	4 mA	GCLK	t_{CO}	7.909	8.534	9.221	ns
		GCLK PLL	t_{CO}	5.890	3.226	3.544	ns
	8 mA	GCLK	t_{CO}	6.303	6.847	7.448	ns
		GCLK PLL	t_{CO}	4.284	2.957	3.268	ns
	12 mA	GCLK	t_{CO}	5.654	6.172	6.728	ns
		GCLK PLL	t_{CO}	3.635	2.837	3.144	ns
16 mA	GCLK	t_{CO}	5.350	5.846	6.394	ns	
	GCLK PLL	t_{CO}	3.331	2.781	3.086	ns	

Table 1–48. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Current Strength	Clock	Parameter	-6	-7	-8	Unit	
1.8V	2 mA	GCLK	t _{CO}	12.152	13.256	14.479	ns	
		GCLK PLL	t _{CO}	10.133	4.524	5.001	ns	
	4 mA	GCLK	t _{CO}	8.762	9.607	10.552	ns	
		GCLK PLL	t _{CO}	6.743	3.954	4.409	ns	
	6 mA	GCLK	t _{CO}	7.441	8.164	8.969	ns	
		GCLK PLL	t _{CO}	5.422	3.659	4.077	ns	
	8 mA	GCLK	t _{CO}	6.781	7.445	8.182	ns	
		GCLK PLL	t _{CO}	4.762	3.531	3.932	ns	
	10 mA	GCLK	t _{CO}	6.432	7.076	7.796	ns	
		GCLK PLL	t _{CO}	4.413	3.477	3.885	ns	
	12 mA	GCLK	t _{CO}	6.129	6.749	7.426	ns	
		GCLK PLL	t _{CO}	4.110	3.401	3.796	ns	
	16 mA	GCLK	t _{CO}	5.823	6.413	7.071	ns	
		GCLK PLL	t _{CO}	3.804	3.352	3.741	ns	
	1.5V	2 mA	GCLK	t _{CO}	11.517	12.805	14.272	ns
			GCLK PLL	t _{CO}	9.498	5.095	5.753	ns
		4 mA	GCLK	t _{CO}	8.461	9.400	10.452	ns
			GCLK PLL	t _{CO}	6.442	4.452	5.011	ns
6 mA		GCLK	t _{CO}	7.446	8.278	9.218	ns	
		GCLK PLL	t _{CO}	5.427	4.247	4.795	ns	
8 mA		GCLK	t _{CO}	6.939	7.707	8.569	ns	
		GCLK PLL	t _{CO}	4.920	4.136	4.655	ns	
10 mA		GCLK	t _{CO}	6.620	7.362	8.187	ns	
		GCLK PLL	t _{CO}	4.601	4.064	4.586	ns	
12 mA		GCLK	t _{CO}	6.418	7.134	7.928	ns	
		GCLK PLL	t _{CO}	4.399	4.013	4.522	ns	
16 mA		GCLK	t _{CO}	6.075	6.746	7.481	ns	
		GCLK PLL	t _{CO}	4.056	3.932	4.434	ns	
1.2V		2 mA	GCLK	t _{CO}	11.722	13.378	15.348	ns
			GCLK PLL	t _{CO}	9.703	6.470	7.499	ns
		4 mA	GCLK	t _{CO}	9.108	10.366	11.849	ns
			GCLK PLL	t _{CO}	7.089	5.904	6.840	ns
	6 mA	GCLK	t _{CO}	8.315	9.448	10.781	ns	
		GCLK PLL	t _{CO}	6.296	5.720	6.625	ns	
	8 mA	GCLK	t _{CO}	7.902	8.974	10.232	ns	
		GCLK PLL	t _{CO}	5.883	5.622	6.512	ns	
	10 mA	GCLK	t _{CO}	7.563	8.566	9.728	ns	
		GCLK PLL	t _{CO}	5.544	5.478	6.333	ns	

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.618	5.058	5.544	ns
		GCLK PLL	t_{CO}	2.589	2.844	3.143	ns
	12 mA	GCLK	t_{CO}	4.586	5.024	5.508	ns
		GCLK PLL	t_{CO}	2.557	2.810	3.107	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.535	4.971	5.451	ns
		GCLK PLL	t_{CO}	2.506	2.757	3.050	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.025	5.532	6.097	ns
		GCLK PLL	t_{CO}	3.006	3.328	3.706	ns
	10 mA	GCLK	t_{CO}	5.006	5.508	6.067	ns
		GCLK PLL	t_{CO}	2.987	3.304	3.676	ns
	12 mA	GCLK	t_{CO}	4.984	5.484	6.040	ns
		GCLK PLL	t_{CO}	2.965	3.280	3.649	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	4.976	5.476	6.033	ns
		GCLK PLL	t_{CO}	2.957	3.272	3.642	ns
	16 mA	GCLK	t_{CO}	4.961	5.462	6.019	ns
		GCLK PLL	t_{CO}	2.942	3.258	3.628	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.005	5.504	6.058	ns
		GCLK PLL	t_{CO}	2.986	3.300	3.667	ns
	10 mA	GCLK	t_{CO}	4.998	5.500	6.057	ns
		GCLK PLL	t_{CO}	2.979	3.296	3.666	ns
	12 mA	GCLK	t_{CO}	4.988	5.486	6.040	ns
		GCLK PLL	t_{CO}	2.969	3.282	3.649	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	4.955	5.448	5.998	ns
		GCLK PLL	t_{CO}	2.936	3.244	3.607	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.510	6.103	6.766	ns
		GCLK PLL	t_{CO}	3.491	3.899	4.375	ns
	10 mA	GCLK	t_{CO}	5.508	6.098	6.757	ns
		GCLK PLL	t_{CO}	3.489	3.894	4.366	ns
	12 mA	GCLK	t_{CO}	5.499	6.091	6.753	ns
		GCLK PLL	t_{CO}	3.480	3.887	4.362	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.460	6.045	6.700	ns
		GCLK PLL	t_{CO}	3.441	3.841	4.309	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.701	7.568	8.579	ns
		GCLK PLL	t_{CO}	4.682	5.364	6.188	ns
	10 mA	GCLK	t_{CO}	6.618	7.454	8.415	ns
		GCLK PLL	t_{CO}	4.599	5.250	6.024	ns
3.0-V PCI	—	GCLK	t_{CO}	5.079	5.550	6.079	ns
		GCLK PLL	t_{CO}	3.060	2.919	3.209	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.079	5.550	6.079	ns
		GCLK PLL	t_{CO}	3.060	2.919	3.209	ns

Table 1–49. EP3C5 Column Pin Differential I/O Timing Parameters

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.986	1.069	1.133	ns
			t_H	–0.718	–0.766	–0.793	ns
		GCLK PLL	t_{SU}	3.015	3.284	3.533	ns
			t_H	–2.747	–2.981	–3.193	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.571	5.048	5.552	ns
		GCLK PLL	t_{CO}	4.571	5.048	5.552	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.571	5.048	5.552	ns
		GCLK PLL	t_{CO}	4.571	5.048	5.552	ns
PPDS_E_3R	—	GCLK	t_{CO}	4.571	5.048	5.552	ns
		GCLK PLL	t_{CO}	4.571	5.048	5.552	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.571	5.048	5.552	ns
		GCLK PLL	t_{CO}	4.571	5.048	5.552	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.571	5.048	5.552	ns
		GCLK PLL	t_{CO}	4.571	5.048	5.552	ns

Table 1–50. EP3C5 Row Pin Differential I/O Timing Parameters

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.991	1.076	1.146	ns
			t_H	–0.724	–0.774	–0.805	ns
			t_{CO}	3.782	4.154	4.553	ns
		GCLK PLL	t_{SU}	3.020	3.293	3.549	ns
			t_H	–2.753	–2.991	–3.208	ns
			t_{CO}	1.743	1.930	2.142	ns
mini-LVDS	—	GCLK	t_{CO}	3.782	4.154	4.553	ns
		GCLK PLL	t_{CO}	1.743	1.930	2.142	ns
PPDS	—	GCLK	t_{CO}	3.782	4.154	4.553	ns
		GCLK PLL	t_{CO}	1.743	1.930	2.142	ns
RSDS	—	GCLK	t_{CO}	3.782	4.154	4.553	ns
		GCLK PLL	t_{CO}	1.743	1.930	2.142	ns

EP3C10 I/O Timing Parameters

Tables 1–51 through 1–56 show the maximum I/O timing parameters for EP3C10 devices.

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	1.158	1.192	1.207	ns
			t_H	–0.888	–0.887	–0.866	ns
		GCLK PLL	t_{SU}	3.187	3.407	3.607	ns
			t_H	–2.917	–3.102	–3.266	ns
	8 mA	GCLK	t_{SU}	1.158	1.192	1.207	ns
			t_H	–0.888	–0.887	–0.866	ns
		GCLK PLL	t_{SU}	3.187	3.407	3.607	ns
			t_H	–2.917	–3.102	–3.266	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.158	1.192	1.207	ns
			t_H	–0.888	–0.887	–0.866	ns
		GCLK PLL	t_{SU}	3.187	3.407	3.607	ns
			t_H	–2.917	–3.102	–3.266	ns
3.0-V LVTTTL	4 mA	GCLK	t_{SU}	1.158	1.192	1.207	ns
			t_H	–0.888	–0.887	–0.866	ns
		GCLK PLL	t_{SU}	3.187	3.407	3.607	ns
			t_H	–2.917	–3.102	–3.266	ns
	8 mA	GCLK	t_{SU}	1.158	1.192	1.207	ns
			t_H	–0.888	–0.887	–0.866	ns
		GCLK PLL	t_{SU}	3.187	3.407	3.607	ns
			t_H	–2.917	–3.102	–3.266	ns
	12 mA	GCLK	t_{SU}	1.158	1.192	1.207	ns
			t_H	–0.888	–0.887	–0.866	ns
		GCLK PLL	t_{SU}	3.187	3.407	3.607	ns
			t_H	–2.917	–3.102	–3.266	ns
	16 mA	GCLK	t_{SU}	1.158	1.192	1.207	ns
			t_H	–0.888	–0.887	–0.866	ns
		GCLK PLL	t_{SU}	3.187	3.407	3.607	ns
			t_H	–2.917	–3.102	–3.266	ns

Table 1–51. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.158	1.192	1.207	ns
			t_H	–0.888	–0.887	–0.866	ns
		GCLK PLL	t_{SU}	3.187	3.407	3.607	ns
			t_H	–2.917	–3.102	–3.266	ns
	8 mA	GCLK	t_{SU}	1.158	1.192	1.207	ns
			t_H	–0.888	–0.887	–0.866	ns
		GCLK PLL	t_{SU}	3.187	3.407	3.607	ns
			t_H	–2.917	–3.102	–3.266	ns
	12 mA	GCLK	t_{SU}	1.158	1.192	1.207	ns
			t_H	–0.888	–0.887	–0.866	ns
		GCLK PLL	t_{SU}	3.187	3.407	3.607	ns
			t_H	–2.917	–3.102	–3.266	ns
	16 mA	GCLK	t_{SU}	1.158	1.192	1.207	ns
			t_H	–0.888	–0.887	–0.866	ns
		GCLK PLL	t_{SU}	3.187	3.407	3.607	ns
			t_H	–2.917	–3.102	–3.266	ns
2.5V	4 mA	GCLK	t_{SU}	1.101	1.147	1.175	ns
			t_H	–0.831	–0.843	–0.835	ns
		GCLK PLL	t_{SU}	3.130	3.362	3.575	ns
			t_H	–2.860	–3.058	–3.235	ns
	8 mA	GCLK	t_{SU}	1.101	1.147	1.175	ns
			t_H	–0.831	–0.843	–0.835	ns
		GCLK PLL	t_{SU}	3.130	3.362	3.575	ns
			t_H	–2.860	–3.058	–3.235	ns
	12 mA	GCLK	t_{SU}	1.101	1.147	1.175	ns
			t_H	–0.831	–0.843	–0.835	ns
		GCLK PLL	t_{SU}	3.130	3.362	3.575	ns
			t_H	–2.860	–3.058	–3.235	ns
	16 mA	GCLK	t_{SU}	1.101	1.147	1.175	ns
			t_H	–0.831	–0.843	–0.835	ns
		GCLK PLL	t_{SU}	3.130	3.362	3.575	ns
			t_H	–2.860	–3.058	–3.235	ns

Table 1–51. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.8V	2 mA	GCLK	t_{SU}	1.036	1.108	1.162	ns
			t_H	–0.768	–0.805	–0.821	ns
		GCLK PLL	t_{SU}	3.065	3.323	3.562	ns
			t_H	–2.797	–3.020	–3.221	ns
	4 mA	GCLK	t_{SU}	1.036	1.108	1.162	ns
			t_H	–0.768	–0.805	–0.821	ns
		GCLK PLL	t_{SU}	3.065	3.323	3.562	ns
			t_H	–2.797	–3.020	–3.221	ns
	6 mA	GCLK	t_{SU}	1.036	1.108	1.162	ns
			t_H	–0.768	–0.805	–0.821	ns
		GCLK PLL	t_{SU}	3.065	3.323	3.562	ns
			t_H	–2.797	–3.020	–3.221	ns
	8 mA	GCLK	t_{SU}	1.036	1.108	1.162	ns
			t_H	–0.768	–0.805	–0.821	ns
		GCLK PLL	t_{SU}	3.065	3.323	3.562	ns
			t_H	–2.797	–3.020	–3.221	ns
	10 mA	GCLK	t_{SU}	1.036	1.108	1.162	ns
			t_H	–0.768	–0.805	–0.821	ns
		GCLK PLL	t_{SU}	3.065	3.323	3.562	ns
			t_H	–2.797	–3.020	–3.221	ns
	12 mA	GCLK	t_{SU}	1.036	1.108	1.162	ns
			t_H	–0.768	–0.805	–0.821	ns
		GCLK PLL	t_{SU}	3.065	3.323	3.562	ns
			t_H	–2.797	–3.020	–3.221	ns
16 mA	GCLK	t_{SU}	1.036	1.108	1.162	ns	
		t_H	–0.768	–0.805	–0.821	ns	
	GCLK PLL	t_{SU}	3.065	3.323	3.562	ns	
		t_H	–2.797	–3.020	–3.221	ns	

Table 1–51. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	1.105	1.200	1.279	ns
			t_H	–0.835	–0.895	–0.936	ns
		GCLK PLL	t_{SU}	3.134	3.415	3.679	ns
			t_H	–2.864	–3.110	–3.336	ns
	4 mA	GCLK	t_{SU}	1.105	1.200	1.279	ns
			t_H	–0.835	–0.895	–0.936	ns
		GCLK PLL	t_{SU}	3.134	3.415	3.679	ns
			t_H	–2.864	–3.110	–3.336	ns
	6 mA	GCLK	t_{SU}	1.105	1.200	1.279	ns
			t_H	–0.835	–0.895	–0.936	ns
		GCLK PLL	t_{SU}	3.134	3.415	3.679	ns
			t_H	–2.864	–3.110	–3.336	ns
	8 mA	GCLK	t_{SU}	1.105	1.200	1.279	ns
			t_H	–0.835	–0.895	–0.936	ns
		GCLK PLL	t_{SU}	3.134	3.415	3.679	ns
			t_H	–2.864	–3.110	–3.336	ns
	10 mA	GCLK	t_{SU}	1.105	1.200	1.279	ns
			t_H	–0.835	–0.895	–0.936	ns
		GCLK PLL	t_{SU}	3.134	3.415	3.679	ns
			t_H	–2.864	–3.110	–3.336	ns
	12 mA	GCLK	t_{SU}	1.105	1.200	1.279	ns
			t_H	–0.835	–0.895	–0.936	ns
		GCLK PLL	t_{SU}	3.134	3.415	3.679	ns
			t_H	–2.864	–3.110	–3.336	ns
16 mA	GCLK	t_{SU}	1.105	1.200	1.279	ns	
		t_H	–0.835	–0.895	–0.936	ns	
	GCLK PLL	t_{SU}	3.134	3.415	3.679	ns	
		t_H	–2.864	–3.110	–3.336	ns	

Table 1–51. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.2V	2 mA	GCLK	t_{SU}	1.257	1.380	1.485	ns
			t_H	–0.985	–1.071	–1.138	ns
		GCLK PLL	t_{SU}	3.286	3.595	3.885	ns
			t_H	–3.014	–3.286	–3.538	ns
	4 mA	GCLK	t_{SU}	1.257	1.380	1.485	ns
			t_H	–0.985	–1.071	–1.138	ns
		GCLK PLL	t_{SU}	3.286	3.595	3.885	ns
			t_H	–3.014	–3.286	–3.538	ns
	6 mA	GCLK	t_{SU}	1.257	1.380	1.485	ns
			t_H	–0.985	–1.071	–1.138	ns
		GCLK PLL	t_{SU}	3.286	3.595	3.885	ns
			t_H	–3.014	–3.286	–3.538	ns
	8 mA	GCLK	t_{SU}	1.257	1.380	1.485	ns
			t_H	–0.985	–1.071	–1.138	ns
		GCLK PLL	t_{SU}	3.286	3.595	3.885	ns
			t_H	–3.014	–3.286	–3.538	ns
	10 mA	GCLK	t_{SU}	1.257	1.380	1.485	ns
			t_H	–0.985	–1.071	–1.138	ns
		GCLK PLL	t_{SU}	3.286	3.595	3.885	ns
			t_H	–3.014	–3.286	–3.538	ns
	12 mA	GCLK	t_{SU}	1.257	1.380	1.485	ns
			t_H	–0.985	–1.071	–1.138	ns
		GCLK PLL	t_{SU}	3.286	3.595	3.885	ns
			t_H	–3.014	–3.286	–3.538	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.090	1.165	1.224	ns
			t_H	–0.820	–0.861	–0.882	ns
		GCLK PLL	t_{SU}	3.119	3.380	3.624	ns
			t_H	–2.849	–3.076	–3.282	ns
	12 mA	GCLK	t_{SU}	1.090	1.165	1.224	ns
			t_H	–0.820	–0.861	–0.882	ns
		GCLK PLL	t_{SU}	3.119	3.380	3.624	ns
			t_H	–2.849	–3.076	–3.282	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.090	1.165	1.224	ns
			t_H	–0.820	–0.861	–0.882	ns
		GCLK PLL	t_{SU}	3.119	3.380	3.624	ns
			t_H	–2.849	–3.076	–3.282	ns

Table 1–51. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.151	1.254	1.339	ns	
			t_H	–0.881	–0.948	–0.995	ns	
		GCLK PLL	t_{SU}	3.180	3.469	3.739	ns	
			t_H	–2.910	–3.163	–3.395	ns	
		10 mA	GCLK	t_{SU}	1.151	1.254	1.339	ns
				t_H	–0.881	–0.948	–0.995	ns
	GCLK PLL		t_{SU}	3.180	3.469	3.739	ns	
			t_H	–2.910	–3.163	–3.395	ns	
	12 mA	GCLK	t_{SU}	1.151	1.254	1.339	ns	
			t_H	–0.881	–0.948	–0.995	ns	
		GCLK PLL	t_{SU}	3.180	3.469	3.739	ns	
			t_H	–2.910	–3.163	–3.395	ns	
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.151	1.254	1.339	ns	
			t_H	–0.881	–0.948	–0.995	ns	
		GCLK PLL	t_{SU}	3.180	3.469	3.739	ns	
			t_H	–2.910	–3.163	–3.395	ns	
		16 mA	GCLK	t_{SU}	1.151	1.254	1.339	ns
				t_H	–0.881	–0.948	–0.995	ns
	GCLK PLL		t_{SU}	3.180	3.469	3.739	ns	
			t_H	–2.910	–3.163	–3.395	ns	
	1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.151	1.254	1.339	ns
				t_H	–0.881	–0.948	–0.995	ns
GCLK PLL			t_{SU}	3.180	3.469	3.739	ns	
			t_H	–2.910	–3.163	–3.395	ns	
10 mA			GCLK	t_{SU}	1.151	1.254	1.339	ns
				t_H	–0.881	–0.948	–0.995	ns
		GCLK PLL	t_{SU}	3.180	3.469	3.739	ns	
			t_H	–2.910	–3.163	–3.395	ns	
12 mA		GCLK	t_{SU}	1.151	1.254	1.339	ns	
			t_H	–0.881	–0.948	–0.995	ns	
		GCLK PLL	t_{SU}	3.180	3.469	3.739	ns	
			t_H	–2.910	–3.163	–3.395	ns	
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.151	1.254	1.339	ns	
			t_H	–0.881	–0.948	–0.995	ns	
		GCLK PLL	t_{SU}	3.180	3.469	3.739	ns	
			t_H	–2.910	–3.163	–3.395	ns	

Table 1–51. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.107	1.214	1.305	ns	
			t_H	–0.837	–0.909	–0.962	ns	
		GCLK PLL	t_{SU}	3.136	3.429	3.705	ns	
			t_H	–2.866	–3.124	–3.362	ns	
		10 mA	GCLK	t_{SU}	1.107	1.214	1.305	ns
				t_H	–0.837	–0.909	–0.962	ns
	GCLK PLL		t_{SU}	3.136	3.429	3.705	ns	
			t_H	–2.866	–3.124	–3.362	ns	
	12 mA	GCLK	t_{SU}	1.107	1.214	1.305	ns	
			t_H	–0.837	–0.909	–0.962	ns	
		GCLK PLL	t_{SU}	3.136	3.429	3.705	ns	
			t_H	–2.866	–3.124	–3.362	ns	
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.107	1.214	1.305	ns	
			t_H	–0.837	–0.909	–0.962	ns	
		GCLK PLL	t_{SU}	3.136	3.429	3.705	ns	
			t_H	–2.866	–3.124	–3.362	ns	
	1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.239	1.373	1.489	ns
				t_H	–0.967	–1.064	–1.142	ns
GCLK PLL			t_{SU}	3.268	3.588	3.889	ns	
			t_H	–2.996	–3.279	–3.542	ns	
10 mA			GCLK	t_{SU}	1.239	1.373	1.489	ns
				t_H	–0.967	–1.064	–1.142	ns
		GCLK PLL	t_{SU}	3.268	3.588	3.889	ns	
			t_H	–2.996	–3.279	–3.542	ns	
12 mA		GCLK	t_{SU}	1.239	1.373	1.489	ns	
			t_H	–0.967	–1.064	–1.142	ns	
		GCLK PLL	t_{SU}	3.268	3.588	3.889	ns	
			t_H	–2.996	–3.279	–3.542	ns	
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	1.239	1.373	1.489	ns	
			t_H	–0.967	–1.064	–1.142	ns	
		GCLK PLL	t_{SU}	3.268	3.588	3.889	ns	
			t_H	–2.996	–3.279	–3.542	ns	
	3.0-V PCI	—	GCLK	t_{SU}	1.154	1.188	1.202	ns
				t_H	–0.884	–0.883	–0.861	ns
GCLK PLL			t_{SU}	3.183	3.403	3.602	ns	
			t_H	–2.913	–3.098	–3.261	ns	
3.0-V PCI-X	—	GCLK	t_{SU}	1.154	1.188	1.202	ns	
			t_H	–0.884	–0.883	–0.861	ns	
		GCLK PLL	t_{SU}	3.183	3.403	3.602	ns	
			t_H	–2.913	–3.098	–3.261	ns	

Table 1–52. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	1.185	1.224	1.243	ns	
			t_H	–0.916	–0.919	–0.901	ns	
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns	
			t_H	–2.925	–3.113	–3.282	ns	
	8 mA	GCLK	t_{SU}	1.185	1.224	1.243	ns	
			t_H	–0.916	–0.919	–0.901	ns	
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns	
			t_H	–2.925	–3.113	–3.282	ns	
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.185	1.224	1.243	ns	
			t_H	–0.916	–0.919	–0.901	ns	
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns	
			t_H	–2.925	–3.113	–3.282	ns	
	3.0-V LVTTTL	4 mA	GCLK	t_{SU}	1.185	1.224	1.243	ns
				t_H	–0.916	–0.919	–0.901	ns
GCLK PLL			t_{SU}	3.194	3.418	3.624	ns	
			t_H	–2.925	–3.113	–3.282	ns	
8 mA		GCLK	t_{SU}	1.185	1.224	1.243	ns	
			t_H	–0.916	–0.919	–0.901	ns	
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns	
			t_H	–2.925	–3.113	–3.282	ns	
12 mA	GCLK	t_{SU}	1.185	1.224	1.243	ns		
		t_H	–0.916	–0.919	–0.901	ns		
	GCLK PLL	t_{SU}	3.194	3.418	3.624	ns		
		t_H	–2.925	–3.113	–3.282	ns		
16 mA	GCLK	t_{SU}	1.185	1.224	1.243	ns		
		t_H	–0.916	–0.919	–0.901	ns		
	GCLK PLL	t_{SU}	3.194	3.418	3.624	ns		
		t_H	–2.925	–3.113	–3.282	ns		

Table 1–52. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.185	1.224	1.243	ns
			t_H	–0.916	–0.919	–0.901	ns
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns
			t_H	–2.925	–3.113	–3.282	ns
	8 mA	GCLK	t_{SU}	1.185	1.224	1.243	ns
			t_H	–0.916	–0.919	–0.901	ns
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns
			t_H	–2.925	–3.113	–3.282	ns
	12 mA	GCLK	t_{SU}	1.185	1.224	1.243	ns
			t_H	–0.916	–0.919	–0.901	ns
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns
			t_H	–2.925	–3.113	–3.282	ns
	16 mA	GCLK	t_{SU}	1.185	1.224	1.243	ns
			t_H	–0.916	–0.919	–0.901	ns
		GCLK PLL	t_{SU}	3.194	3.418	3.624	ns
			t_H	–2.925	–3.113	–3.282	ns
2.5V	4 mA	GCLK	t_{SU}	1.128	1.180	1.214	ns
			t_H	–0.859	–0.876	–0.873	ns
		GCLK PLL	t_{SU}	3.137	3.374	3.595	ns
			t_H	–2.868	–3.070	–3.254	ns
	8 mA	GCLK	t_{SU}	1.128	1.180	1.214	ns
			t_H	–0.859	–0.876	–0.873	ns
		GCLK PLL	t_{SU}	3.137	3.374	3.595	ns
			t_H	–2.868	–3.070	–3.254	ns
	12 mA	GCLK	t_{SU}	1.128	1.180	1.214	ns
			t_H	–0.859	–0.876	–0.873	ns
		GCLK PLL	t_{SU}	3.137	3.374	3.595	ns
			t_H	–2.868	–3.070	–3.254	ns
	16 mA	GCLK	t_{SU}	1.128	1.180	1.214	ns
			t_H	–0.859	–0.876	–0.873	ns
		GCLK PLL	t_{SU}	3.137	3.374	3.595	ns
			t_H	–2.868	–3.070	–3.254	ns

Table 1–52. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	-6	-7	-8	Unit
1.8V	2 mA	GCLK	t_{SU}	1.064	1.141	1.200	ns
			t_H	-0.797	-0.838	-0.858	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns
	4 mA	GCLK	t_{SU}	1.064	1.141	1.200	ns
			t_H	-0.797	-0.838	-0.858	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns
	6 mA	GCLK	t_{SU}	1.064	1.141	1.200	ns
			t_H	-0.797	-0.838	-0.858	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns
	8 mA	GCLK	t_{SU}	1.064	1.141	1.200	ns
			t_H	-0.797	-0.838	-0.858	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns
	10 mA	GCLK	t_{SU}	1.064	1.141	1.200	ns
			t_H	-0.797	-0.838	-0.858	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns
	12 mA	GCLK	t_{SU}	1.064	1.141	1.200	ns
			t_H	-0.797	-0.838	-0.858	ns
		GCLK PLL	t_{SU}	3.063	3.325	3.571	ns
			t_H	-2.796	-3.022	-3.229	ns
16 mA	GCLK	t_{SU}	1.064	1.141	1.200	ns	
		t_H	-0.797	-0.838	-0.858	ns	
	GCLK PLL	t_{SU}	3.063	3.325	3.571	ns	
		t_H	-2.796	-3.022	-3.229	ns	

Table 1–52. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	1.133	1.234	1.318	ns
			t_H	–0.864	–0.929	–0.975	ns
		GCLK PLL	t_{SU}	3.132	3.418	3.689	ns
			t_H	–2.863	–3.113	–3.346	ns
	4 mA	GCLK	t_{SU}	1.133	1.234	1.318	ns
			t_H	–0.864	–0.929	–0.975	ns
		GCLK PLL	t_{SU}	3.132	3.418	3.689	ns
			t_H	–2.863	–3.113	–3.346	ns
	6 mA	GCLK	t_{SU}	1.133	1.234	1.318	ns
			t_H	–0.864	–0.929	–0.975	ns
		GCLK PLL	t_{SU}	3.132	3.418	3.689	ns
			t_H	–2.863	–3.113	–3.346	ns
	8 mA	GCLK	t_{SU}	1.133	1.234	1.318	ns
			t_H	–0.864	–0.929	–0.975	ns
		GCLK PLL	t_{SU}	3.132	3.418	3.689	ns
			t_H	–2.863	–3.113	–3.346	ns
	10 mA	GCLK	t_{SU}	1.133	1.234	1.318	ns
			t_H	–0.864	–0.929	–0.975	ns
		GCLK PLL	t_{SU}	3.132	3.418	3.689	ns
			t_H	–2.863	–3.113	–3.346	ns
	12 mA	GCLK	t_{SU}	1.133	1.234	1.318	ns
			t_H	–0.864	–0.929	–0.975	ns
		GCLK PLL	t_{SU}	3.132	3.418	3.689	ns
			t_H	–2.863	–3.113	–3.346	ns
16 mA	GCLK	t_{SU}	1.133	1.234	1.318	ns	
		t_H	–0.864	–0.929	–0.975	ns	
	GCLK PLL	t_{SU}	3.132	3.418	3.689	ns	
		t_H	–2.863	–3.113	–3.346	ns	

Table 1–52. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.2V	2 mA	GCLK	t_{SU}	1.286	1.414	1.525	ns	
			t_H	–1.015	–1.105	–1.177	ns	
		GCLK PLL	t_{SU}	3.285	3.598	3.896	ns	
			t_H	–3.014	–3.289	–3.548	ns	
	4 mA	GCLK	t_{SU}	1.286	1.414	1.525	ns	
			t_H	–1.015	–1.105	–1.177	ns	
		GCLK PLL	t_{SU}	3.285	3.598	3.896	ns	
			t_H	–3.014	–3.289	–3.548	ns	
	6 mA	GCLK	t_{SU}	1.286	1.414	1.525	ns	
			t_H	–1.015	–1.105	–1.177	ns	
		GCLK PLL	t_{SU}	3.285	3.598	3.896	ns	
			t_H	–3.014	–3.289	–3.548	ns	
	8 mA	GCLK	t_{SU}	1.286	1.414	1.525	ns	
			t_H	–1.015	–1.105	–1.177	ns	
		GCLK PLL	t_{SU}	3.285	3.598	3.896	ns	
			t_H	–3.014	–3.289	–3.548	ns	
	10 mA	GCLK	t_{SU}	1.286	1.414	1.525	ns	
			t_H	–1.015	–1.105	–1.177	ns	
		GCLK PLL	t_{SU}	3.285	3.598	3.896	ns	
			t_H	–3.014	–3.289	–3.548	ns	
	SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.118	1.199	1.252	ns
				t_H	–0.849	–0.894	–0.909	ns
			GCLK PLL	t_{SU}	3.129	3.394	3.643	ns
				t_H	–2.860	–3.089	–3.300	ns
12 mA		GCLK	t_{SU}	1.118	1.199	1.252	ns	
			t_H	–0.849	–0.894	–0.909	ns	
		GCLK PLL	t_{SU}	3.129	3.394	3.643	ns	
			t_H	–2.860	–3.089	–3.300	ns	
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.118	1.199	1.252	ns	
			t_H	–0.849	–0.894	–0.909	ns	
		GCLK PLL	t_{SU}	3.129	3.394	3.643	ns	
			t_H	–2.860	–3.089	–3.300	ns	

Table 1–52. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.180	1.288	1.369	ns
			t_H	–0.911	–0.982	–1.024	ns
		GCLK PLL	t_{SU}	3.181	3.473	3.750	ns
			t_H	–2.912	–3.167	–3.405	ns
	10 mA	GCLK	t_{SU}	1.180	1.288	1.369	ns
			t_H	–0.911	–0.982	–1.024	ns
		GCLK PLL	t_{SU}	3.181	3.473	3.750	ns
			t_H	–2.912	–3.167	–3.405	ns
	12 mA	GCLK	t_{SU}	1.180	1.288	1.369	ns
			t_H	–0.911	–0.982	–1.024	ns
		GCLK PLL	t_{SU}	3.181	3.473	3.750	ns
			t_H	–2.912	–3.167	–3.405	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.180	1.288	1.369	ns
			t_H	–0.911	–0.982	–1.024	ns
		GCLK PLL	t_{SU}	3.181	3.473	3.750	ns
			t_H	–2.912	–3.167	–3.405	ns
	16 mA	GCLK	t_{SU}	1.180	1.288	1.369	ns
			t_H	–0.911	–0.982	–1.024	ns
		GCLK PLL	t_{SU}	3.181	3.473	3.750	ns
			t_H	–2.912	–3.167	–3.405	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.180	1.288	1.369	ns
			t_H	–0.911	–0.982	–1.024	ns
		GCLK PLL	t_{SU}	3.181	3.473	3.750	ns
			t_H	–2.912	–3.167	–3.405	ns
	10 mA	GCLK	t_{SU}	1.180	1.288	1.369	ns
			t_H	–0.911	–0.982	–1.024	ns
		GCLK PLL	t_{SU}	3.181	3.473	3.750	ns
			t_H	–2.912	–3.167	–3.405	ns
	12 mA	GCLK	t_{SU}	1.180	1.288	1.369	ns
			t_H	–0.911	–0.982	–1.024	ns
		GCLK PLL	t_{SU}	3.181	3.473	3.750	ns
			t_H	–2.912	–3.167	–3.405	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.180	1.288	1.369	ns
			t_H	–0.911	–0.982	–1.024	ns
		GCLK PLL	t_{SU}	3.181	3.473	3.750	ns
			t_H	–2.912	–3.167	–3.405	ns

Table 1–52. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit		
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.135	1.247	1.332	ns		
			t_H	–0.866	–0.942	–0.988	ns		
		GCLK PLL	t_{SU}	3.136	3.432	3.713	ns		
			t_H	–2.867	–3.127	–3.369	ns		
		10 mA	GCLK	t_{SU}	1.135	1.247	1.332	ns	
				t_H	–0.866	–0.942	–0.988	ns	
	GCLK PLL		t_{SU}	3.136	3.432	3.713	ns		
			t_H	–2.867	–3.127	–3.369	ns		
	12 mA	GCLK	t_{SU}	1.135	1.247	1.332	ns		
			t_H	–0.866	–0.942	–0.988	ns		
		GCLK PLL	t_{SU}	3.136	3.432	3.713	ns		
			t_H	–2.867	–3.127	–3.369	ns		
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.135	1.247	1.332	ns		
			t_H	–0.866	–0.942	–0.988	ns		
		GCLK PLL	t_{SU}	3.136	3.432	3.713	ns		
			t_H	–2.867	–3.127	–3.369	ns		
		1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.266	1.405	1.517	ns
					t_H	–0.995	–1.096	–1.170	ns
GCLK PLL	t_{SU}			3.267	3.590	3.898	ns		
	t_H			–2.996	–3.281	–3.551	ns		
10 mA	GCLK		t_{SU}	1.266	1.405	1.517	ns		
			t_H	–0.995	–1.096	–1.170	ns		
	GCLK PLL		t_{SU}	3.267	3.590	3.898	ns		
			t_H	–2.996	–3.281	–3.551	ns		
3.0-V PCI	—	GCLK	t_{SU}	1.181	1.220	1.239	ns		
			t_H	–0.912	–0.915	–0.897	ns		
		GCLK PLL	t_{SU}	3.190	3.414	3.620	ns		
			t_H	–2.921	–3.109	–3.278	ns		
		3.0-V PCI-X	—	GCLK	t_{SU}	1.181	1.220	1.239	ns
					t_H	–0.912	–0.915	–0.897	ns
GCLK PLL	t_{SU}			3.190	3.414	3.620	ns		
	t_H			–2.921	–3.109	–3.278	ns		

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{CO}	5.140	5.611	6.127	ns
		GCLK PLL	t_{CO}	3.121	3.406	3.737	ns
	8 mA	GCLK	t_{CO}	4.691	5.142	5.635	ns
		GCLK PLL	t_{CO}	2.672	2.937	3.245	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	4.777	5.233	5.731	ns
		GCLK PLL	t_{CO}	2.758	3.028	3.341	ns
3.0-V LVTTTL	4 mA	GCLK	t_{CO}	4.871	5.315	5.822	ns
		GCLK PLL	t_{CO}	2.852	3.110	3.432	ns
	8 mA	GCLK	t_{CO}	4.613	5.055	5.540	ns
		GCLK PLL	t_{CO}	2.594	2.850	3.150	ns
	12 mA	GCLK	t_{CO}	4.489	4.933	5.419	ns
		GCLK PLL	t_{CO}	2.470	2.728	3.029	ns
	16 mA	GCLK	t_{CO}	4.439	4.868	5.340	ns
		GCLK PLL	t_{CO}	2.420	2.663	2.950	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.611	5.054	5.539	ns
		GCLK PLL	t_{CO}	2.592	2.849	3.149	ns
	8 mA	GCLK	t_{CO}	4.442	4.872	5.355	ns
		GCLK PLL	t_{CO}	2.423	2.667	2.965	ns
	12 mA	GCLK	t_{CO}	4.401	4.831	5.304	ns
		GCLK PLL	t_{CO}	2.382	2.626	2.914	ns
	16 mA	GCLK	t_{CO}	4.381	4.812	5.285	ns
		GCLK PLL	t_{CO}	2.362	2.607	2.895	ns
2.5V	4 mA	GCLK	t_{CO}	4.993	5.453	5.968	ns
		GCLK PLL	t_{CO}	2.974	3.248	3.578	ns
	8 mA	GCLK	t_{CO}	4.721	5.176	5.678	ns
		GCLK PLL	t_{CO}	2.702	2.971	3.288	ns
	12 mA	GCLK	t_{CO}	4.603	5.054	5.554	ns
		GCLK PLL	t_{CO}	2.584	2.849	3.164	ns
16 mA	GCLK	t_{CO}	4.551	4.998	5.494	ns	
	GCLK PLL	t_{CO}	2.532	2.793	3.104	ns	

Table 1–53. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t _{CO}	6.166	6.761	7.433	ns	
		GCLK PLL	t _{CO}	4.147	4.556	5.043	ns	
	4 mA	GCLK	t _{CO}	5.592	6.175	6.821	ns	
		GCLK PLL	t _{CO}	3.573	3.970	4.431	ns	
	6 mA	GCLK	t _{CO}	5.322	5.870	6.480	ns	
		GCLK PLL	t _{CO}	3.303	3.665	4.090	ns	
	8 mA	GCLK	t _{CO}	5.208	5.754	6.351	ns	
		GCLK PLL	t _{CO}	3.189	3.549	3.961	ns	
	10 mA	GCLK	t _{CO}	5.145	5.688	6.287	ns	
		GCLK PLL	t _{CO}	3.126	3.483	3.897	ns	
	12 mA	GCLK	t _{CO}	5.080	5.607	6.193	ns	
		GCLK PLL	t _{CO}	3.061	3.402	3.803	ns	
	16 mA	GCLK	t _{CO}	5.026	5.553	6.130	ns	
		GCLK PLL	t _{CO}	3.007	3.348	3.740	ns	
	1.5V	2 mA	GCLK	t _{CO}	6.574	7.329	8.183	ns
			GCLK PLL	t _{CO}	4.555	5.124	5.793	ns
		4 mA	GCLK	t _{CO}	6.003	6.666	7.423	ns
			GCLK PLL	t _{CO}	3.984	4.461	5.033	ns
6 mA		GCLK	t _{CO}	5.806	6.456	7.200	ns	
		GCLK PLL	t _{CO}	3.787	4.251	4.810	ns	
8 mA		GCLK	t _{CO}	5.688	6.320	7.030	ns	
		GCLK PLL	t _{CO}	3.669	4.115	4.640	ns	
10 mA		GCLK	t _{CO}	5.621	6.250	6.963	ns	
		GCLK PLL	t _{CO}	3.602	4.045	4.573	ns	
12 mA		GCLK	t _{CO}	5.585	6.201	6.903	ns	
		GCLK PLL	t _{CO}	3.566	3.996	4.513	ns	
16 mA		GCLK	t _{CO}	5.467	6.075	6.745	ns	
		GCLK PLL	t _{CO}	3.448	3.870	4.355	ns	
1.2V		2 mA	GCLK	t _{CO}	7.650	8.694	9.917	ns
			GCLK PLL	t _{CO}	5.631	6.489	7.527	ns
		4 mA	GCLK	t _{CO}	7.151	8.117	9.246	ns
			GCLK PLL	t _{CO}	5.132	5.912	6.856	ns
	6 mA	GCLK	t _{CO}	6.970	7.903	8.992	ns	
		GCLK PLL	t _{CO}	4.951	5.698	6.602	ns	
	8 mA	GCLK	t _{CO}	6.887	7.810	8.886	ns	
		GCLK PLL	t _{CO}	4.868	5.605	6.496	ns	
	10 mA	GCLK	t _{CO}	6.742	7.626	8.644	ns	
		GCLK PLL	t _{CO}	4.723	5.421	6.254	ns	
	12 mA	GCLK	t _{CO}	6.716	7.598	8.616	ns	
		GCLK PLL	t _{CO}	4.697	5.393	6.226	ns	

Table 1–53. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.621	5.065	5.555	ns
		GCLK PLL	t_{CO}	2.602	2.860	3.165	ns
	12 mA	GCLK	t_{CO}	4.586	5.029	5.518	ns
		GCLK PLL	t_{CO}	2.567	2.824	3.128	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.529	4.967	5.451	ns
		GCLK PLL	t_{CO}	2.510	2.762	3.061	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.025	5.539	6.107	ns
		GCLK PLL	t_{CO}	3.006	3.334	3.717	ns
	10 mA	GCLK	t_{CO}	4.994	5.501	6.061	ns
		GCLK PLL	t_{CO}	2.975	3.296	3.671	ns
	12 mA	GCLK	t_{CO}	4.979	5.486	6.043	ns
		GCLK PLL	t_{CO}	2.960	3.281	3.653	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	4.966	5.471	6.030	ns
		GCLK PLL	t_{CO}	2.947	3.266	3.640	ns
	16 mA	GCLK	t_{CO}	4.947	5.452	6.010	ns
		GCLK PLL	t_{CO}	2.928	3.247	3.620	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.006	5.511	6.069	ns
		GCLK PLL	t_{CO}	2.987	3.306	3.679	ns
	10 mA	GCLK	t_{CO}	4.997	5.504	6.066	ns
		GCLK PLL	t_{CO}	2.978	3.299	3.676	ns
	12 mA	GCLK	t_{CO}	4.976	5.479	6.035	ns
		GCLK PLL	t_{CO}	2.957	3.274	3.645	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	4.948	5.446	5.999	ns
		GCLK PLL	t_{CO}	2.929	3.241	3.609	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.511	6.106	6.776	ns
		GCLK PLL	t_{CO}	3.492	3.901	4.386	ns
	10 mA	GCLK	t_{CO}	5.498	6.087	6.751	ns
		GCLK PLL	t_{CO}	3.479	3.882	4.361	ns
	12 mA	GCLK	t_{CO}	5.489	6.081	6.747	ns
		GCLK PLL	t_{CO}	3.470	3.876	4.357	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.446	6.028	6.683	ns
		GCLK PLL	t_{CO}	3.427	3.823	4.293	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.682	7.546	8.554	ns
		GCLK PLL	t_{CO}	4.663	5.341	6.164	ns
	10 mA	GCLK	t_{CO}	6.604	7.440	8.399	ns
		GCLK PLL	t_{CO}	4.585	5.235	6.009	ns
	12 mA	GCLK	t_{CO}	6.602	7.440	8.403	ns
		GCLK PLL	t_{CO}	4.583	5.235	6.013	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.545	7.369	8.322	ns
		GCLK PLL	t_{CO}	4.526	5.164	5.932	ns

Table 1–53. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V PCI	—	GCLK	t _{CO}	4.703	5.142	5.623	ns
		GCLK PLL	t _{CO}	2.684	2.937	3.233	ns
3.0-V PCI-X	—	GCLK	t _{CO}	4.703	5.142	5.623	ns
		GCLK PLL	t _{CO}	2.684	2.937	3.233	ns

Table 1–54. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t _{CO}	8.944	9.632	10.374	ns
		GCLK PLL	t _{CO}	6.898	7.399	7.951	ns
	8 mA	GCLK	t _{CO}	6.536	7.048	7.647	ns
		GCLK PLL	t _{CO}	4.490	4.815	5.224	ns
3.3-V LVCMOS	2 mA	GCLK	t _{CO}	7.316	7.864	8.431	ns
		GCLK PLL	t _{CO}	5.270	5.631	6.008	ns
3.0-V LVTTTL	4 mA	GCLK	t _{CO}	7.748	8.309	8.921	ns
		GCLK PLL	t _{CO}	5.702	6.076	6.498	ns
	8 mA	GCLK	t _{CO}	6.192	6.697	7.275	ns
		GCLK PLL	t _{CO}	4.146	4.464	4.852	ns
	12 mA	GCLK	t _{CO}	5.545	6.044	6.580	ns
		GCLK PLL	t _{CO}	3.499	3.811	4.157	ns
	16 mA	GCLK	t _{CO}	5.190	5.646	6.158	ns
		GCLK PLL	t _{CO}	3.144	3.413	3.735	ns
3.0-V LVCMOS	4 mA	GCLK	t _{CO}	6.190	6.695	7.273	ns
		GCLK PLL	t _{CO}	4.144	4.462	4.850	ns
	8 mA	GCLK	t _{CO}	5.219	5.680	6.201	ns
		GCLK PLL	t _{CO}	3.173	3.447	3.778	ns
	12 mA	GCLK	t _{CO}	4.909	5.359	5.851	ns
		GCLK PLL	t _{CO}	2.863	3.126	3.428	ns
	16 mA	GCLK	t _{CO}	4.735	5.177	5.672	ns
		GCLK PLL	t _{CO}	2.689	2.944	3.249	ns
2.5V	4 mA	GCLK	t _{CO}	7.927	8.553	9.244	ns
		GCLK PLL	t _{CO}	5.881	6.320	6.821	ns
	8 mA	GCLK	t _{CO}	6.321	6.866	7.471	ns
		GCLK PLL	t _{CO}	4.275	4.633	5.048	ns
	12 mA	GCLK	t _{CO}	5.672	6.191	6.751	ns
		GCLK PLL	t _{CO}	3.626	3.958	4.328	ns
16 mA	GCLK	t _{CO}	5.368	5.865	6.417	ns	
	GCLK PLL	t _{CO}	3.322	3.632	3.994	ns	

Table 1–54. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t_{CO}	12.170	13.275	14.502	ns	
		GCLK PLL	t_{CO}	10.124	11.042	12.079	ns	
	4 mA	GCLK	t_{CO}	8.780	9.626	10.575	ns	
		GCLK PLL	t_{CO}	6.734	7.393	8.152	ns	
	6 mA	GCLK	t_{CO}	7.459	8.183	8.992	ns	
		GCLK PLL	t_{CO}	5.413	5.950	6.569	ns	
	8 mA	GCLK	t_{CO}	6.799	7.464	8.205	ns	
		GCLK PLL	t_{CO}	4.753	5.231	5.782	ns	
	10 mA	GCLK	t_{CO}	6.450	7.095	7.819	ns	
		GCLK PLL	t_{CO}	4.404	4.862	5.396	ns	
	12 mA	GCLK	t_{CO}	6.147	6.768	7.449	ns	
		GCLK PLL	t_{CO}	4.101	4.535	5.026	ns	
	16 mA	GCLK	t_{CO}	5.841	6.432	7.094	ns	
		GCLK PLL	t_{CO}	3.795	4.199	4.671	ns	
	1.5V	2 mA	GCLK	t_{CO}	11.535	12.824	14.295	ns
			GCLK PLL	t_{CO}	9.489	10.591	11.872	ns
		4 mA	GCLK	t_{CO}	8.479	9.419	10.475	ns
			GCLK PLL	t_{CO}	6.433	7.186	8.052	ns
6 mA		GCLK	t_{CO}	7.464	8.297	9.241	ns	
		GCLK PLL	t_{CO}	5.418	6.064	6.818	ns	
8 mA		GCLK	t_{CO}	6.957	7.726	8.592	ns	
		GCLK PLL	t_{CO}	4.911	5.493	6.169	ns	
10 mA		GCLK	t_{CO}	6.638	7.381	8.210	ns	
		GCLK PLL	t_{CO}	4.592	5.148	5.787	ns	
12 mA		GCLK	t_{CO}	6.436	7.153	7.951	ns	
		GCLK PLL	t_{CO}	4.390	4.920	5.528	ns	
16 mA		GCLK	t_{CO}	6.093	6.765	7.504	ns	
		GCLK PLL	t_{CO}	4.047	4.532	5.081	ns	
1.2V		2 mA	GCLK	t_{CO}	11.740	13.397	15.371	ns
			GCLK PLL	t_{CO}	9.694	11.164	12.948	ns
		4 mA	GCLK	t_{CO}	9.126	10.385	11.872	ns
			GCLK PLL	t_{CO}	7.080	8.152	9.449	ns
	6 mA	GCLK	t_{CO}	8.333	9.467	10.804	ns	
		GCLK PLL	t_{CO}	6.287	7.234	8.381	ns	
	8 mA	GCLK	t_{CO}	7.920	8.993	10.255	ns	
		GCLK PLL	t_{CO}	5.874	6.760	7.832	ns	
	10 mA	GCLK	t_{CO}	7.581	8.585	9.751	ns	
		GCLK PLL	t_{CO}	5.535	6.352	7.328	ns	

Table 1–54. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.618	5.058	5.544	ns
		GCLK PLL	t_{CO}	2.577	2.833	3.133	ns
	12 mA	GCLK	t_{CO}	4.586	5.024	5.508	ns
		GCLK PLL	t_{CO}	2.545	2.799	3.097	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.535	4.971	5.451	ns
		GCLK PLL	t_{CO}	2.494	2.746	3.040	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.025	5.532	6.097	ns
		GCLK PLL	t_{CO}	2.994	3.317	3.696	ns
	10 mA	GCLK	t_{CO}	5.006	5.508	6.067	ns
		GCLK PLL	t_{CO}	2.975	3.293	3.666	ns
	12 mA	GCLK	t_{CO}	4.984	5.484	6.040	ns
		GCLK PLL	t_{CO}	2.953	3.269	3.639	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	4.976	5.476	6.033	ns
		GCLK PLL	t_{CO}	2.945	3.261	3.632	ns
	16 mA	GCLK	t_{CO}	4.961	5.462	6.019	ns
		GCLK PLL	t_{CO}	2.930	3.247	3.618	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.005	5.504	6.058	ns
		GCLK PLL	t_{CO}	2.974	3.289	3.657	ns
	10 mA	GCLK	t_{CO}	4.998	5.500	6.057	ns
		GCLK PLL	t_{CO}	2.967	3.285	3.656	ns
	12 mA	GCLK	t_{CO}	4.988	5.486	6.040	ns
		GCLK PLL	t_{CO}	2.957	3.271	3.639	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	4.955	5.448	5.998	ns
		GCLK PLL	t_{CO}	2.924	3.233	3.597	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.510	6.103	6.766	ns
		GCLK PLL	t_{CO}	3.479	3.888	4.365	ns
	10 mA	GCLK	t_{CO}	5.508	6.098	6.757	ns
		GCLK PLL	t_{CO}	3.477	3.883	4.356	ns
	12 mA	GCLK	t_{CO}	5.499	6.091	6.753	ns
		GCLK PLL	t_{CO}	3.468	3.876	4.352	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.460	6.045	6.700	ns
		GCLK PLL	t_{CO}	3.429	3.830	4.299	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.701	7.568	8.579	ns
		GCLK PLL	t_{CO}	4.670	5.353	6.178	ns
	10 mA	GCLK	t_{CO}	6.618	7.454	8.415	ns
		GCLK PLL	t_{CO}	4.587	5.239	6.014	ns
3.0-V PCI	—	GCLK	t_{CO}	5.097	5.569	6.102	ns
		GCLK PLL	t_{CO}	3.051	3.336	3.679	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.097	5.569	6.102	ns
		GCLK PLL	t_{CO}	3.051	3.336	3.679	ns

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.986	1.069	1.133	ns
			t_H	–0.718	–0.766	–0.793	ns
		GCLK PLL	t_{SU}	3.015	3.284	3.533	ns
			t_H	–2.747	–2.981	–3.193	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.571	5.048	5.552	ns
		GCLK PLL	t_{CO}	4.571	5.048	5.552	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.571	5.048	5.552	ns
		GCLK PLL	t_{CO}	4.571	5.048	5.552	ns
PPDS_E_3R	—	GCLK	t_{CO}	4.571	5.048	5.552	ns
		GCLK PLL	t_{CO}	4.571	5.048	5.552	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.571	5.048	5.552	ns
		GCLK PLL	t_{CO}	4.571	5.048	5.552	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.571	5.048	5.552	ns
		GCLK PLL	t_{CO}	4.571	5.048	5.552	ns

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.991	1.076	1.146	ns
			t_H	–0.724	–0.774	–0.805	ns
			t_{CO}	3.782	4.154	4.553	ns
		GCLK PLL	t_{SU}	3.020	3.293	3.549	ns
			t_H	–2.753	–2.991	–3.208	ns
			t_{CO}	1.743	1.930	2.142	ns
mini-LVDS	—	GCLK	t_{CO}	3.782	4.154	4.553	ns
		GCLK PLL	t_{CO}	1.743	1.930	2.142	ns
PPDS	—	GCLK	t_{CO}	3.782	4.154	4.553	ns
		GCLK PLL	t_{CO}	1.743	1.930	2.142	ns
RSDS	—	GCLK	t_{CO}	3.782	4.154	4.553	ns
		GCLK PLL	t_{CO}	1.743	1.930	2.142	ns

EP3C16 I/O Timing Parameters

Tables 1–57 through 1–62 show the maximum I/O timing parameters for EP3C16 devices.

Table 1–57. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	0.945	0.960	0.966	ns
			t_H	–0.675	–0.655	–0.625	ns
		GCLK PLL	t_{SU}	3.067	3.270	3.453	ns
			t_H	–2.797	–2.965	–3.112	ns
	8 mA	GCLK	t_{SU}	0.945	0.960	0.966	ns
			t_H	–0.675	–0.655	–0.625	ns
		GCLK PLL	t_{SU}	3.067	3.270	3.453	ns
			t_H	–2.797	–2.965	–3.112	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.945	0.960	0.966	ns
			t_H	–0.675	–0.655	–0.625	ns
		GCLK PLL	t_{SU}	3.067	3.270	3.453	ns
			t_H	–2.797	–2.965	–3.112	ns
3.0-V LVTTTL	4 mA	GCLK	t_{SU}	0.945	0.960	0.966	ns
			t_H	–0.675	–0.655	–0.625	ns
		GCLK PLL	t_{SU}	3.067	3.270	3.453	ns
			t_H	–2.797	–2.965	–3.112	ns
	8 mA	GCLK	t_{SU}	0.945	0.960	0.966	ns
			t_H	–0.675	–0.655	–0.625	ns
		GCLK PLL	t_{SU}	3.067	3.270	3.453	ns
			t_H	–2.797	–2.965	–3.112	ns
	12 mA	GCLK	t_{SU}	0.945	0.960	0.966	ns
			t_H	–0.675	–0.655	–0.625	ns
		GCLK PLL	t_{SU}	3.067	3.270	3.453	ns
			t_H	–2.797	–2.965	–3.112	ns
	16 mA	GCLK	t_{SU}	0.945	0.960	0.966	ns
			t_H	–0.675	–0.655	–0.625	ns
		GCLK PLL	t_{SU}	3.067	3.270	3.453	ns
			t_H	–2.797	–2.965	–3.112	ns

Table 1–57. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.945	0.960	0.966	ns
			t_H	–0.675	–0.655	–0.625	ns
		GCLK PLL	t_{SU}	3.067	3.270	3.453	ns
			t_H	–2.797	–2.965	–3.112	ns
	8 mA	GCLK	t_{SU}	0.945	0.960	0.966	ns
			t_H	–0.675	–0.655	–0.625	ns
		GCLK PLL	t_{SU}	3.067	3.270	3.453	ns
			t_H	–2.797	–2.965	–3.112	ns
	12 mA	GCLK	t_{SU}	0.945	0.960	0.966	ns
			t_H	–0.675	–0.655	–0.625	ns
		GCLK PLL	t_{SU}	3.067	3.270	3.453	ns
			t_H	–2.797	–2.965	–3.112	ns
	16 mA	GCLK	t_{SU}	0.945	0.960	0.966	ns
			t_H	–0.675	–0.655	–0.625	ns
		GCLK PLL	t_{SU}	3.067	3.270	3.453	ns
			t_H	–2.797	–2.965	–3.112	ns
2.5V	4 mA	GCLK	t_{SU}	0.888	0.915	0.934	ns
			t_H	–0.618	–0.611	–0.594	ns
		GCLK PLL	t_{SU}	3.010	3.225	3.421	ns
			t_H	–2.740	–2.921	–3.081	ns
	8 mA	GCLK	t_{SU}	0.888	0.915	0.934	ns
			t_H	–0.618	–0.611	–0.594	ns
		GCLK PLL	t_{SU}	3.010	3.225	3.421	ns
			t_H	–2.740	–2.921	–3.081	ns
	12 mA	GCLK	t_{SU}	0.888	0.915	0.934	ns
			t_H	–0.618	–0.611	–0.594	ns
		GCLK PLL	t_{SU}	3.010	3.225	3.421	ns
			t_H	–2.740	–2.921	–3.081	ns
	16 mA	GCLK	t_{SU}	0.888	0.915	0.934	ns
			t_H	–0.618	–0.611	–0.594	ns
		GCLK PLL	t_{SU}	3.010	3.225	3.421	ns
			t_H	–2.740	–2.921	–3.081	ns

Table 1–57. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.8V	2 mA	GCLK	t_{SU}	0.823	0.876	0.921	ns
			t_H	–0.555	–0.573	–0.580	ns
		GCLK PLL	t_{SU}	2.945	3.186	3.408	ns
			t_H	–2.677	–2.883	–3.067	ns
	4 mA	GCLK	t_{SU}	0.823	0.876	0.921	ns
			t_H	–0.555	–0.573	–0.580	ns
		GCLK PLL	t_{SU}	2.945	3.186	3.408	ns
			t_H	–2.677	–2.883	–3.067	ns
	6 mA	GCLK	t_{SU}	0.823	0.876	0.921	ns
			t_H	–0.555	–0.573	–0.580	ns
		GCLK PLL	t_{SU}	2.945	3.186	3.408	ns
			t_H	–2.677	–2.883	–3.067	ns
	8 mA	GCLK	t_{SU}	0.823	0.876	0.921	ns
			t_H	–0.555	–0.573	–0.580	ns
		GCLK PLL	t_{SU}	2.945	3.186	3.408	ns
			t_H	–2.677	–2.883	–3.067	ns
	10 mA	GCLK	t_{SU}	0.823	0.876	0.921	ns
			t_H	–0.555	–0.573	–0.580	ns
		GCLK PLL	t_{SU}	2.945	3.186	3.408	ns
			t_H	–2.677	–2.883	–3.067	ns
	12 mA	GCLK	t_{SU}	0.823	0.876	0.921	ns
			t_H	–0.555	–0.573	–0.580	ns
		GCLK PLL	t_{SU}	2.945	3.186	3.408	ns
			t_H	–2.677	–2.883	–3.067	ns
	16 mA	GCLK	t_{SU}	0.823	0.876	0.921	ns
			t_H	–0.555	–0.573	–0.580	ns
		GCLK PLL	t_{SU}	2.945	3.186	3.408	ns
			t_H	–2.677	–2.883	–3.067	ns

Table 1–57. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	0.892	0.968	1.038	ns
			t_H	–0.622	–0.663	–0.695	ns
		GCLK PLL	t_{SU}	3.014	3.278	3.525	ns
			t_H	–2.744	–2.973	–3.182	ns
	4 mA	GCLK	t_{SU}	0.892	0.968	1.038	ns
			t_H	–0.622	–0.663	–0.695	ns
		GCLK PLL	t_{SU}	3.014	3.278	3.525	ns
			t_H	–2.744	–2.973	–3.182	ns
	6 mA	GCLK	t_{SU}	0.892	0.968	1.038	ns
			t_H	–0.622	–0.663	–0.695	ns
		GCLK PLL	t_{SU}	3.014	3.278	3.525	ns
			t_H	–2.744	–2.973	–3.182	ns
	8 mA	GCLK	t_{SU}	0.892	0.968	1.038	ns
			t_H	–0.622	–0.663	–0.695	ns
		GCLK PLL	t_{SU}	3.014	3.278	3.525	ns
			t_H	–2.744	–2.973	–3.182	ns
	10 mA	GCLK	t_{SU}	0.892	0.968	1.038	ns
			t_H	–0.622	–0.663	–0.695	ns
		GCLK PLL	t_{SU}	3.014	3.278	3.525	ns
			t_H	–2.744	–2.973	–3.182	ns
	12 mA	GCLK	t_{SU}	0.892	0.968	1.038	ns
			t_H	–0.622	–0.663	–0.695	ns
		GCLK PLL	t_{SU}	3.014	3.278	3.525	ns
			t_H	–2.744	–2.973	–3.182	ns
16 mA	GCLK	t_{SU}	0.892	0.968	1.038	ns	
		t_H	–0.622	–0.663	–0.695	ns	
	GCLK PLL	t_{SU}	3.014	3.278	3.525	ns	
		t_H	–2.744	–2.973	–3.182	ns	

Table 1–57. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.2V	2 mA	GCLK	t_{SU}	1.044	1.148	1.244	ns
			t_H	–0.772	–0.839	–0.897	ns
		GCLK PLL	t_{SU}	3.166	3.458	3.731	ns
			t_H	–2.894	–3.149	–3.384	ns
	4 mA	GCLK	t_{SU}	1.044	1.148	1.244	ns
			t_H	–0.772	–0.839	–0.897	ns
		GCLK PLL	t_{SU}	3.166	3.458	3.731	ns
			t_H	–2.894	–3.149	–3.384	ns
	6 mA	GCLK	t_{SU}	1.044	1.148	1.244	ns
			t_H	–0.772	–0.839	–0.897	ns
		GCLK PLL	t_{SU}	3.166	3.458	3.731	ns
			t_H	–2.894	–3.149	–3.384	ns
	8 mA	GCLK	t_{SU}	1.044	1.148	1.244	ns
			t_H	–0.772	–0.839	–0.897	ns
		GCLK PLL	t_{SU}	3.166	3.458	3.731	ns
			t_H	–2.894	–3.149	–3.384	ns
	10 mA	GCLK	t_{SU}	1.044	1.148	1.244	ns
			t_H	–0.772	–0.839	–0.897	ns
		GCLK PLL	t_{SU}	3.166	3.458	3.731	ns
			t_H	–2.894	–3.149	–3.384	ns
	12 mA	GCLK	t_{SU}	1.044	1.148	1.244	ns
			t_H	–0.772	–0.839	–0.897	ns
		GCLK PLL	t_{SU}	3.166	3.458	3.731	ns
			t_H	–2.894	–3.149	–3.384	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.877	0.943	0.973	ns
			t_H	–0.607	–0.639	–0.631	ns
		GCLK PLL	t_{SU}	3.018	3.262	3.468	ns
			t_H	–2.748	–2.958	–3.126	ns
	12 mA	GCLK	t_{SU}	0.877	0.943	0.973	ns
			t_H	–0.607	–0.639	–0.631	ns
		GCLK PLL	t_{SU}	3.018	3.262	3.468	ns
			t_H	–2.748	–2.958	–3.126	ns

Table 1–57. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.877	0.943	0.973	ns
			t_H	–0.607	–0.639	–0.631	ns
		GCLK PLL	t_{SU}	3.018	3.262	3.468	ns
			t_H	–2.748	–2.958	–3.126	ns
	8 mA	GCLK	t_{SU}	0.938	1.032	1.088	ns
			t_H	–0.668	–0.726	–0.744	ns
		GCLK PLL	t_{SU}	3.079	3.351	3.583	ns
			t_H	–2.809	–3.045	–3.239	ns
	10 mA	GCLK	t_{SU}	0.938	1.032	1.088	ns
			t_H	–0.668	–0.726	–0.744	ns
		GCLK PLL	t_{SU}	3.079	3.351	3.583	ns
			t_H	–2.809	–3.045	–3.239	ns
SSTL-18 Class I	12 mA	GCLK	t_{SU}	0.938	1.032	1.088	ns
			t_H	–0.668	–0.726	–0.744	ns
		GCLK PLL	t_{SU}	3.079	3.351	3.583	ns
			t_H	–2.809	–3.045	–3.239	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.938	1.032	1.088	ns
			t_H	–0.668	–0.726	–0.744	ns
		GCLK PLL	t_{SU}	3.079	3.351	3.583	ns
			t_H	–2.809	–3.045	–3.239	ns
	16 mA	GCLK	t_{SU}	0.938	1.032	1.088	ns
			t_H	–0.668	–0.726	–0.744	ns
		GCLK PLL	t_{SU}	3.079	3.351	3.583	ns
			t_H	–2.809	–3.045	–3.239	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.938	1.032	1.088	ns
			t_H	–0.668	–0.726	–0.744	ns
		GCLK PLL	t_{SU}	3.079	3.351	3.583	ns
			t_H	–2.809	–3.045	–3.239	ns
	10 mA	GCLK	t_{SU}	0.938	1.032	1.088	ns
			t_H	–0.668	–0.726	–0.744	ns
		GCLK PLL	t_{SU}	3.079	3.351	3.583	ns
			t_H	–2.809	–3.045	–3.239	ns
	12 mA	GCLK	t_{SU}	0.938	1.032	1.088	ns
			t_H	–0.668	–0.726	–0.744	ns
		GCLK PLL	t_{SU}	3.079	3.351	3.583	ns
			t_H	–2.809	–3.045	–3.239	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.938	1.032	1.088	ns
			t_H	–0.668	–0.726	–0.744	ns
		GCLK PLL	t_{SU}	3.079	3.351	3.583	ns
			t_H	–2.809	–3.045	–3.239	ns

Table 1–57. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.894	0.992	1.054	ns	
			t_H	–0.624	–0.687	–0.711	ns	
		GCLK PLL	t_{SU}	3.035	3.311	3.549	ns	
			t_H	–2.765	–3.006	–3.206	ns	
		10 mA	GCLK	t_{SU}	0.894	0.992	1.054	ns
				t_H	–0.624	–0.687	–0.711	ns
	GCLK PLL		t_{SU}	3.035	3.311	3.549	ns	
			t_H	–2.765	–3.006	–3.206	ns	
	12 mA	GCLK	t_{SU}	0.894	0.992	1.054	ns	
			t_H	–0.624	–0.687	–0.711	ns	
		GCLK PLL	t_{SU}	3.035	3.311	3.549	ns	
			t_H	–2.765	–3.006	–3.206	ns	
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.894	0.992	1.054	ns	
			t_H	–0.624	–0.687	–0.711	ns	
		GCLK PLL	t_{SU}	3.035	3.311	3.549	ns	
			t_H	–2.765	–3.006	–3.206	ns	
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.026	1.151	1.238	ns	
			t_H	–0.754	–0.842	–0.891	ns	
		GCLK PLL	t_{SU}	3.167	3.470	3.733	ns	
			t_H	–2.895	–3.161	–3.386	ns	
		10 mA	GCLK	t_{SU}	1.026	1.151	1.238	ns
				t_H	–0.754	–0.842	–0.891	ns
	GCLK PLL		t_{SU}	3.167	3.470	3.733	ns	
			t_H	–2.895	–3.161	–3.386	ns	
	12 mA	GCLK	t_{SU}	1.026	1.151	1.238	ns	
			t_H	–0.754	–0.842	–0.891	ns	
		GCLK PLL	t_{SU}	3.167	3.470	3.733	ns	
			t_H	–2.895	–3.161	–3.386	ns	
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	1.026	1.151	1.238	ns	
			t_H	–0.754	–0.842	–0.891	ns	
		GCLK PLL	t_{SU}	3.167	3.470	3.733	ns	
			t_H	–2.895	–3.161	–3.386	ns	
3.0-V PCI	—	GCLK	t_{SU}	0.941	0.956	0.961	ns	
			t_H	–0.671	–0.651	–0.620	ns	
		GCLK PLL	t_{SU}	3.063	3.266	3.448	ns	
			t_H	–2.793	–2.961	–3.107	ns	
3.0-V PCI-X	—	GCLK	t_{SU}	0.941	0.956	0.961	ns	
			t_H	–0.671	–0.651	–0.620	ns	
		GCLK PLL	t_{SU}	3.063	3.266	3.448	ns	
			t_H	–2.793	–2.961	–3.107	ns	

Table 1–58. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit		
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	0.963	0.983	0.987	ns		
			t_H	–0.694	–0.678	–0.645	ns		
		GCLK PLL	t_{SU}	3.087	3.296	3.486	ns		
			t_H	–2.818	–2.991	–3.144	ns		
	8 mA	GCLK	t_{SU}	0.963	0.983	0.987	ns		
			t_H	–0.694	–0.678	–0.645	ns		
		GCLK PLL	t_{SU}	3.087	3.296	3.486	ns		
			t_H	–2.818	–2.991	–3.144	ns		
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.963	0.983	0.987	ns		
			t_H	–0.694	–0.678	–0.645	ns		
		GCLK PLL	t_{SU}	3.087	3.296	3.486	ns		
			t_H	–2.818	–2.991	–3.144	ns		
		3.0-V LVTTTL	4 mA	GCLK	t_{SU}	0.963	0.983	0.987	ns
					t_H	–0.694	–0.678	–0.645	ns
GCLK PLL	t_{SU}			3.087	3.296	3.486	ns		
	t_H			–2.818	–2.991	–3.144	ns		
8 mA	GCLK			t_{SU}	0.963	0.983	0.987	ns	
				t_H	–0.694	–0.678	–0.645	ns	
	GCLK PLL		t_{SU}	3.087	3.296	3.486	ns		
			t_H	–2.818	–2.991	–3.144	ns		
12 mA	GCLK		t_{SU}	0.963	0.983	0.987	ns		
			t_H	–0.694	–0.678	–0.645	ns		
	GCLK PLL		t_{SU}	3.087	3.296	3.486	ns		
			t_H	–2.818	–2.991	–3.144	ns		
	16 mA	GCLK	t_{SU}	0.963	0.983	0.987	ns		
			t_H	–0.694	–0.678	–0.645	ns		
GCLK PLL		t_{SU}	3.087	3.296	3.486	ns			
		t_H	–2.818	–2.991	–3.144	ns			

Table 1–58. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.963	0.983	0.987	ns
			t_H	–0.694	–0.678	–0.645	ns
		GCLK PLL	t_{SU}	3.087	3.296	3.486	ns
			t_H	–2.818	–2.991	–3.144	ns
	8 mA	GCLK	t_{SU}	0.963	0.983	0.987	ns
			t_H	–0.694	–0.678	–0.645	ns
		GCLK PLL	t_{SU}	3.087	3.296	3.486	ns
			t_H	–2.818	–2.991	–3.144	ns
	12 mA	GCLK	t_{SU}	0.963	0.983	0.987	ns
			t_H	–0.694	–0.678	–0.645	ns
		GCLK PLL	t_{SU}	3.087	3.296	3.486	ns
			t_H	–2.818	–2.991	–3.144	ns
	16 mA	GCLK	t_{SU}	0.963	0.983	0.987	ns
			t_H	–0.694	–0.678	–0.645	ns
		GCLK PLL	t_{SU}	3.087	3.296	3.486	ns
			t_H	–2.818	–2.991	–3.144	ns
2.5V	4 mA	GCLK	t_{SU}	0.906	0.939	0.958	ns
			t_H	–0.637	–0.635	–0.617	ns
		GCLK PLL	t_{SU}	3.030	3.252	3.457	ns
			t_H	–2.761	–2.948	–3.116	ns
	8 mA	GCLK	t_{SU}	0.906	0.939	0.958	ns
			t_H	–0.637	–0.635	–0.617	ns
		GCLK PLL	t_{SU}	3.030	3.252	3.457	ns
			t_H	–2.761	–2.948	–3.116	ns
	12 mA	GCLK	t_{SU}	0.906	0.939	0.958	ns
			t_H	–0.637	–0.635	–0.617	ns
		GCLK PLL	t_{SU}	3.030	3.252	3.457	ns
			t_H	–2.761	–2.948	–3.116	ns
	16 mA	GCLK	t_{SU}	0.906	0.939	0.958	ns
			t_H	–0.637	–0.635	–0.617	ns
		GCLK PLL	t_{SU}	3.030	3.252	3.457	ns
			t_H	–2.761	–2.948	–3.116	ns

Table 1–58. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.8V	2 mA	GCLK	t_{SU}	0.842	0.900	0.944	ns
			t_H	–0.575	–0.597	–0.602	ns
		GCLK PLL	t_{SU}	2.966	3.213	3.443	ns
			t_H	–2.699	–2.910	–3.101	ns
	4 mA	GCLK	t_{SU}	0.842	0.900	0.944	ns
			t_H	–0.575	–0.597	–0.602	ns
		GCLK PLL	t_{SU}	2.966	3.213	3.443	ns
			t_H	–2.699	–2.910	–3.101	ns
	6 mA	GCLK	t_{SU}	0.842	0.900	0.944	ns
			t_H	–0.575	–0.597	–0.602	ns
		GCLK PLL	t_{SU}	2.966	3.213	3.443	ns
			t_H	–2.699	–2.910	–3.101	ns
	8 mA	GCLK	t_{SU}	0.842	0.900	0.944	ns
			t_H	–0.575	–0.597	–0.602	ns
		GCLK PLL	t_{SU}	2.966	3.213	3.443	ns
			t_H	–2.699	–2.910	–3.101	ns
	10 mA	GCLK	t_{SU}	0.842	0.900	0.944	ns
			t_H	–0.575	–0.597	–0.602	ns
		GCLK PLL	t_{SU}	2.966	3.213	3.443	ns
			t_H	–2.699	–2.910	–3.101	ns
	12 mA	GCLK	t_{SU}	0.842	0.900	0.944	ns
			t_H	–0.575	–0.597	–0.602	ns
		GCLK PLL	t_{SU}	2.966	3.213	3.443	ns
			t_H	–2.699	–2.910	–3.101	ns
16 mA	GCLK	t_{SU}	0.842	0.900	0.944	ns	
		t_H	–0.575	–0.597	–0.602	ns	
	GCLK PLL	t_{SU}	2.966	3.213	3.443	ns	
		t_H	–2.699	–2.910	–3.101	ns	

Table 1–58. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	0.911	0.993	1.062	ns
			t_H	–0.642	–0.688	–0.719	ns
		GCLK PLL	t_{SU}	3.035	3.306	3.561	ns
			t_H	–2.766	–3.001	–3.218	ns
	4 mA	GCLK	t_{SU}	0.911	0.993	1.062	ns
			t_H	–0.642	–0.688	–0.719	ns
		GCLK PLL	t_{SU}	3.035	3.306	3.561	ns
			t_H	–2.766	–3.001	–3.218	ns
	6 mA	GCLK	t_{SU}	0.911	0.993	1.062	ns
			t_H	–0.642	–0.688	–0.719	ns
		GCLK PLL	t_{SU}	3.035	3.306	3.561	ns
			t_H	–2.766	–3.001	–3.218	ns
	8 mA	GCLK	t_{SU}	0.911	0.993	1.062	ns
			t_H	–0.642	–0.688	–0.719	ns
		GCLK PLL	t_{SU}	3.035	3.306	3.561	ns
			t_H	–2.766	–3.001	–3.218	ns
	10 mA	GCLK	t_{SU}	0.911	0.993	1.062	ns
			t_H	–0.642	–0.688	–0.719	ns
		GCLK PLL	t_{SU}	3.035	3.306	3.561	ns
			t_H	–2.766	–3.001	–3.218	ns
	12 mA	GCLK	t_{SU}	0.911	0.993	1.062	ns
			t_H	–0.642	–0.688	–0.719	ns
		GCLK PLL	t_{SU}	3.035	3.306	3.561	ns
			t_H	–2.766	–3.001	–3.218	ns
16 mA	GCLK	t_{SU}	0.911	0.993	1.062	ns	
		t_H	–0.642	–0.688	–0.719	ns	
	GCLK PLL	t_{SU}	3.035	3.306	3.561	ns	
		t_H	–2.766	–3.001	–3.218	ns	

Table 1–58. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.2V	2 mA	GCLK	t_{SU}	1.064	1.173	1.269	ns	
			t_H	–0.793	–0.864	–0.921	ns	
		GCLK PLL	t_{SU}	3.188	3.486	3.768	ns	
			t_H	–2.917	–3.177	–3.420	ns	
	4 mA	GCLK	t_{SU}	1.064	1.173	1.269	ns	
			t_H	–0.793	–0.864	–0.921	ns	
		GCLK PLL	t_{SU}	3.188	3.486	3.768	ns	
			t_H	–2.917	–3.177	–3.420	ns	
	6 mA	GCLK	t_{SU}	1.064	1.173	1.269	ns	
			t_H	–0.793	–0.864	–0.921	ns	
		GCLK PLL	t_{SU}	3.188	3.486	3.768	ns	
			t_H	–2.917	–3.177	–3.420	ns	
	8 mA	GCLK	t_{SU}	1.064	1.173	1.269	ns	
			t_H	–0.793	–0.864	–0.921	ns	
		GCLK PLL	t_{SU}	3.188	3.486	3.768	ns	
			t_H	–2.917	–3.177	–3.420	ns	
	10 mA	GCLK	t_{SU}	1.064	1.173	1.269	ns	
			t_H	–0.793	–0.864	–0.921	ns	
		GCLK PLL	t_{SU}	3.188	3.486	3.768	ns	
			t_H	–2.917	–3.177	–3.420	ns	
	SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.928	0.991	1.016	ns
				t_H	–0.659	–0.686	–0.673	ns
			GCLK PLL	t_{SU}	3.023	3.273	3.505	ns
				t_H	–2.754	–2.968	–3.162	ns
12 mA		GCLK	t_{SU}	0.928	0.991	1.016	ns	
			t_H	–0.659	–0.686	–0.673	ns	
		GCLK PLL	t_{SU}	3.023	3.273	3.505	ns	
			t_H	–2.754	–2.968	–3.162	ns	
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.928	0.991	1.016	ns	
			t_H	–0.659	–0.686	–0.673	ns	
		GCLK PLL	t_{SU}	3.023	3.273	3.505	ns	
			t_H	–2.754	–2.968	–3.162	ns	

Table 1–58. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.978	1.069	1.133	ns
			t_H	–0.709	–0.763	–0.788	ns
		GCLK PLL	t_{SU}	3.085	3.362	3.622	ns
			t_H	–2.816	–3.056	–3.277	ns
	10 mA	GCLK	t_{SU}	0.978	1.069	1.133	ns
			t_H	–0.709	–0.763	–0.788	ns
		GCLK PLL	t_{SU}	3.085	3.362	3.622	ns
			t_H	–2.816	–3.056	–3.277	ns
	12 mA	GCLK	t_{SU}	0.978	1.069	1.133	ns
			t_H	–0.709	–0.763	–0.788	ns
		GCLK PLL	t_{SU}	3.085	3.362	3.622	ns
			t_H	–2.816	–3.056	–3.277	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.978	1.069	1.133	ns
			t_H	–0.709	–0.763	–0.788	ns
		GCLK PLL	t_{SU}	3.085	3.362	3.622	ns
			t_H	–2.816	–3.056	–3.277	ns
	16 mA	GCLK	t_{SU}	0.978	1.069	1.133	ns
			t_H	–0.709	–0.763	–0.788	ns
		GCLK PLL	t_{SU}	3.085	3.362	3.622	ns
			t_H	–2.816	–3.056	–3.277	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.978	1.069	1.133	ns
			t_H	–0.709	–0.763	–0.788	ns
		GCLK PLL	t_{SU}	3.085	3.362	3.622	ns
			t_H	–2.816	–3.056	–3.277	ns
	10 mA	GCLK	t_{SU}	0.978	1.069	1.133	ns
			t_H	–0.709	–0.763	–0.788	ns
		GCLK PLL	t_{SU}	3.085	3.362	3.622	ns
			t_H	–2.816	–3.056	–3.277	ns
	12 mA	GCLK	t_{SU}	0.978	1.069	1.133	ns
			t_H	–0.709	–0.763	–0.788	ns
		GCLK PLL	t_{SU}	3.085	3.362	3.622	ns
			t_H	–2.816	–3.056	–3.277	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.978	1.069	1.133	ns
			t_H	–0.709	–0.763	–0.788	ns
		GCLK PLL	t_{SU}	3.085	3.362	3.622	ns
			t_H	–2.816	–3.056	–3.277	ns

Table 1–58. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.933	1.028	1.096	ns
			t_H	–0.664	–0.723	–0.752	ns
		GCLK PLL	t_{SU}	3.040	3.321	3.585	ns
			t_H	–2.771	–3.016	–3.241	ns
	10 mA	GCLK	t_{SU}	0.933	1.028	1.096	ns
			t_H	–0.664	–0.723	–0.752	ns
		GCLK PLL	t_{SU}	3.040	3.321	3.585	ns
			t_H	–2.771	–3.016	–3.241	ns
	12 mA	GCLK	t_{SU}	0.933	1.028	1.096	ns
			t_H	–0.664	–0.723	–0.752	ns
		GCLK PLL	t_{SU}	3.040	3.321	3.585	ns
			t_H	–2.771	–3.016	–3.241	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.933	1.028	1.096	ns
			t_H	–0.664	–0.723	–0.752	ns
		GCLK PLL	t_{SU}	3.040	3.321	3.585	ns
			t_H	–2.771	–3.016	–3.241	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.064	1.186	1.281	ns
			t_H	–0.793	–0.877	–0.934	ns
		GCLK PLL	t_{SU}	3.171	3.479	3.770	ns
			t_H	–2.900	–3.170	–3.423	ns
	10 mA	GCLK	t_{SU}	1.064	1.186	1.281	ns
			t_H	–0.793	–0.877	–0.934	ns
		GCLK PLL	t_{SU}	3.171	3.479	3.770	ns
			t_H	–2.900	–3.170	–3.423	ns
3.0-V PCI	—	GCLK	t_{SU}	0.959	0.979	0.983	ns
			t_H	–0.690	–0.674	–0.641	ns
		GCLK PLL	t_{SU}	3.083	3.292	3.482	ns
			t_H	–2.814	–2.987	–3.140	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.959	0.979	0.983	ns
			t_H	–0.690	–0.674	–0.641	ns
		GCLK PLL	t_{SU}	3.083	3.292	3.482	ns
			t_H	–2.814	–2.987	–3.140	ns

Table 1–59. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{CO}	5.383	5.883	6.448	ns
		GCLK PLL	t_{CO}	3.282	7.622	8.196	ns
	8 mA	GCLK	t_{CO}	4.934	5.414	5.956	ns
		GCLK PLL	t_{CO}	2.833	5.029	5.464	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.020	5.505	6.052	ns
		GCLK PLL	t_{CO}	2.919	5.826	6.239	ns
3.0-V LVTTTL	4 mA	GCLK	t_{CO}	5.114	5.587	6.143	ns
		GCLK PLL	t_{CO}	3.013	6.282	6.723	ns
	8 mA	GCLK	t_{CO}	4.856	5.327	5.861	ns
		GCLK PLL	t_{CO}	2.755	4.657	5.072	ns
	12 mA	GCLK	t_{CO}	4.732	5.205	5.740	ns
		GCLK PLL	t_{CO}	2.631	4.004	4.370	ns
	16 mA	GCLK	t_{CO}	4.682	5.140	5.661	ns
		GCLK PLL	t_{CO}	2.581	3.600	3.948	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.854	5.326	5.860	ns
		GCLK PLL	t_{CO}	2.753	4.654	5.069	ns
	8 mA	GCLK	t_{CO}	4.685	5.144	5.676	ns
		GCLK PLL	t_{CO}	2.584	3.635	3.994	ns
	12mA	GCLK	t_{CO}	4.644	5.103	5.625	ns
		GCLK PLL	t_{CO}	2.543	3.307	3.633	ns
	16 mA	GCLK	t_{CO}	4.624	5.084	5.606	ns
		GCLK PLL	t_{CO}	2.523	3.126	3.455	ns
2.5V	4 mA	GCLK	t_{CO}	5.236	5.725	6.289	ns
		GCLK PLL	t_{CO}	3.135	6.519	7.042	ns
	8 mA	GCLK	t_{CO}	4.964	5.448	5.999	ns
		GCLK PLL	t_{CO}	2.863	4.825	5.263	ns
	12 mA	GCLK	t_{CO}	4.846	5.326	5.875	ns
		GCLK PLL	t_{CO}	2.745	4.148	4.540	ns
16 mA	GCLK	t_{CO}	4.794	5.270	5.815	ns	
	GCLK PLL	t_{CO}	2.693	3.821	4.207	ns	

Table 1–59. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t_{CO}	6.409	7.033	7.754	ns	
		GCLK PLL	t_{CO}	4.308	11.265	12.331	ns	
	4 mA	GCLK	t_{CO}	5.835	6.447	7.142	ns	
		GCLK PLL	t_{CO}	3.734	7.594	8.382	ns	
	6 mA	GCLK	t_{CO}	5.565	6.142	6.801	ns	
		GCLK PLL	t_{CO}	3.464	6.143	6.788	ns	
	8 mA	GCLK	t_{CO}	5.451	6.026	6.672	ns	
		GCLK PLL	t_{CO}	3.350	5.426	6.002	ns	
	10 mA	GCLK	t_{CO}	5.388	5.960	6.608	ns	
		GCLK PLL	t_{CO}	3.287	5.054	5.614	ns	
	12 mA	GCLK	t_{CO}	5.323	5.879	6.514	ns	
		GCLK PLL	t_{CO}	3.222	4.722	5.239	ns	
	16 mA	GCLK	t_{CO}	5.269	5.825	6.451	ns	
		GCLK PLL	t_{CO}	3.168	4.376	4.869	ns	
	1.5V	2 mA	GCLK	t_{CO}	6.817	7.601	8.504	ns
			GCLK PLL	t_{CO}	4.716	10.807	12.118	ns
		4 mA	GCLK	t_{CO}	6.246	6.938	7.744	ns
			GCLK PLL	t_{CO}	4.145	7.384	8.282	ns
6 mA		GCLK	t_{CO}	6.049	6.728	7.521	ns	
		GCLK PLL	t_{CO}	3.948	6.257	7.040	ns	
8 mA		GCLK	t_{CO}	5.931	6.592	7.351	ns	
		GCLK PLL	t_{CO}	3.830	5.659	6.361	ns	
10 mA		GCLK	t_{CO}	5.864	6.522	7.284	ns	
		GCLK PLL	t_{CO}	3.763	5.317	5.981	ns	
12 mA		GCLK	t_{CO}	5.828	6.473	7.224	ns	
		GCLK PLL	t_{CO}	3.727	5.091	5.726	ns	
16 mA		GCLK	t_{CO}	5.710	6.347	7.066	ns	
		GCLK PLL	t_{CO}	3.609	4.704	5.282	ns	
1.2V		2 mA	GCLK	t_{CO}	7.893	8.966	10.238	ns
			GCLK PLL	t_{CO}	5.792	11.371	13.183	ns
		4 mA	GCLK	t_{CO}	7.394	8.389	9.567	ns
			GCLK PLL	t_{CO}	5.293	8.346	9.670	ns
	6 mA	GCLK	t_{CO}	7.213	8.175	9.313	ns	
		GCLK PLL	t_{CO}	5.112	7.399	8.565	ns	
	8 mA	GCLK	t_{CO}	7.130	8.082	9.207	ns	
		GCLK PLL	t_{CO}	5.029	6.929	8.022	ns	
	10 mA	GCLK	t_{CO}	6.985	7.898	8.965	ns	
		GCLK PLL	t_{CO}	4.884	6.525	7.525	ns	
	12 mA	GCLK	t_{CO}	6.959	7.870	8.937	ns	
		GCLK PLL	t_{CO}	4.858	6.349	7.325	ns	

Table 1–59. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.874	5.346	5.836	ns
		GCLK PLL	t_{CO}	2.772	3.047	3.370	ns
	12 mA	GCLK	t_{CO}	4.839	5.310	5.799	ns
		GCLK PLL	t_{CO}	2.737	3.011	3.333	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.782	5.248	5.732	ns
		GCLK PLL	t_{CO}	2.680	2.949	3.266	ns
	8 mA	GCLK	t_{CO}	5.278	5.820	6.388	ns
		GCLK PLL	t_{CO}	3.176	3.521	3.922	ns
	10 mA	GCLK	t_{CO}	5.247	5.782	6.342	ns
		GCLK PLL	t_{CO}	3.145	3.483	3.876	ns
SSTL-18 Class I	12 mA	GCLK	t_{CO}	5.232	5.767	6.324	ns
		GCLK PLL	t_{CO}	3.130	3.468	3.858	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.219	5.752	6.311	ns
		GCLK PLL	t_{CO}	3.117	3.453	3.845	ns
	16 mA	GCLK	t_{CO}	5.200	5.733	6.291	ns
		GCLK PLL	t_{CO}	3.098	3.434	3.825	ns
1.8-V HSTL Class I	8mA	GCLK	t_{CO}	5.259	5.792	6.350	ns
		GCLK PLL	t_{CO}	3.157	3.493	3.884	ns
	10mA	GCLK	t_{CO}	5.250	5.785	6.347	ns
		GCLK PLL	t_{CO}	3.148	3.486	3.881	ns
	12 mA	GCLK	t_{CO}	5.229	5.760	6.316	ns
		GCLK PLL	t_{CO}	3.127	3.461	3.850	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.201	5.727	6.280	ns
		GCLK PLL	t_{CO}	3.099	3.428	3.814	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.764	6.387	7.057	ns
		GCLK PLL	t_{CO}	3.662	4.088	4.591	ns
	10 mA	GCLK	t_{CO}	5.751	6.368	7.032	ns
		GCLK PLL	t_{CO}	3.649	4.069	4.566	ns
	12 mA	GCLK	t_{CO}	5.742	6.362	7.028	ns
		GCLK PLL	t_{CO}	3.640	4.063	4.562	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.699	6.309	6.964	ns
		GCLK PLL	t_{CO}	3.597	4.010	4.498	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.935	7.827	8.835	ns
		GCLK PLL	t_{CO}	4.833	5.528	6.369	ns
	10 mA	GCLK	t_{CO}	6.857	7.721	8.680	ns
		GCLK PLL	t_{CO}	4.755	5.422	6.214	ns
	12 mA	GCLK	t_{CO}	6.855	7.721	8.684	ns
		GCLK PLL	t_{CO}	4.753	5.422	6.218	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.798	7.650	8.603	ns
		GCLK PLL	t_{CO}	4.696	5.351	6.137	ns

Table 1–59. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V PCI	—	GCLK	t_{CO}	4.946	5.414	5.944	ns
		GCLK PLL	t_{CO}	2.845	3.537	3.906	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.946	5.414	5.944	ns
		GCLK PLL	t_{CO}	2.845	3.537	3.906	ns

Table 1–60. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{CO}	5.333	5.821	6.345	ns
		GCLK PLL	t_{CO}	3.215	3.514	3.876	ns
	8 mA	GCLK	t_{CO}	4.885	5.357	5.863	ns
		GCLK PLL	t_{CO}	2.767	3.050	3.394	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	4.979	5.444	5.954	ns
		GCLK PLL	t_{CO}	2.861	3.137	3.485	ns
3.0-V LVTTTL	4 mA	GCLK	t_{CO}	5.084	5.542	6.045	ns
		GCLK PLL	t_{CO}	2.966	3.235	3.576	ns
	8 mA	GCLK	t_{CO}	4.828	5.287	5.784	ns
		GCLK PLL	t_{CO}	2.710	2.980	3.315	ns
	12 mA	GCLK	t_{CO}	4.713	5.161	5.657	ns
		GCLK PLL	t_{CO}	2.595	2.854	3.188	ns
	16 mA	GCLK	t_{CO}	4.663	5.107	5.590	ns
		GCLK PLL	t_{CO}	2.545	2.800	3.121	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.826	5.286	5.782	ns
		GCLK PLL	t_{CO}	2.708	2.979	3.313	ns
	8 mA	GCLK	t_{CO}	4.664	5.109	5.593	ns
		GCLK PLL	t_{CO}	2.546	2.802	3.124	ns
	12 mA	GCLK	t_{CO}	4.624	5.069	5.554	ns
		GCLK PLL	t_{CO}	2.506	2.762	3.085	ns
	16 mA	GCLK	t_{CO}	4.603	5.049	5.534	ns
		GCLK PLL	t_{CO}	2.485	2.742	3.065	ns
2.5V	4 mA	GCLK	t_{CO}	5.210	5.681	6.201	ns
		GCLK PLL	t_{CO}	3.092	3.374	3.732	ns
	8 mA	GCLK	t_{CO}	4.941	5.412	5.925	ns
		GCLK PLL	t_{CO}	2.823	3.105	3.456	ns
	12 mA	GCLK	t_{CO}	4.827	5.292	5.801	ns
		GCLK PLL	t_{CO}	2.709	2.985	3.332	ns
16 mA	GCLK	t_{CO}	4.774	5.236	5.743	ns	
	GCLK PLL	t_{CO}	2.656	2.929	3.274	ns	

Table 1–60. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t_{CO}	6.360	6.969	7.648	ns	
		GCLK PLL	t_{CO}	4.242	4.662	5.179	ns	
	4 mA	GCLK	t_{CO}	5.805	6.399	7.056	ns	
		GCLK PLL	t_{CO}	3.687	4.092	4.587	ns	
	6 mA	GCLK	t_{CO}	5.543	6.104	6.724	ns	
		GCLK PLL	t_{CO}	3.425	3.797	4.255	ns	
	8 mA	GCLK	t_{CO}	5.427	5.976	6.579	ns	
		GCLK PLL	t_{CO}	3.309	3.669	4.110	ns	
	10 mA	GCLK	t_{CO}	5.366	5.922	6.532	ns	
		GCLK PLL	t_{CO}	3.248	3.615	4.063	ns	
	12 mA	GCLK	t_{CO}	5.306	5.846	6.443	ns	
		GCLK PLL	t_{CO}	3.188	3.539	3.974	ns	
	16 mA	GCLK	t_{CO}	5.262	5.797	6.388	ns	
		GCLK PLL	t_{CO}	3.144	3.490	3.919	ns	
	1.5V	2 mA	GCLK	t_{CO}	6.774	7.540	8.400	ns
			GCLK PLL	t_{CO}	4.656	5.233	5.931	ns
		4 mA	GCLK	t_{CO}	6.215	6.897	7.658	ns
			GCLK PLL	t_{CO}	4.097	4.590	5.189	ns
6 mA		GCLK	t_{CO}	6.025	6.692	7.442	ns	
		GCLK PLL	t_{CO}	3.907	4.385	4.973	ns	
8 mA		GCLK	t_{CO}	5.927	6.581	7.302	ns	
		GCLK PLL	t_{CO}	3.809	4.274	4.833	ns	
10 mA		GCLK	t_{CO}	5.860	6.509	7.233	ns	
		GCLK PLL	t_{CO}	3.742	4.202	4.764	ns	
12 mA		GCLK	t_{CO}	5.820	6.458	7.169	ns	
		GCLK PLL	t_{CO}	3.702	4.151	4.700	ns	
16 mA		GCLK	t_{CO}	5.748	6.377	7.081	ns	
		GCLK PLL	t_{CO}	3.630	4.070	4.612	ns	
1.2V		2 mA	GCLK	t_{CO}	7.860	8.915	10.146	ns
			GCLK PLL	t_{CO}	5.742	6.608	7.677	ns
		4 mA	GCLK	t_{CO}	7.369	8.349	9.487	ns
			GCLK PLL	t_{CO}	5.251	6.042	7.018	ns
	6 mA	GCLK	t_{CO}	7.214	8.165	9.272	ns	
		GCLK PLL	t_{CO}	5.096	5.858	6.803	ns	
	8 mA	GCLK	t_{CO}	7.126	8.067	9.159	ns	
		GCLK PLL	t_{CO}	5.008	5.760	6.690	ns	
	10 mA	GCLK	t_{CO}	7.008	7.923	8.980	ns	
		GCLK PLL	t_{CO}	4.890	5.616	6.511	ns	

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.855	5.314	5.800	ns
		GCLK PLL	t_{CO}	2.718	3.004	3.286	ns
	12 mA	GCLK	t_{CO}	4.823	5.280	5.764	ns
		GCLK PLL	t_{CO}	2.686	2.970	3.250	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.772	5.227	5.707	ns
		GCLK PLL	t_{CO}	2.635	2.917	3.193	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.262	5.788	6.353	ns
		GCLK PLL	t_{CO}	3.125	3.478	3.839	ns
	10 mA	GCLK	t_{CO}	5.243	5.764	6.323	ns
		GCLK PLL	t_{CO}	3.106	3.454	3.809	ns
	12 mA	GCLK	t_{CO}	5.221	5.740	6.296	ns
		GCLK PLL	t_{CO}	3.084	3.430	3.782	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.213	5.732	6.289	ns
		GCLK PLL	t_{CO}	3.076	3.422	3.775	ns
	16 mA	GCLK	t_{CO}	5.198	5.718	6.275	ns
		GCLK PLL	t_{CO}	3.061	3.408	3.761	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.242	5.760	6.314	ns
		GCLK PLL	t_{CO}	3.105	3.450	3.800	ns
	10 mA	GCLK	t_{CO}	5.235	5.756	6.313	ns
		GCLK PLL	t_{CO}	3.098	3.446	3.799	ns
	12 mA	GCLK	t_{CO}	5.225	5.742	6.296	ns
		GCLK PLL	t_{CO}	3.088	3.432	3.782	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.192	5.704	6.254	ns
		GCLK PLL	t_{CO}	3.055	3.394	3.740	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.747	6.359	7.022	ns
		GCLK PLL	t_{CO}	3.610	4.049	4.508	ns
	10 mA	GCLK	t_{CO}	5.745	6.354	7.013	ns
		GCLK PLL	t_{CO}	3.608	4.044	4.499	ns
	12 mA	GCLK	t_{CO}	5.736	6.347	7.009	ns
		GCLK PLL	t_{CO}	3.599	4.037	4.495	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.697	6.301	6.956	ns
		GCLK PLL	t_{CO}	3.560	3.991	4.442	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.938	7.824	8.835	ns
		GCLK PLL	t_{CO}	4.801	5.514	6.321	ns
	10 mA	GCLK	t_{CO}	6.855	7.710	8.671	ns
		GCLK PLL	t_{CO}	4.718	5.400	6.157	ns
3.0-V PCI	—	GCLK	t_{CO}	4.922	5.374	5.866	ns
		GCLK PLL	t_{CO}	2.804	3.067	3.397	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.922	5.374	5.866	ns
		GCLK PLL	t_{CO}	2.804	3.067	3.397	ns

Table 1–61. EP3C16 Column Pin Differential I/O Timing Parameters

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.772	0.837	0.881	ns
			t_H	–0.504	–0.534	–0.541	ns
		GCLK PLL	t_{SU}	2.913	3.166	3.397	ns
			t_H	–2.645	–2.863	–3.057	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.815	5.311	5.834	ns
		GCLK PLL	t_{CO}	4.825	5.321	5.844	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.815	5.311	5.834	ns
		GCLK PLL	t_{CO}	4.825	5.321	5.844	ns
PPDS_E_3R	—	GCLK	t_{CO}	4.815	5.311	5.834	ns
		GCLK PLL	t_{CO}	4.825	5.321	5.844	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.815	5.311	5.834	ns
		GCLK PLL	t_{CO}	4.825	5.321	5.844	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.815	5.311	5.834	ns
		GCLK PLL	t_{CO}	4.825	5.321	5.844	ns

Table 1–62. EP3C16 Row Pin Differential I/O Timing Parameters

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.785	0.855	0.909	ns
			t_H	–0.518	–0.553	–0.568	ns
			t_{CO}	4.033	4.423	4.835	ns
		GCLK PLL	t_{SU}	2.917	3.175	3.415	ns
			t_H	–2.650	–2.873	–3.074	ns
			t_{CO}	1.888	2.092	2.322	ns
mini-LVDS	—	GCLK	t_{CO}	4.033	4.423	4.835	ns
		GCLK PLL	t_{CO}	1.888	2.092	2.322	ns
PPDS	—	GCLK	t_{CO}	4.033	4.423	4.835	ns
		GCLK PLL	t_{CO}	1.888	2.092	2.322	ns
RSDS	—	GCLK	t_{CO}	4.033	4.423	4.835	ns
		GCLK PLL	t_{CO}	1.888	2.092	2.322	ns

EP3C25 I/O Timing Parameters

Tables 1–63 through 1–68 show the maximum I/O timing parameters for EP3C25 devices.

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	0.907	0.920	0.911	ns
			t_H	–0.637	–0.615	–0.570	ns
		GCLK PLL	t_{SU}	3.084	3.298	3.493	ns
			t_H	–2.814	–2.993	–3.152	ns
	8 mA	GCLK	t_{SU}	0.907	0.920	0.911	ns
			t_H	–0.637	–0.615	–0.570	ns
		GCLK PLL	t_{SU}	3.084	3.298	3.493	ns
			t_H	–2.814	–2.993	–3.152	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.907	0.920	0.911	ns
			t_H	–0.637	–0.615	–0.570	ns
		GCLK PLL	t_{SU}	3.084	3.298	3.493	ns
			t_H	–2.814	–2.993	–3.152	ns
3.0-V LVTTTL	4 mA	GCLK	t_{SU}	0.907	0.920	0.911	ns
			t_H	–0.637	–0.615	–0.570	ns
		GCLK PLL	t_{SU}	3.084	3.298	3.493	ns
			t_H	–2.814	–2.993	–3.152	ns
	8 mA	GCLK	t_{SU}	0.907	0.920	0.911	ns
			t_H	–0.637	–0.615	–0.570	ns
		GCLK PLL	t_{SU}	3.084	3.298	3.493	ns
			t_H	–2.814	–2.993	–3.152	ns
	12 mA	GCLK	t_{SU}	0.907	0.920	0.911	ns
			t_H	–0.637	–0.615	–0.570	ns
		GCLK PLL	t_{SU}	3.084	3.298	3.493	ns
			t_H	–2.814	–2.993	–3.152	ns
	16 mA	GCLK	t_{SU}	0.907	0.920	0.911	ns
			t_H	–0.637	–0.615	–0.570	ns
		GCLK PLL	t_{SU}	3.084	3.298	3.493	ns
			t_H	–2.814	–2.993	–3.152	ns

Table 1–63. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.907	0.920	0.911	ns
			t_H	–0.637	–0.615	–0.570	ns
		GCLK PLL	t_{SU}	3.084	3.298	3.493	ns
			t_H	–2.814	–2.993	–3.152	ns
	8 mA	GCLK	t_{SU}	0.907	0.920	0.911	ns
			t_H	–0.637	–0.615	–0.570	ns
		GCLK PLL	t_{SU}	3.084	3.298	3.493	ns
			t_H	–2.814	–2.993	–3.152	ns
	12 mA	GCLK	t_{SU}	0.907	0.920	0.911	ns
			t_H	–0.637	–0.615	–0.570	ns
		GCLK PLL	t_{SU}	3.084	3.298	3.493	ns
			t_H	–2.814	–2.993	–3.152	ns
	16 mA	GCLK	t_{SU}	0.907	0.920	0.911	ns
			t_H	–0.637	–0.615	–0.570	ns
		GCLK PLL	t_{SU}	3.084	3.298	3.493	ns
			t_H	–2.814	–2.993	–3.152	ns
2.5V	4 mA	GCLK	t_{SU}	0.850	0.875	0.879	ns
			t_H	–0.580	–0.571	–0.539	ns
		GCLK PLL	t_{SU}	3.027	3.253	3.461	ns
			t_H	–2.757	–2.949	–3.121	ns
	8 mA	GCLK	t_{SU}	0.850	0.875	0.879	ns
			t_H	–0.580	–0.571	–0.539	ns
		GCLK PLL	t_{SU}	3.027	3.253	3.461	ns
			t_H	–2.757	–2.949	–3.121	ns
	12 mA	GCLK	t_{SU}	0.850	0.875	0.879	ns
			t_H	–0.580	–0.571	–0.539	ns
		GCLK PLL	t_{SU}	3.027	3.253	3.461	ns
			t_H	–2.757	–2.949	–3.121	ns
	16 mA	GCLK	t_{SU}	0.850	0.875	0.879	ns
			t_H	–0.580	–0.571	–0.539	ns
		GCLK PLL	t_{SU}	3.027	3.253	3.461	ns
			t_H	–2.757	–2.949	–3.121	ns

Table 1–63. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.8V	2 mA	GCLK	t_{SU}	0.785	0.836	0.866	ns
			t_H	–0.517	–0.533	–0.525	ns
		GCLK PLL	t_{SU}	2.962	3.214	3.448	ns
			t_H	–2.694	–2.911	–3.107	ns
	4 mA	GCLK	t_{SU}	0.785	0.836	0.866	ns
			t_H	–0.517	–0.533	–0.525	ns
		GCLK PLL	t_{SU}	2.962	3.214	3.448	ns
			t_H	–2.694	–2.911	–3.107	ns
	6 mA	GCLK	t_{SU}	0.785	0.836	0.866	ns
			t_H	–0.517	–0.533	–0.525	ns
		GCLK PLL	t_{SU}	2.962	3.214	3.448	ns
			t_H	–2.694	–2.911	–3.107	ns
	8 mA	GCLK	t_{SU}	0.785	0.836	0.866	ns
			t_H	–0.517	–0.533	–0.525	ns
		GCLK PLL	t_{SU}	2.962	3.214	3.448	ns
			t_H	–2.694	–2.911	–3.107	ns
	10 mA	GCLK	t_{SU}	0.785	0.836	0.866	ns
			t_H	–0.517	–0.533	–0.525	ns
		GCLK PLL	t_{SU}	2.962	3.214	3.448	ns
			t_H	–2.694	–2.911	–3.107	ns
	12 mA	GCLK	t_{SU}	0.785	0.836	0.866	ns
			t_H	–0.517	–0.533	–0.525	ns
		GCLK PLL	t_{SU}	2.962	3.214	3.448	ns
			t_H	–2.694	–2.911	–3.107	ns
16 mA	GCLK	t_{SU}	0.785	0.836	0.866	ns	
		t_H	–0.517	–0.533	–0.525	ns	
	GCLK PLL	t_{SU}	2.962	3.214	3.448	ns	
		t_H	–2.694	–2.911	–3.107	ns	

Table 1–63. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	0.854	0.928	0.983	ns
			t_H	–0.584	–0.623	–0.640	ns
		GCLK PLL	t_{SU}	3.031	3.306	3.565	ns
			t_H	–2.761	–3.001	–3.222	ns
	4 mA	GCLK	t_{SU}	0.854	0.928	0.983	ns
			t_H	–0.584	–0.623	–0.640	ns
		GCLK PLL	t_{SU}	3.031	3.306	3.565	ns
			t_H	–2.761	–3.001	–3.222	ns
	6 mA	GCLK	t_{SU}	0.854	0.928	0.983	ns
			t_H	–0.584	–0.623	–0.640	ns
		GCLK PLL	t_{SU}	3.031	3.306	3.565	ns
			t_H	–2.761	–3.001	–3.222	ns
	8 mA	GCLK	t_{SU}	0.854	0.928	0.983	ns
			t_H	–0.584	–0.623	–0.640	ns
		GCLK PLL	t_{SU}	3.031	3.306	3.565	ns
			t_H	–2.761	–3.001	–3.222	ns
	10 mA	GCLK	t_{SU}	0.854	0.928	0.983	ns
			t_H	–0.584	–0.623	–0.640	ns
		GCLK PLL	t_{SU}	3.031	3.306	3.565	ns
			t_H	–2.761	–3.001	–3.222	ns
	12 mA	GCLK	t_{SU}	0.854	0.928	0.983	ns
			t_H	–0.584	–0.623	–0.640	ns
		GCLK PLL	t_{SU}	3.031	3.306	3.565	ns
			t_H	–2.761	–3.001	–3.222	ns
16 mA	GCLK	t_{SU}	0.854	0.928	0.983	ns	
		t_H	–0.584	–0.623	–0.640	ns	
	GCLK PLL	t_{SU}	3.031	3.306	3.565	ns	
		t_H	–2.761	–3.001	–3.222	ns	

Table 1–63. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.2V	2 mA	GCLK	t_{SU}	1.006	1.108	1.189	ns
			t_H	–0.734	–0.799	–0.842	ns
		GCLK PLL	t_{SU}	3.183	3.486	3.771	ns
			t_H	–2.911	–3.177	–3.424	ns
	4 mA	GCLK	t_{SU}	1.006	1.108	1.189	ns
			t_H	–0.734	–0.799	–0.842	ns
		GCLK PLL	t_{SU}	3.183	3.486	3.771	ns
			t_H	–2.911	–3.177	–3.424	ns
	6 mA	GCLK	t_{SU}	1.006	1.108	1.189	ns
			t_H	–0.734	–0.799	–0.842	ns
		GCLK PLL	t_{SU}	3.183	3.486	3.771	ns
			t_H	–2.911	–3.177	–3.424	ns
	8 mA	GCLK	t_{SU}	1.006	1.108	1.189	ns
			t_H	–0.734	–0.799	–0.842	ns
		GCLK PLL	t_{SU}	3.183	3.486	3.771	ns
			t_H	–2.911	–3.177	–3.424	ns
	10 mA	GCLK	t_{SU}	1.006	1.108	1.189	ns
			t_H	–0.734	–0.799	–0.842	ns
		GCLK PLL	t_{SU}	3.183	3.486	3.771	ns
			t_H	–2.911	–3.177	–3.424	ns
	12 mA	GCLK	t_{SU}	1.006	1.108	1.189	ns
			t_H	–0.734	–0.799	–0.842	ns
		GCLK PLL	t_{SU}	3.183	3.486	3.771	ns
			t_H	–2.911	–3.177	–3.424	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.836	0.890	0.931	ns
			t_H	–0.566	–0.586	–0.589	ns
		GCLK PLL	t_{SU}	3.019	3.278	3.513	ns
			t_H	–2.749	–2.974	–3.171	ns
	12 mA	GCLK	t_{SU}	0.836	0.890	0.931	ns
			t_H	–0.566	–0.586	–0.589	ns
		GCLK PLL	t_{SU}	3.019	3.278	3.513	ns
			t_H	–2.749	–2.974	–3.171	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.836	0.890	0.931	ns
			t_H	–0.566	–0.586	–0.589	ns
		GCLK PLL	t_{SU}	3.019	3.278	3.513	ns
			t_H	–2.749	–2.974	–3.171	ns

Table 1–63. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.897	0.979	1.046	ns
			t_H	–0.627	–0.673	–0.702	ns
		GCLK PLL	t_{SU}	3.080	3.367	3.628	ns
			t_H	–2.810	–3.061	–3.284	ns
	10 mA	GCLK	t_{SU}	0.897	0.979	1.046	ns
			t_H	–0.627	–0.673	–0.702	ns
		GCLK PLL	t_{SU}	3.080	3.367	3.628	ns
			t_H	–2.810	–3.061	–3.284	ns
	12 mA	GCLK	t_{SU}	0.897	0.979	1.046	ns
			t_H	–0.627	–0.673	–0.702	ns
		GCLK PLL	t_{SU}	3.080	3.367	3.628	ns
			t_H	–2.810	–3.061	–3.284	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.897	0.979	1.046	ns
			t_H	–0.627	–0.673	–0.702	ns
		GCLK PLL	t_{SU}	3.080	3.367	3.628	ns
			t_H	–2.810	–3.061	–3.284	ns
	16 mA	GCLK	t_{SU}	0.897	0.979	1.046	ns
			t_H	–0.627	–0.673	–0.702	ns
		GCLK PLL	t_{SU}	3.080	3.367	3.628	ns
			t_H	–2.810	–3.061	–3.284	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.897	0.979	1.046	ns
			t_H	–0.627	–0.673	–0.702	ns
		GCLK PLL	t_{SU}	3.080	3.367	3.628	ns
			t_H	–2.810	–3.061	–3.284	ns
	10 mA	GCLK	t_{SU}	0.897	0.979	1.046	ns
			t_H	–0.627	–0.673	–0.702	ns
		GCLK PLL	t_{SU}	3.080	3.367	3.628	ns
			t_H	–2.810	–3.061	–3.284	ns
	12 mA	GCLK	t_{SU}	0.897	0.979	1.046	ns
			t_H	–0.627	–0.673	–0.702	ns
		GCLK PLL	t_{SU}	3.080	3.367	3.628	ns
			t_H	–2.810	–3.061	–3.284	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.897	0.979	1.046	ns
			t_H	–0.627	–0.673	–0.702	ns
		GCLK PLL	t_{SU}	3.080	3.367	3.628	ns
			t_H	–2.810	–3.061	–3.284	ns

Table 1–63. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit		
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.853	0.939	1.012	ns		
			t_H	–0.583	–0.634	–0.669	ns		
		GCLK PLL	t_{SU}	3.036	3.327	3.594	ns		
			t_H	–2.766	–3.022	–3.251	ns		
		10 mA	GCLK	t_{SU}	0.853	0.939	1.012	ns	
				t_H	–0.583	–0.634	–0.669	ns	
	GCLK PLL	t_{SU}	3.036	3.327	3.594	ns			
		t_H	–2.766	–3.022	–3.251	ns			
	12 mA	GCLK	t_{SU}	0.853	0.939	1.012	ns		
			t_H	–0.583	–0.634	–0.669	ns		
		GCLK PLL	t_{SU}	3.036	3.327	3.594	ns		
			t_H	–2.766	–3.022	–3.251	ns		
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.853	0.939	1.012	ns		
			t_H	–0.583	–0.634	–0.669	ns		
		GCLK PLL	t_{SU}	3.036	3.327	3.594	ns		
			t_H	–2.766	–3.022	–3.251	ns		
		1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.985	1.098	1.196	ns
					t_H	–0.713	–0.789	–0.849	ns
GCLK PLL	t_{SU}			3.168	3.486	3.778	ns		
	t_H			–2.896	–3.177	–3.431	ns		
10 mA	GCLK			t_{SU}	0.985	1.098	1.196	ns	
				t_H	–0.713	–0.789	–0.849	ns	
GCLK PLL	t_{SU}		3.168	3.486	3.778	ns			
	t_H		–2.896	–3.177	–3.431	ns			
12 mA	GCLK		t_{SU}	0.985	1.098	1.196	ns		
			t_H	–0.713	–0.789	–0.849	ns		
	GCLK PLL		t_{SU}	3.168	3.486	3.778	ns		
			t_H	–2.896	–3.177	–3.431	ns		
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	0.985	1.098	1.196	ns		
			t_H	–0.713	–0.789	–0.849	ns		
		GCLK PLL	t_{SU}	3.168	3.486	3.778	ns		
			t_H	–2.896	–3.177	–3.431	ns		
		3.0-V PCI	—	GCLK	t_{SU}	0.903	0.916	0.906	ns
					t_H	–0.633	–0.611	–0.565	ns
GCLK PLL	t_{SU}			3.080	3.294	3.488	ns		
	t_H			–2.810	–2.989	–3.147	ns		
3.0-V PCI-X	—	GCLK	t_{SU}	0.903	0.916	0.906	ns		
			t_H	–0.633	–0.611	–0.565	ns		
		GCLK PLL	t_{SU}	3.080	3.294	3.488	ns		
			t_H	–2.810	–2.989	–3.147	ns		

Table 1–64. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit		
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	0.936	0.958	0.955	ns		
			t_H	–0.667	–0.653	–0.613	ns		
		GCLK PLL	t_{SU}	3.113	3.328	3.522	ns		
			t_H	–2.844	–3.023	–3.180	ns		
	8 mA	GCLK	t_{SU}	0.936	0.958	0.955	ns		
			t_H	–0.667	–0.653	–0.613	ns		
		GCLK PLL	t_{SU}	3.113	3.328	3.522	ns		
			t_H	–2.844	–3.023	–3.180	ns		
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.936	0.958	0.955	ns		
			t_H	–0.667	–0.653	–0.613	ns		
		GCLK PLL	t_{SU}	3.113	3.328	3.522	ns		
			t_H	–2.844	–3.023	–3.180	ns		
		3.0-V LVTTTL	4 mA	GCLK	t_{SU}	0.936	0.958	0.955	ns
					t_H	–0.667	–0.653	–0.613	ns
GCLK PLL	t_{SU}			3.113	3.328	3.522	ns		
	t_H			–2.844	–3.023	–3.180	ns		
8 mA	GCLK		t_{SU}	0.936	0.958	0.955	ns		
			t_H	–0.667	–0.653	–0.613	ns		
	GCLK PLL		t_{SU}	3.113	3.328	3.522	ns		
			t_H	–2.844	–3.023	–3.180	ns		
12 mA	GCLK		t_{SU}	0.936	0.958	0.955	ns		
			t_H	–0.667	–0.653	–0.613	ns		
	GCLK PLL		t_{SU}	3.113	3.328	3.522	ns		
			t_H	–2.844	–3.023	–3.180	ns		
16 mA	GCLK	t_{SU}	0.936	0.958	0.955	ns			
		t_H	–0.667	–0.653	–0.613	ns			
	GCLK PLL	t_{SU}	3.113	3.328	3.522	ns			
		t_H	–2.844	–3.023	–3.180	ns			

Table 1–64. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.936	0.958	0.955	ns
			t_H	–0.667	–0.653	–0.613	ns
		GCLK PLL	t_{SU}	3.113	3.328	3.522	ns
			t_H	–2.844	–3.023	–3.180	ns
	8 mA	GCLK	t_{SU}	0.936	0.958	0.955	ns
			t_H	–0.667	–0.653	–0.613	ns
		GCLK PLL	t_{SU}	3.113	3.328	3.522	ns
			t_H	–2.844	–3.023	–3.180	ns
	12 mA	GCLK	t_{SU}	0.936	0.958	0.955	ns
			t_H	–0.667	–0.653	–0.613	ns
		GCLK PLL	t_{SU}	3.113	3.328	3.522	ns
			t_H	–2.844	–3.023	–3.180	ns
	16 mA	GCLK	t_{SU}	0.936	0.958	0.955	ns
			t_H	–0.667	–0.653	–0.613	ns
		GCLK PLL	t_{SU}	3.113	3.328	3.522	ns
			t_H	–2.844	–3.023	–3.180	ns
2.5V	4 mA	GCLK	t_{SU}	0.879	0.914	0.926	ns
			t_H	–0.610	–0.610	–0.585	ns
		GCLK PLL	t_{SU}	3.056	3.284	3.493	ns
			t_H	–2.787	–2.980	–3.152	ns
	8 mA	GCLK	t_{SU}	0.879	0.914	0.926	ns
			t_H	–0.610	–0.610	–0.585	ns
		GCLK PLL	t_{SU}	3.056	3.284	3.493	ns
			t_H	–2.787	–2.980	–3.152	ns
	12 mA	GCLK	t_{SU}	0.879	0.914	0.926	ns
			t_H	–0.610	–0.610	–0.585	ns
		GCLK PLL	t_{SU}	3.056	3.284	3.493	ns
			t_H	–2.787	–2.980	–3.152	ns
	16 mA	GCLK	t_{SU}	0.879	0.914	0.926	ns
			t_H	–0.610	–0.610	–0.585	ns
		GCLK PLL	t_{SU}	3.056	3.284	3.493	ns
			t_H	–2.787	–2.980	–3.152	ns

Table 1–64. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.8V	2 mA	GCLK	t_{SU}	0.815	0.875	0.912	ns
			t_H	–0.548	–0.572	–0.570	ns
		GCLK PLL	t_{SU}	2.992	3.245	3.479	ns
			t_H	–2.725	–2.942	–3.137	ns
	4 mA	GCLK	t_{SU}	0.815	0.875	0.912	ns
			t_H	–0.548	–0.572	–0.570	ns
		GCLK PLL	t_{SU}	2.992	3.245	3.479	ns
			t_H	–2.725	–2.942	–3.137	ns
	6 mA	GCLK	t_{SU}	0.815	0.875	0.912	ns
			t_H	–0.548	–0.572	–0.570	ns
		GCLK PLL	t_{SU}	2.992	3.245	3.479	ns
			t_H	–2.725	–2.942	–3.137	ns
	8 mA	GCLK	t_{SU}	0.815	0.875	0.912	ns
			t_H	–0.548	–0.572	–0.570	ns
		GCLK PLL	t_{SU}	2.992	3.245	3.479	ns
			t_H	–2.725	–2.942	–3.137	ns
	10 mA	GCLK	t_{SU}	0.815	0.875	0.912	ns
			t_H	–0.548	–0.572	–0.570	ns
		GCLK PLL	t_{SU}	2.992	3.245	3.479	ns
			t_H	–2.725	–2.942	–3.137	ns
	12 mA	GCLK	t_{SU}	0.815	0.875	0.912	ns
			t_H	–0.548	–0.572	–0.570	ns
		GCLK PLL	t_{SU}	2.992	3.245	3.479	ns
			t_H	–2.725	–2.942	–3.137	ns
16 mA	GCLK	t_{SU}	0.815	0.875	0.912	ns	
		t_H	–0.548	–0.572	–0.570	ns	
	GCLK PLL	t_{SU}	2.992	3.245	3.479	ns	
		t_H	–2.725	–2.942	–3.137	ns	

Table 1–64. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	0.884	0.968	1.030	ns
			t_H	–0.615	–0.663	–0.687	ns
		GCLK PLL	t_{SU}	3.061	3.338	3.597	ns
			t_H	–2.792	–3.033	–3.254	ns
	4 mA	GCLK	t_{SU}	0.884	0.968	1.030	ns
			t_H	–0.615	–0.663	–0.687	ns
		GCLK PLL	t_{SU}	3.061	3.338	3.597	ns
			t_H	–2.792	–3.033	–3.254	ns
	6 mA	GCLK	t_{SU}	0.884	0.968	1.030	ns
			t_H	–0.615	–0.663	–0.687	ns
		GCLK PLL	t_{SU}	3.061	3.338	3.597	ns
			t_H	–2.792	–3.033	–3.254	ns
	8 mA	GCLK	t_{SU}	0.884	0.968	1.030	ns
			t_H	–0.615	–0.663	–0.687	ns
		GCLK PLL	t_{SU}	3.061	3.338	3.597	ns
			t_H	–2.792	–3.033	–3.254	ns
	10 mA	GCLK	t_{SU}	0.884	0.968	1.030	ns
			t_H	–0.615	–0.663	–0.687	ns
		GCLK PLL	t_{SU}	3.061	3.338	3.597	ns
			t_H	–2.792	–3.033	–3.254	ns
	12 mA	GCLK	t_{SU}	0.884	0.968	1.030	ns
			t_H	–0.615	–0.663	–0.687	ns
		GCLK PLL	t_{SU}	3.061	3.338	3.597	ns
			t_H	–2.792	–3.033	–3.254	ns
	16 mA	GCLK	t_{SU}	0.884	0.968	1.030	ns
			t_H	–0.615	–0.663	–0.687	ns
		GCLK PLL	t_{SU}	3.061	3.338	3.597	ns
			t_H	–2.792	–3.033	–3.254	ns

Table 1–64. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.2V	2 mA	GCLK	t_{SU}	1.037	1.148	1.237	ns	
			t_H	–0.766	–0.839	–0.889	ns	
		GCLK PLL	t_{SU}	3.214	3.518	3.804	ns	
			t_H	–2.943	–3.209	–3.456	ns	
	4 mA	GCLK	t_{SU}	1.037	1.148	1.237	ns	
			t_H	–0.766	–0.839	–0.889	ns	
		GCLK PLL	t_{SU}	3.214	3.518	3.804	ns	
			t_H	–2.943	–3.209	–3.456	ns	
	6 mA	GCLK	t_{SU}	1.037	1.148	1.237	ns	
			t_H	–0.766	–0.839	–0.889	ns	
		GCLK PLL	t_{SU}	3.214	3.518	3.804	ns	
			t_H	–2.943	–3.209	–3.456	ns	
	8 mA	GCLK	t_{SU}	1.037	1.148	1.237	ns	
			t_H	–0.766	–0.839	–0.889	ns	
		GCLK PLL	t_{SU}	3.214	3.518	3.804	ns	
			t_H	–2.943	–3.209	–3.456	ns	
	10 mA	GCLK	t_{SU}	1.037	1.148	1.237	ns	
			t_H	–0.766	–0.839	–0.889	ns	
		GCLK PLL	t_{SU}	3.214	3.518	3.804	ns	
			t_H	–2.943	–3.209	–3.456	ns	
	SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.862	0.921	0.961	ns
				t_H	–0.593	–0.616	–0.618	ns
			GCLK PLL	t_{SU}	3.046	3.306	3.547	ns
				t_H	–2.777	–3.001	–3.204	ns
12 mA		GCLK	t_{SU}	0.862	0.921	0.961	ns	
			t_H	–0.593	–0.616	–0.618	ns	
		GCLK PLL	t_{SU}	3.046	3.306	3.547	ns	
			t_H	–2.777	–3.001	–3.204	ns	
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.862	0.921	0.961	ns	
			t_H	–0.593	–0.616	–0.618	ns	
		GCLK PLL	t_{SU}	3.046	3.306	3.547	ns	
			t_H	–2.777	–3.001	–3.204	ns	

Table 1–64. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.924	1.010	1.078	ns
			t_H	–0.655	–0.704	–0.733	ns
		GCLK PLL	t_{SU}	3.108	3.395	3.664	ns
			t_H	–2.839	–3.089	–3.319	ns
	10 mA	GCLK	t_{SU}	0.924	1.010	1.078	ns
			t_H	–0.655	–0.704	–0.733	ns
		GCLK PLL	t_{SU}	3.108	3.395	3.664	ns
			t_H	–2.839	–3.089	–3.319	ns
	12 mA	GCLK	t_{SU}	0.924	1.010	1.078	ns
			t_H	–0.655	–0.704	–0.733	ns
		GCLK PLL	t_{SU}	3.108	3.395	3.664	ns
			t_H	–2.839	–3.089	–3.319	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.924	1.010	1.078	ns
			t_H	–0.655	–0.704	–0.733	ns
		GCLK PLL	t_{SU}	3.108	3.395	3.664	ns
			t_H	–2.839	–3.089	–3.319	ns
	16 mA	GCLK	t_{SU}	0.924	1.010	1.078	ns
			t_H	–0.655	–0.704	–0.733	ns
		GCLK PLL	t_{SU}	3.108	3.395	3.664	ns
			t_H	–2.839	–3.089	–3.319	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.924	1.010	1.078	ns
			t_H	–0.655	–0.704	–0.733	ns
		GCLK PLL	t_{SU}	3.108	3.395	3.664	ns
			t_H	–2.839	–3.089	–3.319	ns
	10 mA	GCLK	t_{SU}	0.924	1.010	1.078	ns
			t_H	–0.655	–0.704	–0.733	ns
		GCLK PLL	t_{SU}	3.108	3.395	3.664	ns
			t_H	–2.839	–3.089	–3.319	ns
	12 mA	GCLK	t_{SU}	0.924	1.010	1.078	ns
			t_H	–0.655	–0.704	–0.733	ns
		GCLK PLL	t_{SU}	3.108	3.395	3.664	ns
			t_H	–2.839	–3.089	–3.319	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.924	1.010	1.078	ns
			t_H	–0.655	–0.704	–0.733	ns
		GCLK PLL	t_{SU}	3.108	3.395	3.664	ns
			t_H	–2.839	–3.089	–3.319	ns

Table 1–64. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.879	0.969	1.041	ns
			t_H	–0.610	–0.664	–0.697	ns
		GCLK PLL	t_{SU}	3.063	3.354	3.627	ns
			t_H	–2.794	–3.049	–3.283	ns
	10 mA	GCLK	t_{SU}	0.879	0.969	1.041	ns
			t_H	–0.610	–0.664	–0.697	ns
		GCLK PLL	t_{SU}	3.063	3.354	3.627	ns
			t_H	–2.794	–3.049	–3.283	ns
	12 mA	GCLK	t_{SU}	0.879	0.969	1.041	ns
			t_H	–0.610	–0.664	–0.697	ns
		GCLK PLL	t_{SU}	3.063	3.354	3.627	ns
			t_H	–2.794	–3.049	–3.283	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.879	0.969	1.041	ns
			t_H	–0.610	–0.664	–0.697	ns
		GCLK PLL	t_{SU}	3.063	3.354	3.627	ns
			t_H	–2.794	–3.049	–3.283	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.010	1.127	1.226	ns
			t_H	–0.739	–0.818	–0.879	ns
		GCLK PLL	t_{SU}	3.194	3.512	3.812	ns
			t_H	–2.923	–3.203	–3.465	ns
	10 mA	GCLK	t_{SU}	1.010	1.127	1.226	ns
			t_H	–0.739	–0.818	–0.879	ns
		GCLK PLL	t_{SU}	3.194	3.512	3.812	ns
			t_H	–2.923	–3.203	–3.465	ns
3.0-V PCI	—	GCLK	t_{SU}	0.932	0.954	0.951	ns
			t_H	–0.663	–0.649	–0.609	ns
		GCLK PLL	t_{SU}	3.109	3.324	3.518	ns
			t_H	–2.840	–3.019	–3.176	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.932	0.954	0.951	ns
			t_H	–0.663	–0.649	–0.609	ns
		GCLK PLL	t_{SU}	3.109	3.324	3.518	ns
			t_H	–2.840	–3.019	–3.176	ns

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{CO}	9.230	9.942	6.432	ns
		GCLK PLL	t_{CO}	3.228	3.519	3.856	ns
	8 mA	GCLK	t_{CO}	6.804	7.349	5.940	ns
		GCLK PLL	t_{CO}	2.779	3.050	3.364	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	7.583	8.146	6.036	ns
		GCLK PLL	t_{CO}	2.865	3.141	3.460	ns
3.0-V LVTTTL	4 mA	GCLK	t_{CO}	8.006	8.602	6.127	ns
		GCLK PLL	t_{CO}	2.959	3.223	3.551	ns
	8 mA	GCLK	t_{CO}	6.446	6.977	5.845	ns
		GCLK PLL	t_{CO}	2.701	2.963	3.269	ns
	12 mA	GCLK	t_{CO}	5.798	6.324	5.724	ns
		GCLK PLL	t_{CO}	2.577	2.841	3.148	ns
	16 mA	GCLK	t_{CO}	5.438	5.920	5.645	ns
		GCLK PLL	t_{CO}	2.527	2.776	3.069	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	6.444	6.974	5.844	ns
		GCLK PLL	t_{CO}	2.699	2.962	3.268	ns
	8 mA	GCLK	t_{CO}	5.467	5.955	5.660	ns
		GCLK PLL	t_{CO}	2.530	2.780	3.084	ns
	12 mA	GCLK	t_{CO}	5.155	5.627	5.609	ns
		GCLK PLL	t_{CO}	2.489	2.739	3.033	ns
	16 mA	GCLK	t_{CO}	4.978	5.446	5.590	ns
		GCLK PLL	t_{CO}	2.469	2.720	3.014	ns
2.5V	4 mA	GCLK	t_{CO}	8.190	8.839	6.273	ns
		GCLK PLL	t_{CO}	3.081	3.361	3.697	ns
	8 mA	GCLK	t_{CO}	6.572	7.145	5.983	ns
		GCLK PLL	t_{CO}	2.809	3.084	3.407	ns
	12 mA	GCLK	t_{CO}	5.924	6.468	5.859	ns
		GCLK PLL	t_{CO}	2.691	2.962	3.283	ns
16 mA	GCLK	t_{CO}	5.616	6.141	5.799	ns	
	GCLK PLL	t_{CO}	2.639	2.906	3.223	ns	

Table 1–65. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t _{CO}	12.449	13.585	7.738	ns	
		GCLK PLL	t _{CO}	4.254	4.669	5.162	ns	
	4 mA	GCLK	t _{CO}	9.043	9.914	7.126	ns	
		GCLK PLL	t _{CO}	3.680	4.083	4.550	ns	
	6 mA	GCLK	t _{CO}	7.713	8.463	6.785	ns	
		GCLK PLL	t _{CO}	3.410	3.778	4.209	ns	
	8 mA	GCLK	t _{CO}	7.052	7.746	6.656	ns	
		GCLK PLL	t _{CO}	3.296	3.662	4.080	ns	
	10 mA	GCLK	t _{CO}	6.704	7.374	6.592	ns	
		GCLK PLL	t _{CO}	3.233	3.596	4.016	ns	
	12 mA	GCLK	t _{CO}	6.396	7.042	6.498	ns	
		GCLK PLL	t _{CO}	3.168	3.515	3.922	ns	
	16 mA	GCLK	t _{CO}	6.078	6.696	6.435	ns	
		GCLK PLL	t _{CO}	3.114	3.461	3.859	ns	
	1.5V	2 mA	GCLK	t _{CO}	11.813	13.127	8.488	ns
			GCLK PLL	t _{CO}	4.662	5.237	5.912	ns
		4 mA	GCLK	t _{CO}	8.742	9.704	7.728	ns
			GCLK PLL	t _{CO}	4.091	4.574	5.152	ns
6 mA		GCLK	t _{CO}	7.721	8.577	7.505	ns	
		GCLK PLL	t _{CO}	3.894	4.364	4.929	ns	
8 mA		GCLK	t _{CO}	7.192	7.979	7.335	ns	
		GCLK PLL	t _{CO}	3.776	4.228	4.759	ns	
10 mA		GCLK	t _{CO}	6.875	7.637	7.268	ns	
		GCLK PLL	t _{CO}	3.709	4.158	4.692	ns	
12 mA		GCLK	t _{CO}	6.675	7.411	7.208	ns	
		GCLK PLL	t _{CO}	3.673	4.109	4.632	ns	
16 mA		GCLK	t _{CO}	6.335	7.024	7.050	ns	
		GCLK PLL	t _{CO}	3.555	3.983	4.474	ns	
1.2V		2 mA	GCLK	t _{CO}	12.005	13.691	10.222	ns
			GCLK PLL	t _{CO}	5.738	6.602	7.646	ns
		4 mA	GCLK	t _{CO}	9.382	10.666	9.551	ns
			GCLK PLL	t _{CO}	5.239	6.025	6.975	ns
	6 mA	GCLK	t _{CO}	8.563	9.719	9.297	ns	
		GCLK PLL	t _{CO}	5.058	5.811	6.721	ns	
	8 mA	GCLK	t _{CO}	8.155	9.249	9.191	ns	
		GCLK PLL	t _{CO}	4.975	5.718	6.615	ns	
	10 mA	GCLK	t _{CO}	7.819	8.845	8.949	ns	
		GCLK PLL	t _{CO}	4.830	5.534	6.373	ns	
	12 mA	GCLK	t _{CO}	7.663	8.669	8.921	ns	
		GCLK PLL	t _{CO}	4.804	5.506	6.345	ns	

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.885	5.350	5.870	ns
		GCLK PLL	t_{CO}	2.693	2.973	3.284	ns
	12 mA	GCLK	t_{CO}	4.850	5.314	5.833	ns
		GCLK PLL	t_{CO}	2.658	2.937	3.247	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.793	5.252	5.766	ns
		GCLK PLL	t_{CO}	2.601	2.875	3.180	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.289	5.824	6.422	ns
		GCLK PLL	t_{CO}	3.097	3.447	3.836	ns
	10 mA	GCLK	t_{CO}	5.258	5.786	6.376	ns
		GCLK PLL	t_{CO}	3.066	3.409	3.790	ns
	12 mA	GCLK	t_{CO}	5.243	5.771	6.358	ns
		GCLK PLL	t_{CO}	3.051	3.394	3.772	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.230	5.756	6.345	ns
		GCLK PLL	t_{CO}	3.038	3.379	3.759	ns
	16 mA	GCLK	t_{CO}	5.211	5.737	6.325	ns
		GCLK PLL	t_{CO}	3.019	3.360	3.739	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.270	5.796	6.384	ns
		GCLK PLL	t_{CO}	3.078	3.419	3.798	ns
	10 mA	GCLK	t_{CO}	5.261	5.789	6.381	ns
		GCLK PLL	t_{CO}	3.069	3.412	3.795	ns
	12 mA	GCLK	t_{CO}	5.240	5.764	6.350	ns
		GCLK PLL	t_{CO}	3.048	3.387	3.764	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.212	5.731	6.314	ns
		GCLK PLL	t_{CO}	3.020	3.354	3.728	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.775	6.391	7.091	ns
		GCLK PLL	t_{CO}	3.583	4.014	4.505	ns
	10 mA	GCLK	t_{CO}	5.762	6.372	7.066	ns
		GCLK PLL	t_{CO}	3.570	3.995	4.480	ns
	12 mA	GCLK	t_{CO}	5.753	6.366	7.062	ns
		GCLK PLL	t_{CO}	3.561	3.989	4.476	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.710	6.313	6.998	ns
		GCLK PLL	t_{CO}	3.518	3.936	4.412	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.946	7.831	8.869	ns
		GCLK PLL	t_{CO}	4.754	5.454	6.283	ns
	10 mA	GCLK	t_{CO}	6.868	7.725	8.714	ns
		GCLK PLL	t_{CO}	4.676	5.348	6.128	ns
	12 mA	GCLK	t_{CO}	6.866	7.725	8.718	ns
		GCLK PLL	t_{CO}	4.674	5.348	6.132	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.809	7.654	8.637	ns
		GCLK PLL	t_{CO}	4.617	5.277	6.051	ns

Table 1–65. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V PCI	—	GCLK	t _{CO}	5.357	5.857	5.928	ns
		GCLK PLL	t _{CO}	2.791	3.050	3.352	ns
3.0-V PCI-X	—	GCLK	t _{CO}	5.357	5.857	5.928	ns
		GCLK PLL	t _{CO}	2.791	3.050	3.352	ns

Table 1–66. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
3.3-V LVTTTL	4 mA	GCLK	t _{CO}	5.343	9.881	6.367	ns	
		GCLK PLL	t _{CO}	3.160	3.450	3.777	ns	
	8 mA	GCLK	t _{CO}	4.895	7.297	5.885	ns	
		GCLK PLL	t _{CO}	2.712	2.986	3.295	ns	
3.3-V LVCMOS	2 mA	GCLK	t _{CO}	4.989	8.113	5.976	ns	
		GCLK PLL	t _{CO}	2.806	3.073	3.386	ns	
3.0-V LVTTTL	4 mA	GCLK	t _{CO}	5.094	8.558	6.067	ns	
		GCLK PLL	t _{CO}	2.911	3.171	3.477	ns	
	8 mA	GCLK	t _{CO}	4.838	6.946	5.806	ns	
		GCLK PLL	t _{CO}	2.655	2.916	3.216	ns	
	12 mA	GCLK	t _{CO}	4.723	6.293	5.679	ns	
		GCLK PLL	t _{CO}	2.540	2.790	3.089	ns	
	16 mA	GCLK	t _{CO}	4.673	5.895	5.612	ns	
		GCLK PLL	t _{CO}	2.490	2.736	3.022	ns	
3.0-V LVCMOS	4 mA	GCLK	t _{CO}	4.836	6.944	5.804	ns	
		GCLK PLL	t _{CO}	2.653	2.915	3.214	ns	
	8 mA	GCLK	t _{CO}	4.674	5.929	5.615	ns	
		GCLK PLL	t _{CO}	2.491	2.738	3.025	ns	
	12mA	GCLK	t _{CO}	4.634	5.608	5.576	ns	
		GCLK PLL	t _{CO}	2.451	2.698	2.986	ns	
	16 mA	GCLK	t _{CO}	4.613	5.426	5.556	ns	
		GCLK PLL	t _{CO}	2.430	2.678	2.966	ns	
	2.5V	4 mA	GCLK	t _{CO}	5.220	8.802	6.223	ns
			GCLK PLL	t _{CO}	3.037	3.310	3.633	ns
8 mA		GCLK	t _{CO}	4.951	7.115	5.947	ns	
		GCLK PLL	t _{CO}	2.768	3.041	3.357	ns	
12 mA		GCLK	t _{CO}	4.837	6.440	5.823	ns	
		GCLK PLL	t _{CO}	2.654	2.921	3.233	ns	
16 mA		GCLK	t _{CO}	4.784	6.114	5.765	ns	
		GCLK PLL	t _{CO}	2.601	2.865	3.175	ns	

Table 1–66. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t_{CO}	6.370	13.524	7.670	ns	
		GCLK PLL	t_{CO}	4.187	4.598	5.080	ns	
	4 mA	GCLK	t_{CO}	5.815	9.875	7.078	ns	
		GCLK PLL	t_{CO}	3.632	4.028	4.488	ns	
	6 mA	GCLK	t_{CO}	5.553	8.432	6.746	ns	
		GCLK PLL	t_{CO}	3.370	3.733	4.156	ns	
	8 mA	GCLK	t_{CO}	5.437	7.713	6.601	ns	
		GCLK PLL	t_{CO}	3.254	3.605	4.011	ns	
	10 mA	GCLK	t_{CO}	5.376	7.344	6.554	ns	
		GCLK PLL	t_{CO}	3.193	3.551	3.964	ns	
	12 mA	GCLK	t_{CO}	5.316	7.017	6.465	ns	
		GCLK PLL	t_{CO}	3.133	3.475	3.875	ns	
	16 mA	GCLK	t_{CO}	5.272	6.681	6.410	ns	
		GCLK PLL	t_{CO}	3.089	3.426	3.820	ns	
	1.5V	2 mA	GCLK	t_{CO}	6.784	13.073	8.422	ns
			GCLK PLL	t_{CO}	4.601	5.169	5.832	ns
		4 mA	GCLK	t_{CO}	6.225	9.668	7.680	ns
			GCLK PLL	t_{CO}	4.042	4.526	5.090	ns
6 mA		GCLK	t_{CO}	6.035	8.546	7.464	ns	
		GCLK PLL	t_{CO}	3.852	4.321	4.874	ns	
8 mA		GCLK	t_{CO}	5.937	7.975	7.324	ns	
		GCLK PLL	t_{CO}	3.754	4.210	4.734	ns	
10 mA		GCLK	t_{CO}	5.870	7.630	7.255	ns	
		GCLK PLL	t_{CO}	3.687	4.138	4.665	ns	
12 mA		GCLK	t_{CO}	5.830	7.402	7.191	ns	
		GCLK PLL	t_{CO}	3.647	4.087	4.601	ns	
16 mA		GCLK	t_{CO}	5.758	7.014	7.103	ns	
		GCLK PLL	t_{CO}	3.575	4.006	4.513	ns	
1.2V		2 mA	GCLK	t_{CO}	7.870	13.646	10.168	ns
			GCLK PLL	t_{CO}	5.687	6.544	7.578	ns
		4 mA	GCLK	t_{CO}	7.379	10.634	9.509	ns
			GCLK PLL	t_{CO}	5.196	5.978	6.919	ns
	6 mA	GCLK	t_{CO}	7.224	9.716	9.294	ns	
		GCLK PLL	t_{CO}	5.041	5.794	6.704	ns	
	8 mA	GCLK	t_{CO}	7.136	9.242	9.181	ns	
		GCLK PLL	t_{CO}	4.953	5.696	6.591	ns	
	10 mA	GCLK	t_{CO}	7.018	8.834	9.002	ns	
		GCLK PLL	t_{CO}	4.835	5.552	6.412	ns	

Table 1–66. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.855	5.318	5.806	ns
		GCLK PLL	t_{CO}	2.680	2.943	3.247	ns
	12 mA	GCLK	t_{CO}	4.823	5.284	5.770	ns
		GCLK PLL	t_{CO}	2.648	2.909	3.211	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.772	5.231	5.713	ns
		GCLK PLL	t_{CO}	2.597	2.856	3.154	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.262	5.792	6.359	ns
		GCLK PLL	t_{CO}	3.087	3.417	3.800	ns
	10 mA	GCLK	t_{CO}	5.243	5.768	6.329	ns
		GCLK PLL	t_{CO}	3.068	3.393	3.770	ns
	12 mA	GCLK	t_{CO}	5.221	5.744	6.302	ns
		GCLK PLL	t_{CO}	3.046	3.369	3.743	ns
SSTL–18 Class II	12 mA	GCLK	t_{CO}	5.213	5.736	6.295	ns
		GCLK PLL	t_{CO}	3.038	3.361	3.736	ns
	16 mA	GCLK	t_{CO}	5.198	5.722	6.281	ns
		GCLK PLL	t_{CO}	3.023	3.347	3.722	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.242	5.764	6.320	ns
		GCLK PLL	t_{CO}	3.067	3.389	3.761	ns
	10 mA	GCLK	t_{CO}	5.235	5.760	6.319	ns
		GCLK PLL	t_{CO}	3.060	3.385	3.760	ns
	12 mA	GCLK	t_{CO}	5.225	5.746	6.302	ns
		GCLK PLL	t_{CO}	3.050	3.371	3.743	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.192	5.708	6.260	ns
		GCLK PLL	t_{CO}	3.017	3.333	3.701	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.747	6.363	7.028	ns
		GCLK PLL	t_{CO}	3.572	3.988	4.469	ns
	10 mA	GCLK	t_{CO}	5.745	6.358	7.019	ns
		GCLK PLL	t_{CO}	3.570	3.983	4.460	ns
	12 mA	GCLK	t_{CO}	5.736	6.351	7.015	ns
		GCLK PLL	t_{CO}	3.561	3.976	4.456	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.697	6.305	6.962	ns
		GCLK PLL	t_{CO}	3.522	3.930	4.403	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.938	7.828	8.841	ns
		GCLK PLL	t_{CO}	4.763	5.453	6.282	ns
	10 mA	GCLK	t_{CO}	6.855	7.714	8.677	ns
		GCLK PLL	t_{CO}	4.680	5.339	6.118	ns
3.0-V PCI	—	GCLK	t_{CO}	4.932	5.818	5.888	ns
		GCLK PLL	t_{CO}	2.749	3.003	3.298	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.932	5.818	5.888	ns
		GCLK PLL	t_{CO}	2.749	3.003	3.298	ns

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.726	0.788	0.828	ns
			t_H	–0.458	–0.485	–0.488	ns
		GCLK PLL	t_{SU}	2.916	3.179	3.422	ns
			t_H	–2.648	–2.876	–3.082	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.835	5.333	5.860	ns
		GCLK PLL	t_{CO}	4.835	5.333	5.860	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.835	5.333	5.860	ns
		GCLK PLL	t_{CO}	4.835	5.333	5.860	ns
PPDS_E_3R	—	GCLK	t_{CO}	4.835	5.333	5.860	ns
		GCLK PLL	t_{CO}	4.835	5.333	5.860	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.835	5.333	5.860	ns
		GCLK PLL	t_{CO}	4.835	5.333	5.860	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.835	5.333	5.860	ns
		GCLK PLL	t_{CO}	4.835	5.333	5.860	ns

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.761	0.826	0.873	ns
			t_H	–0.494	–0.524	–0.532	ns
			t_{CO}	4.029	4.426	4.846	ns
		GCLK PLL	t_{SU}	2.930	3.196	3.446	ns
			t_H	–2.663	–2.894	–3.105	ns
			t_{CO}	1.841	2.035	2.252	ns
mini-LVDS	—	GCLK	t_{CO}	4.029	4.426	4.846	ns
		GCLK PLL	t_{CO}	1.841	2.035	2.252	ns
PPDS	—	GCLK	t_{CO}	4.029	4.426	4.846	ns
		GCLK PLL	t_{CO}	1.841	2.035	2.252	ns
RSDS	—	GCLK	t_{CO}	4.029	4.426	4.846	ns
		GCLK PLL	t_{CO}	1.841	2.035	2.252	ns

EP3C40 I/O Timing Parameters

Tables 1–69 through 1–74 show the maximum I/O timing parameters for EP3C40 devices.

Table 1–69. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	0.751	0.755	0.728	ns
			t_H	–0.481	–0.450	–0.387	ns
		GCLK PLL	t_{SU}	3.192	3.418	3.623	ns
			t_H	–2.922	–3.113	–3.282	ns
	8 mA	GCLK	t_{SU}	0.751	0.755	0.728	ns
			t_H	–0.481	–0.450	–0.387	ns
		GCLK PLL	t_{SU}	3.192	3.418	3.623	ns
			t_H	–2.922	–3.113	–3.282	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.751	0.755	0.728	ns
			t_H	–0.481	–0.450	–0.387	ns
		GCLK PLL	t_{SU}	3.192	3.418	3.623	ns
			t_H	–2.922	–3.113	–3.282	ns
3.0-V LVTTTL	4 mA	GCLK	t_{SU}	0.751	0.755	0.728	ns
			t_H	–0.481	–0.450	–0.387	ns
		GCLK PLL	t_{SU}	3.192	3.418	3.623	ns
			t_H	–2.922	–3.113	–3.282	ns
	8 mA	GCLK	t_{SU}	0.751	0.755	0.728	ns
			t_H	–0.481	–0.450	–0.387	ns
		GCLK PLL	t_{SU}	3.192	3.418	3.623	ns
			t_H	–2.922	–3.113	–3.282	ns
	12 mA	GCLK	t_{SU}	0.751	0.755	0.728	ns
			t_H	–0.481	–0.450	–0.387	ns
		GCLK PLL	t_{SU}	3.192	3.418	3.623	ns
			t_H	–2.922	–3.113	–3.282	ns
	16 mA	GCLK	t_{SU}	0.751	0.755	0.728	ns
			t_H	–0.481	–0.450	–0.387	ns
		GCLK PLL	t_{SU}	3.192	3.418	3.623	ns
			t_H	–2.922	–3.113	–3.282	ns

Table 1–69. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.751	0.755	0.728	ns
			t_H	–0.481	–0.450	–0.387	ns
		GCLK PLL	t_{SU}	3.192	3.418	3.623	ns
			t_H	–2.922	–3.113	–3.282	ns
	8 mA	GCLK	t_{SU}	0.751	0.755	0.728	ns
			t_H	–0.481	–0.450	–0.387	ns
		GCLK PLL	t_{SU}	3.192	3.418	3.623	ns
			t_H	–2.922	–3.113	–3.282	ns
	12 mA	GCLK	t_{SU}	0.751	0.755	0.728	ns
			t_H	–0.481	–0.450	–0.387	ns
		GCLK PLL	t_{SU}	3.192	3.418	3.623	ns
			t_H	–2.922	–3.113	–3.282	ns
	16 mA	GCLK	t_{SU}	0.751	0.755	0.728	ns
			t_H	–0.481	–0.450	–0.387	ns
		GCLK PLL	t_{SU}	3.192	3.418	3.623	ns
			t_H	–2.922	–3.113	–3.282	ns
2.5V	4 mA	GCLK	t_{SU}	0.694	0.710	0.696	ns
			t_H	–0.424	–0.406	–0.356	ns
		GCLK PLL	t_{SU}	3.135	3.373	3.591	ns
			t_H	–2.865	–3.069	–3.251	ns
	8 mA	GCLK	t_{SU}	0.694	0.710	0.696	ns
			t_H	–0.424	–0.406	–0.356	ns
		GCLK PLL	t_{SU}	3.135	3.373	3.591	ns
			t_H	–2.865	–3.069	–3.251	ns
	12 mA	GCLK	t_{SU}	0.694	0.710	0.696	ns
			t_H	–0.424	–0.406	–0.356	ns
		GCLK PLL	t_{SU}	3.135	3.373	3.591	ns
			t_H	–2.865	–3.069	–3.251	ns
	16 mA	GCLK	t_{SU}	0.694	0.710	0.696	ns
			t_H	–0.424	–0.406	–0.356	ns
		GCLK PLL	t_{SU}	3.135	3.373	3.591	ns
			t_H	–2.865	–3.069	–3.251	ns

Table 1–69. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.8V	2 mA	GCLK	t_{SU}	0.629	0.671	0.683	ns
			t_H	–0.361	–0.368	–0.342	ns
		GCLK PLL	t_{SU}	3.070	3.334	3.578	ns
			t_H	–2.802	–3.031	–3.237	ns
	4 mA	GCLK	t_{SU}	0.629	0.671	0.683	ns
			t_H	–0.361	–0.368	–0.342	ns
		GCLK PLL	t_{SU}	3.070	3.334	3.578	ns
			t_H	–2.802	–3.031	–3.237	ns
	6 mA	GCLK	t_{SU}	0.629	0.671	0.683	ns
			t_H	–0.361	–0.368	–0.342	ns
		GCLK PLL	t_{SU}	3.070	3.334	3.578	ns
			t_H	–2.802	–3.031	–3.237	ns
	8 mA	GCLK	t_{SU}	0.629	0.671	0.683	ns
			t_H	–0.361	–0.368	–0.342	ns
		GCLK PLL	t_{SU}	3.070	3.334	3.578	ns
			t_H	–2.802	–3.031	–3.237	ns
	10 mA	GCLK	t_{SU}	0.629	0.671	0.683	ns
			t_H	–0.361	–0.368	–0.342	ns
		GCLK PLL	t_{SU}	3.070	3.334	3.578	ns
			t_H	–2.802	–3.031	–3.237	ns
	12 mA	GCLK	t_{SU}	0.629	0.671	0.683	ns
			t_H	–0.361	–0.368	–0.342	ns
		GCLK PLL	t_{SU}	3.070	3.334	3.578	ns
			t_H	–2.802	–3.031	–3.237	ns
16 mA	GCLK	t_{SU}	0.629	0.671	0.683	ns	
		t_H	–0.361	–0.368	–0.342	ns	
	GCLK PLL	t_{SU}	3.070	3.334	3.578	ns	
		t_H	–2.802	–3.031	–3.237	ns	

Table 1–69. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	0.698	0.763	0.800	ns
			t_H	–0.428	–0.458	–0.457	ns
		GCLK PLL	t_{SU}	3.139	3.426	3.695	ns
			t_H	–2.869	–3.121	–3.352	ns
	4 mA	GCLK	t_{SU}	0.698	0.763	0.800	ns
			t_H	–0.428	–0.458	–0.457	ns
		GCLK PLL	t_{SU}	3.139	3.426	3.695	ns
			t_H	–2.869	–3.121	–3.352	ns
	6 mA	GCLK	t_{SU}	0.698	0.763	0.800	ns
			t_H	–0.428	–0.458	–0.457	ns
		GCLK PLL	t_{SU}	3.139	3.426	3.695	ns
			t_H	–2.869	–3.121	–3.352	ns
	8 mA	GCLK	t_{SU}	0.698	0.763	0.800	ns
			t_H	–0.428	–0.458	–0.457	ns
		GCLK PLL	t_{SU}	3.139	3.426	3.695	ns
			t_H	–2.869	–3.121	–3.352	ns
	10 mA	GCLK	t_{SU}	0.698	0.763	0.800	ns
			t_H	–0.428	–0.458	–0.457	ns
		GCLK PLL	t_{SU}	3.139	3.426	3.695	ns
			t_H	–2.869	–3.121	–3.352	ns
	12 mA	GCLK	t_{SU}	0.698	0.763	0.800	ns
			t_H	–0.428	–0.458	–0.457	ns
		GCLK PLL	t_{SU}	3.139	3.426	3.695	ns
			t_H	–2.869	–3.121	–3.352	ns
16 mA	GCLK	t_{SU}	0.698	0.763	0.800	ns	
		t_H	–0.428	–0.458	–0.457	ns	
	GCLK PLL	t_{SU}	3.139	3.426	3.695	ns	
		t_H	–2.869	–3.121	–3.352	ns	

Table 1–69. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.2V	2 mA	GCLK	t_{SU}	0.850	0.943	1.006	ns
			t_H	–0.578	–0.634	–0.659	ns
		GCLK PLL	t_{SU}	3.291	3.606	3.901	ns
			t_H	–3.019	–3.297	–3.554	ns
	4 mA	GCLK	t_{SU}	0.850	0.943	1.006	ns
			t_H	–0.578	–0.634	–0.659	ns
		GCLK PLL	t_{SU}	3.291	3.606	3.901	ns
			t_H	–3.019	–3.297	–3.554	ns
	6 mA	GCLK	t_{SU}	0.850	0.943	1.006	ns
			t_H	–0.578	–0.634	–0.659	ns
		GCLK PLL	t_{SU}	3.291	3.606	3.901	ns
			t_H	–3.019	–3.297	–3.554	ns
	8 mA	GCLK	t_{SU}	0.850	0.943	1.006	ns
			t_H	–0.578	–0.634	–0.659	ns
		GCLK PLL	t_{SU}	3.291	3.606	3.901	ns
			t_H	–3.019	–3.297	–3.554	ns
	10 mA	GCLK	t_{SU}	0.850	0.943	1.006	ns
			t_H	–0.578	–0.634	–0.659	ns
		GCLK PLL	t_{SU}	3.291	3.606	3.901	ns
			t_H	–3.019	–3.297	–3.554	ns
	12 mA	GCLK	t_{SU}	0.850	0.943	1.006	ns
			t_H	–0.578	–0.634	–0.659	ns
		GCLK PLL	t_{SU}	3.291	3.606	3.901	ns
			t_H	–3.019	–3.297	–3.554	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.683	0.736	0.753	ns
			t_H	–0.413	–0.432	–0.411	ns
		GCLK PLL	t_{SU}	3.141	3.406	3.643	ns
			t_H	–2.871	–3.102	–3.301	ns
	12 mA	GCLK	t_{SU}	0.683	0.736	0.753	ns
			t_H	–0.413	–0.432	–0.411	ns
		GCLK PLL	t_{SU}	3.141	3.406	3.643	ns
			t_H	–2.871	–3.102	–3.301	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.683	0.736	0.753	ns
			t_H	–0.413	–0.432	–0.411	ns
		GCLK PLL	t_{SU}	3.141	3.406	3.643	ns
			t_H	–2.871	–3.102	–3.301	ns

Table 1–69. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.744	0.825	0.868	ns
			t_H	–0.474	–0.519	–0.524	ns
		GCLK PLL	t_{SU}	3.202	3.495	3.758	ns
			t_H	–2.932	–3.189	–3.414	ns
	10 mA	GCLK	t_{SU}	0.744	0.825	0.868	ns
			t_H	–0.474	–0.519	–0.524	ns
		GCLK PLL	t_{SU}	3.202	3.495	3.758	ns
			t_H	–2.932	–3.189	–3.414	ns
	12 mA	GCLK	t_{SU}	0.744	0.825	0.868	ns
			t_H	–0.474	–0.519	–0.524	ns
		GCLK PLL	t_{SU}	3.202	3.495	3.758	ns
			t_H	–2.932	–3.189	–3.414	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.744	0.825	0.868	ns
			t_H	–0.474	–0.519	–0.524	ns
		GCLK PLL	t_{SU}	3.202	3.495	3.758	ns
			t_H	–2.932	–3.189	–3.414	ns
	16 mA	GCLK	t_{SU}	0.744	0.825	0.868	ns
			t_H	–0.474	–0.519	–0.524	ns
		GCLK PLL	t_{SU}	3.202	3.495	3.758	ns
			t_H	–2.932	–3.189	–3.414	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.744	0.825	0.868	ns
			t_H	–0.474	–0.519	–0.524	ns
		GCLK PLL	t_{SU}	3.202	3.495	3.758	ns
			t_H	–2.932	–3.189	–3.414	ns
	10 mA	GCLK	t_{SU}	0.744	0.825	0.868	ns
			t_H	–0.474	–0.519	–0.524	ns
		GCLK PLL	t_{SU}	3.202	3.495	3.758	ns
			t_H	–2.932	–3.189	–3.414	ns
	12 mA	GCLK	t_{SU}	0.744	0.825	0.868	ns
			t_H	–0.474	–0.519	–0.524	ns
		GCLK PLL	t_{SU}	3.202	3.495	3.758	ns
			t_H	–2.932	–3.189	–3.414	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.744	0.825	0.868	ns
			t_H	–0.474	–0.519	–0.524	ns
		GCLK PLL	t_{SU}	3.202	3.495	3.758	ns
			t_H	–2.932	–3.189	–3.414	ns

Table 1–69. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit		
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.700	0.785	0.834	ns		
			t_H	–0.430	–0.480	–0.491	ns		
		GCLK PLL	t_{SU}	3.158	3.455	3.724	ns		
			t_H	–2.888	–3.150	–3.381	ns		
		10 mA	GCLK	t_{SU}	0.700	0.785	0.834	ns	
				t_H	–0.430	–0.480	–0.491	ns	
	GCLK PLL		t_{SU}	3.158	3.455	3.724	ns		
			t_H	–2.888	–3.150	–3.381	ns		
	12 mA	GCLK	t_{SU}	0.700	0.785	0.834	ns		
			t_H	–0.430	–0.480	–0.491	ns		
		GCLK PLL	t_{SU}	3.158	3.455	3.724	ns		
			t_H	–2.888	–3.150	–3.381	ns		
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.700	0.785	0.834	ns		
			t_H	–0.430	–0.480	–0.491	ns		
		GCLK PLL	t_{SU}	3.158	3.455	3.724	ns		
			t_H	–2.888	–3.150	–3.381	ns		
		1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.832	0.944	1.018	ns
					t_H	–0.560	–0.635	–0.671	ns
GCLK PLL	t_{SU}			3.290	3.614	3.908	ns		
	t_H			–3.018	–3.305	–3.561	ns		
10 mA	GCLK			t_{SU}	0.832	0.944	1.018	ns	
				t_H	–0.560	–0.635	–0.671	ns	
	GCLK PLL		t_{SU}	3.290	3.614	3.908	ns		
			t_H	–3.018	–3.305	–3.561	ns		
12 mA	GCLK		t_{SU}	0.832	0.944	1.018	ns		
			t_H	–0.560	–0.635	–0.671	ns		
	GCLK PLL		t_{SU}	3.290	3.614	3.908	ns		
			t_H	–3.018	–3.305	–3.561	ns		
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	0.832	0.944	1.018	ns		
			t_H	–0.560	–0.635	–0.671	ns		
		GCLK PLL	t_{SU}	3.290	3.614	3.908	ns		
			t_H	–3.018	–3.305	–3.561	ns		
		3.0-V PCI	—	GCLK	t_{SU}	0.747	0.751	0.723	ns
					t_H	–0.477	–0.446	–0.382	ns
GCLK PLL	t_{SU}			3.188	3.414	3.618	ns		
	t_H			–2.918	–3.109	–3.277	ns		
3.0-V PCI-X	—	GCLK	t_{SU}	0.747	0.751	0.723	ns		
			t_H	–0.477	–0.446	–0.382	ns		
		GCLK PLL	t_{SU}	3.188	3.414	3.618	ns		
			t_H	–2.918	–3.109	–3.277	ns		

Table 1–70. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit		
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	0.774	0.787	0.793	ns		
			t_H	–0.505	–0.482	–0.451	ns		
		GCLK PLL	t_{SU}	3.206	3.433	3.669	ns		
			t_H	–2.937	–3.128	–3.327	ns		
	8 mA	GCLK	t_{SU}	0.774	0.787	0.793	ns		
			t_H	–0.505	–0.482	–0.451	ns		
		GCLK PLL	t_{SU}	3.206	3.433	3.669	ns		
			t_H	–2.937	–3.128	–3.327	ns		
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.774	0.787	0.793	ns		
			t_H	–0.505	–0.482	–0.451	ns		
		GCLK PLL	t_{SU}	3.206	3.433	3.669	ns		
			t_H	–2.937	–3.128	–3.327	ns		
		3.0-V LVTTTL	4 mA	GCLK	t_{SU}	0.774	0.787	0.793	ns
					t_H	–0.505	–0.482	–0.451	ns
GCLK PLL	t_{SU}			3.206	3.433	3.669	ns		
	t_H			–2.937	–3.128	–3.327	ns		
8 mA	GCLK		t_{SU}	0.774	0.787	0.793	ns		
			t_H	–0.505	–0.482	–0.451	ns		
	GCLK PLL		t_{SU}	3.206	3.433	3.669	ns		
			t_H	–2.937	–3.128	–3.327	ns		
12 mA	GCLK		t_{SU}	0.774	0.787	0.793	ns		
			t_H	–0.505	–0.482	–0.451	ns		
	GCLK PLL		t_{SU}	3.206	3.433	3.669	ns		
			t_H	–2.937	–3.128	–3.327	ns		
16 mA	GCLK	t_{SU}	0.774	0.787	0.793	ns			
		t_H	–0.505	–0.482	–0.451	ns			
	GCLK PLL	t_{SU}	3.206	3.433	3.669	ns			
		t_H	–2.937	–3.128	–3.327	ns			

Table 1–70. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.774	0.787	0.793	ns
			t_H	–0.505	–0.482	–0.451	ns
		GCLK PLL	t_{SU}	3.206	3.433	3.669	ns
			t_H	–2.937	–3.128	–3.327	ns
	8 mA	GCLK	t_{SU}	0.774	0.787	0.793	ns
			t_H	–0.505	–0.482	–0.451	ns
		GCLK PLL	t_{SU}	3.206	3.433	3.669	ns
			t_H	–2.937	–3.128	–3.327	ns
	12 mA	GCLK	t_{SU}	0.774	0.787	0.793	ns
			t_H	–0.505	–0.482	–0.451	ns
		GCLK PLL	t_{SU}	3.206	3.433	3.669	ns
			t_H	–2.937	–3.128	–3.327	ns
	16 mA	GCLK	t_{SU}	0.774	0.787	0.793	ns
			t_H	–0.505	–0.482	–0.451	ns
		GCLK PLL	t_{SU}	3.206	3.433	3.669	ns
			t_H	–2.937	–3.128	–3.327	ns
2.5V	4 mA	GCLK	t_{SU}	0.717	0.743	0.764	ns
			t_H	–0.448	–0.439	–0.423	ns
		GCLK PLL	t_{SU}	3.149	3.389	3.640	ns
			t_H	–2.880	–3.085	–3.299	ns
	8 mA	GCLK	t_{SU}	0.717	0.743	0.764	ns
			t_H	–0.448	–0.439	–0.423	ns
		GCLK PLL	t_{SU}	3.149	3.389	3.640	ns
			t_H	–2.880	–3.085	–3.299	ns
	12 mA	GCLK	t_{SU}	0.717	0.743	0.764	ns
			t_H	–0.448	–0.439	–0.423	ns
		GCLK PLL	t_{SU}	3.149	3.389	3.640	ns
			t_H	–2.880	–3.085	–3.299	ns
	16 mA	GCLK	t_{SU}	0.717	0.743	0.764	ns
			t_H	–0.448	–0.439	–0.423	ns
		GCLK PLL	t_{SU}	3.149	3.389	3.640	ns
			t_H	–2.880	–3.085	–3.299	ns

Table 1–70. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.8V	2 mA	GCLK	t_{SU}	0.643	0.704	0.750	ns
			t_H	–0.376	–0.401	–0.408	ns
		GCLK PLL	t_{SU}	3.085	3.350	3.598	ns
			t_H	–2.818	–3.047	–3.256	ns
	4 mA	GCLK	t_{SU}	0.643	0.704	0.750	ns
			t_H	–0.376	–0.401	–0.408	ns
		GCLK PLL	t_{SU}	3.085	3.350	3.598	ns
			t_H	–2.818	–3.047	–3.256	ns
	6 mA	GCLK	t_{SU}	0.643	0.704	0.750	ns
			t_H	–0.376	–0.401	–0.408	ns
		GCLK PLL	t_{SU}	3.085	3.350	3.598	ns
			t_H	–2.818	–3.047	–3.256	ns
	8 mA	GCLK	t_{SU}	0.643	0.704	0.750	ns
			t_H	–0.376	–0.401	–0.408	ns
		GCLK PLL	t_{SU}	3.085	3.350	3.598	ns
			t_H	–2.818	–3.047	–3.256	ns
	10 mA	GCLK	t_{SU}	0.643	0.704	0.750	ns
			t_H	–0.376	–0.401	–0.408	ns
		GCLK PLL	t_{SU}	3.085	3.350	3.598	ns
			t_H	–2.818	–3.047	–3.256	ns
	12 mA	GCLK	t_{SU}	0.643	0.704	0.750	ns
			t_H	–0.376	–0.401	–0.408	ns
		GCLK PLL	t_{SU}	3.085	3.350	3.598	ns
			t_H	–2.818	–3.047	–3.256	ns
16 mA	GCLK	t_{SU}	0.643	0.704	0.750	ns	
		t_H	–0.376	–0.401	–0.408	ns	
	GCLK PLL	t_{SU}	3.085	3.350	3.598	ns	
		t_H	–2.818	–3.047	–3.256	ns	

Table 1–70. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	0.712	0.797	0.868	ns
			t_H	–0.443	–0.492	–0.525	ns
		GCLK PLL	t_{SU}	3.154	3.443	3.716	ns
			t_H	–2.885	–3.138	–3.373	ns
	4 mA	GCLK	t_{SU}	0.712	0.797	0.868	ns
			t_H	–0.443	–0.492	–0.525	ns
		GCLK PLL	t_{SU}	3.154	3.443	3.716	ns
			t_H	–2.885	–3.138	–3.373	ns
	6 mA	GCLK	t_{SU}	0.712	0.797	0.868	ns
			t_H	–0.443	–0.492	–0.525	ns
		GCLK PLL	t_{SU}	3.154	3.443	3.716	ns
			t_H	–2.885	–3.138	–3.373	ns
	8 mA	GCLK	t_{SU}	0.712	0.797	0.868	ns
			t_H	–0.443	–0.492	–0.525	ns
		GCLK PLL	t_{SU}	3.154	3.443	3.716	ns
			t_H	–2.885	–3.138	–3.373	ns
	10 mA	GCLK	t_{SU}	0.712	0.797	0.868	ns
			t_H	–0.443	–0.492	–0.525	ns
		GCLK PLL	t_{SU}	3.154	3.443	3.716	ns
			t_H	–2.885	–3.138	–3.373	ns
	12 mA	GCLK	t_{SU}	0.712	0.797	0.868	ns
			t_H	–0.443	–0.492	–0.525	ns
		GCLK PLL	t_{SU}	3.154	3.443	3.716	ns
			t_H	–2.885	–3.138	–3.373	ns
16 mA	GCLK	t_{SU}	0.712	0.797	0.868	ns	
		t_H	–0.443	–0.492	–0.525	ns	
	GCLK PLL	t_{SU}	3.154	3.443	3.716	ns	
		t_H	–2.885	–3.138	–3.373	ns	

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.2V	2 mA	GCLK	t_{SU}	0.865	0.977	1.075	ns
			t_H	–0.594	–0.668	–0.727	ns
		GCLK PLL	t_{SU}	3.307	3.623	3.923	ns
			t_H	–3.036	–3.314	–3.575	ns
	4 mA	GCLK	t_{SU}	0.865	0.977	1.075	ns
			t_H	–0.594	–0.668	–0.727	ns
		GCLK PLL	t_{SU}	3.307	3.623	3.923	ns
			t_H	–3.036	–3.314	–3.575	ns
	6 mA	GCLK	t_{SU}	0.865	0.977	1.075	ns
			t_H	–0.594	–0.668	–0.727	ns
		GCLK PLL	t_{SU}	3.307	3.623	3.923	ns
			t_H	–3.036	–3.314	–3.575	ns
	8 mA	GCLK	t_{SU}	0.865	0.977	1.075	ns
			t_H	–0.594	–0.668	–0.727	ns
		GCLK PLL	t_{SU}	3.307	3.623	3.923	ns
			t_H	–3.036	–3.314	–3.575	ns
1.2V	10 mA	GCLK	t_{SU}	0.865	0.977	1.075	ns
			t_H	–0.594	–0.668	–0.727	ns
		GCLK PLL	t_{SU}	3.307	3.623	3.923	ns
			t_H	–3.036	–3.314	–3.575	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.717	0.763	0.810	ns
			t_H	–0.448	–0.458	–0.467	ns
		GCLK PLL	t_{SU}	3.185	3.454	3.675	ns
			t_H	–2.916	–3.149	–3.332	ns
	12 mA	GCLK	t_{SU}	0.717	0.763	0.810	ns
			t_H	–0.448	–0.458	–0.467	ns
		GCLK PLL	t_{SU}	3.185	3.454	3.675	ns
			t_H	–2.916	–3.149	–3.332	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.717	0.763	0.810	ns
			t_H	–0.448	–0.458	–0.467	ns
		GCLK PLL	t_{SU}	3.185	3.454	3.675	ns
			t_H	–2.916	–3.149	–3.332	ns

Table 1–70. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.769	0.842	0.917	ns
			t_H	–0.500	–0.536	–0.572	ns
		GCLK PLL	t_{SU}	3.219	3.510	3.784	ns
			t_H	–2.950	–3.204	–3.439	ns
	10 mA	GCLK	t_{SU}	0.769	0.842	0.917	ns
			t_H	–0.500	–0.536	–0.572	ns
		GCLK PLL	t_{SU}	3.219	3.510	3.784	ns
			t_H	–2.950	–3.204	–3.439	ns
	12 mA	GCLK	t_{SU}	0.769	0.842	0.917	ns
			t_H	–0.500	–0.536	–0.572	ns
		GCLK PLL	t_{SU}	3.219	3.510	3.784	ns
			t_H	–2.950	–3.204	–3.439	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.769	0.842	0.917	ns
			t_H	–0.500	–0.536	–0.572	ns
		GCLK PLL	t_{SU}	3.219	3.510	3.784	ns
			t_H	–2.950	–3.204	–3.439	ns
	16 mA	GCLK	t_{SU}	0.769	0.842	0.917	ns
			t_H	–0.500	–0.536	–0.572	ns
		GCLK PLL	t_{SU}	3.219	3.510	3.784	ns
			t_H	–2.950	–3.204	–3.439	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.769	0.842	0.917	ns
			t_H	–0.500	–0.536	–0.572	ns
		GCLK PLL	t_{SU}	3.219	3.510	3.784	ns
			t_H	–2.950	–3.204	–3.439	ns
	10 mA	GCLK	t_{SU}	0.769	0.842	0.917	ns
			t_H	–0.500	–0.536	–0.572	ns
		GCLK PLL	t_{SU}	3.219	3.510	3.784	ns
			t_H	–2.950	–3.204	–3.439	ns
	12 mA	GCLK	t_{SU}	0.769	0.842	0.917	ns
			t_H	–0.500	–0.536	–0.572	ns
		GCLK PLL	t_{SU}	3.219	3.510	3.784	ns
			t_H	–2.950	–3.204	–3.439	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.769	0.842	0.917	ns
			t_H	–0.500	–0.536	–0.572	ns
		GCLK PLL	t_{SU}	3.219	3.510	3.784	ns
			t_H	–2.950	–3.204	–3.439	ns

Table 1–70. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.724	0.801	0.880	ns	
			t_H	–0.455	–0.496	–0.536	ns	
		GCLK PLL	t_{SU}	3.174	3.469	3.747	ns	
			t_H	–2.905	–3.164	–3.403	ns	
		10 mA	GCLK	t_{SU}	0.724	0.801	0.880	ns
				t_H	–0.455	–0.496	–0.536	ns
	GCLK PLL		t_{SU}	3.174	3.469	3.747	ns	
			t_H	–2.905	–3.164	–3.403	ns	
	12 mA	GCLK	t_{SU}	0.724	0.801	0.880	ns	
			t_H	–0.455	–0.496	–0.536	ns	
		GCLK PLL	t_{SU}	3.174	3.469	3.747	ns	
			t_H	–2.905	–3.164	–3.403	ns	
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.724	0.801	0.880	ns	
			t_H	–0.455	–0.496	–0.536	ns	
		GCLK PLL	t_{SU}	3.174	3.469	3.747	ns	
			t_H	–2.905	–3.164	–3.403	ns	
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.855	0.959	1.065	ns	
			t_H	–0.584	–0.650	–0.718	ns	
		GCLK PLL	t_{SU}	3.305	3.627	3.932	ns	
			t_H	–3.034	–3.318	–3.585	ns	
	10 mA	GCLK	t_{SU}	0.855	0.959	1.065	ns	
			t_H	–0.584	–0.650	–0.718	ns	
		GCLK PLL	t_{SU}	3.305	3.627	3.932	ns	
			t_H	–3.034	–3.318	–3.585	ns	
3.0-V PCI	—	GCLK	t_{SU}	0.770	0.783	0.789	ns	
			t_H	–0.501	–0.478	–0.447	ns	
		GCLK PLL	t_{SU}	3.202	3.429	3.665	ns	
			t_H	–2.933	–3.124	–3.323	ns	
3.0-V PCI-X	—	GCLK	t_{SU}	0.770	0.783	0.789	ns	
			t_H	–0.501	–0.478	–0.447	ns	
		GCLK PLL	t_{SU}	3.202	3.429	3.665	ns	
			t_H	–2.933	–3.124	–3.323	ns	

Table 1–71. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{CO}	5.614	6.118	6.676	ns
		GCLK PLL	t_{CO}	3.185	3.466	3.778	ns
	8 mA	GCLK	t_{CO}	5.165	5.649	6.184	ns
		GCLK PLL	t_{CO}	2.736	2.997	3.286	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.251	5.740	6.280	ns
		GCLK PLL	t_{CO}	2.822	3.088	3.382	ns
3.0-V LVTTTL	4 mA	GCLK	t_{CO}	5.345	5.822	6.371	ns
		GCLK PLL	t_{CO}	2.916	3.170	3.473	ns
	8 mA	GCLK	t_{CO}	5.087	5.562	6.089	ns
		GCLK PLL	t_{CO}	2.658	2.910	3.191	ns
	12 mA	GCLK	t_{CO}	4.963	5.440	5.968	ns
		GCLK PLL	t_{CO}	2.534	2.788	3.070	ns
	16 mA	GCLK	t_{CO}	4.913	5.375	5.889	ns
		GCLK PLL	t_{CO}	2.484	2.723	2.991	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.085	5.561	6.088	ns
		GCLK PLL	t_{CO}	2.656	2.909	3.190	ns
	8 mA	GCLK	t_{CO}	4.916	5.379	5.904	ns
		GCLK PLL	t_{CO}	2.487	2.727	3.006	ns
	12 mA	GCLK	t_{CO}	4.875	5.338	5.853	ns
		GCLK PLL	t_{CO}	2.446	2.686	2.955	ns
	16 mA	GCLK	t_{CO}	4.855	5.319	5.834	ns
		GCLK PLL	t_{CO}	2.426	2.667	2.936	ns
2.5V	4 mA	GCLK	t_{CO}	5.467	5.960	6.517	ns
		GCLK PLL	t_{CO}	3.038	3.308	3.619	ns
	8 mA	GCLK	t_{CO}	5.195	5.683	6.227	ns
		GCLK PLL	t_{CO}	2.766	3.031	3.329	ns
	12 mA	GCLK	t_{CO}	5.077	5.561	6.103	ns
		GCLK PLL	t_{CO}	2.648	2.909	3.205	ns
16 mA	GCLK	t_{CO}	5.025	5.505	6.043	ns	
	GCLK PLL	t_{CO}	2.596	2.853	3.145	ns	

Table 1–71. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t _{CO}	6.640	7.268	7.982	ns	
		GCLK PLL	t _{CO}	4.211	4.616	5.084	ns	
	4 mA	GCLK	t _{CO}	6.066	6.682	7.370	ns	
		GCLK PLL	t _{CO}	3.637	4.030	4.472	ns	
	6 mA	GCLK	t _{CO}	5.796	6.377	7.029	ns	
		GCLK PLL	t _{CO}	3.367	3.725	4.131	ns	
	8 mA	GCLK	t _{CO}	5.682	6.261	6.900	ns	
		GCLK PLL	t _{CO}	3.253	3.609	4.002	ns	
	10 mA	GCLK	t _{CO}	5.619	6.195	6.836	ns	
		GCLK PLL	t _{CO}	3.190	3.543	3.938	ns	
	12 mA	GCLK	t _{CO}	5.554	6.114	6.742	ns	
		GCLK PLL	t _{CO}	3.125	3.462	3.844	ns	
	16 mA	GCLK	t _{CO}	5.500	6.060	6.679	ns	
		GCLK PLL	t _{CO}	3.071	3.408	3.781	ns	
	1.5V	2 mA	GCLK	t _{CO}	7.048	7.836	8.732	ns
			GCLK PLL	t _{CO}	4.619	5.184	5.834	ns
		4 mA	GCLK	t _{CO}	6.477	7.173	7.972	ns
			GCLK PLL	t _{CO}	4.048	4.521	5.074	ns
6 mA		GCLK	t _{CO}	6.280	6.963	7.749	ns	
		GCLK PLL	t _{CO}	3.851	4.311	4.851	ns	
8 mA		GCLK	t _{CO}	6.162	6.827	7.579	ns	
		GCLK PLL	t _{CO}	3.733	4.175	4.681	ns	
10 mA		GCLK	t _{CO}	6.095	6.757	7.512	ns	
		GCLK PLL	t _{CO}	3.666	4.105	4.614	ns	
12 mA		GCLK	t _{CO}	6.059	6.708	7.452	ns	
		GCLK PLL	t _{CO}	3.630	4.056	4.554	ns	
16 mA		GCLK	t _{CO}	5.941	6.582	7.294	ns	
		GCLK PLL	t _{CO}	3.512	3.930	4.396	ns	
1.2V		2 mA	GCLK	t _{CO}	8.124	9.201	10.466	ns
			GCLK PLL	t _{CO}	5.695	6.549	7.568	ns
		4 mA	GCLK	t _{CO}	7.625	8.624	9.795	ns
			GCLK PLL	t _{CO}	5.196	5.972	6.897	ns
	6 mA	GCLK	t _{CO}	7.444	8.410	9.541	ns	
		GCLK PLL	t _{CO}	5.015	5.758	6.643	ns	
	8 mA	GCLK	t _{CO}	7.361	8.317	9.435	ns	
		GCLK PLL	t _{CO}	4.932	5.665	6.537	ns	
	10mA	GCLK	t _{CO}	7.216	8.133	9.193	ns	
		GCLK PLL	t _{CO}	4.787	5.481	6.295	ns	
	12 mA	GCLK	t _{CO}	7.190	8.105	9.165	ns	
		GCLK PLL	t _{CO}	4.761	5.453	6.267	ns	

Table 1–71. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t _{CO}	5.098	5.575	6.104	ns
		GCLK PLL	t _{CO}	2.640	2.891	3.206	ns
	12 mA	GCLK	t _{CO}	5.063	5.539	6.067	ns
		GCLK PLL	t _{CO}	2.605	2.855	3.169	ns
SSTL-2 Class II	16 mA	GCLK	t _{CO}	5.006	5.477	6.000	ns
		GCLK PLL	t _{CO}	2.548	2.793	3.102	ns
SSTL-18 Class I	8 mA	GCLK	t _{CO}	5.502	6.049	6.656	ns
		GCLK PLL	t _{CO}	3.044	3.365	3.758	ns
	10 mA	GCLK	t _{CO}	5.471	6.011	6.610	ns
		GCLK PLL	t _{CO}	3.013	3.327	3.712	ns
	12 mA	GCLK	t _{CO}	5.456	5.996	6.592	ns
		GCLK PLL	t _{CO}	2.998	3.312	3.694	ns
SSTL-18 Class II	12 mA	GCLK	t _{CO}	5.443	5.981	6.579	ns
		GCLK PLL	t _{CO}	2.985	3.297	3.681	ns
	16 mA	GCLK	t _{CO}	5.424	5.962	6.559	ns
		GCLK PLL	t _{CO}	2.966	3.278	3.661	ns
1.8-V HSTL Class I	8 mA	GCLK	t _{CO}	5.483	6.021	6.618	ns
		GCLK PLL	t _{CO}	3.025	3.337	3.720	ns
	10 mA	GCLK	t _{CO}	5.474	6.014	6.615	ns
		GCLK PLL	t _{CO}	3.016	3.330	3.717	ns
	12 mA	GCLK	t _{CO}	5.453	5.989	6.584	ns
		GCLK PLL	t _{CO}	2.995	3.305	3.686	ns
1.8-V HSTL Class II	16 mA	GCLK	t _{CO}	5.425	5.956	6.548	ns
		GCLK PLL	t _{CO}	2.967	3.272	3.650	ns
1.5-V HSTL Class I	8 mA	GCLK	t _{CO}	5.988	6.616	7.325	ns
		GCLK PLL	t _{CO}	3.530	3.932	4.427	ns
	10 mA	GCLK	t _{CO}	5.975	6.597	7.300	ns
		GCLK PLL	t _{CO}	3.517	3.913	4.402	ns
	12 mA	GCLK	t _{CO}	5.966	6.591	7.296	ns
		GCLK PLL	t _{CO}	3.508	3.907	4.398	ns
1.5-V HSTL Class II	16 mA	GCLK	t _{CO}	5.923	6.538	7.232	ns
		GCLK PLL	t _{CO}	3.465	3.854	4.334	ns
1.2-V HSTL Class I	8 mA	GCLK	t _{CO}	7.159	8.056	9.103	ns
		GCLK PLL	t _{CO}	4.701	5.372	6.205	ns
	10 mA	GCLK	t _{CO}	7.081	7.950	8.948	ns
		GCLK PLL	t _{CO}	4.623	5.266	6.050	ns
	12 mA	GCLK	t _{CO}	7.079	7.950	8.952	ns
		GCLK PLL	t _{CO}	4.621	5.266	6.054	ns
1.2-V HSTL Class II	14 mA	GCLK	t _{CO}	7.022	7.879	8.871	ns
		GCLK PLL	t _{CO}	4.564	5.195	5.973	ns

Table 1–71. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V PCI	—	GCLK	t_{CO}	5.177	5.649	6.172	ns
		GCLK PLL	t_{CO}	2.748	2.997	3.274	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.177	5.649	6.172	ns
		GCLK PLL	t_{CO}	2.748	2.997	3.274	ns

Table 1–72. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{CO}	5.552	6.071	6.614	ns
		GCLK PLL	t_{CO}	3.110	3.391	3.733	ns
	8 mA	GCLK	t_{CO}	5.104	5.607	6.132	ns
		GCLK PLL	t_{CO}	2.662	2.927	3.251	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.198	5.694	6.223	ns
		GCLK PLL	t_{CO}	2.756	3.014	3.342	ns
3.0-V LVTTTL	4 mA	GCLK	t_{CO}	5.303	5.792	6.314	ns
		GCLK PLL	t_{CO}	2.861	3.112	3.433	ns
	8 mA	GCLK	t_{CO}	5.047	5.537	6.053	ns
		GCLK PLL	t_{CO}	2.605	2.857	3.172	ns
	12 mA	GCLK	t_{CO}	4.932	5.411	5.926	ns
		GCLK PLL	t_{CO}	2.490	2.731	3.045	ns
	16 mA	GCLK	t_{CO}	4.882	5.357	5.859	ns
		GCLK PLL	t_{CO}	2.440	2.677	2.978	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.045	5.536	6.051	ns
		GCLK PLL	t_{CO}	2.603	2.856	3.170	ns
	8 mA	GCLK	t_{CO}	4.883	5.359	5.862	ns
		GCLK PLL	t_{CO}	2.441	2.679	2.981	ns
	12 mA	GCLK	t_{CO}	4.843	5.319	5.823	ns
		GCLK PLL	t_{CO}	2.401	2.639	2.942	ns
	16 mA	GCLK	t_{CO}	4.822	5.299	5.803	ns
		GCLK PLL	t_{CO}	2.380	2.619	2.922	ns
2.5V	4 mA	GCLK	t_{CO}	5.429	5.931	6.470	ns
		GCLK PLL	t_{CO}	2.987	3.251	3.589	ns
	8 mA	GCLK	t_{CO}	5.160	5.662	6.194	ns
		GCLK PLL	t_{CO}	2.718	2.982	3.313	ns
	12 mA	GCLK	t_{CO}	5.046	5.542	6.070	ns
		GCLK PLL	t_{CO}	2.604	2.862	3.189	ns
16 mA	GCLK	t_{CO}	4.993	5.486	6.012	ns	
	GCLK PLL	t_{CO}	2.551	2.806	3.131	ns	

Table 1–72. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t _{CO}	6.589	7.229	7.927	ns	
		GCLK PLL	t _{CO}	4.151	4.560	5.094	ns	
	4 mA	GCLK	t _{CO}	6.034	6.659	7.335	ns	
		GCLK PLL	t _{CO}	3.596	3.990	4.502	ns	
	6 mA	GCLK	t _{CO}	5.772	6.364	7.003	ns	
		GCLK PLL	t _{CO}	3.334	3.695	4.170	ns	
	8 mA	GCLK	t _{CO}	5.656	6.236	6.858	ns	
		GCLK PLL	t _{CO}	3.218	3.567	4.025	ns	
	10 mA	GCLK	t _{CO}	5.595	6.182	6.811	ns	
		GCLK PLL	t _{CO}	3.157	3.513	3.978	ns	
	12 mA	GCLK	t _{CO}	5.535	6.106	6.722	ns	
		GCLK PLL	t _{CO}	3.097	3.437	3.889	ns	
	16 mA	GCLK	t _{CO}	5.491	6.057	6.667	ns	
		GCLK PLL	t _{CO}	3.053	3.388	3.834	ns	
	1.5V	2 mA	GCLK	t _{CO}	7.003	7.800	8.679	ns
			GCLK PLL	t _{CO}	4.565	5.131	5.846	ns
		4 mA	GCLK	t _{CO}	6.444	7.157	7.937	ns
			GCLK PLL	t _{CO}	4.006	4.488	5.104	ns
6 mA		GCLK	t _{CO}	6.254	6.952	7.721	ns	
		GCLK PLL	t _{CO}	3.816	4.283	4.888	ns	
8 mA		GCLK	t _{CO}	6.156	6.841	7.581	ns	
		GCLK PLL	t _{CO}	3.718	4.172	4.748	ns	
10 mA		GCLK	t _{CO}	6.089	6.769	7.512	ns	
		GCLK PLL	t _{CO}	3.651	4.100	4.679	ns	
12 mA		GCLK	t _{CO}	6.049	6.718	7.448	ns	
		GCLK PLL	t _{CO}	3.611	4.049	4.615	ns	
16 mA		GCLK	t _{CO}	5.977	6.637	7.360	ns	
		GCLK PLL	t _{CO}	3.539	3.968	4.527	ns	
1.2V		2 mA	GCLK	t _{CO}	8.089	9.175	10.425	ns
			GCLK PLL	t _{CO}	5.651	6.506	7.592	ns
		4 mA	GCLK	t _{CO}	7.598	8.609	9.766	ns
			GCLK PLL	t _{CO}	5.160	5.940	6.933	ns
	6 mA	GCLK	t _{CO}	7.443	8.425	9.551	ns	
		GCLK PLL	t _{CO}	5.005	5.756	6.718	ns	
	8 mA	GCLK	t _{CO}	7.355	8.327	9.438	ns	
		GCLK PLL	t _{CO}	4.917	5.658	6.605	ns	
	10 mA	GCLK	t _{CO}	7.237	8.183	9.259	ns	
		GCLK PLL	t _{CO}	4.799	5.514	6.426	ns	

Table 1–72. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.059	5.534	6.052	ns
		GCLK PLL	t_{CO}	2.645	2.897	3.171	ns
	12 mA	GCLK	t_{CO}	5.027	5.500	6.016	ns
		GCLK PLL	t_{CO}	2.613	2.863	3.135	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.976	5.447	5.959	ns
		GCLK PLL	t_{CO}	2.562	2.810	3.078	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.476	6.018	6.605	ns
		GCLK PLL	t_{CO}	3.096	3.420	3.724	ns
	10 mA	GCLK	t_{CO}	5.457	5.994	6.575	ns
		GCLK PLL	t_{CO}	3.077	3.396	3.694	ns
	12 mA	GCLK	t_{CO}	5.435	5.970	6.548	ns
		GCLK PLL	t_{CO}	3.055	3.372	3.667	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.427	5.962	6.541	ns
		GCLK PLL	t_{CO}	3.047	3.364	3.660	ns
	16 mA	GCLK	t_{CO}	5.412	5.948	6.527	ns
		GCLK PLL	t_{CO}	3.032	3.350	3.646	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.456	5.990	6.566	ns
		GCLK PLL	t_{CO}	3.076	3.392	3.685	ns
	10 mA	GCLK	t_{CO}	5.449	5.986	6.565	ns
		GCLK PLL	t_{CO}	3.069	3.388	3.684	ns
	12 mA	GCLK	t_{CO}	5.439	5.972	6.548	ns
		GCLK PLL	t_{CO}	3.059	3.374	3.667	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.406	5.934	6.506	ns
		GCLK PLL	t_{CO}	3.026	3.336	3.625	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.961	6.589	7.274	ns
		GCLK PLL	t_{CO}	3.581	3.991	4.393	ns
	10 mA	GCLK	t_{CO}	5.959	6.584	7.265	ns
		GCLK PLL	t_{CO}	3.579	3.986	4.384	ns
	12 mA	GCLK	t_{CO}	5.950	6.577	7.261	ns
		GCLK PLL	t_{CO}	3.570	3.979	4.380	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.911	6.531	7.208	ns
		GCLK PLL	t_{CO}	3.531	3.933	4.327	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.152	8.054	9.087	ns
		GCLK PLL	t_{CO}	4.772	5.456	6.206	ns
	10 mA	GCLK	t_{CO}	7.069	7.940	8.923	ns
		GCLK PLL	t_{CO}	4.689	5.342	6.042	ns
3.0-V PCI	—	GCLK	t_{CO}	5.141	5.624	6.135	ns
		GCLK PLL	t_{CO}	2.699	2.944	3.254	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.141	5.624	6.135	ns
		GCLK PLL	t_{CO}	2.699	2.944	3.254	ns

Table 1–73. EP3C40 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.566	0.616	0.641	ns
			t_H	–0.298	–0.313	–0.301	ns
		GCLK PLL	t_{SU}	3.021	3.294	3.548	ns
			t_H	–2.753	–2.991	–3.208	ns
LVDS_E_3R	—	GCLK	t_{CO}	5.041	5.551	6.095	ns
		GCLK PLL	t_{CO}	5.051	5.561	6.105	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	5.041	5.551	6.095	ns
		GCLK PLL	t_{CO}	5.051	5.561	6.105	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.041	5.551	6.095	ns
		GCLK PLL	t_{CO}	5.051	5.561	6.105	ns
RSDS_E_1R	—	GCLK	t_{CO}	5.041	5.551	6.095	ns
		GCLK PLL	t_{CO}	5.051	5.561	6.105	ns
RSDS_E_3R	—	GCLK	t_{CO}	5.041	5.551	6.095	ns
		GCLK PLL	t_{CO}	5.051	5.561	6.105	ns

Table 1–74. EP3C40 Row Pin Differential I/O Timing Parameters

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.615	0.668	0.704	ns
			t_H	–0.348	–0.366	–0.363	ns
			t_{CO}	4.236	4.643	5.076	ns
		GCLK PLL	t_{SU}	3.038	3.314	3.578	ns
			t_H	–2.771	–3.012	–3.237	ns
			t_{CO}	1.802	1.986	2.189	ns
mini-LVDS	—	GCLK	t_{CO}	4.236	4.643	5.076	ns
		GCLK PLL	t_{CO}	1.802	1.986	2.189	ns
PPDS	—	GCLK	t_{CO}	4.236	4.643	5.076	ns
		GCLK PLL	t_{CO}	1.802	1.986	2.189	ns
RSDS	—	GCLK	t_{CO}	4.236	4.643	5.076	ns
		GCLK PLL	t_{CO}	1.802	1.986	2.189	ns

EP3C55 I/O Timing Parameters

Tables 1–75 through 1–80 show the maximum I/O timing parameters for EP3C55 devices.

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	0.770	0.769	0.740	ns
			t_H	–0.500	–0.464	–0.399	ns
		GCLK PLL	t_{SU}	3.115	3.318	3.497	ns
			t_H	–2.845	–3.013	–3.156	ns
	8 mA	GCLK	t_{SU}	0.770	0.769	0.740	ns
			t_H	–0.500	–0.464	–0.399	ns
		GCLK PLL	t_{SU}	3.115	3.318	3.497	ns
			t_H	–2.845	–3.013	–3.156	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.770	0.769	0.740	ns
			t_H	–0.500	–0.464	–0.399	ns
		GCLK PLL	t_{SU}	3.115	3.318	3.497	ns
			t_H	–2.845	–3.013	–3.156	ns
3.0-V LVTTTL	4 mA	GCLK	t_{SU}	0.770	0.769	0.740	ns
			t_H	–0.500	–0.464	–0.399	ns
		GCLK PLL	t_{SU}	3.115	3.318	3.497	ns
			t_H	–2.845	–3.013	–3.156	ns
	8 mA	GCLK	t_{SU}	0.770	0.769	0.740	ns
			t_H	–0.500	–0.464	–0.399	ns
		GCLK PLL	t_{SU}	3.115	3.318	3.497	ns
			t_H	–2.845	–3.013	–3.156	ns
	12 mA	GCLK	t_{SU}	0.770	0.769	0.740	ns
			t_H	–0.500	–0.464	–0.399	ns
		GCLK PLL	t_{SU}	3.115	3.318	3.497	ns
			t_H	–2.845	–3.013	–3.156	ns
	16 mA	GCLK	t_{SU}	0.770	0.769	0.740	ns
			t_H	–0.500	–0.464	–0.399	ns
		GCLK PLL	t_{SU}	3.115	3.318	3.497	ns
			t_H	–2.845	–3.013	–3.156	ns

Table 1–75. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.770	0.769	0.740	ns
			t_H	–0.500	–0.464	–0.399	ns
		GCLK PLL	t_{SU}	3.115	3.318	3.497	ns
			t_H	–2.845	–3.013	–3.156	ns
	8 mA	GCLK	t_{SU}	0.770	0.769	0.740	ns
			t_H	–0.500	–0.464	–0.399	ns
		GCLK PLL	t_{SU}	3.115	3.318	3.497	ns
			t_H	–2.845	–3.013	–3.156	ns
	12 mA	GCLK	t_{SU}	0.770	0.769	0.740	ns
			t_H	–0.500	–0.464	–0.399	ns
		GCLK PLL	t_{SU}	3.115	3.318	3.497	ns
			t_H	–2.845	–3.013	–3.156	ns
	16 mA	GCLK	t_{SU}	0.770	0.769	0.740	ns
			t_H	–0.500	–0.464	–0.399	ns
		GCLK PLL	t_{SU}	3.115	3.318	3.497	ns
			t_H	–2.845	–3.013	–3.156	ns
2.5V	4 mA	GCLK	t_{SU}	0.713	0.724	0.708	ns
			t_H	–0.443	–0.420	–0.368	ns
		GCLK PLL	t_{SU}	3.058	3.273	3.465	ns
			t_H	–2.788	–2.969	–3.125	ns
	8 mA	GCLK	t_{SU}	0.713	0.724	0.708	ns
			t_H	–0.443	–0.420	–0.368	ns
		GCLK PLL	t_{SU}	3.058	3.273	3.465	ns
			t_H	–2.788	–2.969	–3.125	ns
	12 mA	GCLK	t_{SU}	0.713	0.724	0.708	ns
			t_H	–0.443	–0.420	–0.368	ns
		GCLK PLL	t_{SU}	3.058	3.273	3.465	ns
			t_H	–2.788	–2.969	–3.125	ns
	16 mA	GCLK	t_{SU}	0.713	0.724	0.708	ns
			t_H	–0.443	–0.420	–0.368	ns
		GCLK PLL	t_{SU}	3.058	3.273	3.465	ns
			t_H	–2.788	–2.969	–3.125	ns

Table 1–75. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.8V	2 mA	GCLK	t_{SU}	0.648	0.685	0.695	ns
			t_H	–0.380	–0.382	–0.354	ns
		GCLK PLL	t_{SU}	2.993	3.234	3.452	ns
			t_H	–2.725	–2.931	–3.111	ns
	4 mA	GCLK	t_{SU}	0.648	0.685	0.695	ns
			t_H	–0.380	–0.382	–0.354	ns
		GCLK PLL	t_{SU}	2.993	3.234	3.452	ns
			t_H	–2.725	–2.931	–3.111	ns
	6 mA	GCLK	t_{SU}	0.648	0.685	0.695	ns
			t_H	–0.380	–0.382	–0.354	ns
		GCLK PLL	t_{SU}	2.993	3.234	3.452	ns
			t_H	–2.725	–2.931	–3.111	ns
	8 mA	GCLK	t_{SU}	0.648	0.685	0.695	ns
			t_H	–0.380	–0.382	–0.354	ns
		GCLK PLL	t_{SU}	2.993	3.234	3.452	ns
			t_H	–2.725	–2.931	–3.111	ns
	10 mA	GCLK	t_{SU}	0.648	0.685	0.695	ns
			t_H	–0.380	–0.382	–0.354	ns
		GCLK PLL	t_{SU}	2.993	3.234	3.452	ns
			t_H	–2.725	–2.931	–3.111	ns
	12 mA	GCLK	t_{SU}	0.648	0.685	0.695	ns
			t_H	–0.380	–0.382	–0.354	ns
		GCLK PLL	t_{SU}	2.993	3.234	3.452	ns
			t_H	–2.725	–2.931	–3.111	ns
16 mA	GCLK	t_{SU}	0.648	0.685	0.695	ns	
		t_H	–0.380	–0.382	–0.354	ns	
	GCLK PLL	t_{SU}	2.993	3.234	3.452	ns	
		t_H	–2.725	–2.931	–3.111	ns	

Table 1–75. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	0.717	0.777	0.812	ns
			t_H	–0.447	–0.472	–0.469	ns
		GCLK PLL	t_{SU}	3.062	3.326	3.569	ns
			t_H	–2.792	–3.021	–3.226	ns
	4 mA	GCLK	t_{SU}	0.717	0.777	0.812	ns
			t_H	–0.447	–0.472	–0.469	ns
		GCLK PLL	t_{SU}	3.062	3.326	3.569	ns
			t_H	–2.792	–3.021	–3.226	ns
	6 mA	GCLK	t_{SU}	0.717	0.777	0.812	ns
			t_H	–0.447	–0.472	–0.469	ns
		GCLK PLL	t_{SU}	3.062	3.326	3.569	ns
			t_H	–2.792	–3.021	–3.226	ns
	8 mA	GCLK	t_{SU}	0.717	0.777	0.812	ns
			t_H	–0.447	–0.472	–0.469	ns
		GCLK PLL	t_{SU}	3.062	3.326	3.569	ns
			t_H	–2.792	–3.021	–3.226	ns
	10 mA	GCLK	t_{SU}	0.717	0.777	0.812	ns
			t_H	–0.447	–0.472	–0.469	ns
		GCLK PLL	t_{SU}	3.062	3.326	3.569	ns
			t_H	–2.792	–3.021	–3.226	ns
	12 mA	GCLK	t_{SU}	0.717	0.777	0.812	ns
			t_H	–0.447	–0.472	–0.469	ns
		GCLK PLL	t_{SU}	3.062	3.326	3.569	ns
			t_H	–2.792	–3.021	–3.226	ns
16 mA	GCLK	t_{SU}	0.717	0.777	0.812	ns	
		t_H	–0.447	–0.472	–0.469	ns	
	GCLK PLL	t_{SU}	3.062	3.326	3.569	ns	
		t_H	–2.792	–3.021	–3.226	ns	

Table 1–75. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.2V	2 mA	GCLK	t_{SU}	0.869	0.957	1.018	ns
			t_H	–0.597	–0.648	–0.671	ns
		GCLK PLL	t_{SU}	3.214	3.506	3.775	ns
			t_H	–2.942	–3.197	–3.428	ns
	4 mA	GCLK	t_{SU}	0.869	0.957	1.018	ns
			t_H	–0.597	–0.648	–0.671	ns
		GCLK PLL	t_{SU}	3.214	3.506	3.775	ns
			t_H	–2.942	–3.197	–3.428	ns
	6 mA	GCLK	t_{SU}	0.869	0.957	1.018	ns
			t_H	–0.597	–0.648	–0.671	ns
		GCLK PLL	t_{SU}	3.214	3.506	3.775	ns
			t_H	–2.942	–3.197	–3.428	ns
	8 mA	GCLK	t_{SU}	0.869	0.957	1.018	ns
			t_H	–0.597	–0.648	–0.671	ns
		GCLK PLL	t_{SU}	3.214	3.506	3.775	ns
			t_H	–2.942	–3.197	–3.428	ns
	10 mA	GCLK	t_{SU}	0.869	0.957	1.018	ns
			t_H	–0.597	–0.648	–0.671	ns
		GCLK PLL	t_{SU}	3.214	3.506	3.775	ns
			t_H	–2.942	–3.197	–3.428	ns
	12 mA	GCLK	t_{SU}	0.869	0.957	1.018	ns
			t_H	–0.597	–0.648	–0.671	ns
		GCLK PLL	t_{SU}	3.214	3.506	3.775	ns
			t_H	–2.942	–3.197	–3.428	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.703	0.745	0.755	ns
			t_H	–0.433	–0.441	–0.413	ns
		GCLK PLL	t_{SU}	3.043	3.289	3.512	ns
			t_H	–2.773	–2.985	–3.170	ns
	12 mA	GCLK	t_{SU}	0.703	0.745	0.755	ns
			t_H	–0.433	–0.441	–0.413	ns
		GCLK PLL	t_{SU}	3.043	3.289	3.512	ns
			t_H	–2.773	–2.985	–3.170	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.703	0.745	0.755	ns
			t_H	–0.433	–0.441	–0.413	ns
		GCLK PLL	t_{SU}	3.043	3.289	3.512	ns
			t_H	–2.773	–2.985	–3.170	ns

Table 1–75. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.764	0.834	0.870	ns
			t_H	–0.494	–0.528	–0.526	ns
		GCLK PLL	t_{SU}	3.104	3.378	3.627	ns
			t_H	–2.834	–3.072	–3.283	ns
	10 mA	GCLK	t_{SU}	0.764	0.834	0.870	ns
			t_H	–0.494	–0.528	–0.526	ns
		GCLK PLL	t_{SU}	3.104	3.378	3.627	ns
			t_H	–2.834	–3.072	–3.283	ns
	12 mA	GCLK	t_{SU}	0.764	0.834	0.870	ns
			t_H	–0.494	–0.528	–0.526	ns
		GCLK PLL	t_{SU}	3.104	3.378	3.627	ns
			t_H	–2.834	–3.072	–3.283	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.764	0.834	0.870	ns
			t_H	–0.494	–0.528	–0.526	ns
		GCLK PLL	t_{SU}	3.104	3.378	3.627	ns
			t_H	–2.834	–3.072	–3.283	ns
	16 mA	GCLK	t_{SU}	0.764	0.834	0.870	ns
			t_H	–0.494	–0.528	–0.526	ns
		GCLK PLL	t_{SU}	3.104	3.378	3.627	ns
			t_H	–2.834	–3.072	–3.283	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.764	0.834	0.870	ns
			t_H	–0.494	–0.528	–0.526	ns
		GCLK PLL	t_{SU}	3.104	3.378	3.627	ns
			t_H	–2.834	–3.072	–3.283	ns
	10 mA	GCLK	t_{SU}	0.764	0.834	0.870	ns
			t_H	–0.494	–0.528	–0.526	ns
		GCLK PLL	t_{SU}	3.104	3.378	3.627	ns
			t_H	–2.834	–3.072	–3.283	ns
	12 mA	GCLK	t_{SU}	0.764	0.834	0.870	ns
			t_H	–0.494	–0.528	–0.526	ns
		GCLK PLL	t_{SU}	3.104	3.378	3.627	ns
			t_H	–2.834	–3.072	–3.283	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.764	0.834	0.870	ns
			t_H	–0.494	–0.528	–0.526	ns
		GCLK PLL	t_{SU}	3.104	3.378	3.627	ns
			t_H	–2.834	–3.072	–3.283	ns

Table 1–75. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.720	0.794	0.836	ns
			t_H	–0.450	–0.489	–0.493	ns
		GCLK PLL	t_{SU}	3.060	3.338	3.593	ns
			t_H	–2.790	–3.033	–3.250	ns
	10 mA	GCLK	t_{SU}	0.720	0.794	0.836	ns
			t_H	–0.450	–0.489	–0.493	ns
		GCLK PLL	t_{SU}	3.060	3.338	3.593	ns
			t_H	–2.790	–3.033	–3.250	ns
	12 mA	GCLK	t_{SU}	0.720	0.794	0.836	ns
			t_H	–0.450	–0.489	–0.493	ns
		GCLK PLL	t_{SU}	3.060	3.338	3.593	ns
			t_H	–2.790	–3.033	–3.250	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.720	0.794	0.836	ns
			t_H	–0.450	–0.489	–0.493	ns
		GCLK PLL	t_{SU}	3.060	3.338	3.593	ns
			t_H	–2.790	–3.033	–3.250	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.852	0.953	1.020	ns
			t_H	–0.580	–0.644	–0.673	ns
		GCLK PLL	t_{SU}	3.192	3.497	3.777	ns
			t_H	–2.920	–3.188	–3.430	ns
	10 mA	GCLK	t_{SU}	0.852	0.953	1.020	ns
			t_H	–0.580	–0.644	–0.673	ns
		GCLK PLL	t_{SU}	3.192	3.497	3.777	ns
			t_H	–2.920	–3.188	–3.430	ns
	12 mA	GCLK	t_{SU}	0.852	0.953	1.020	ns
			t_H	–0.580	–0.644	–0.673	ns
		GCLK PLL	t_{SU}	3.192	3.497	3.777	ns
			t_H	–2.920	–3.188	–3.430	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	0.852	0.953	1.020	ns
			t_H	–0.580	–0.644	–0.673	ns
		GCLK PLL	t_{SU}	3.192	3.497	3.777	ns
			t_H	–2.920	–3.188	–3.430	ns
3.0-V PCI	—	GCLK	t_{SU}	0.766	0.765	0.735	ns
			t_H	–0.496	–0.460	–0.394	ns
		GCLK PLL	t_{SU}	3.111	3.314	3.492	ns
			t_H	–2.841	–3.009	–3.151	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.766	0.765	0.735	ns
			t_H	–0.496	–0.460	–0.394	ns
		GCLK PLL	t_{SU}	3.111	3.314	3.492	ns
			t_H	–2.841	–3.009	–3.151	ns

Table 1–76. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	0.795	0.785	0.764	ns
			t_H	–0.526	–0.480	–0.422	ns
		GCLK PLL	t_{SU}	3.127	3.333	3.515	ns
			t_H	–2.858	–3.028	–3.173	ns
	8 mA	GCLK	t_{SU}	0.795	0.785	0.764	ns
			t_H	–0.526	–0.480	–0.422	ns
		GCLK PLL	t_{SU}	3.127	3.333	3.515	ns
			t_H	–2.858	–3.028	–3.173	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.795	0.785	0.764	ns
			t_H	–0.526	–0.480	–0.422	ns
		GCLK PLL	t_{SU}	3.127	3.333	3.515	ns
			t_H	–2.858	–3.028	–3.173	ns
3.0-V LVTTTL	4 mA	GCLK	t_{SU}	0.795	0.785	0.764	ns
			t_H	–0.526	–0.480	–0.422	ns
		GCLK PLL	t_{SU}	3.127	3.333	3.515	ns
			t_H	–2.858	–3.028	–3.173	ns
	8 mA	GCLK	t_{SU}	0.795	0.785	0.764	ns
			t_H	–0.526	–0.480	–0.422	ns
		GCLK PLL	t_{SU}	3.127	3.333	3.515	ns
			t_H	–2.858	–3.028	–3.173	ns
	12 mA	GCLK	t_{SU}	0.795	0.785	0.764	ns
			t_H	–0.526	–0.480	–0.422	ns
		GCLK PLL	t_{SU}	3.127	3.333	3.515	ns
			t_H	–2.858	–3.028	–3.173	ns
	16 mA	GCLK	t_{SU}	0.795	0.785	0.764	ns
			t_H	–0.526	–0.480	–0.422	ns
		GCLK PLL	t_{SU}	3.127	3.333	3.515	ns
			t_H	–2.858	–3.028	–3.173	ns

Table 1–76. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.795	0.785	0.764	ns
			t_H	–0.526	–0.480	–0.422	ns
		GCLK PLL	t_{SU}	3.127	3.333	3.515	ns
			t_H	–2.858	–3.028	–3.173	ns
	8 mA	GCLK	t_{SU}	0.795	0.785	0.764	ns
			t_H	–0.526	–0.480	–0.422	ns
		GCLK PLL	t_{SU}	3.127	3.333	3.515	ns
			t_H	–2.858	–3.028	–3.173	ns
	12 mA	GCLK	t_{SU}	0.795	0.785	0.764	ns
			t_H	–0.526	–0.480	–0.422	ns
		GCLK PLL	t_{SU}	3.127	3.333	3.515	ns
			t_H	–2.858	–3.028	–3.173	ns
	16 mA	GCLK	t_{SU}	0.795	0.785	0.764	ns
			t_H	–0.526	–0.480	–0.422	ns
		GCLK PLL	t_{SU}	3.127	3.333	3.515	ns
			t_H	–2.858	–3.028	–3.173	ns
2.5V	4 mA	GCLK	t_{SU}	0.738	0.741	0.735	ns
			t_H	–0.469	–0.437	–0.394	ns
		GCLK PLL	t_{SU}	3.070	3.289	3.486	ns
			t_H	–2.801	–2.985	–3.145	ns
	8 mA	GCLK	t_{SU}	0.738	0.741	0.735	ns
			t_H	–0.469	–0.437	–0.394	ns
		GCLK PLL	t_{SU}	3.070	3.289	3.486	ns
			t_H	–2.801	–2.985	–3.145	ns
	12 mA	GCLK	t_{SU}	0.738	0.741	0.735	ns
			t_H	–0.469	–0.437	–0.394	ns
		GCLK PLL	t_{SU}	3.070	3.289	3.486	ns
			t_H	–2.801	–2.985	–3.145	ns
	16 mA	GCLK	t_{SU}	0.738	0.741	0.735	ns
			t_H	–0.469	–0.437	–0.394	ns
		GCLK PLL	t_{SU}	3.070	3.289	3.486	ns
			t_H	–2.801	–2.985	–3.145	ns

Table 1–76. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	-6	-7	-8	Unit
1.8V	2 mA	GCLK	t_{SU}	0.674	0.702	0.721	ns
			t_H	-0.407	-0.399	-0.379	ns
		GCLK PLL	t_{SU}	3.006	3.250	3.472	ns
			t_H	-2.739	-2.947	-3.130	ns
	4 mA	GCLK	t_{SU}	0.674	0.702	0.721	ns
			t_H	-0.407	-0.399	-0.379	ns
		GCLK PLL	t_{SU}	3.006	3.250	3.472	ns
			t_H	-2.739	-2.947	-3.130	ns
	6 mA	GCLK	t_{SU}	0.674	0.702	0.721	ns
			t_H	-0.407	-0.399	-0.379	ns
		GCLK PLL	t_{SU}	3.006	3.250	3.472	ns
			t_H	-2.739	-2.947	-3.130	ns
	8 mA	GCLK	t_{SU}	0.674	0.702	0.721	ns
			t_H	-0.407	-0.399	-0.379	ns
		GCLK PLL	t_{SU}	3.006	3.250	3.472	ns
			t_H	-2.739	-2.947	-3.130	ns
	10 mA	GCLK	t_{SU}	0.674	0.702	0.721	ns
			t_H	-0.407	-0.399	-0.379	ns
		GCLK PLL	t_{SU}	3.006	3.250	3.472	ns
			t_H	-2.739	-2.947	-3.130	ns
	12 mA	GCLK	t_{SU}	0.674	0.702	0.721	ns
			t_H	-0.407	-0.399	-0.379	ns
		GCLK PLL	t_{SU}	3.006	3.250	3.472	ns
			t_H	-2.739	-2.947	-3.130	ns
	16 mA	GCLK	t_{SU}	0.674	0.702	0.721	ns
			t_H	-0.407	-0.399	-0.379	ns
		GCLK PLL	t_{SU}	3.006	3.250	3.472	ns
			t_H	-2.739	-2.947	-3.130	ns

Table 1–76. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	0.743	0.795	0.839	ns
			t_H	–0.474	–0.490	–0.496	ns
		GCLK PLL	t_{SU}	3.075	3.343	3.590	ns
			t_H	–2.806	–3.038	–3.247	ns
	4 mA	GCLK	t_{SU}	0.743	0.795	0.839	ns
			t_H	–0.474	–0.490	–0.496	ns
		GCLK PLL	t_{SU}	3.075	3.343	3.590	ns
			t_H	–2.806	–3.038	–3.247	ns
	6 mA	GCLK	t_{SU}	0.743	0.795	0.839	ns
			t_H	–0.474	–0.490	–0.496	ns
		GCLK PLL	t_{SU}	3.075	3.343	3.590	ns
			t_H	–2.806	–3.038	–3.247	ns
	8 mA	GCLK	t_{SU}	0.743	0.795	0.839	ns
			t_H	–0.474	–0.490	–0.496	ns
		GCLK PLL	t_{SU}	3.075	3.343	3.590	ns
			t_H	–2.806	–3.038	–3.247	ns
	10 mA	GCLK	t_{SU}	0.743	0.795	0.839	ns
			t_H	–0.474	–0.490	–0.496	ns
		GCLK PLL	t_{SU}	3.075	3.343	3.590	ns
			t_H	–2.806	–3.038	–3.247	ns
	12 mA	GCLK	t_{SU}	0.743	0.795	0.839	ns
			t_H	–0.474	–0.490	–0.496	ns
		GCLK PLL	t_{SU}	3.075	3.343	3.590	ns
			t_H	–2.806	–3.038	–3.247	ns
16 mA	GCLK	t_{SU}	0.743	0.795	0.839	ns	
		t_H	–0.474	–0.490	–0.496	ns	
	GCLK PLL	t_{SU}	3.075	3.343	3.590	ns	
		t_H	–2.806	–3.038	–3.247	ns	

Table 1–76. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.2V	2 mA	GCLK	t_{SU}	0.896	0.975	1.046	ns
			t_H	–0.625	–0.666	–0.698	ns
		GCLK PLL	t_{SU}	3.228	3.523	3.797	ns
			t_H	–2.957	–3.214	–3.449	ns
	4 mA	GCLK	t_{SU}	0.896	0.975	1.046	ns
			t_H	–0.625	–0.666	–0.698	ns
		GCLK PLL	t_{SU}	3.228	3.523	3.797	ns
			t_H	–2.957	–3.214	–3.449	ns
	6 mA	GCLK	t_{SU}	0.896	0.975	1.046	ns
			t_H	–0.625	–0.666	–0.698	ns
		GCLK PLL	t_{SU}	3.228	3.523	3.797	ns
			t_H	–2.957	–3.214	–3.449	ns
	8 mA	GCLK	t_{SU}	0.896	0.975	1.046	ns
			t_H	–0.625	–0.666	–0.698	ns
		GCLK PLL	t_{SU}	3.228	3.523	3.797	ns
			t_H	–2.957	–3.214	–3.449	ns
	10 mA	GCLK	t_{SU}	0.896	0.975	1.046	ns
			t_H	–0.625	–0.666	–0.698	ns
		GCLK PLL	t_{SU}	3.228	3.523	3.797	ns
			t_H	–2.957	–3.214	–3.449	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.725	0.768	0.791	ns
			t_H	–0.456	–0.463	–0.448	ns
		GCLK PLL	t_{SU}	3.051	3.302	3.541	ns
			t_H	–2.782	–2.997	–3.198	ns
	12 mA	GCLK	t_{SU}	0.725	0.768	0.791	ns
			t_H	–0.456	–0.463	–0.448	ns
		GCLK PLL	t_{SU}	3.051	3.302	3.541	ns
			t_H	–2.782	–2.997	–3.198	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.725	0.768	0.791	ns
			t_H	–0.456	–0.463	–0.448	ns
		GCLK PLL	t_{SU}	3.051	3.302	3.541	ns
			t_H	–2.782	–2.997	–3.198	ns

Table 1–76. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.787	0.857	0.908	ns
			t_H	–0.518	–0.551	–0.563	ns
		GCLK PLL	t_{SU}	3.113	3.391	3.658	ns
			t_H	–2.844	–3.085	–3.313	ns
	10 mA	GCLK	t_{SU}	0.787	0.857	0.908	ns
			t_H	–0.518	–0.551	–0.563	ns
		GCLK PLL	t_{SU}	3.113	3.391	3.658	ns
			t_H	–2.844	–3.085	–3.313	ns
	12 mA	GCLK	t_{SU}	0.787	0.857	0.908	ns
			t_H	–0.518	–0.551	–0.563	ns
		GCLK PLL	t_{SU}	3.113	3.391	3.658	ns
			t_H	–2.844	–3.085	–3.313	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.787	0.857	0.908	ns
			t_H	–0.518	–0.551	–0.563	ns
		GCLK PLL	t_{SU}	3.113	3.391	3.658	ns
			t_H	–2.844	–3.085	–3.313	ns
SSTL-18 Class II	16 mA	GCLK	t_{SU}	0.787	0.857	0.908	ns
			t_H	–0.518	–0.551	–0.563	ns
		GCLK PLL	t_{SU}	3.113	3.391	3.658	ns
			t_H	–2.844	–3.085	–3.313	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.787	0.857	0.908	ns
			t_H	–0.518	–0.551	–0.563	ns
		GCLK PLL	t_{SU}	3.113	3.391	3.658	ns
			t_H	–2.844	–3.085	–3.313	ns
	10 mA	GCLK	t_{SU}	0.787	0.857	0.908	ns
			t_H	–0.518	–0.551	–0.563	ns
		GCLK PLL	t_{SU}	3.113	3.391	3.658	ns
			t_H	–2.844	–3.085	–3.313	ns
	12 mA	GCLK	t_{SU}	0.787	0.857	0.908	ns
			t_H	–0.518	–0.551	–0.563	ns
		GCLK PLL	t_{SU}	3.113	3.391	3.658	ns
			t_H	–2.844	–3.085	–3.313	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.787	0.857	0.908	ns
			t_H	–0.518	–0.551	–0.563	ns
		GCLK PLL	t_{SU}	3.113	3.391	3.658	ns
			t_H	–2.844	–3.085	–3.313	ns

Table 1–76. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.742	0.816	0.871	ns	
			t_H	–0.473	–0.511	–0.527	ns	
		GCLK PLL	t_{SU}	3.068	3.350	3.621	ns	
			t_H	–2.799	–3.045	–3.277	ns	
		10 mA	GCLK	t_{SU}	0.742	0.816	0.871	ns
				t_H	–0.473	–0.511	–0.527	ns
	GCLK PLL		t_{SU}	3.068	3.350	3.621	ns	
			t_H	–2.799	–3.045	–3.277	ns	
	12 mA	GCLK	t_{SU}	0.742	0.816	0.871	ns	
			t_H	–0.473	–0.511	–0.527	ns	
		GCLK PLL	t_{SU}	3.068	3.350	3.621	ns	
			t_H	–2.799	–3.045	–3.277	ns	
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.742	0.816	0.871	ns	
			t_H	–0.473	–0.511	–0.527	ns	
		GCLK PLL	t_{SU}	3.068	3.350	3.621	ns	
			t_H	–2.799	–3.045	–3.277	ns	
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.873	0.974	1.056	ns	
			t_H	–0.602	–0.665	–0.709	ns	
		GCLK PLL	t_{SU}	3.199	3.508	3.806	ns	
			t_H	–2.928	–3.199	–3.459	ns	
	10 mA	GCLK	t_{SU}	0.873	0.974	1.056	ns	
			t_H	–0.602	–0.665	–0.709	ns	
		GCLK PLL	t_{SU}	3.199	3.508	3.806	ns	
			t_H	–2.928	–3.199	–3.459	ns	
3.0-V PCI	—	GCLK	t_{SU}	0.791	0.781	0.760	ns	
			t_H	–0.522	–0.476	–0.418	ns	
		GCLK PLL	t_{SU}	3.123	3.329	3.511	ns	
			t_H	–2.854	–3.024	–3.169	ns	
3.0-V PCI-X	—	GCLK	t_{SU}	0.791	0.781	0.760	ns	
			t_H	–0.522	–0.476	–0.418	ns	
		GCLK PLL	t_{SU}	3.123	3.329	3.511	ns	
			t_H	–2.854	–3.024	–3.169	ns	

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{CO}	5.588	6.094	6.654	ns
		GCLK PLL	t_{CO}	7.102	3.545	8.204	ns
	8 mA	GCLK	t_{CO}	5.139	5.625	6.162	ns
		GCLK PLL	t_{CO}	4.676	3.076	5.472	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.225	5.716	6.258	ns
		GCLK PLL	t_{CO}	5.455	3.167	6.247	ns
3.0-V LVTTTL	4 mA	GCLK	t_{CO}	5.319	5.798	6.349	ns
		GCLK PLL	t_{CO}	5.878	3.249	6.731	ns
	8 mA	GCLK	t_{CO}	5.061	5.538	6.067	ns
		GCLK PLL	t_{CO}	4.318	2.989	5.080	ns
	12 mA	GCLK	t_{CO}	4.937	5.416	5.946	ns
		GCLK PLL	t_{CO}	3.670	2.867	4.378	ns
	16 mA	GCLK	t_{CO}	4.887	5.351	5.867	ns
		GCLK PLL	t_{CO}	3.310	2.802	3.956	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.059	5.537	6.066	ns
		GCLK PLL	t_{CO}	4.316	2.988	5.077	ns
	8 mA	GCLK	t_{CO}	4.890	5.355	5.882	ns
		GCLK PLL	t_{CO}	3.339	2.806	4.002	ns
	12 mA	GCLK	t_{CO}	4.849	5.314	5.831	ns
		GCLK PLL	t_{CO}	3.027	2.765	3.641	ns
	16 mA	GCLK	t_{CO}	4.829	5.295	5.812	ns
		GCLK PLL	t_{CO}	2.850	2.746	3.463	ns
2.5V	4 mA	GCLK	t_{CO}	5.441	5.936	6.495	ns
		GCLK PLL	t_{CO}	6.062	3.387	7.050	ns
	8 mA	GCLK	t_{CO}	5.169	5.659	6.205	ns
		GCLK PLL	t_{CO}	4.444	3.110	5.271	ns
	12 mA	GCLK	t_{CO}	5.051	5.537	6.081	ns
		GCLK PLL	t_{CO}	3.796	2.988	4.548	ns
16 mA	GCLK	t_{CO}	4.999	5.481	6.021	ns	
	GCLK PLL	t_{CO}	3.488	2.932	4.215	ns	

Table 1–77. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t_{CO}	6.614	7.244	7.960	ns	
		GCLK PLL	t_{CO}	10.321	4.695	12.339	ns	
	4 mA	GCLK	t_{CO}	6.040	6.658	7.348	ns	
		GCLK PLL	t_{CO}	6.915	4.109	8.390	ns	
	6 mA	GCLK	t_{CO}	5.770	6.353	7.007	ns	
		GCLK PLL	t_{CO}	5.585	3.804	6.796	ns	
	8 mA	GCLK	t_{CO}	5.656	6.237	6.878	ns	
		GCLK PLL	t_{CO}	4.924	3.688	6.010	ns	
	10 mA	GCLK	t_{CO}	5.593	6.171	6.814	ns	
		GCLK PLL	t_{CO}	4.576	3.622	5.622	ns	
	12 mA	GCLK	t_{CO}	5.528	6.090	6.720	ns	
		GCLK PLL	t_{CO}	4.268	3.541	5.247	ns	
	16 mA	GCLK	t_{CO}	5.474	6.036	6.657	ns	
		GCLK PLL	t_{CO}	3.950	3.487	4.877	ns	
	1.5V	2 mA	GCLK	t_{CO}	7.022	7.812	8.710	ns
			GCLK PLL	t_{CO}	9.685	5.263	12.126	ns
		4 mA	GCLK	t_{CO}	6.451	7.149	7.950	ns
			GCLK PLL	t_{CO}	6.614	4.600	8.290	ns
6 mA		GCLK	t_{CO}	6.254	6.939	7.727	ns	
		GCLK PLL	t_{CO}	5.593	4.390	7.048	ns	
8 mA		GCLK	t_{CO}	6.136	6.803	7.557	ns	
		GCLK PLL	t_{CO}	5.064	4.254	6.369	ns	
10 mA		GCLK	t_{CO}	6.069	6.733	7.490	ns	
		GCLK PLL	t_{CO}	4.747	4.184	5.989	ns	
12 mA		GCLK	t_{CO}	6.033	6.684	7.430	ns	
		GCLK PLL	t_{CO}	4.547	4.135	5.734	ns	
16 mA		GCLK	t_{CO}	5.915	6.558	7.272	ns	
		GCLK PLL	t_{CO}	4.207	4.009	5.290	ns	
1.2V		2 mA	GCLK	t_{CO}	8.098	9.177	10.444	ns
			GCLK PLL	t_{CO}	9.877	6.628	13.191	ns
		4 mA	GCLK	t_{CO}	7.599	8.600	9.773	ns
			GCLK PLL	t_{CO}	7.254	6.051	9.678	ns
	6 mA	GCLK	t_{CO}	7.418	8.386	9.519	ns	
		GCLK PLL	t_{CO}	6.435	5.837	8.573	ns	
	8 mA	GCLK	t_{CO}	7.335	8.293	9.413	ns	
		GCLK PLL	t_{CO}	6.027	5.744	8.030	ns	
	10 mA	GCLK	t_{CO}	7.190	8.109	9.171	ns	
		GCLK PLL	t_{CO}	5.691	5.560	7.533	ns	
	12 mA	GCLK	t_{CO}	7.164	8.081	9.143	ns	
		GCLK PLL	t_{CO}	5.535	5.532	7.333	ns	

Table 1–77. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.068	5.545	6.084	ns
		GCLK PLL	t_{CO}	2.728	3.001	3.327	ns
	12 mA	GCLK	t_{CO}	5.033	5.509	6.047	ns
		GCLK PLL	t_{CO}	2.693	2.965	3.290	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.976	5.447	5.980	ns
		GCLK PLL	t_{CO}	2.636	2.903	3.223	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.472	6.019	6.636	ns
		GCLK PLL	t_{CO}	3.132	3.475	3.879	ns
	10 mA	GCLK	t_{CO}	5.441	5.981	6.590	ns
		GCLK PLL	t_{CO}	3.101	3.437	3.833	ns
	12 mA	GCLK	t_{CO}	5.426	5.966	6.572	ns
		GCLK PLL	t_{CO}	3.086	3.422	3.815	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.413	5.951	6.559	ns
		GCLK PLL	t_{CO}	3.073	3.407	3.802	ns
	16 mA	GCLK	t_{CO}	5.394	5.932	6.539	ns
		GCLK PLL	t_{CO}	3.054	3.388	3.782	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.453	5.991	6.598	ns
		GCLK PLL	t_{CO}	3.113	3.447	3.841	ns
	10 mA	GCLK	t_{CO}	5.444	5.984	6.595	ns
		GCLK PLL	t_{CO}	3.104	3.440	3.838	ns
	12 mA	GCLK	t_{CO}	5.423	5.959	6.564	ns
		GCLK PLL	t_{CO}	3.083	3.415	3.807	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.395	5.926	6.528	ns
		GCLK PLL	t_{CO}	3.055	3.382	3.771	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.958	6.586	7.305	ns
		GCLK PLL	t_{CO}	3.618	4.042	4.548	ns
	10 mA	GCLK	t_{CO}	5.945	6.567	7.280	ns
		GCLK PLL	t_{CO}	3.605	4.023	4.523	ns
	12 mA	GCLK	t_{CO}	5.936	6.561	7.276	ns
		GCLK PLL	t_{CO}	3.596	4.017	4.519	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.893	6.508	7.212	ns
		GCLK PLL	t_{CO}	3.553	3.964	4.455	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.129	8.026	9.083	ns
		GCLK PLL	t_{CO}	4.789	5.482	6.326	ns
	10 mA	GCLK	t_{CO}	7.051	7.920	8.928	ns
		GCLK PLL	t_{CO}	4.711	5.376	6.171	ns
	12 mA	GCLK	t_{CO}	7.049	7.920	8.932	ns
		GCLK PLL	t_{CO}	4.709	5.376	6.175	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.992	7.849	8.851	ns
		GCLK PLL	t_{CO}	4.652	5.305	6.094	ns

Table 1–77. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V PCI	—	GCLK	t_{CO}	5.151	5.625	6.150	ns
		GCLK PLL	t_{CO}	3.229	3.076	3.914	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.151	5.625	6.150	ns
		GCLK PLL	t_{CO}	3.229	3.076	3.914	ns

Table 1–78. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
3.3-V LVTTTL	4 mA	GCLK	t_{CO}	5.531	6.033	6.598	ns	
		GCLK PLL	t_{CO}	3.199	3.501	3.847	ns	
	8 mA	GCLK	t_{CO}	5.083	5.569	6.116	ns	
		GCLK PLL	t_{CO}	2.751	3.037	3.365	ns	
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.177	5.656	6.207	ns	
		GCLK PLL	t_{CO}	2.845	3.124	3.456	ns	
3.0-V LVTTTL	4 mA	GCLK	t_{CO}	5.282	5.754	6.298	ns	
		GCLK PLL	t_{CO}	2.950	3.222	3.547	ns	
	8 mA	GCLK	t_{CO}	5.026	5.499	6.037	ns	
		GCLK PLL	t_{CO}	2.694	2.967	3.286	ns	
	12 mA	GCLK	t_{CO}	4.911	5.373	5.910	ns	
		GCLK PLL	t_{CO}	2.579	2.841	3.159	ns	
	16 mA	GCLK	t_{CO}	4.861	5.319	5.843	ns	
		GCLK PLL	t_{CO}	2.529	2.787	3.092	ns	
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.024	5.498	6.035	ns	
		GCLK PLL	t_{CO}	2.692	2.966	3.284	ns	
	8 mA	GCLK	t_{CO}	4.862	5.321	5.846	ns	
		GCLK PLL	t_{CO}	2.530	2.789	3.095	ns	
	12 mA	GCLK	t_{CO}	4.822	5.281	5.807	ns	
		GCLK PLL	t_{CO}	2.490	2.749	3.056	ns	
	16 mA	GCLK	t_{CO}	4.801	5.261	5.787	ns	
		GCLK PLL	t_{CO}	2.469	2.729	3.036	ns	
	2.5V	4 mA	GCLK	t_{CO}	5.408	5.893	6.454	ns
			GCLK PLL	t_{CO}	3.076	3.361	3.703	ns
8 mA		GCLK	t_{CO}	5.139	5.624	6.178	ns	
		GCLK PLL	t_{CO}	2.807	3.092	3.427	ns	
12 mA		GCLK	t_{CO}	5.025	5.504	6.054	ns	
		GCLK PLL	t_{CO}	2.693	2.972	3.303	ns	
16 mA		GCLK	t_{CO}	4.972	5.448	5.996	ns	
		GCLK PLL	t_{CO}	2.640	2.916	3.245	ns	

Table 1–78. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t_{CO}	6.558	7.181	7.901	ns	
		GCLK PLL	t_{CO}	4.226	4.649	5.150	ns	
	4 mA	GCLK	t_{CO}	6.003	6.611	7.309	ns	
		GCLK PLL	t_{CO}	3.671	4.079	4.558	ns	
	6 mA	GCLK	t_{CO}	5.741	6.316	6.977	ns	
		GCLK PLL	t_{CO}	3.409	3.784	4.226	ns	
	8 mA	GCLK	t_{CO}	5.625	6.188	6.832	ns	
		GCLK PLL	t_{CO}	3.293	3.656	4.081	ns	
	10 mA	GCLK	t_{CO}	5.564	6.134	6.785	ns	
		GCLK PLL	t_{CO}	3.232	3.602	4.034	ns	
	12 mA	GCLK	t_{CO}	5.504	6.058	6.696	ns	
		GCLK PLL	t_{CO}	3.172	3.526	3.945	ns	
	16 mA	GCLK	t_{CO}	5.460	6.009	6.641	ns	
		GCLK PLL	t_{CO}	3.128	3.477	3.890	ns	
	1.5V	2 mA	GCLK	t_{CO}	6.972	7.752	8.653	ns
			GCLK PLL	t_{CO}	4.640	5.220	5.902	ns
		4 mA	GCLK	t_{CO}	6.413	7.109	7.911	ns
			GCLK PLL	t_{CO}	4.081	4.577	5.160	ns
6 mA		GCLK	t_{CO}	6.223	6.904	7.695	ns	
		GCLK PLL	t_{CO}	3.891	4.372	4.944	ns	
8 mA		GCLK	t_{CO}	6.125	6.793	7.555	ns	
		GCLK PLL	t_{CO}	3.793	4.261	4.804	ns	
10 mA		GCLK	t_{CO}	6.058	6.721	7.486	ns	
		GCLK PLL	t_{CO}	3.726	4.189	4.735	ns	
12 mA		GCLK	t_{CO}	6.018	6.670	7.422	ns	
		GCLK PLL	t_{CO}	3.686	4.138	4.671	ns	
16 mA		GCLK	t_{CO}	5.946	6.589	7.334	ns	
		GCLK PLL	t_{CO}	3.614	4.057	4.583	ns	
1.2V		2 mA	GCLK	t_{CO}	8.058	9.127	10.399	ns
			GCLK PLL	t_{CO}	5.726	6.595	7.648	ns
		4 mA	GCLK	t_{CO}	7.567	8.561	9.740	ns
			GCLK PLL	t_{CO}	5.235	6.029	6.989	ns
	6 mA	GCLK	t_{CO}	7.412	8.377	9.525	ns	
		GCLK PLL	t_{CO}	5.080	5.845	6.774	ns	
	8 mA	GCLK	t_{CO}	7.324	8.279	9.412	ns	
		GCLK PLL	t_{CO}	4.992	5.747	6.661	ns	
	10 mA	GCLK	t_{CO}	7.206	8.135	9.233	ns	
		GCLK PLL	t_{CO}	4.874	5.603	6.482	ns	

Table 1–78. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.041	5.519	6.045	ns
		GCLK PLL	t_{CO}	2.715	2.985	3.295	ns
	12 mA	GCLK	t_{CO}	5.009	5.485	6.009	ns
		GCLK PLL	t_{CO}	2.683	2.951	3.259	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.958	5.432	5.952	ns
		GCLK PLL	t_{CO}	2.632	2.898	3.202	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.448	5.993	6.598	ns
		GCLK PLL	t_{CO}	3.122	3.459	3.848	ns
	10 mA	GCLK	t_{CO}	5.429	5.969	6.568	ns
		GCLK PLL	t_{CO}	3.103	3.435	3.818	ns
	12 mA	GCLK	t_{CO}	5.407	5.945	6.541	ns
		GCLK PLL	t_{CO}	3.081	3.411	3.791	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.399	5.937	6.534	ns
		GCLK PLL	t_{CO}	3.073	3.403	3.784	ns
	16 mA	GCLK	t_{CO}	5.384	5.923	6.520	ns
		GCLK PLL	t_{CO}	3.058	3.389	3.770	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.428	5.965	6.559	ns
		GCLK PLL	t_{CO}	3.102	3.431	3.809	ns
	10 mA	GCLK	t_{CO}	5.421	5.961	6.558	ns
		GCLK PLL	t_{CO}	3.095	3.427	3.808	ns
	12 mA	GCLK	t_{CO}	5.411	5.947	6.541	ns
		GCLK PLL	t_{CO}	3.085	3.413	3.791	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.378	5.909	6.499	ns
		GCLK PLL	t_{CO}	3.052	3.375	3.749	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.933	6.564	7.267	ns
		GCLK PLL	t_{CO}	3.607	4.030	4.517	ns
	10 mA	GCLK	t_{CO}	5.931	6.559	7.258	ns
		GCLK PLL	t_{CO}	3.605	4.025	4.508	ns
	12 mA	GCLK	t_{CO}	5.922	6.552	7.254	ns
		GCLK PLL	t_{CO}	3.596	4.018	4.504	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.883	6.506	7.201	ns
		GCLK PLL	t_{CO}	3.557	3.972	4.451	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.124	8.029	9.080	ns
		GCLK PLL	t_{CO}	4.798	5.495	6.330	ns
	10 mA	GCLK	t_{CO}	7.041	7.915	8.916	ns
		GCLK PLL	t_{CO}	4.715	5.381	6.166	ns
3.0-V PCI	—	GCLK	t_{CO}	5.120	5.586	6.119	ns
		GCLK PLL	t_{CO}	2.788	3.054	3.368	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.120	5.586	6.119	ns
		GCLK PLL	t_{CO}	2.788	3.054	3.368	ns

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.597	0.644	0.664	ns
			t_H	–0.329	–0.341	–0.324	ns
		GCLK PLL	t_{SU}	2.939	3.193	3.419	ns
			t_H	–2.671	–2.890	–3.079	ns
LVDS_E_3R	—	GCLK	t_{CO}	5.020	5.533	6.081	ns
		GCLK PLL	t_{CO}	5.020	5.533	6.081	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	5.020	5.533	6.081	ns
		GCLK PLL	t_{CO}	5.020	5.533	6.081	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.020	5.533	6.081	ns
		GCLK PLL	t_{CO}	5.020	5.533	6.081	ns
RSDS_E_1R	—	GCLK	t_{CO}	5.020	5.533	6.081	ns
		GCLK PLL	t_{CO}	5.020	5.533	6.081	ns
RSDS_E_3R	—	GCLK	t_{CO}	5.020	5.533	6.081	ns
		GCLK PLL	t_{CO}	5.020	5.533	6.081	ns

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.599	0.649	0.676	ns
			t_H	–0.332	–0.347	–0.335	ns
			t_{CO}	4.221	4.631	5.071	ns
		GCLK PLL	t_{SU}	2.943	3.199	3.432	ns
			t_H	–2.676	–2.897	–3.091	ns
			t_{CO}	1.879	2.081	2.317	ns
mini-LVDS	—	GCLK	t_{CO}	4.221	4.631	5.071	ns
		GCLK PLL	t_{CO}	1.879	2.081	2.317	ns
PPDS	—	GCLK	t_{CO}	4.221	4.631	5.071	ns
		GCLK PLL	t_{CO}	1.879	2.081	2.317	ns
RSDS	—	GCLK	t_{CO}	4.221	4.631	5.071	ns
		GCLK PLL	t_{CO}	1.879	2.081	2.317	ns

EP3C80 I/O Timing Parameters

Tables 1–81 through 1–86 show the maximum I/O timing parameters for EP3C80 devices.

Table 1–81. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	0.598	0.578	0.532	ns	
			t_H	–0.328	–0.273	–0.191	ns	
		GCLK PLL	t_{SU}	3.260	3.481	3.687	ns	
			t_H	–2.990	–3.176	–3.346	ns	
	8 mA	GCLK	t_{SU}	0.598	0.578	0.532	ns	
			t_H	–0.328	–0.273	–0.191	ns	
		GCLK PLL	t_{SU}	3.260	3.481	3.687	ns	
			t_H	–2.990	–3.176	–3.346	ns	
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.598	0.578	0.532	ns	
			t_H	–0.328	–0.273	–0.191	ns	
		GCLK PLL	t_{SU}	3.260	3.481	3.687	ns	
			t_H	–2.990	–3.176	–3.346	ns	
	3.0-V LVTTTL	4 mA	GCLK	t_{SU}	0.598	0.578	0.532	ns
				t_H	–0.328	–0.273	–0.191	ns
			GCLK PLL	t_{SU}	3.260	3.481	3.687	ns
				t_H	–2.990	–3.176	–3.346	ns
8 mA		GCLK	t_{SU}	0.598	0.578	0.532	ns	
			t_H	–0.328	–0.273	–0.191	ns	
		GCLK PLL	t_{SU}	3.260	3.481	3.687	ns	
			t_H	–2.990	–3.176	–3.346	ns	
12 mA		GCLK	t_{SU}	0.598	0.578	0.532	ns	
			t_H	–0.328	–0.273	–0.191	ns	
		GCLK PLL	t_{SU}	3.260	3.481	3.687	ns	
			t_H	–2.990	–3.176	–3.346	ns	
16 mA		GCLK	t_{SU}	0.598	0.578	0.532	ns	
			t_H	–0.328	–0.273	–0.191	ns	
		GCLK PLL	t_{SU}	3.260	3.481	3.687	ns	
			t_H	–2.990	–3.176	–3.346	ns	

Table 1–81. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.598	0.578	0.532	ns
			t_H	–0.328	–0.273	–0.191	ns
		GCLK PLL	t_{SU}	3.260	3.481	3.687	ns
			t_H	–2.990	–3.176	–3.346	ns
	8 mA	GCLK	t_{SU}	0.598	0.578	0.532	ns
			t_H	–0.328	–0.273	–0.191	ns
		GCLK PLL	t_{SU}	3.260	3.481	3.687	ns
			t_H	–2.990	–3.176	–3.346	ns
	12 mA	GCLK	t_{SU}	0.598	0.578	0.532	ns
			t_H	–0.328	–0.273	–0.191	ns
		GCLK PLL	t_{SU}	3.260	3.481	3.687	ns
			t_H	–2.990	–3.176	–3.346	ns
	16 mA	GCLK	t_{SU}	0.598	0.578	0.532	ns
			t_H	–0.328	–0.273	–0.191	ns
		GCLK PLL	t_{SU}	3.260	3.481	3.687	ns
			t_H	–2.990	–3.176	–3.346	ns
2.5V	4 mA	GCLK	t_{SU}	0.541	0.533	0.500	ns
			t_H	–0.271	–0.229	–0.160	ns
		GCLK PLL	t_{SU}	3.203	3.436	3.655	ns
			t_H	–2.933	–3.132	–3.315	ns
	8 mA	GCLK	t_{SU}	0.541	0.533	0.500	ns
			t_H	–0.271	–0.229	–0.160	ns
		GCLK PLL	t_{SU}	3.203	3.436	3.655	ns
			t_H	–2.933	–3.132	–3.315	ns
	12 mA	GCLK	t_{SU}	0.541	0.533	0.500	ns
			t_H	–0.271	–0.229	–0.160	ns
		GCLK PLL	t_{SU}	3.203	3.436	3.655	ns
			t_H	–2.933	–3.132	–3.315	ns
	16 mA	GCLK	t_{SU}	0.541	0.533	0.500	ns
			t_H	–0.271	–0.229	–0.160	ns
		GCLK PLL	t_{SU}	3.203	3.436	3.655	ns
			t_H	–2.933	–3.132	–3.315	ns

Table 1–81. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.8V	2 mA	GCLK	t_{SU}	0.476	0.494	0.487	ns
			t_H	–0.208	–0.191	–0.146	ns
		GCLK PLL	t_{SU}	3.138	3.397	3.642	ns
			t_H	–2.870	–3.094	–3.301	ns
	4 mA	GCLK	t_{SU}	0.476	0.494	0.487	ns
			t_H	–0.208	–0.191	–0.146	ns
		GCLK PLL	t_{SU}	3.138	3.397	3.642	ns
			t_H	–2.870	–3.094	–3.301	ns
	6 mA	GCLK	t_{SU}	0.476	0.494	0.487	ns
			t_H	–0.208	–0.191	–0.146	ns
		GCLK PLL	t_{SU}	3.138	3.397	3.642	ns
			t_H	–2.870	–3.094	–3.301	ns
	8 mA	GCLK	t_{SU}	0.476	0.494	0.487	ns
			t_H	–0.208	–0.191	–0.146	ns
		GCLK PLL	t_{SU}	3.138	3.397	3.642	ns
			t_H	–2.870	–3.094	–3.301	ns
	10 mA	GCLK	t_{SU}	0.476	0.494	0.487	ns
			t_H	–0.208	–0.191	–0.146	ns
		GCLK PLL	t_{SU}	3.138	3.397	3.642	ns
			t_H	–2.870	–3.094	–3.301	ns
	12 mA	GCLK	t_{SU}	0.476	0.494	0.487	ns
			t_H	–0.208	–0.191	–0.146	ns
		GCLK PLL	t_{SU}	3.138	3.397	3.642	ns
			t_H	–2.870	–3.094	–3.301	ns
16 mA	GCLK	t_{SU}	0.476	0.494	0.487	ns	
		t_H	–0.208	–0.191	–0.146	ns	
	GCLK PLL	t_{SU}	3.138	3.397	3.642	ns	
		t_H	–2.870	–3.094	–3.301	ns	

Table 1–81. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	0.545	0.586	0.604	ns
			t_H	–0.275	–0.281	–0.261	ns
		GCLK PLL	t_{SU}	3.207	3.489	3.759	ns
			t_H	–2.937	–3.184	–3.416	ns
	4 mA	GCLK	t_{SU}	0.545	0.586	0.604	ns
			t_H	–0.275	–0.281	–0.261	ns
		GCLK PLL	t_{SU}	3.207	3.489	3.759	ns
			t_H	–2.937	–3.184	–3.416	ns
	6 mA	GCLK	t_{SU}	0.545	0.586	0.604	ns
			t_H	–0.275	–0.281	–0.261	ns
		GCLK PLL	t_{SU}	3.207	3.489	3.759	ns
			t_H	–2.937	–3.184	–3.416	ns
	8 mA	GCLK	t_{SU}	0.545	0.586	0.604	ns
			t_H	–0.275	–0.281	–0.261	ns
		GCLK PLL	t_{SU}	3.207	3.489	3.759	ns
			t_H	–2.937	–3.184	–3.416	ns
	10 mA	GCLK	t_{SU}	0.545	0.586	0.604	ns
			t_H	–0.275	–0.281	–0.261	ns
		GCLK PLL	t_{SU}	3.207	3.489	3.759	ns
			t_H	–2.937	–3.184	–3.416	ns
	12 mA	GCLK	t_{SU}	0.545	0.586	0.604	ns
			t_H	–0.275	–0.281	–0.261	ns
		GCLK PLL	t_{SU}	3.207	3.489	3.759	ns
			t_H	–2.937	–3.184	–3.416	ns
16 mA	GCLK	t_{SU}	0.545	0.586	0.604	ns	
		t_H	–0.275	–0.281	–0.261	ns	
	GCLK PLL	t_{SU}	3.207	3.489	3.759	ns	
		t_H	–2.937	–3.184	–3.416	ns	

Table 1–81. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.2V	2 mA	GCLK	t_{SU}	0.697	0.766	0.810	ns
			t_H	–0.425	–0.457	–0.463	ns
		GCLK PLL	t_{SU}	3.359	3.669	3.965	ns
			t_H	–3.087	–3.360	–3.618	ns
	4 mA	GCLK	t_{SU}	0.697	0.766	0.810	ns
			t_H	–0.425	–0.457	–0.463	ns
		GCLK PLL	t_{SU}	3.359	3.669	3.965	ns
			t_H	–3.087	–3.360	–3.618	ns
	6 mA	GCLK	t_{SU}	0.697	0.766	0.810	ns
			t_H	–0.425	–0.457	–0.463	ns
		GCLK PLL	t_{SU}	3.359	3.669	3.965	ns
			t_H	–3.087	–3.360	–3.618	ns
	8 mA	GCLK	t_{SU}	0.697	0.766	0.810	ns
			t_H	–0.425	–0.457	–0.463	ns
		GCLK PLL	t_{SU}	3.359	3.669	3.965	ns
			t_H	–3.087	–3.360	–3.618	ns
	10 mA	GCLK	t_{SU}	0.697	0.766	0.810	ns
			t_H	–0.425	–0.457	–0.463	ns
		GCLK PLL	t_{SU}	3.359	3.669	3.965	ns
			t_H	–3.087	–3.360	–3.618	ns
	12 mA	GCLK	t_{SU}	0.697	0.766	0.810	ns
			t_H	–0.425	–0.457	–0.463	ns
		GCLK PLL	t_{SU}	3.359	3.669	3.965	ns
			t_H	–3.087	–3.360	–3.618	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.531	0.547	0.550	ns
			t_H	–0.261	–0.243	–0.208	ns
		GCLK PLL	t_{SU}	3.192	3.454	3.702	ns
			t_H	–2.922	–3.150	–3.360	ns
	12 mA	GCLK	t_{SU}	0.531	0.547	0.550	ns
			t_H	–0.261	–0.243	–0.208	ns
		GCLK PLL	t_{SU}	3.192	3.454	3.702	ns
			t_H	–2.922	–3.150	–3.360	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.531	0.547	0.550	ns
			t_H	–0.261	–0.243	–0.208	ns
		GCLK PLL	t_{SU}	3.192	3.454	3.702	ns
			t_H	–2.922	–3.150	–3.360	ns

Table 1–81. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.592	0.636	0.665	ns
			t_H	–0.322	–0.330	–0.321	ns
		GCLK PLL	t_{SU}	3.253	3.543	3.817	ns
			t_H	–2.983	–3.237	–3.473	ns
	10 mA	GCLK	t_{SU}	0.592	0.636	0.665	ns
			t_H	–0.322	–0.330	–0.321	ns
		GCLK PLL	t_{SU}	3.253	3.543	3.817	ns
			t_H	–2.983	–3.237	–3.473	ns
	12 mA	GCLK	t_{SU}	0.592	0.636	0.665	ns
			t_H	–0.322	–0.330	–0.321	ns
		GCLK PLL	t_{SU}	3.253	3.543	3.817	ns
			t_H	–2.983	–3.237	–3.473	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.592	0.636	0.665	ns
			t_H	–0.322	–0.330	–0.321	ns
		GCLK PLL	t_{SU}	3.253	3.543	3.817	ns
			t_H	–2.983	–3.237	–3.473	ns
	16 mA	GCLK	t_{SU}	0.592	0.636	0.665	ns
			t_H	–0.322	–0.330	–0.321	ns
		GCLK PLL	t_{SU}	3.253	3.543	3.817	ns
			t_H	–2.983	–3.237	–3.473	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.592	0.636	0.665	ns
			t_H	–0.322	–0.330	–0.321	ns
		GCLK PLL	t_{SU}	3.253	3.543	3.817	ns
			t_H	–2.983	–3.237	–3.473	ns
	10 mA	GCLK	t_{SU}	0.592	0.636	0.665	ns
			t_H	–0.322	–0.330	–0.321	ns
		GCLK PLL	t_{SU}	3.253	3.543	3.817	ns
			t_H	–2.983	–3.237	–3.473	ns
	12 mA	GCLK	t_{SU}	0.592	0.636	0.665	ns
			t_H	–0.322	–0.330	–0.321	ns
		GCLK PLL	t_{SU}	3.253	3.543	3.817	ns
			t_H	–2.983	–3.237	–3.473	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.592	0.636	0.665	ns
			t_H	–0.322	–0.330	–0.321	ns
		GCLK PLL	t_{SU}	3.253	3.543	3.817	ns
			t_H	–2.983	–3.237	–3.473	ns

Table 1–81. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.548	0.596	0.631	ns
			t_H	–0.278	–0.291	–0.288	ns
		GCLK PLL	t_{SU}	3.209	3.503	3.783	ns
			t_H	–2.939	–3.198	–3.440	ns
	10 mA	GCLK	t_{SU}	0.548	0.596	0.631	ns
			t_H	–0.278	–0.291	–0.288	ns
		GCLK PLL	t_{SU}	3.209	3.503	3.783	ns
			t_H	–2.939	–3.198	–3.440	ns
	12 mA	GCLK	t_{SU}	0.548	0.596	0.631	ns
			t_H	–0.278	–0.291	–0.288	ns
		GCLK PLL	t_{SU}	3.209	3.503	3.783	ns
			t_H	–2.939	–3.198	–3.440	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.548	0.596	0.631	ns
			t_H	–0.278	–0.291	–0.288	ns
		GCLK PLL	t_{SU}	3.209	3.503	3.783	ns
			t_H	–2.939	–3.198	–3.440	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.680	0.755	0.815	ns
			t_H	–0.408	–0.446	–0.468	ns
		GCLK PLL	t_{SU}	3.341	3.662	3.967	ns
			t_H	–3.069	–3.353	–3.620	ns
	10 mA	GCLK	t_{SU}	0.680	0.755	0.815	ns
			t_H	–0.408	–0.446	–0.468	ns
		GCLK PLL	t_{SU}	3.341	3.662	3.967	ns
			t_H	–3.069	–3.353	–3.620	ns
	12 mA	GCLK	t_{SU}	0.680	0.755	0.815	ns
			t_H	–0.408	–0.446	–0.468	ns
		GCLK PLL	t_{SU}	3.341	3.662	3.967	ns
			t_H	–3.069	–3.353	–3.620	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	0.680	0.755	0.815	ns
			t_H	–0.408	–0.446	–0.468	ns
		GCLK PLL	t_{SU}	3.341	3.662	3.967	ns
			t_H	–3.069	–3.353	–3.620	ns
3.0-V PCI	—	GCLK	t_{SU}	0.594	0.574	0.527	ns
			t_H	–0.324	–0.269	–0.186	ns
		GCLK PLL	t_{SU}	3.256	3.477	3.682	ns
			t_H	–2.986	–3.172	–3.341	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.594	0.574	0.527	ns
			t_H	–0.324	–0.269	–0.186	ns
		GCLK PLL	t_{SU}	3.256	3.477	3.682	ns
			t_H	–2.986	–3.172	–3.341	ns

Table 1–82. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	0.614	0.601	0.548	ns
			t_H	–0.345	–0.296	–0.206	ns
		GCLK PLL	t_{SU}	3.271	3.499	3.703	ns
			t_H	–3.002	–3.194	–3.361	ns
	8 mA	GCLK	t_{SU}	0.614	0.601	0.548	ns
			t_H	–0.345	–0.296	–0.206	ns
		GCLK PLL	t_{SU}	3.271	3.499	3.703	ns
			t_H	–3.002	–3.194	–3.361	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.614	0.601	0.548	ns
			t_H	–0.345	–0.296	–0.206	ns
		GCLK PLL	t_{SU}	3.271	3.499	3.703	ns
			t_H	–3.002	–3.194	–3.361	ns
3.0-V LVTTTL	4 mA	GCLK	t_{SU}	0.614	0.601	0.548	ns
			t_H	–0.345	–0.296	–0.206	ns
		GCLK PLL	t_{SU}	3.271	3.499	3.703	ns
			t_H	–3.002	–3.194	–3.361	ns
	8 mA	GCLK	t_{SU}	0.614	0.601	0.548	ns
			t_H	–0.345	–0.296	–0.206	ns
		GCLK PLL	t_{SU}	3.271	3.499	3.703	ns
			t_H	–3.002	–3.194	–3.361	ns
	12 mA	GCLK	t_{SU}	0.614	0.601	0.548	ns
			t_H	–0.345	–0.296	–0.206	ns
		GCLK PLL	t_{SU}	3.271	3.499	3.703	ns
			t_H	–3.002	–3.194	–3.361	ns
	16 mA	GCLK	t_{SU}	0.614	0.601	0.548	ns
			t_H	–0.345	–0.296	–0.206	ns
		GCLK PLL	t_{SU}	3.271	3.499	3.703	ns
			t_H	–3.002	–3.194	–3.361	ns

Table 1–82. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.614	0.601	0.548	ns
			t_H	–0.345	–0.296	–0.206	ns
		GCLK PLL	t_{SU}	3.271	3.499	3.703	ns
			t_H	–3.002	–3.194	–3.361	ns
	8 mA	GCLK	t_{SU}	0.614	0.601	0.548	ns
			t_H	–0.345	–0.296	–0.206	ns
		GCLK PLL	t_{SU}	3.271	3.499	3.703	ns
			t_H	–3.002	–3.194	–3.361	ns
	12 mA	GCLK	t_{SU}	0.614	0.601	0.548	ns
			t_H	–0.345	–0.296	–0.206	ns
		GCLK PLL	t_{SU}	3.271	3.499	3.703	ns
			t_H	–3.002	–3.194	–3.361	ns
	16 mA	GCLK	t_{SU}	0.614	0.601	0.548	ns
			t_H	–0.345	–0.296	–0.206	ns
		GCLK PLL	t_{SU}	3.271	3.499	3.703	ns
			t_H	–3.002	–3.194	–3.361	ns
2.5V	4 mA	GCLK	t_{SU}	0.557	0.557	0.519	ns
			t_H	–0.288	–0.253	–0.178	ns
		GCLK PLL	t_{SU}	3.214	3.455	3.674	ns
			t_H	–2.945	–3.151	–3.333	ns
	8 mA	GCLK	t_{SU}	0.557	0.557	0.519	ns
			t_H	–0.288	–0.253	–0.178	ns
		GCLK PLL	t_{SU}	3.214	3.455	3.674	ns
			t_H	–2.945	–3.151	–3.333	ns
	12 mA	GCLK	t_{SU}	0.557	0.557	0.519	ns
			t_H	–0.288	–0.253	–0.178	ns
		GCLK PLL	t_{SU}	3.214	3.455	3.674	ns
			t_H	–2.945	–3.151	–3.333	ns
	16 mA	GCLK	t_{SU}	0.557	0.557	0.519	ns
			t_H	–0.288	–0.253	–0.178	ns
		GCLK PLL	t_{SU}	3.214	3.455	3.674	ns
			t_H	–2.945	–3.151	–3.333	ns

Table 1–82. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.8V	2 mA	GCLK	t_{SU}	0.493	0.518	0.505	ns
			t_H	–0.226	–0.215	–0.163	ns
		GCLK PLL	t_{SU}	3.150	3.416	3.660	ns
			t_H	–2.883	–3.113	–3.318	ns
	4 mA	GCLK	t_{SU}	0.493	0.518	0.505	ns
			t_H	–0.226	–0.215	–0.163	ns
		GCLK PLL	t_{SU}	3.150	3.416	3.660	ns
			t_H	–2.883	–3.113	–3.318	ns
	6 mA	GCLK	t_{SU}	0.493	0.518	0.505	ns
			t_H	–0.226	–0.215	–0.163	ns
		GCLK PLL	t_{SU}	3.150	3.416	3.660	ns
			t_H	–2.883	–3.113	–3.318	ns
	8 mA	GCLK	t_{SU}	0.493	0.518	0.505	ns
			t_H	–0.226	–0.215	–0.163	ns
		GCLK PLL	t_{SU}	3.150	3.416	3.660	ns
			t_H	–2.883	–3.113	–3.318	ns
	10 mA	GCLK	t_{SU}	0.493	0.518	0.505	ns
			t_H	–0.226	–0.215	–0.163	ns
		GCLK PLL	t_{SU}	3.150	3.416	3.660	ns
			t_H	–2.883	–3.113	–3.318	ns
	12 mA	GCLK	t_{SU}	0.493	0.518	0.505	ns
			t_H	–0.226	–0.215	–0.163	ns
		GCLK PLL	t_{SU}	3.150	3.416	3.660	ns
			t_H	–2.883	–3.113	–3.318	ns
	16 mA	GCLK	t_{SU}	0.493	0.518	0.505	ns
			t_H	–0.226	–0.215	–0.163	ns
		GCLK PLL	t_{SU}	3.150	3.416	3.660	ns
			t_H	–2.883	–3.113	–3.318	ns

Table 1–82. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	-6	-7	-8	Unit
1.5V	2 mA	GCLK	t_{SU}	0.562	0.611	0.623	ns
			t_H	-0.293	-0.306	-0.280	ns
		GCLK PLL	t_{SU}	3.219	3.509	3.778	ns
			t_H	-2.950	-3.204	-3.435	ns
	4 mA	GCLK	t_{SU}	0.562	0.611	0.623	ns
			t_H	-0.293	-0.306	-0.280	ns
		GCLK PLL	t_{SU}	3.219	3.509	3.778	ns
			t_H	-2.950	-3.204	-3.435	ns
	6 mA	GCLK	t_{SU}	0.562	0.611	0.623	ns
			t_H	-0.293	-0.306	-0.280	ns
		GCLK PLL	t_{SU}	3.219	3.509	3.778	ns
			t_H	-2.950	-3.204	-3.435	ns
	8 mA	GCLK	t_{SU}	0.562	0.611	0.623	ns
			t_H	-0.293	-0.306	-0.280	ns
		GCLK PLL	t_{SU}	3.219	3.509	3.778	ns
			t_H	-2.950	-3.204	-3.435	ns
	10 mA	GCLK	t_{SU}	0.562	0.611	0.623	ns
			t_H	-0.293	-0.306	-0.280	ns
		GCLK PLL	t_{SU}	3.219	3.509	3.778	ns
			t_H	-2.950	-3.204	-3.435	ns
	12 mA	GCLK	t_{SU}	0.562	0.611	0.623	ns
			t_H	-0.293	-0.306	-0.280	ns
		GCLK PLL	t_{SU}	3.219	3.509	3.778	ns
			t_H	-2.950	-3.204	-3.435	ns
	16 mA	GCLK	t_{SU}	0.562	0.611	0.623	ns
			t_H	-0.293	-0.306	-0.280	ns
		GCLK PLL	t_{SU}	3.219	3.509	3.778	ns
			t_H	-2.950	-3.204	-3.435	ns

Table 1–82. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
1.2V	2 mA	GCLK	t_{SU}	0.715	0.791	0.830	ns
			t_H	–0.444	–0.482	–0.482	ns
		GCLK PLL	t_{SU}	3.372	3.689	3.985	ns
			t_H	–3.101	–3.380	–3.637	ns
	4 mA	GCLK	t_{SU}	0.715	0.791	0.830	ns
			t_H	–0.444	–0.482	–0.482	ns
		GCLK PLL	t_{SU}	3.372	3.689	3.985	ns
			t_H	–3.101	–3.380	–3.637	ns
	6 mA	GCLK	t_{SU}	0.715	0.791	0.830	ns
			t_H	–0.444	–0.482	–0.482	ns
		GCLK PLL	t_{SU}	3.372	3.689	3.985	ns
			t_H	–3.101	–3.380	–3.637	ns
	8 mA	GCLK	t_{SU}	0.715	0.791	0.830	ns
			t_H	–0.444	–0.482	–0.482	ns
		GCLK PLL	t_{SU}	3.372	3.689	3.985	ns
			t_H	–3.101	–3.380	–3.637	ns
	10 mA	GCLK	t_{SU}	0.715	0.791	0.830	ns
			t_H	–0.444	–0.482	–0.482	ns
		GCLK PLL	t_{SU}	3.372	3.689	3.985	ns
			t_H	–3.101	–3.380	–3.637	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.547	0.564	0.564	ns
			t_H	–0.278	–0.259	–0.221	ns
		GCLK PLL	t_{SU}	3.209	3.465	3.718	ns
			t_H	–2.940	–3.160	–3.375	ns
	12 mA	GCLK	t_{SU}	0.547	0.564	0.564	ns
			t_H	–0.278	–0.259	–0.221	ns
		GCLK PLL	t_{SU}	3.209	3.465	3.718	ns
			t_H	–2.940	–3.160	–3.375	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.547	0.564	0.564	ns
			t_H	–0.278	–0.259	–0.221	ns
		GCLK PLL	t_{SU}	3.209	3.465	3.718	ns
			t_H	–2.940	–3.160	–3.375	ns

Table 1–82. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.609	0.653	0.681	ns
			t_H	–0.340	–0.347	–0.336	ns
		GCLK PLL	t_{SU}	3.271	3.554	3.835	ns
			t_H	–3.002	–3.248	–3.490	ns
	10 mA	GCLK	t_{SU}	0.609	0.653	0.681	ns
			t_H	–0.340	–0.347	–0.336	ns
		GCLK PLL	t_{SU}	3.271	3.554	3.835	ns
			t_H	–3.002	–3.248	–3.490	ns
	12 mA	GCLK	t_{SU}	0.609	0.653	0.681	ns
			t_H	–0.340	–0.347	–0.336	ns
		GCLK PLL	t_{SU}	3.271	3.554	3.835	ns
			t_H	–3.002	–3.248	–3.490	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.609	0.653	0.681	ns
			t_H	–0.340	–0.347	–0.336	ns
		GCLK PLL	t_{SU}	3.271	3.554	3.835	ns
			t_H	–3.002	–3.248	–3.490	ns
	16 mA	GCLK	t_{SU}	0.609	0.653	0.681	ns
			t_H	–0.340	–0.347	–0.336	ns
		GCLK PLL	t_{SU}	3.271	3.554	3.835	ns
			t_H	–3.002	–3.248	–3.490	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.609	0.653	0.681	ns
			t_H	–0.340	–0.347	–0.336	ns
		GCLK PLL	t_{SU}	3.271	3.554	3.835	ns
			t_H	–3.002	–3.248	–3.490	ns
	10 mA	GCLK	t_{SU}	0.609	0.653	0.681	ns
			t_H	–0.340	–0.347	–0.336	ns
		GCLK PLL	t_{SU}	3.271	3.554	3.835	ns
			t_H	–3.002	–3.248	–3.490	ns
	12 mA	GCLK	t_{SU}	0.609	0.653	0.681	ns
			t_H	–0.340	–0.347	–0.336	ns
		GCLK PLL	t_{SU}	3.271	3.554	3.835	ns
			t_H	–3.002	–3.248	–3.490	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.609	0.653	0.681	ns
			t_H	–0.340	–0.347	–0.336	ns
		GCLK PLL	t_{SU}	3.271	3.554	3.835	ns
			t_H	–3.002	–3.248	–3.490	ns

Table 1–82. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.564	0.612	0.644	ns	
			t_H	–0.295	–0.307	–0.300	ns	
		GCLK PLL	t_{SU}	3.226	3.513	3.798	ns	
			t_H	–2.957	–3.208	–3.454	ns	
		10 mA	GCLK	t_{SU}	0.564	0.612	0.644	ns
				t_H	–0.295	–0.307	–0.300	ns
	GCLK PLL		t_{SU}	3.226	3.513	3.798	ns	
			t_H	–2.957	–3.208	–3.454	ns	
	12 mA	GCLK	t_{SU}	0.564	0.612	0.644	ns	
			t_H	–0.295	–0.307	–0.300	ns	
		GCLK PLL	t_{SU}	3.226	3.513	3.798	ns	
			t_H	–2.957	–3.208	–3.454	ns	
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.564	0.612	0.644	ns	
			t_H	–0.295	–0.307	–0.300	ns	
		GCLK PLL	t_{SU}	3.226	3.513	3.798	ns	
			t_H	–2.957	–3.208	–3.454	ns	
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.695	0.770	0.829	ns	
			t_H	–0.424	–0.461	–0.482	ns	
		GCLK PLL	t_{SU}	3.357	3.671	3.983	ns	
			t_H	–3.086	–3.362	–3.636	ns	
	10 mA	GCLK	t_{SU}	0.695	0.770	0.829	ns	
			t_H	–0.424	–0.461	–0.482	ns	
		GCLK PLL	t_{SU}	3.357	3.671	3.983	ns	
			t_H	–3.086	–3.362	–3.636	ns	
3.0-V PCI	—	GCLK	t_{SU}	0.610	0.597	0.544	ns	
			t_H	–0.341	–0.292	–0.202	ns	
		GCLK PLL	t_{SU}	3.267	3.495	3.699	ns	
			t_H	–2.998	–3.190	–3.357	ns	
3.0-V PCI-X	—	GCLK	t_{SU}	0.610	0.597	0.544	ns	
			t_H	–0.341	–0.292	–0.202	ns	
		GCLK PLL	t_{SU}	3.267	3.495	3.699	ns	
			t_H	–2.998	–3.190	–3.357	ns	

Table 1–83. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{CO}	5.756	6.285	6.862	ns
		GCLK PLL	t_{CO}	3.098	7.448	3.707	ns
	8 mA	GCLK	t_{CO}	5.307	5.816	6.370	ns
		GCLK PLL	t_{CO}	2.649	4.855	3.215	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.393	5.907	6.466	ns
		GCLK PLL	t_{CO}	2.735	5.652	3.311	ns
3.0-V LVTTTL	4 mA	GCLK	t_{CO}	5.487	5.989	6.557	ns
		GCLK PLL	t_{CO}	2.829	6.108	3.402	ns
	8 mA	GCLK	t_{CO}	5.229	5.729	6.275	ns
		GCLK PLL	t_{CO}	2.571	4.483	3.120	ns
	12 mA	GCLK	t_{CO}	5.105	5.607	6.154	ns
		GCLK PLL	t_{CO}	2.447	3.830	2.999	ns
	16 mA	GCLK	t_{CO}	5.055	5.542	6.075	ns
		GCLK PLL	t_{CO}	2.397	3.426	2.920	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.227	5.728	6.274	ns
		GCLK PLL	t_{CO}	2.569	4.480	3.119	ns
	8 mA	GCLK	t_{CO}	5.058	5.546	6.090	ns
		GCLK PLL	t_{CO}	2.400	3.461	2.935	ns
	12 mA	GCLK	t_{CO}	5.017	5.505	6.039	ns
		GCLK PLL	t_{CO}	2.359	3.133	2.884	ns
	16 mA	GCLK	t_{CO}	4.997	5.486	6.020	ns
		GCLK PLL	t_{CO}	2.339	2.952	2.865	ns
2.5V	4 mA	GCLK	t_{CO}	5.609	6.127	6.703	ns
		GCLK PLL	t_{CO}	2.951	6.345	3.548	ns
	8 mA	GCLK	t_{CO}	5.337	5.850	6.413	ns
		GCLK PLL	t_{CO}	2.679	4.651	3.258	ns
	12 mA	GCLK	t_{CO}	5.219	5.728	6.289	ns
		GCLK PLL	t_{CO}	2.561	3.974	3.134	ns
16 mA	GCLK	t_{CO}	5.167	5.672	6.229	ns	
	GCLK PLL	t_{CO}	2.509	3.647	3.074	ns	

Table 1–83. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t_{CO}	6.782	7.435	8.168	ns	
		GCLK PLL	t_{CO}	4.124	11.091	5.013	ns	
	4 mA	GCLK	t_{CO}	6.208	6.849	7.556	ns	
		GCLK PLL	t_{CO}	3.550	7.420	4.401	ns	
	6 mA	GCLK	t_{CO}	5.938	6.544	7.215	ns	
		GCLK PLL	t_{CO}	3.280	5.969	4.060	ns	
	8 mA	GCLK	t_{CO}	5.824	6.428	7.086	ns	
		GCLK PLL	t_{CO}	3.166	5.252	3.931	ns	
	10 mA	GCLK	t_{CO}	5.761	6.362	7.022	ns	
		GCLK PLL	t_{CO}	3.103	4.880	3.867	ns	
	12 mA	GCLK	t_{CO}	5.696	6.281	6.928	ns	
		GCLK PLL	t_{CO}	3.038	4.548	3.773	ns	
	16 mA	GCLK	t_{CO}	5.642	6.227	6.865	ns	
		GCLK PLL	t_{CO}	2.984	4.202	3.710	ns	
	1.5V	2 mA	GCLK	t_{CO}	7.190	8.003	8.918	ns
			GCLK PLL	t_{CO}	4.532	10.633	5.763	ns
		4 mA	GCLK	t_{CO}	6.619	7.340	8.158	ns
			GCLK PLL	t_{CO}	3.961	7.210	5.003	ns
6 mA		GCLK	t_{CO}	6.422	7.130	7.935	ns	
		GCLK PLL	t_{CO}	3.764	6.083	4.780	ns	
8 mA		GCLK	t_{CO}	6.304	6.994	7.765	ns	
		GCLK PLL	t_{CO}	3.646	5.485	4.610	ns	
10 mA		GCLK	t_{CO}	6.237	6.924	7.698	ns	
		GCLK PLL	t_{CO}	3.579	5.143	4.543	ns	
12 mA		GCLK	t_{CO}	6.201	6.875	7.638	ns	
		GCLK PLL	t_{CO}	3.543	4.917	4.483	ns	
16 mA		GCLK	t_{CO}	6.083	6.749	7.480	ns	
		GCLK PLL	t_{CO}	3.425	4.530	4.325	ns	
1.2V		2 mA	GCLK	t_{CO}	8.266	9.368	10.652	ns
			GCLK PLL	t_{CO}	5.608	11.197	7.497	ns
		4 mA	GCLK	t_{CO}	7.767	8.791	9.981	ns
			GCLK PLL	t_{CO}	5.109	8.172	6.826	ns
	6 mA	GCLK	t_{CO}	7.586	8.577	9.727	ns	
		GCLK PLL	t_{CO}	4.928	7.225	6.572	ns	
	8 mA	GCLK	t_{CO}	7.503	8.484	9.621	ns	
		GCLK PLL	t_{CO}	4.845	6.755	6.466	ns	
	10 mA	GCLK	t_{CO}	7.358	8.300	9.379	ns	
		GCLK PLL	t_{CO}	4.700	6.351	6.224	ns	
	12 mA	GCLK	t_{CO}	7.332	8.272	9.351	ns	
		GCLK PLL	t_{CO}	4.674	6.175	6.196	ns	

Table 1–83. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t _{CO}	5.24	5.739	6.289	ns
		GCLK PLL	t _{CO}	2.579	2.834	3.135	ns
	12 mA	GCLK	t _{CO}	5.205	5.703	6.252	ns
		GCLK PLL	t _{CO}	2.544	2.798	3.098	ns
SSTL-2 Class II	16 mA	GCLK	t _{CO}	5.148	5.641	6.185	ns
		GCLK PLL	t _{CO}	2.487	2.736	3.031	ns
SSTL-18 Class I	8 mA	GCLK	t _{CO}	5.644	6.213	6.841	ns
		GCLK PLL	t _{CO}	2.983	3.308	3.687	ns
	10 mA	GCLK	t _{CO}	5.613	6.175	6.795	ns
		GCLK PLL	t _{CO}	2.952	3.270	3.641	ns
	12 mA	GCLK	t _{CO}	5.598	6.160	6.777	ns
		GCLK PLL	t _{CO}	2.937	3.255	3.623	ns
SSTL-18 Class II	12 mA	GCLK	t _{CO}	5.585	6.145	6.764	ns
		GCLK PLL	t _{CO}	2.924	3.240	3.610	ns
	16 mA	GCLK	t _{CO}	5.566	6.126	6.744	ns
		GCLK PLL	t _{CO}	2.905	3.221	3.590	ns
1.8-V HSTL Class I	8 mA	GCLK	t _{CO}	5.625	6.185	6.803	ns
		GCLK PLL	t _{CO}	2.964	3.280	3.649	ns
	10 mA	GCLK	t _{CO}	5.616	6.178	6.800	ns
		GCLK PLL	t _{CO}	2.955	3.273	3.646	ns
	12 mA	GCLK	t _{CO}	5.595	6.153	6.769	ns
		GCLK PLL	t _{CO}	2.934	3.248	3.615	ns
1.8-V HSTL Class II	16 mA	GCLK	t _{CO}	5.567	6.120	6.733	ns
		GCLK PLL	t _{CO}	2.906	3.215	3.579	ns
1.5-V HSTL Class I	8 mA	GCLK	t _{CO}	6.130	6.780	7.510	ns
		GCLK PLL	t _{CO}	3.469	3.875	4.356	ns
	10 mA	GCLK	t _{CO}	6.117	6.761	7.485	ns
		GCLK PLL	t _{CO}	3.456	3.856	4.331	ns
	12 mA	GCLK	t _{CO}	6.108	6.755	7.481	ns
		GCLK PLL	t _{CO}	3.447	3.850	4.327	ns
1.5-V HSTL Class II	16 mA	GCLK	t _{CO}	6.065	6.702	7.417	ns
		GCLK PLL	t _{CO}	3.404	3.797	4.263	ns
1.2-V HSTL Class I	8 mA	GCLK	t _{CO}	7.301	8.220	9.288	ns
		GCLK PLL	t _{CO}	4.640	5.315	6.134	ns
	10 mA	GCLK	t _{CO}	7.223	8.114	9.133	ns
		GCLK PLL	t _{CO}	4.562	5.209	5.979	ns
	12 mA	GCLK	t _{CO}	7.221	8.114	9.137	ns
		GCLK PLL	t _{CO}	4.560	5.209	5.983	ns
1.2-V HSTL Class II	14 mA	GCLK	t _{CO}	7.164	8.043	9.056	ns
		GCLK PLL	t _{CO}	4.503	5.138	5.902	ns

Table 1–83. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.0-V PCI	—	GCLK	t_{CO}	5.319	5.816	6.358	ns
		GCLK PLL	t_{CO}	2.661	3.363	3.203	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.319	5.816	6.358	ns
		GCLK PLL	t_{CO}	2.661	3.363	3.203	ns

Table 1–84. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{CO}	9.559	10.300	6.814	ns
		GCLK PLL	t_{CO}	3.055	3.335	3.659	ns
	8 mA	GCLK	t_{CO}	7.151	7.716	6.332	ns
		GCLK PLL	t_{CO}	2.607	2.871	3.177	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	7.931	8.532	6.423	ns
		GCLK PLL	t_{CO}	2.701	2.958	3.268	ns
3.0-V LVTTTL	4 mA	GCLK	t_{CO}	8.363	8.977	6.514	ns
		GCLK PLL	t_{CO}	2.806	3.056	3.359	ns
	8 mA	GCLK	t_{CO}	6.807	7.365	6.253	ns
		GCLK PLL	t_{CO}	2.550	2.801	3.098	ns
	12 mA	GCLK	t_{CO}	6.160	6.712	6.126	ns
		GCLK PLL	t_{CO}	2.435	2.675	2.971	ns
	16 mA	GCLK	t_{CO}	5.805	6.314	6.059	ns
		GCLK PLL	t_{CO}	2.385	2.621	2.904	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	6.805	7.363	6.251	ns
		GCLK PLL	t_{CO}	2.548	2.800	3.096	ns
	8 mA	GCLK	t_{CO}	5.834	6.348	6.062	ns
		GCLK PLL	t_{CO}	2.386	2.623	2.907	ns
	12 mA	GCLK	t_{CO}	5.524	6.027	6.023	ns
		GCLK PLL	t_{CO}	2.346	2.583	2.868	ns
	16 mA	GCLK	t_{CO}	5.350	5.845	6.003	ns
		GCLK PLL	t_{CO}	2.325	2.563	2.848	ns
2.5V	4 mA	GCLK	t_{CO}	8.542	9.221	6.670	ns
		GCLK PLL	t_{CO}	2.932	3.195	3.515	ns
	8 mA	GCLK	t_{CO}	6.936	7.534	6.394	ns
		GCLK PLL	t_{CO}	2.663	2.926	3.239	ns
	12 mA	GCLK	t_{CO}	6.287	6.859	6.270	ns
		GCLK PLL	t_{CO}	2.549	2.806	3.115	ns
16 mA	GCLK	t_{CO}	5.983	6.533	6.212	ns	
	GCLK PLL	t_{CO}	2.496	2.750	3.057	ns	

Table 1–84. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit	
1.8V	2 mA	GCLK	t _{CO}	12.785	13.943	8.117	ns	
		GCLK PLL	t _{CO}	4.082	4.483	4.962	ns	
	4 mA	GCLK	t _{CO}	9.395	10.294	7.525	ns	
		GCLK PLL	t _{CO}	3.527	3.913	4.370	ns	
	6 mA	GCLK	t _{CO}	8.074	8.851	7.193	ns	
		GCLK PLL	t _{CO}	3.265	3.618	4.038	ns	
	8 mA	GCLK	t _{CO}	7.414	8.132	7.048	ns	
		GCLK PLL	t _{CO}	3.149	3.490	3.893	ns	
	10 mA	GCLK	t _{CO}	7.065	7.763	7.001	ns	
		GCLK PLL	t _{CO}	3.088	3.436	3.846	ns	
	12 mA	GCLK	t _{CO}	6.762	7.436	6.912	ns	
		GCLK PLL	t _{CO}	3.028	3.360	3.757	ns	
	16 mA	GCLK	t _{CO}	6.456	7.100	6.857	ns	
		GCLK PLL	t _{CO}	2.984	3.311	3.702	ns	
	1.5V	2 mA	GCLK	t _{CO}	12.150	13.492	8.869	ns
			GCLK PLL	t _{CO}	4.496	5.054	5.714	ns
		4 mA	GCLK	t _{CO}	9.094	10.087	8.127	ns
			GCLK PLL	t _{CO}	3.937	4.411	4.972	ns
6 mA		GCLK	t _{CO}	8.079	8.965	7.911	ns	
		GCLK PLL	t _{CO}	3.747	4.206	4.756	ns	
8 mA		GCLK	t _{CO}	7.572	8.394	7.771	ns	
		GCLK PLL	t _{CO}	3.649	4.095	4.616	ns	
10 mA		GCLK	t _{CO}	7.253	8.049	7.702	ns	
		GCLK PLL	t _{CO}	3.582	4.023	4.547	ns	
12 mA		GCLK	t _{CO}	7.051	7.821	7.638	ns	
		GCLK PLL	t _{CO}	3.542	3.972	4.483	ns	
16 mA		GCLK	t _{CO}	6.708	7.433	7.550	ns	
		GCLK PLL	t _{CO}	3.470	3.891	4.395	ns	
1.2V		2 mA	GCLK	t _{CO}	12.355	14.065	10.615	ns
			GCLK PLL	t _{CO}	5.582	6.429	7.460	ns
		4 mA	GCLK	t _{CO}	9.741	11.053	9.956	ns
			GCLK PLL	t _{CO}	5.091	5.863	6.801	ns
	6 mA	GCLK	t _{CO}	8.948	10.135	9.741	ns	
		GCLK PLL	t _{CO}	4.936	5.679	6.586	ns	
	8 mA	GCLK	t _{CO}	8.535	9.661	9.628	ns	
		GCLK PLL	t _{CO}	4.848	5.581	6.473	ns	
	10 mA	GCLK	t _{CO}	8.196	9.253	9.449	ns	
		GCLK PLL	t _{CO}	4.730	5.437	6.294	ns	

Table 1–84. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.219	5.723	6.272	ns
		GCLK PLL	t_{CO}	2.557	2.822	3.118	ns
	12 mA	GCLK	t_{CO}	5.187	5.689	6.236	ns
		GCLK PLL	t_{CO}	2.525	2.788	3.082	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.136	5.636	6.179	ns
		GCLK PLL	t_{CO}	2.474	2.735	3.025	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.626	6.197	6.825	ns
		GCLK PLL	t_{CO}	2.964	3.296	3.671	ns
	10 mA	GCLK	t_{CO}	5.607	6.173	6.795	ns
		GCLK PLL	t_{CO}	2.945	3.272	3.641	ns
	12 mA	GCLK	t_{CO}	5.585	6.149	6.768	ns
		GCLK PLL	t_{CO}	2.923	3.248	3.614	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.577	6.141	6.761	ns
		GCLK PLL	t_{CO}	2.915	3.240	3.607	ns
	16 mA	GCLK	t_{CO}	5.562	6.127	6.747	ns
		GCLK PLL	t_{CO}	2.900	3.226	3.593	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.606	6.169	6.786	ns
		GCLK PLL	t_{CO}	2.944	3.268	3.632	ns
	10 mA	GCLK	t_{CO}	5.599	6.165	6.785	ns
		GCLK PLL	t_{CO}	2.937	3.264	3.631	ns
	12 mA	GCLK	t_{CO}	5.589	6.151	6.768	ns
		GCLK PLL	t_{CO}	2.927	3.250	3.614	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.556	6.113	6.726	ns
		GCLK PLL	t_{CO}	2.894	3.212	3.572	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.111	6.768	7.494	ns
		GCLK PLL	t_{CO}	3.449	3.867	4.340	ns
	10 mA	GCLK	t_{CO}	6.109	6.763	7.485	ns
		GCLK PLL	t_{CO}	3.447	3.862	4.331	ns
	12 mA	GCLK	t_{CO}	6.100	6.756	7.481	ns
		GCLK PLL	t_{CO}	3.438	3.855	4.327	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	6.061	6.710	7.428	ns
		GCLK PLL	t_{CO}	3.399	3.809	4.274	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.302	8.233	9.307	ns
		GCLK PLL	t_{CO}	4.640	5.332	6.153	ns
	10 mA	GCLK	t_{CO}	7.219	8.119	9.143	ns
		GCLK PLL	t_{CO}	4.557	5.218	5.989	ns
3.0-V PCI	—	GCLK	t_{CO}	5.712	6.237	6.335	ns
		GCLK PLL	t_{CO}	2.644	2.888	3.180	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.712	6.237	6.335	ns
		GCLK PLL	t_{CO}	2.644	2.888	3.180	ns

Table 1–85. EP3C80 Column Pin Differential I/O Timing Parameters

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.423	0.450	0.451	ns
			t_H	–0.155	–0.147	–0.111	ns
		GCLK PLL	t_{SU}	3.083	3.354	3.606	ns
			t_H	–2.815	–3.051	–3.266	ns
LVDS_E_3R	—	GCLK	t_{CO}	5.194	5.727	6.294	ns
		GCLK PLL	t_{CO}	5.194	5.727	6.294	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	5.194	5.727	6.294	ns
		GCLK PLL	t_{CO}	5.194	5.727	6.294	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.194	5.727	6.294	ns
		GCLK PLL	t_{CO}	5.194	5.727	6.294	ns
RSDS_E_1R	—	GCLK	t_{CO}	5.194	5.727	6.294	ns
		GCLK PLL	t_{CO}	5.194	5.727	6.294	ns
RSDS_E_3R	—	GCLK	t_{CO}	5.194	5.727	6.294	ns
		GCLK PLL	t_{CO}	5.194	5.727	6.294	ns

Table 1–86. EP3C80 Row Pin Differential I/O Timing Parameters

I/O Standard	Current Strength	Clock	Parameter	–6	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.426	0.458	0.467	ns
			t_H	–0.159	–0.156	–0.126	ns
			t_{CO}	4.395	4.822	5.283	ns
		GCLK PLL	t_{SU}	3.088	3.364	3.622	ns
			t_H	–2.821	–3.062	–3.281	ns
			t_{CO}	1.735	1.918	2.127	ns
mini-LVDS	—	GCLK	t_{CO}	4.395	4.822	5.283	ns
		GCLK PLL	t_{CO}	1.735	1.918	2.127	ns
PPDS	—	GCLK	t_{CO}	4.395	4.822	5.283	ns
		GCLK PLL	t_{CO}	1.735	1.918	2.127	ns
RSDS	—	GCLK	t_{CO}	4.395	4.822	5.283	ns
		GCLK PLL	t_{CO}	1.735	1.918	2.127	ns

EP3C120 I/O Timing Parameters

Tables 1–87 through 1–92 show the maximum I/O timing parameters for EP3C120 devices. EP3C120 devices are offered in –7 and –8 speed grades only.

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	0.490	0.440	ns
			t_H	–0.185	–0.099	ns
		GCLK PLL	t_{SU}	3.440	3.635	ns
			t_H	–3.135	–3.294	ns
	8 mA	GCLK	t_{SU}	0.490	0.440	ns
			t_H	–0.185	–0.099	ns
		GCLK PLL	t_{SU}	3.440	3.635	ns
			t_H	–3.135	–3.294	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.490	0.440	ns
			t_H	–0.185	–0.099	ns
		GCLK PLL	t_{SU}	3.440	3.635	ns
			t_H	–3.135	–3.294	ns
3.0-V LVTTTL	4 mA	GCLK	t_{SU}	0.490	0.440	ns
			t_H	–0.185	–0.099	ns
		GCLK PLL	t_{SU}	3.440	3.635	ns
			t_H	–3.135	–3.294	ns
	8 mA	GCLK	t_{SU}	0.490	0.440	ns
			t_H	–0.185	–0.099	ns
		GCLK PLL	t_{SU}	3.440	3.635	ns
			t_H	–3.135	–3.294	ns
	12 mA	GCLK	t_{SU}	0.490	0.440	ns
			t_H	–0.185	–0.099	ns
		GCLK PLL	t_{SU}	3.440	3.635	ns
			t_H	–3.135	–3.294	ns
	16 mA	GCLK	t_{SU}	0.490	0.440	ns
			t_H	–0.185	–0.099	ns
		GCLK PLL	t_{SU}	3.440	3.635	ns
			t_H	–3.135	–3.294	ns

Table 1–87. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.490	0.440	ns
			t_H	–0.185	–0.099	ns
		GCLK PLL	t_{SU}	3.440	3.635	ns
			t_H	–3.135	–3.294	ns
	8 mA	GCLK	t_{SU}	0.490	0.440	ns
			t_H	–0.185	–0.099	ns
		GCLK PLL	t_{SU}	3.440	3.635	ns
			t_H	–3.135	–3.294	ns
	12 mA	GCLK	t_{SU}	0.490	0.440	ns
			t_H	–0.185	–0.099	ns
		GCLK PLL	t_{SU}	3.440	3.635	ns
			t_H	–3.135	–3.294	ns
	16mA	GCLK	t_{SU}	0.490	0.440	ns
			t_H	–0.185	–0.099	ns
		GCLK PLL	t_{SU}	3.440	3.635	ns
			t_H	–3.135	–3.294	ns
2.5V	4 mA	GCLK	t_{SU}	0.445	0.408	ns
			t_H	–0.141	–0.068	ns
		GCLK PLL	t_{SU}	3.395	3.603	ns
			t_H	–3.091	–3.263	ns
	8 mA	GCLK	t_{SU}	0.445	0.408	ns
			t_H	–0.141	–0.068	ns
		GCLK PLL	t_{SU}	3.395	3.603	ns
			t_H	–3.091	–3.263	ns
	12 mA	GCLK	t_{SU}	0.445	0.408	ns
			t_H	–0.141	–0.068	ns
		GCLK PLL	t_{SU}	3.395	3.603	ns
			t_H	–3.091	–3.263	ns
	16 mA	GCLK	t_{SU}	0.445	0.408	ns
			t_H	–0.141	–0.068	ns
		GCLK PLL	t_{SU}	3.395	3.603	ns
			t_H	–3.091	–3.263	ns

Table 1–87. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
1.8V	2 mA	GCLK	t_{SU}	0.406	0.395	ns
			t_H	–0.103	–0.054	ns
		GCLK PLL	t_{SU}	3.356	3.590	ns
			t_H	–3.053	–3.249	ns
	4 mA	GCLK	t_{SU}	0.406	0.395	ns
			t_H	–0.103	–0.054	ns
		GCLK PLL	t_{SU}	3.356	3.590	ns
			t_H	–3.053	–3.249	ns
	6 mA	GCLK	t_{SU}	0.406	0.395	ns
			t_H	–0.103	–0.054	ns
		GCLK PLL	t_{SU}	3.356	3.590	ns
			t_H	–3.053	–3.249	ns
	8 mA	GCLK	t_{SU}	0.406	0.395	ns
			t_H	–0.103	–0.054	ns
		GCLK PLL	t_{SU}	3.356	3.590	ns
			t_H	–3.053	–3.249	ns
	10 mA	GCLK	t_{SU}	0.406	0.395	ns
			t_H	–0.103	–0.054	ns
		GCLK PLL	t_{SU}	3.356	3.590	ns
			t_H	–3.053	–3.249	ns
	12 mA	GCLK	t_{SU}	0.406	0.395	ns
			t_H	–0.103	–0.054	ns
		GCLK PLL	t_{SU}	3.356	3.590	ns
			t_H	–3.053	–3.249	ns
	16 mA	GCLK	t_{SU}	0.406	0.395	ns
			t_H	–0.103	–0.054	ns
		GCLK PLL	t_{SU}	3.356	3.590	ns
			t_H	–3.053	–3.249	ns

Table 1–87. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	0.498	0.512	ns
			t_H	–0.193	–0.169	ns
		GCLK PLL	t_{SU}	3.448	3.707	ns
			t_H	–3.143	–3.364	ns
	4 mA	GCLK	t_{SU}	0.498	0.512	ns
			t_H	–0.193	–0.169	ns
		GCLK PLL	t_{SU}	3.448	3.707	ns
			t_H	–3.143	–3.364	ns
	6 mA	GCLK	t_{SU}	0.498	0.512	ns
			t_H	–0.193	–0.169	ns
		GCLK PLL	t_{SU}	3.448	3.707	ns
			t_H	–3.143	–3.364	ns
	8 mA	GCLK	t_{SU}	0.498	0.512	ns
			t_H	–0.193	–0.169	ns
		GCLK PLL	t_{SU}	3.448	3.707	ns
			t_H	–3.143	–3.364	ns
	10 mA	GCLK	t_{SU}	0.498	0.512	ns
			t_H	–0.193	–0.169	ns
		GCLK PLL	t_{SU}	3.448	3.707	ns
			t_H	–3.143	–3.364	ns
	12 mA	GCLK	t_{SU}	0.498	0.512	ns
			t_H	–0.193	–0.169	ns
		GCLK PLL	t_{SU}	3.448	3.707	ns
			t_H	–3.143	–3.364	ns
	16 mA	GCLK	t_{SU}	0.498	0.512	ns
			t_H	–0.193	–0.169	ns
		GCLK PLL	t_{SU}	3.448	3.707	ns
			t_H	–3.143	–3.364	ns

Table 1–87. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
1.2V	2 mA	GCLK	t_{SU}	0.678	0.718	ns
			t_H	–0.369	–0.371	ns
		GCLK PLL	t_{SU}	3.628	3.913	ns
			t_H	–3.319	–3.566	ns
	4 mA	GCLK	t_{SU}	0.678	0.718	ns
			t_H	–0.369	–0.371	ns
		GCLK PLL	t_{SU}	3.628	3.913	ns
			t_H	–3.319	–3.566	ns
	6 mA	GCLK	t_{SU}	0.678	0.718	ns
			t_H	–0.369	–0.371	ns
		GCLK PLL	t_{SU}	3.628	3.913	ns
			t_H	–3.319	–3.566	ns
	8 mA	GCLK	t_{SU}	0.678	0.718	ns
			t_H	–0.369	–0.371	ns
		GCLK PLL	t_{SU}	3.628	3.913	ns
			t_H	–3.319	–3.566	ns
	10 mA	GCLK	t_{SU}	0.678	0.718	ns
			t_H	–0.369	–0.371	ns
		GCLK PLL	t_{SU}	3.628	3.913	ns
			t_H	–3.319	–3.566	ns
	12 mA	GCLK	t_{SU}	0.678	0.718	ns
			t_H	–0.369	–0.371	ns
		GCLK PLL	t_{SU}	3.628	3.913	ns
			t_H	–3.319	–3.566	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.461	0.464	ns
			t_H	–0.157	–0.122	ns
		GCLK PLL	t_{SU}	3.424	3.629	ns
			t_H	–3.120	–3.287	ns
	12 mA	GCLK	t_{SU}	0.461	0.464	ns
			t_H	–0.157	–0.122	ns
		GCLK PLL	t_{SU}	3.424	3.629	ns
			t_H	–3.120	–3.287	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.461	0.464	ns
			t_H	–0.157	–0.122	ns
		GCLK PLL	t_{SU}	3.424	3.629	ns
			t_H	–3.120	–3.287	ns

Table 1–87. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.550	0.579	ns
			t_H	–0.244	–0.235	ns
		GCLK PLL	t_{SU}	3.513	3.744	ns
			t_H	–3.207	–3.400	ns
	10 mA	GCLK	t_{SU}	0.550	0.579	ns
			t_H	–0.244	–0.235	ns
		GCLK PLL	t_{SU}	3.513	3.744	ns
			t_H	–3.207	–3.400	ns
	12 mA	GCLK	t_{SU}	0.550	0.579	ns
			t_H	–0.244	–0.235	ns
		GCLK PLL	t_{SU}	3.513	3.744	ns
			t_H	–3.207	–3.400	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.550	0.579	ns
			t_H	–0.244	–0.235	ns
		GCLK PLL	t_{SU}	3.513	3.744	ns
			t_H	–3.207	–3.400	ns
	16 mA	GCLK	t_{SU}	0.550	0.579	ns
			t_H	–0.244	–0.235	ns
		GCLK PLL	t_{SU}	3.513	3.744	ns
			t_H	–3.207	–3.400	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.550	0.579	ns
			t_H	–0.244	–0.235	ns
		GCLK PLL	t_{SU}	3.513	3.744	ns
			t_H	–3.207	–3.400	ns
	10 mA	GCLK	t_{SU}	0.550	0.579	ns
			t_H	–0.244	–0.235	ns
		GCLK PLL	t_{SU}	3.513	3.744	ns
			t_H	–3.207	–3.400	ns
	12 mA	GCLK	t_{SU}	0.550	0.579	ns
			t_H	–0.244	–0.235	ns
		GCLK PLL	t_{SU}	3.513	3.744	ns
			t_H	–3.207	–3.400	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.550	0.579	ns
			t_H	–0.244	–0.235	ns
		GCLK PLL	t_{SU}	3.513	3.744	ns
			t_H	–3.207	–3.400	ns

Table 1–87. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit	
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.510	0.545	ns	
			t_H	–0.205	–0.202	ns	
		GCLK PLL	t_{SU}	3.473	3.710	ns	
			t_H	–3.168	–3.367	ns	
		10 mA	GCLK	t_{SU}	0.510	0.545	ns
				t_H	–0.205	–0.202	ns
	GCLK PLL		t_{SU}	3.473	3.710	ns	
			t_H	–3.168	–3.367	ns	
	12 mA	GCLK	t_{SU}	0.510	0.545	ns	
			t_H	–0.205	–0.202	ns	
		GCLK PLL	t_{SU}	3.473	3.710	ns	
			t_H	–3.168	–3.367	ns	
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.510	0.545	ns	
			t_H	–0.205	–0.202	ns	
		GCLK PLL	t_{SU}	3.473	3.710	ns	
			t_H	–3.168	–3.367	ns	
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.669	0.729	ns	
			t_H	–0.360	–0.382	ns	
		GCLK PLL	t_{SU}	3.632	3.894	ns	
			t_H	–3.323	–3.547	ns	
	10 mA	GCLK	t_{SU}	0.669	0.729	ns	
			t_H	–0.360	–0.382	ns	
		GCLK PLL	t_{SU}	3.632	3.894	ns	
			t_H	–3.323	–3.547	ns	
	12 mA	GCLK	t_{SU}	0.669	0.729	ns	
			t_H	–0.360	–0.382	ns	
		GCLK PLL	t_{SU}	3.632	3.894	ns	
			t_H	–3.323	–3.547	ns	
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	0.669	0.729	ns	
			t_H	–0.360	–0.382	ns	
		GCLK PLL	t_{SU}	3.632	3.894	ns	
			t_H	–3.323	–3.547	ns	
3.0-V PCI	—	GCLK	t_{SU}	0.486	0.435	ns	
			t_H	–0.181	–0.094	ns	
		GCLK PLL	t_{SU}	3.436	3.630	ns	
			t_H	–3.131	–3.289	ns	
3.0-V PCI-X	—	GCLK	t_{SU}	0.486	0.435	ns	
			t_H	–0.181	–0.094	ns	
		GCLK PLL	t_{SU}	3.436	3.630	ns	
			t_H	–3.131	–3.289	ns	

Table 1–88. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t_{SU}	0.512	0.477	ns
			t_H	–0.207	–0.135	ns
		GCLK PLL	t_{SU}	3.442	3.649	ns
			t_H	–3.137	–3.307	ns
	8 mA	GCLK	t_{SU}	0.512	0.477	ns
			t_H	–0.207	–0.135	ns
		GCLK PLL	t_{SU}	3.442	3.649	ns
			t_H	–3.137	–3.307	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.512	0.477	ns
			t_H	–0.207	–0.135	ns
		GCLK PLL	t_{SU}	3.442	3.649	ns
			t_H	–3.137	–3.307	ns
3.0-V LVTTTL	4 mA	GCLK	t_{SU}	0.512	0.477	ns
			t_H	–0.207	–0.135	ns
		GCLK PLL	t_{SU}	3.442	3.649	ns
			t_H	–3.137	–3.307	ns
	8 mA	GCLK	t_{SU}	0.512	0.477	ns
			t_H	–0.207	–0.135	ns
		GCLK PLL	t_{SU}	3.442	3.649	ns
			t_H	–3.137	–3.307	ns
	12 mA	GCLK	t_{SU}	0.512	0.477	ns
			t_H	–0.207	–0.135	ns
		GCLK PLL	t_{SU}	3.442	3.649	ns
			t_H	–3.137	–3.307	ns
	16 mA	GCLK	t_{SU}	0.512	0.477	ns
			t_H	–0.207	–0.135	ns
		GCLK PLL	t_{SU}	3.442	3.649	ns
			t_H	–3.137	–3.307	ns

Table 1–88. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.512	0.477	ns
			t_H	–0.207	–0.135	ns
		GCLK PLL	t_{SU}	3.442	3.649	ns
			t_H	–3.137	–3.307	ns
	8 mA	GCLK	t_{SU}	0.512	0.477	ns
			t_H	–0.207	–0.135	ns
		GCLK PLL	t_{SU}	3.442	3.649	ns
			t_H	–3.137	–3.307	ns
	12 mA	GCLK	t_{SU}	0.512	0.477	ns
			t_H	–0.207	–0.135	ns
		GCLK PLL	t_{SU}	3.442	3.649	ns
			t_H	–3.137	–3.307	ns
	16 mA	GCLK	t_{SU}	0.512	0.477	ns
			t_H	–0.207	–0.135	ns
		GCLK PLL	t_{SU}	3.442	3.649	ns
			t_H	–3.137	–3.307	ns
2.5V	4 mA	GCLK	t_{SU}	0.468	0.448	ns
			t_H	–0.164	–0.107	ns
		GCLK PLL	t_{SU}	3.398	3.620	ns
			t_H	–3.094	–3.279	ns
	8 mA	GCLK	t_{SU}	0.468	0.448	ns
			t_H	–0.164	–0.107	ns
		GCLK PLL	t_{SU}	3.398	3.620	ns
			t_H	–3.094	–3.279	ns
	12 mA	GCLK	t_{SU}	0.468	0.448	ns
			t_H	–0.164	–0.107	ns
		GCLK PLL	t_{SU}	3.398	3.620	ns
			t_H	–3.094	–3.279	ns
	16 mA	GCLK	t_{SU}	0.468	0.448	ns
			t_H	–0.164	–0.107	ns
		GCLK PLL	t_{SU}	3.398	3.620	ns
			t_H	–3.094	–3.279	ns

Table 1–88. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
1.8V	2 mA	GCLK	t _{SU}	0.429	0.434	ns
			t _H	–0.126	–0.092	ns
		GCLK PLL	t _{SU}	3.359	3.606	ns
			t _H	–3.056	–3.264	ns
	4 mA	GCLK	t _{SU}	0.429	0.434	ns
			t _H	–0.126	–0.092	ns
		GCLK PLL	t _{SU}	3.359	3.606	ns
			t _H	–3.056	–3.264	ns
	6 mA	GCLK	t _{SU}	0.429	0.434	ns
			t _H	–0.126	–0.092	ns
		GCLK PLL	t _{SU}	3.359	3.606	ns
			t _H	–3.056	–3.264	ns
	8 mA	GCLK	t _{SU}	0.429	0.434	ns
			t _H	–0.126	–0.092	ns
		GCLK PLL	t _{SU}	3.359	3.606	ns
			t _H	–3.056	–3.264	ns
	10 mA	GCLK	t _{SU}	0.429	0.434	ns
			t _H	–0.126	–0.092	ns
		GCLK PLL	t _{SU}	3.359	3.606	ns
			t _H	–3.056	–3.264	ns
	12 mA	GCLK	t _{SU}	0.429	0.434	ns
			t _H	–0.126	–0.092	ns
		GCLK PLL	t _{SU}	3.359	3.606	ns
			t _H	–3.056	–3.264	ns
	16 mA	GCLK	t _{SU}	0.429	0.434	ns
			t _H	–0.126	–0.092	ns
		GCLK PLL	t _{SU}	3.359	3.606	ns
			t _H	–3.056	–3.264	ns

Table 1–88. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
1.5V	2 mA	GCLK	t_{SU}	0.522	0.552	ns
			t_H	–0.217	–0.209	ns
		GCLK PLL	t_{SU}	3.452	3.724	ns
			t_H	–3.147	–3.381	ns
	4 mA	GCLK	t_{SU}	0.522	0.552	ns
			t_H	–0.217	–0.209	ns
		GCLK PLL	t_{SU}	3.452	3.724	ns
			t_H	–3.147	–3.381	ns
	6 mA	GCLK	t_{SU}	0.522	0.552	ns
			t_H	–0.217	–0.209	ns
		GCLK PLL	t_{SU}	3.452	3.724	ns
			t_H	–3.147	–3.381	ns
	8 mA	GCLK	t_{SU}	0.522	0.552	ns
			t_H	–0.217	–0.209	ns
		GCLK PLL	t_{SU}	3.452	3.724	ns
			t_H	–3.147	–3.381	ns
	10 mA	GCLK	t_{SU}	0.522	0.552	ns
			t_H	–0.217	–0.209	ns
		GCLK PLL	t_{SU}	3.452	3.724	ns
			t_H	–3.147	–3.381	ns
	12 mA	GCLK	t_{SU}	0.522	0.552	ns
			t_H	–0.217	–0.209	ns
		GCLK PLL	t_{SU}	3.452	3.724	ns
			t_H	–3.147	–3.381	ns
	16 mA	GCLK	t_{SU}	0.522	0.552	ns
			t_H	–0.217	–0.209	ns
		GCLK PLL	t_{SU}	3.452	3.724	ns
			t_H	–3.147	–3.381	ns

Table 1–88. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
1.2V	2 mA	GCLK	t_{SU}	0.702	0.759	ns
			t_H	–0.393	–0.411	ns
		GCLK PLL	t_{SU}	3.632	3.931	ns
			t_H	–3.323	–3.583	ns
	4 mA	GCLK	t_{SU}	0.702	0.759	ns
			t_H	–0.393	–0.411	ns
		GCLK PLL	t_{SU}	3.632	3.931	ns
			t_H	–3.323	–3.583	ns
	6 mA	GCLK	t_{SU}	0.702	0.759	ns
			t_H	–0.393	–0.411	ns
		GCLK PLL	t_{SU}	3.632	3.931	ns
			t_H	–3.323	–3.583	ns
	8 mA	GCLK	t_{SU}	0.702	0.759	ns
			t_H	–0.393	–0.411	ns
		GCLK PLL	t_{SU}	3.632	3.931	ns
			t_H	–3.323	–3.583	ns
	10 mA	GCLK	t_{SU}	0.702	0.759	ns
			t_H	–0.393	–0.411	ns
		GCLK PLL	t_{SU}	3.632	3.931	ns
			t_H	–3.323	–3.583	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.505	0.494	ns
			t_H	–0.200	–0.151	ns
		GCLK PLL	t_{SU}	3.411	3.716	ns
			t_H	–3.106	–3.373	ns
	12 mA	GCLK	t_{SU}	0.505	0.494	ns
			t_H	–0.200	–0.151	ns
		GCLK PLL	t_{SU}	3.411	3.716	ns
			t_H	–3.106	–3.373	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.505	0.494	ns
			t_H	–0.200	–0.151	ns
		GCLK PLL	t_{SU}	3.411	3.716	ns
			t_H	–3.106	–3.373	ns

Table 1–88. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.594	0.611	ns
			t_H	–0.288	–0.266	ns
		GCLK PLL	t_{SU}	3.500	3.833	ns
			t_H	–3.194	–3.488	ns
	10 mA	GCLK	t_{SU}	0.594	0.611	ns
			t_H	–0.288	–0.266	ns
		GCLK PLL	t_{SU}	3.500	3.833	ns
			t_H	–3.194	–3.488	ns
	12 mA	GCLK	t_{SU}	0.594	0.611	ns
			t_H	–0.288	–0.266	ns
		GCLK PLL	t_{SU}	3.500	3.833	ns
			t_H	–3.194	–3.488	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.594	0.611	ns
			t_H	–0.288	–0.266	ns
		GCLK PLL	t_{SU}	3.500	3.833	ns
			t_H	–3.194	–3.488	ns
	16 mA	GCLK	t_{SU}	0.594	0.611	ns
			t_H	–0.288	–0.266	ns
		GCLK PLL	t_{SU}	3.500	3.833	ns
			t_H	–3.194	–3.488	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.594	0.611	ns
			t_H	–0.288	–0.266	ns
		GCLK PLL	t_{SU}	3.500	3.833	ns
			t_H	–3.194	–3.488	ns
	10 mA	GCLK	t_{SU}	0.594	0.611	ns
			t_H	–0.288	–0.266	ns
		GCLK PLL	t_{SU}	3.500	3.833	ns
			t_H	–3.194	–3.488	ns
	12 mA	GCLK	t_{SU}	0.594	0.611	ns
			t_H	–0.288	–0.266	ns
		GCLK PLL	t_{SU}	3.500	3.833	ns
			t_H	–3.194	–3.488	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.594	0.611	ns
			t_H	–0.288	–0.266	ns
		GCLK PLL	t_{SU}	3.500	3.833	ns
			t_H	–3.194	–3.488	ns

Table 1–88. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.553	0.574	ns
			t_H	–0.248	–0.230	ns
		GCLK PLL	t_{SU}	3.459	3.796	ns
			t_H	–3.154	–3.452	ns
	10 mA	GCLK	t_{SU}	0.553	0.574	ns
			t_H	–0.248	–0.230	ns
		GCLK PLL	t_{SU}	3.459	3.796	ns
			t_H	–3.154	–3.452	ns
	12 mA	GCLK	t_{SU}	0.553	0.574	ns
			t_H	–0.248	–0.230	ns
		GCLK PLL	t_{SU}	3.459	3.796	ns
			t_H	–3.154	–3.452	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.553	0.574	ns
			t_H	–0.248	–0.230	ns
		GCLK PLL	t_{SU}	3.459	3.796	ns
			t_H	–3.154	–3.452	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.711	0.759	ns
			t_H	–0.402	–0.412	ns
		GCLK PLL	t_{SU}	3.617	3.981	ns
			t_H	–3.308	–3.634	ns
	10 mA	GCLK	t_{SU}	0.711	0.759	ns
			t_H	–0.402	–0.412	ns
		GCLK PLL	t_{SU}	3.617	3.981	ns
			t_H	–3.308	–3.634	ns
3.0-V PCI	—	GCLK	t_{SU}	0.508	0.473	ns
			t_H	–0.203	–0.131	ns
		GCLK PLL	t_{SU}	3.438	3.645	ns
			t_H	–3.133	–3.303	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.508	0.473	ns
			t_H	–0.203	–0.131	ns
		GCLK PLL	t_{SU}	3.438	3.645	ns
			t_H	–3.133	–3.303	ns

Table 1–89. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit	
3.3-V LVTTTL	4 mA	GCLK	t _{CO}	6.348	6.939	ns	
		GCLK PLL	t _{CO}	3.398	3.719	ns	
	8 mA	GCLK	t _{CO}	5.879	6.447	ns	
		GCLK PLL	t _{CO}	2.929	3.227	ns	
3.3-V LVCMOS	2 mA	GCLK	t _{CO}	5.970	6.543	ns	
		GCLK PLL	t _{CO}	3.020	3.323	ns	
3.0-V LVTTTL	4 mA	GCLK	t _{CO}	6.052	6.634	ns	
		GCLK PLL	t _{CO}	3.102	3.414	ns	
	8 mA	GCLK	t _{CO}	5.792	6.352	ns	
		GCLK PLL	t _{CO}	2.842	3.132	ns	
	12 mA	GCLK	t _{CO}	5.670	6.231	ns	
		GCLK PLL	t _{CO}	2.720	3.011	ns	
	16 mA	GCLK	t _{CO}	5.605	6.152	ns	
		GCLK PLL	t _{CO}	2.655	2.932	ns	
3.0-V LVCMOS	4 mA	GCLK	t _{CO}	5.791	6.351	ns	
		GCLK PLL	t _{CO}	2.841	3.131	ns	
	8 mA	GCLK	t _{CO}	5.609	6.167	ns	
		GCLK PLL	t _{CO}	2.659	2.947	ns	
	12 mA	GCLK	t _{CO}	5.568	6.116	ns	
		GCLK PLL	t _{CO}	2.618	2.896	ns	
	16 mA	GCLK	t _{CO}	5.549	6.097	ns	
		GCLK PLL	t _{CO}	2.599	2.877	ns	
	2.5V	4 mA	GCLK	t _{CO}	6.190	6.780	ns
			GCLK PLL	t _{CO}	3.240	3.560	ns
8 mA		GCLK	t _{CO}	5.913	6.490	ns	
		GCLK PLL	t _{CO}	2.963	3.270	ns	
12 mA		GCLK	t _{CO}	5.791	6.366	ns	
		GCLK PLL	t _{CO}	2.841	3.146	ns	
16 mA	GCLK	t _{CO}	5.735	6.306	ns		
	GCLK PLL	t _{CO}	2.785	3.086	ns		

**Table 1–89. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards
(Part 2 of 4)**

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit	
1.8V	2 mA	GCLK	t _{CO}	7.498	8.245	ns	
		GCLK PLL	t _{CO}	4.548	5.025	ns	
	4 mA	GCLK	t _{CO}	6.912	7.633	ns	
		GCLK PLL	t _{CO}	3.962	4.413	ns	
	6 mA	GCLK	t _{CO}	6.607	7.292	ns	
		GCLK PLL	t _{CO}	3.657	4.072	ns	
	8 mA	GCLK	t _{CO}	6.491	7.163	ns	
		GCLK PLL	t _{CO}	3.541	3.943	ns	
	10 mA	GCLK	t _{CO}	6.425	7.099	ns	
		GCLK PLL	t _{CO}	3.475	3.879	ns	
	12 mA	GCLK	t _{CO}	6.344	7.005	ns	
		GCLK PLL	t _{CO}	3.394	3.785	ns	
	16 mA	GCLK	t _{CO}	6.290	6.942	ns	
		GCLK PLL	t _{CO}	3.340	3.722	ns	
	1.5V	2 mA	GCLK	t _{CO}	8.066	8.995	ns
			GCLK PLL	t _{CO}	5.116	5.775	ns
		4 mA	GCLK	t _{CO}	7.403	8.235	ns
			GCLK PLL	t _{CO}	4.453	5.015	ns
6 mA		GCLK	t _{CO}	7.193	8.012	ns	
		GCLK PLL	t _{CO}	4.243	4.792	ns	
8 mA		GCLK	t _{CO}	7.057	7.842	ns	
		GCLK PLL	t _{CO}	4.107	4.622	ns	
10 mA		GCLK	t _{CO}	6.987	7.775	ns	
		GCLK PLL	t _{CO}	4.037	4.555	ns	
12 mA		GCLK	t _{CO}	6.938	7.715	ns	
		GCLK PLL	t _{CO}	3.988	4.495	ns	
16 mA		GCLK	t _{CO}	6.812	7.557	ns	
		GCLK PLL	t _{CO}	3.862	4.337	ns	
1.2V		2 mA	GCLK	t _{CO}	9.431	10.729	ns
			GCLK PLL	t _{CO}	6.481	7.509	ns
		4 mA	GCLK	t _{CO}	8.854	10.058	ns
			GCLK PLL	t _{CO}	5.904	6.838	ns
	6 mA	GCLK	t _{CO}	8.640	9.804	ns	
		GCLK PLL	t _{CO}	5.690	6.584	ns	
	8 mA	GCLK	t _{CO}	8.547	9.698	ns	
		GCLK PLL	t _{CO}	5.597	6.478	ns	
	10 mA	GCLK	t _{CO}	8.363	9.456	ns	
		GCLK PLL	t _{CO}	5.413	6.236	ns	
	12 mA	GCLK	t _{CO}	8.335	9.428	ns	
		GCLK PLL	t _{CO}	5.385	6.208	ns	

Table 1–89. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t _{CO}	5.796	6.352	ns
		GCLK PLL	t _{CO}	2.852	3.150	ns
	12 mA	GCLK	t _{CO}	5.760	6.315	ns
		GCLK PLL	t _{CO}	2.816	3.113	ns
SSTL-2 Class II	16 mA	GCLK	t _{CO}	5.698	6.248	ns
		GCLK PLL	t _{CO}	2.754	3.046	ns
SSTL-18 Class I	8 mA	GCLK	t _{CO}	6.270	6.904	ns
		GCLK PLL	t _{CO}	3.326	3.702	ns
	10 mA	GCLK	t _{CO}	6.232	6.858	ns
		GCLK PLL	t _{CO}	3.288	3.656	ns
	12 mA	GCLK	t _{CO}	6.217	6.840	ns
		GCLK PLL	t _{CO}	3.273	3.638	ns
SSTL-18 Class II	12 mA	GCLK	t _{CO}	6.202	6.827	ns
		GCLK PLL	t _{CO}	3.258	3.625	ns
	16 mA	GCLK	t _{CO}	6.183	6.807	ns
		GCLK PLL	t _{CO}	3.239	3.605	ns
1.8-V HSTL Class I	8 mA	GCLK	t _{CO}	6.242	6.866	ns
		GCLK PLL	t _{CO}	3.298	3.664	ns
	10 mA	GCLK	t _{CO}	6.235	6.863	ns
		GCLK PLL	t _{CO}	3.291	3.661	ns
	12 mA	GCLK	t _{CO}	6.210	6.832	ns
		GCLK PLL	t _{CO}	3.266	3.630	ns
1.8-V HSTL Class II	16 mA	GCLK	t _{CO}	6.177	6.796	ns
		GCLK PLL	t _{CO}	3.233	3.594	ns
1.5-V HSTL Class I	8 mA	GCLK	t _{CO}	6.837	7.573	ns
		GCLK PLL	t _{CO}	3.893	4.371	ns
	10 mA	GCLK	t _{CO}	6.818	7.548	ns
		GCLK PLL	t _{CO}	3.874	4.346	ns
	12 mA	GCLK	t _{CO}	6.812	7.544	ns
		GCLK PLL	t _{CO}	3.868	4.342	ns
1.5-V HSTL Class II	16 mA	GCLK	t _{CO}	6.759	7.480	ns
		GCLK PLL	t _{CO}	3.815	4.278	ns
1.2-V HSTL Class I	8 mA	GCLK	t _{CO}	8.277	9.351	ns
		GCLK PLL	t _{CO}	5.333	6.149	ns
	10 mA	GCLK	t _{CO}	8.171	9.196	ns
		GCLK PLL	t _{CO}	5.227	5.994	ns
	12 mA	GCLK	t _{CO}	8.171	9.200	ns
		GCLK PLL	t _{CO}	5.227	5.998	ns
1.2-V HSTL Class II	14 mA	GCLK	t _{CO}	8.100	9.119	ns
		GCLK PLL	t _{CO}	5.156	5.917	ns

Table 1–89. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
3.0-V PCI	—	GCLK	t _{CO}	5.879	6.435	ns
		GCLK PLL	t _{CO}	2.929	3.215	ns
3.0-V PCI-X	—	GCLK	t _{CO}	5.879	6.435	ns
		GCLK PLL	t _{CO}	2.929	3.215	ns

Table 1–90. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
3.3-V LVTTTL	4 mA	GCLK	t _{CO}	6.302	6.839	ns
		GCLK PLL	t _{CO}	3.332	3.683	ns
	8 mA	GCLK	t _{CO}	5.838	6.357	ns
		GCLK PLL	t _{CO}	2.868	3.201	ns
3.3-V LVCMOS	2 mA	GCLK	t _{CO}	5.925	6.448	ns
		GCLK PLL	t _{CO}	2.955	3.292	ns
3.0-V LVTTTL	4 mA	GCLK	t _{CO}	6.023	6.539	ns
		GCLK PLL	t _{CO}	3.053	3.383	ns
	8 mA	GCLK	t _{CO}	5.768	6.278	ns
		GCLK PLL	t _{CO}	2.798	3.122	ns
	12 mA	GCLK	t _{CO}	5.642	6.151	ns
		GCLK PLL	t _{CO}	2.672	2.995	ns
	16 mA	GCLK	t _{CO}	5.588	6.084	ns
		GCLK PLL	t _{CO}	2.618	2.928	ns
3.0-V LVCMOS	4 mA	GCLK	t _{CO}	5.767	6.276	ns
		GCLK PLL	t _{CO}	2.797	3.120	ns
	8 mA	GCLK	t _{CO}	5.590	6.087	ns
		GCLK PLL	t _{CO}	2.620	2.931	ns
	12 mA	GCLK	t _{CO}	5.550	6.048	ns
		GCLK PLL	t _{CO}	2.580	2.892	ns
	16 mA	GCLK	t _{CO}	5.530	6.028	ns
		GCLK PLL	t _{CO}	2.560	2.872	ns
2.5V	4 mA	GCLK	t _{CO}	6.162	6.695	ns
		GCLK PLL	t _{CO}	3.192	3.539	ns
	8 mA	GCLK	t _{CO}	5.893	6.419	ns
		GCLK PLL	t _{CO}	2.923	3.263	ns
	12 mA	GCLK	t _{CO}	5.773	6.295	ns
		GCLK PLL	t _{CO}	2.803	3.139	ns
	16 mA	GCLK	t _{CO}	5.717	6.237	ns
		GCLK PLL	t _{CO}	2.747	3.081	ns

Table 1–90. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit	
1.8V	2 mA	GCLK	t _{CO}	7.450	8.142	ns	
		GCLK PLL	t _{CO}	4.480	4.986	ns	
	4 mA	GCLK	t _{CO}	6.880	7.550	ns	
		GCLK PLL	t _{CO}	3.910	4.394	ns	
	6 mA	GCLK	t _{CO}	6.585	7.218	ns	
		GCLK PLL	t _{CO}	3.615	4.062	ns	
	8 mA	GCLK	t _{CO}	6.457	7.073	ns	
		GCLK PLL	t _{CO}	3.487	3.917	ns	
	10 mA	GCLK	t _{CO}	6.403	7.026	ns	
		GCLK PLL	t _{CO}	3.433	3.870	ns	
	12 mA	GCLK	t _{CO}	6.327	6.937	ns	
		GCLK PLL	t _{CO}	3.357	3.781	ns	
	16 mA	GCLK	t _{CO}	6.278	6.882	ns	
		GCLK PLL	t _{CO}	3.308	3.726	ns	
	1.5V	2 mA	GCLK	t _{CO}	8.021	8.894	ns
			GCLK PLL	t _{CO}	5.051	5.738	ns
		4 mA	GCLK	t _{CO}	7.378	8.152	ns
			GCLK PLL	t _{CO}	4.408	4.996	ns
6 mA		GCLK	t _{CO}	7.173	7.936	ns	
		GCLK PLL	t _{CO}	4.203	4.780	ns	
8 mA		GCLK	t _{CO}	7.062	7.796	ns	
		GCLK PLL	t _{CO}	4.092	4.640	ns	
10 mA		GCLK	t _{CO}	6.990	7.727	ns	
		GCLK PLL	t _{CO}	4.020	4.571	ns	
12 mA		GCLK	t _{CO}	6.939	7.663	ns	
		GCLK PLL	t _{CO}	3.969	4.507	ns	
16 mA		GCLK	t _{CO}	6.858	7.575	ns	
		GCLK PLL	t _{CO}	3.888	4.419	ns	
1.2V		2 mA	GCLK	t _{CO}	9.396	10.640	ns
			GCLK PLL	t _{CO}	6.426	7.484	ns
		4 mA	GCLK	t _{CO}	8.830	9.981	ns
			GCLK PLL	t _{CO}	5.860	6.825	ns
	6 mA	GCLK	t _{CO}	8.646	9.766	ns	
		GCLK PLL	t _{CO}	5.676	6.610	ns	
	8 mA	GCLK	t _{CO}	8.548	9.653	ns	
		GCLK PLL	t _{CO}	5.578	6.497	ns	
	10 mA	GCLK	t _{CO}	8.404	9.474	ns	
		GCLK PLL	t _{CO}	5.434	6.318	ns	

Table 1–90. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.742	6.302	ns
		GCLK PLL	t_{CO}	2.831	3.106	ns
	12 mA	GCLK	t_{CO}	5.708	6.266	ns
		GCLK PLL	t_{CO}	2.797	3.070	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.655	6.209	ns
		GCLK PLL	t_{CO}	2.744	3.013	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	6.216	6.855	ns
		GCLK PLL	t_{CO}	3.305	3.659	ns
	10 mA	GCLK	t_{CO}	6.192	6.825	ns
		GCLK PLL	t_{CO}	3.281	3.629	ns
SSTL-18 Class I	12 mA	GCLK	t_{CO}	6.168	6.798	ns
		GCLK PLL	t_{CO}	3.257	3.602	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	6.160	6.791	ns
		GCLK PLL	t_{CO}	3.249	3.595	ns
	16 mA	GCLK	t_{CO}	6.146	6.777	ns
		GCLK PLL	t_{CO}	3.235	3.581	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	6.188	6.816	ns
		GCLK PLL	t_{CO}	3.277	3.620	ns
	10 mA	GCLK	t_{CO}	6.184	6.815	ns
		GCLK PLL	t_{CO}	3.273	3.619	ns
	12 mA	GCLK	t_{CO}	6.170	6.798	ns
		GCLK PLL	t_{CO}	3.259	3.602	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	6.132	6.756	ns
		GCLK PLL	t_{CO}	3.221	3.560	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.787	7.524	ns
		GCLK PLL	t_{CO}	3.876	4.328	ns
	10 mA	GCLK	t_{CO}	6.782	7.515	ns
		GCLK PLL	t_{CO}	3.871	4.319	ns
	12 mA	GCLK	t_{CO}	6.775	7.511	ns
		GCLK PLL	t_{CO}	3.864	4.315	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	6.729	7.458	ns
		GCLK PLL	t_{CO}	3.818	4.262	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	8.252	9.337	ns
		GCLK PLL	t_{CO}	5.341	6.141	ns
	10 mA	GCLK	t_{CO}	8.138	9.173	ns
		GCLK PLL	t_{CO}	5.227	5.977	ns
3.0-V PCI	—	GCLK	t_{CO}	5.855	6.360	ns
		GCLK PLL	t_{CO}	2.885	3.204	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.855	6.360	ns
		GCLK PLL	t_{CO}	2.885	3.204	ns

Table 1–91. EP3C120 Column Pin Differential I/O Timing Parameters

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.348	0.347	ns
			t_H	–0.045	–0.007	ns
		GCLK PLL	t_{SU}	3.314	3.558	ns
			t_H	–3.011	–3.218	ns
LVDS_E_3R	—	GCLK	t_{CO}	5.779	6.347	ns
		GCLK PLL	t_{CO}	5.788	6.357	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	5.779	6.347	ns
		GCLK PLL	t_{CO}	5.788	6.357	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.779	6.347	ns
		GCLK PLL	t_{CO}	5.788	6.357	ns
RSDS_E_1R	—	GCLK	t_{CO}	5.779	6.347	ns
		GCLK PLL	t_{CO}	5.788	6.357	ns
RSDS_E_3R	—	GCLK	t_{CO}	5.779	6.347	ns
		GCLK PLL	t_{CO}	5.788	6.357	ns

Table 1–92. EP3C120 Row Pin Differential I/O Timing Parameters

I/O Standard	Current Strength	Clock	Parameter	–7	–8	Unit
LVDS	—	GCLK	t_{SU}	0.366	0.370	ns
			t_H	–0.064	–0.029	ns
			t_{CO}	4.876	5.340	ns
		GCLK PLL	t_{SU}	3.313	3.561	ns
			t_H	–3.011	–3.220	ns
			t_{CO}	1.938	2.156	ns
mini-LVDS	—	GCLK	t_{CO}	4.876	5.340	ns
		GCLK PLL	t_{CO}	1.938	2.156	ns
PPDS	—	GCLK	t_{CO}	4.876	5.340	ns
		GCLK PLL	t_{CO}	1.938	2.156	ns
RSDS	—	GCLK	t_{CO}	4.876	5.340	ns
		GCLK PLL	t_{CO}	1.938	2.156	ns

Dedicated Clock Pin Timing Parameters

Tables 1–93 through 1–108 show clock pin timing for Cyclone III devices.

EP3C5 Clock Timing Parameters

Tables 1–93 and 1–94 show the maximum clock timing parameters for EP3C5 devices.

Table 1–93. EP3C5 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
t _{cin}	—	1.493	2.193	2.414	2.703	ns
t _{cout}	—	1.522	2.244	2.473	2.726	ns
t _{pllcin}	—	0.770	1.025	1.102	1.268	ns
t _{pllcout}	—	0.799	1.076	1.161	1.290	ns

Table 1–94. EP3C5 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
t _{cin}	—	1.504	2.202	2.420	2.705	ns
t _{cout}	—	1.533	2.253	2.479	2.730	ns
t _{pllcin}	—	0.781	1.034	1.108	1.270	ns
t _{pllcout}	—	0.810	1.085	1.167	1.294	ns

EP3C10 Clock Timing Parameters

Tables 1–95 and 1–96 show the maximum clock timing parameters for EP3C10 devices.

Table 1–95. EP3C10 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
t _{cin}	—	1.492	2.192	2.412	2.701	ns
t _{cout}	—	1.521	2.243	2.471	2.724	ns
t _{pllcin}	—	0.769	1.024	1.100	1.266	ns
t _{pllcout}	—	0.798	1.075	1.159	1.288	ns

Table 1–96. EP3C10 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
tcin	—	1.501	2.199	2.417	2.701	ns
tcout	—	1.530	2.250	2.476	2.730	ns
tpllcin	—	0.778	1.031	1.105	1.266	ns
tpllcout	—	0.807	1.082	1.164	1.294	ns

EP3C16 Clock Timing Parameters

Tables 1–97 and 1–98 show the maximum clock timing parameters for EP3C16 devices.

Table 1–97. EP3C16 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
tcin	—	1.646	2.421	2.661	2.944	ns
tcout	—	1.675	2.472	2.720	2.991	ns
tpllcin	—	0.985	1.332	1.435	1.576	ns
tpllcout	—	1.014	1.383	1.494	1.643	ns

Table 1–98. EP3C16 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
tcin	—	1.637	2.406	2.642	2.925	ns
tcout	—	1.666	2.457	2.701	2.974	ns
tpllcin	—	0.976	1.317	1.416	1.559	ns
tpllcout	—	1.005	1.368	1.475	1.626	ns

EP3C25 Clock Timing Parameters

Tables 1–99 and 1–100 show the maximum clock timing parameters for EP3C25 devices.

Table 1–99. EP3C25 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
tcin	—	1.654	2.442	2.689	2.974	ns
tcout	—	1.683	2.493	2.748	3.023	ns
tpllcin	—	0.973	1.335	1.442	1.586	ns
tpllcout	—	1.002	1.386	1.501	1.653	ns

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
t _{cin}	—	1.655	2.438	2.678	2.962	ns
t _{cout}	—	1.684	2.489	2.737	3.011	ns
t _{pllcin}	—	0.974	1.331	1.431	1.574	ns
t _{pllcout}	—	1.003	1.382	1.490	1.641	ns

EP3C40 Clock Timing Parameters

Tables 1–101 and 1–102 show the maximum clock timing parameters for EP3C40 device.

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
t _{cin}	—	1.783	2.617	2.871	3.172	ns
t _{cout}	—	1.812	2.668	2.930	3.221	ns
t _{pllcin}	—	1.073	1.451	1.557	1.705	ns
t _{pllcout}	—	1.102	1.502	1.616	1.772	ns

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
t _{cin}	—	1.777	2.603	2.865	3.162	ns
t _{cout}	—	1.806	2.654	2.924	3.211	ns
t _{pllcin}	—	1.067	1.437	1.551	1.695	ns
t _{pllcout}	—	1.096	1.488	1.610	1.762	ns

EP3C55 Clock Timing Parameters

Tables 1–103 and 1–104 show the maximum clock timing parameters for EP3C55 devices.

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
t _{cin}	—	1.775	2.616	2.873	3.177	ns
t _{cout}	—	1.804	2.667	2.932	3.228	ns
t _{pllcin}	—	1.104	1.512	1.631	1.803	ns
t _{pllcout}	—	1.133	1.563	1.690	1.870	ns

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
tcin	—	1.777	2.613	2.867	3.177	ns
tcout	—	1.806	2.664	2.926	3.230	ns
tpllcin	—	1.106	1.509	1.625	1.805	ns
tpllcout	—	1.135	1.560	1.684	1.872	ns

EP3C80 Clock Timing Parameters

Tables 1–105 and 1–106 show the maximum clock timing parameters for EP3C80 devices.

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
tcin	—	1.882	2.787	3.063	3.382	ns
tcout	—	1.911	2.838	3.122	3.436	ns
tpllcin	—	1.132	1.544	1.662	1.830	ns
tpllcout	—	1.161	1.595	1.721	1.897	ns

Parameter	Fast Model		–6	–7	–8	Unit
	Industrial	Commercial				
tcin	—	1.887	2.789	3.069	3.373	ns
tcout	—	1.916	2.840	3.128	3.431	ns
tpllcin	—	1.137	1.546	1.668	1.825	ns
tpllcout	—	1.166	1.597	1.727	1.892	ns

EP3C120 Clock Timing Parameters

Tables 1–107 and 1–108 show the maximum clock timing parameters for EP3C120 devices. EP3C120 devices are offered in –7 and –8 speed grades only.

Parameter	Fast Model		–7	–8	Unit
	Industrial	Commercial			
tcin	—	1.942	3.129	3.448	ns
tcout	—	1.971	3.188	3.504	ns
tpllcin	—	1.183	1.749	1.933	ns
tpllcout	—	1.212	1.808	2.000	ns

Table 1–108. EP3C120 Row Pin Global Clock Timing Parameters					
Parameter	Fast Model		–7	–8	Unit
	Industrial	Commercial			
tcin	—	1.945	3.122	3.430	ns
tcout	—	1.974	3.181	3.486	ns
tpllcin	—	1.186	1.742	1.915	ns
tpllcout	—	1.215	1.801	1.982	ns

Glossary

Table 1–109 shows the glossary for this chapter.

Table 1–109. Glossary (Part 1 of 4)		
Letter	Term	Definitions
A	—	—
B	—	—
C	—	—
D	—	—
E	—	—
F	f_{HSCLK}	HIGH-SPEED I/O Block: High-speed receiver/transmitter input and output clock frequency.
G	GCLK	Input pin directly to Global Clock network.
	GCLK PLL	Input pin to Global Clock network through PLL.
H	HSIODR	HIGH-SPEED I/O Block: Maximum/minimum LVDS data transfer rate ($\text{HSIODR} = 1/\text{TUI}$).
I	Input Waveforms for the SSTL Differential I/O Standard	
J	JTAG Waveform	
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—

Table 1–109. Glossary (Part 2 of 4)

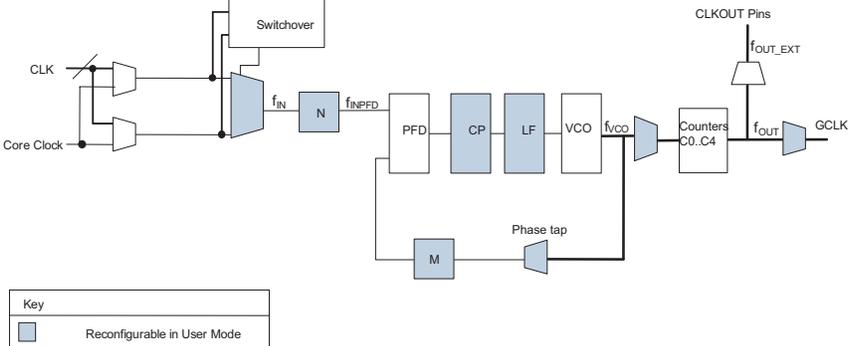
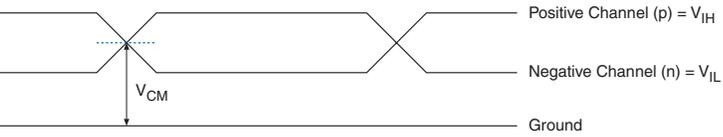
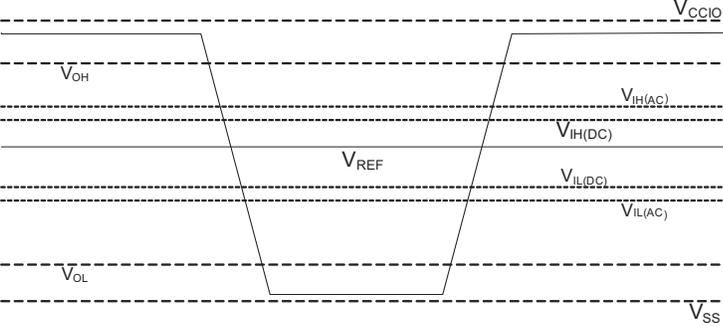
Letter	Term	Definitions
P	PLL Block	<p>The following block diagram highlights the PLL Specification parameters.</p>  <p>Key Reconfigurable in User Mode</p>
Q	—	—
R	<p>R_L</p> <p>Receiver Input Waveform</p>	<p>Receiver differential input discrete resistor (external to Cyclone III device).</p> <p>Receiver Input Waveform for LVDS and LVPECL Differential Standards.</p> <p>Single-Ended Waveform</p>  <p>Positive Channel (p) = V_{IH} Negative Channel (n) = V_{IL} Ground</p> <p>Differential Input Waveform</p>  <p>+ V_{TH} 0 V - V_{TH} p - n</p>
	RSKM (Receiver input skew margin)	HIGH-SPEED I/O Block: The total margin left after accounting for the sampling window and TCCS. $RSKM = (TUI - SW - TCCS) / 2$.
S	Single-ended Voltage referenced I/O Standard	 <p>The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. Once the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform <i>ringing</i>.</p>
	SW (Sampling Window)	HIGH-SPEED I/O Block: The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.

Table 1–109. Glossary (Part 3 of 4)

Letter	Term	Definitions
T	t_c	High-speed receiver/transmitter input and output clock period.
	TCCS (Channel-to-channel-skew)	HIGH-SPEED I/O Block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
	t_{cin}	Delay from clock pad to I/O input register.
	t_{CO}	Delay from clock pad to I/O output.
	t_{cout}	Delay from clock pad to I/O output register.
	t_{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock.
	t_{FALL}	Signal High-to-low transition time (80–20%).
	t_H	Input register hold time.
	Timing Unit Interval (TUI)	HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_c/w$).
	$t_{INJITTER}$	Period jitter on PLL clock input.
	$t_{OUTJITTER_DEDCLK}$	Period jitter on dedicated clock output driven by a PLL.
	$t_{OUTJITTER_IO}$	Period jitter on general purpose I/O driven by a PLL.
		Transmitter Output Waveform
t_{RISE}		Signal Low-to-high transition time (20 – 80%).
t_{SU}		Input register setup time.
U		—

Table 1–109. Glossary (Part 4 of 4)

Letter	Term	Definitions
V	$V_{CM(DC)}$	DC Common Mode Input Voltage.
	$V_{DIF(AC)}$	AC differential Input Voltage: The minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential Input Voltage: The minimum DC input differential voltage required for switching.
	V_{ICM}	Input Common Mode Voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V_{IH}	Voltage Input High: The minimum positive voltage applied to the input which will be accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	V_{IL}	Voltage Input Low: The maximum positive voltage applied to the input which will be accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage.
	$V_{IL(DC)}$	Low-level DC input voltage.
	V_{IN}	DC input voltage.
	V_{OCM}	Output Common Mode Voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} - V_{OL}$.
	V_{OH}	Voltage Output High: The maximum positive voltage from an output which the device considers will be accepted as the minimum positive high level.
	V_{OL}	Voltage Output Low: The maximum positive voltage from an output which the device considers will be accepted as the maximum positive low level.
	V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
	$V_{OX(AC)}$	AC differential Output cross point voltage: The voltage at which the differential output signals must cross.
	V_{REF}	Reference voltage for SSTL, HSTL I/O Standards.
	$V_{REF(AC)}$	AC input reference voltage for SSTL, HSTL I/O Standards. $V_{REF(AC)} = V_{REF(DC)} + \text{noise}$, The peak-to-peak AC noise on V_{REF} should not exceed 2% of $V_{REF(DC)}$.
$V_{REF(DC)}$	DC input reference voltage for SSTL, HSTL I/O Standards.	
$V_{SWING(AC)}$	AC differential Input Voltage: AC Input differential voltage required for switching. Refer to Input Waveforms for the SSTL Differential I/O Standard.	
$V_{SWING(DC)}$	DC differential Input Voltage: DC Input differential voltage required for switching. Refer to Input Waveforms for the SSTL Differential I/O Standard.	
V	V_{TH}	Differential input threshold.
	V_{TT}	Termination voltage for SSTL, HSTL I/O Standards.
	$V_X(AC)$	AC differential Input cross point Voltage: The voltage at which the differential input signals must cross.
W	—	—
X	—	—
Y	—	—
Z	—	—

Referenced Documents

This chapter references the following documents:

- [AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTTL/LVCMOS I/O Systems](#)
- [Cyclone III Device I/O Features](#) chapter in volume 1 of the *Cyclone III Device Handbook*
- [High-Speed Differential Interfaces](#) chapter in volume 1 of the *Cyclone III Device Handbook*

- *PowerPlay Early Power Estimator User Guide for Cyclone III FPGAs*
- *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*

Document Revision History

Table 1–110 shows the revision history for this document.

<i>Table 1–110. Document Revision History</i>		
Date and Document Version	Changes Made	Summary of Changes
October 2007 v1.4	<ul style="list-style-type: none"> ● Updated the C_{VREFTB} value in Table 1–9. ● Updated Table 1–21. ● Under “High-Speed I/O Specification” section, updated Tables 1–25 through 1–30. ● Updated Tables 1–31 and 1–38. ● Added new Table 1–32. ● Under “Maximum Input and Output Clock Toggle Rate” section, updated Tables 1–40 through 1–42. ● Under “IOE Programmable Delay” section, updated Tables 1–43 through 1–44. ● Under “User I/O Pin Timing Parameters” section, updated Tables 1–45 through 1–92. ● Under “Dedicated Clock Pin Timing Parameters” section, updated Tables 1–93 through 1–108. 	Updated I/O Timing section and other parts of the document as well.
July 2007 v1.3	<ul style="list-style-type: none"> ● Updated Table 1–1 with V_{ESDHBM} and V_{ESDCDM} information. ● Updated R_{CONF_PD} information in Table 1–10. ● Added <i>Note (3)</i> to Table 1–12. ● Updated t_{DLOCK} information in Table 1–19. ● Updated Tables 1–40 and 1–41. ● Added “Referenced Documents” section. 	—
June 2007 v1.2	Updated Cyclone III graphic in cover page.	Revised Cover
May 2007 v1.1	<ul style="list-style-type: none"> ● Corrected current unit in Table 1–1, Table 1–12, and Table 1–14. ● Added <i>Note (3)</i> to Table 1–3. ● Updated Table 1–4 with I_{CCINT0}, I_{CCA0}, I_{CCD_PLL0}, and I_{CCIO0} information. ● Updated Table 1–9 and added <i>Note (2)</i>. ● Updated Table 1–19. ● Updated Table 1–22 and added <i>Note (1)</i>. ● Changed I/O standard from 1.5-V LVTTTL/LVCMOS and 1.2-V LVTTTL/LVCMOS to 1.5-V LVCMOS and 1.2-V LVCMOS in Table 1–38, Table 1–39, Table 1–40, Table 1–41, and Table 1–42. ● Updated Table 1–40 with changes to LVPEC and LVDS and added Note 5. ● Updated Table 1–43, Table 1–44, Tables 1–51 through 1–92, and Tables 1–95 through 1–108. ● Removed speed grade –6 from Tables 1–87 through 1–92, and from Tables 1–107 through 1–108. ● Added new Tables 1–45 through 1–50, Table 1–93, and Table 1–94. ● Added a waveform (Receiver Input Waveform) in glossary under letter “R” (Table 1–109). 	Updated I/O Timing section and other parts of the document as well.
March 2007 v1.0	Initial Release.	—