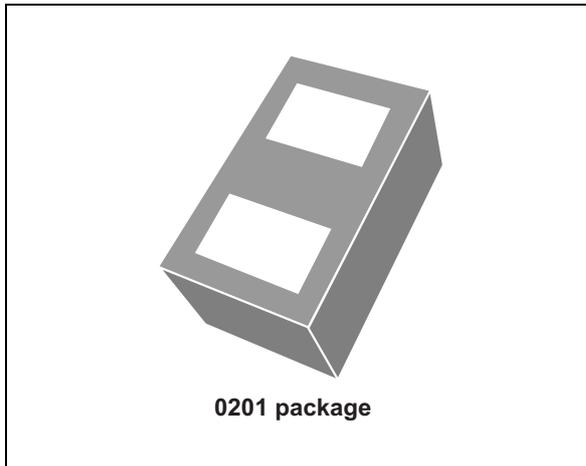


Low clamping and ultra low capacitance single line bidirectional ESD protection

Datasheet - production data



Features

- Low clamping voltage
- Bidirectional device
- Dynamic resistance $R_d = 0.3 \Omega$ typ.
- Low leakage current
- 0201 package size compatible
- Ultra small PCB area: 0.18 mm^2
- ECOPACK^{®2} compliant component

Complies with the following standards

- IEC 61000-4-2 level 4:
 - $\pm 30 \text{ kV}$ (air discharge)
 - $\pm 30 \text{ kV}$ (contact discharge)

Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

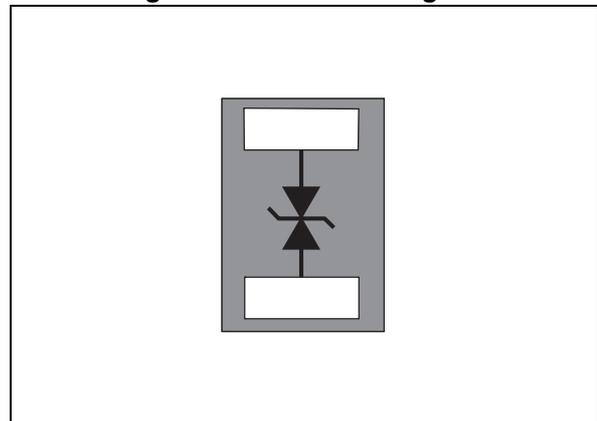
- Smartphones, mobile phones and accessories
- Tablet, PC, netbooks and notebooks
- Portable multimedia devices and accessories
- Digital cameras and camcorders
- Communication and highly integrated systems

Description

The ESDAULC5-1BF4 is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

Figure 1. Functional diagram



1 Characteristics

Table 1. Absolute maximum ratings

Symbol	Parameter		Value	Unit
$V_{PP}^{(1)}$	Peak pulse voltage	IEC 61000-4-2 contact discharge	30	kV
		IEC 61000-4-2 air discharge	30	
$P_{PP}^{(1)}$	Peak pulse power (8/20 μ s)		140	W
$I_{PP}^{(1)}$	Peak pulse current (8/20 μ s)		10	A
T_j	Operating junction temperature range		-40 to 150	$^{\circ}$ C
T_{stg}	Storage temperature range		-65 to +150	$^{\circ}$ C
T_L	Maximum lead temperature for soldering during 10 s		260	$^{\circ}$ C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

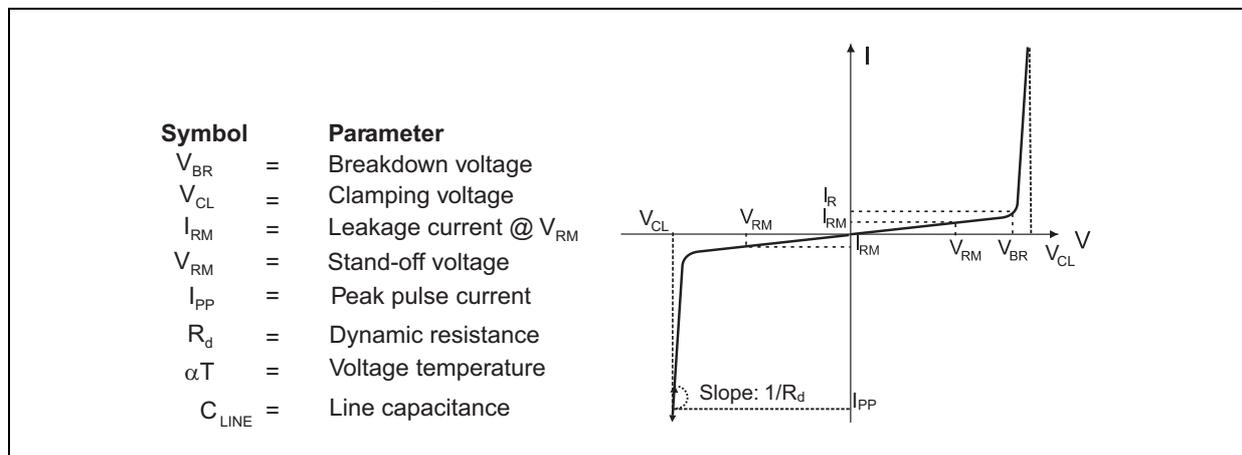


Table 2. Electrical characteristics (values, $T_{amb} = 25^{\circ}$ C)

Symbol	Test conditions	Value			Unit
		Min.	Typ.	Max.	
V_{BR}	$I_R = 1$ mA	5.8		8.5	V
I_{RM}	$V_{RM} = 3$ V			70	nA
V_{CL}	8 kV contact discharge after 30 ns, IEC 61000-4-2		13.5		V
C_{LINE}	$V_{LINE} = 0$ V, $F = 1$ MHz, $V_{OSC} = 30$ mV		1.5	3	pF
R_d	Dynamic resistance, pulse duration 100 ns, I/O to GND		0.3		Ω

Figure 3. Leakage current versus junction temperature (typical values)

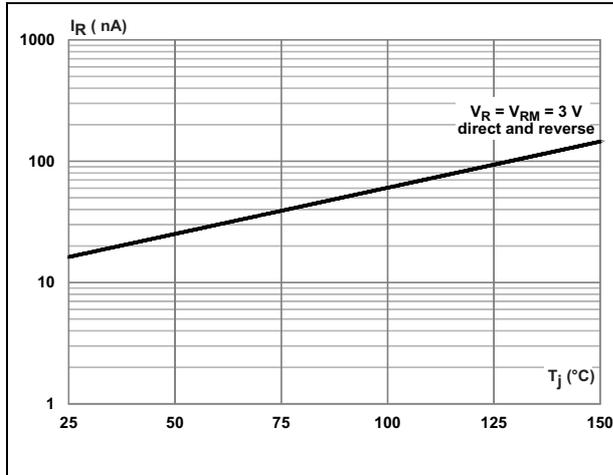


Figure 4. S21 attenuation measurement result

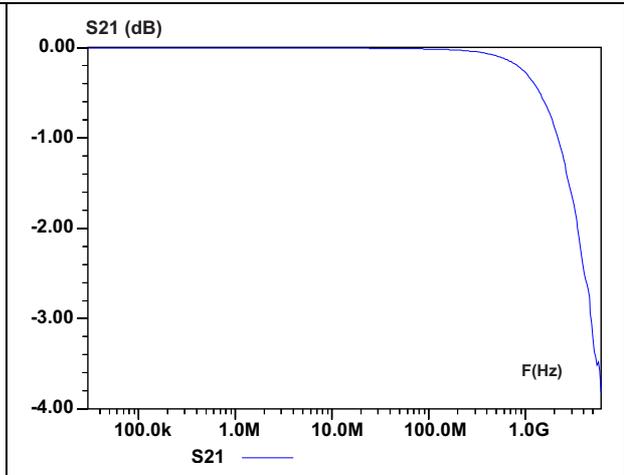


Figure 5. Eye diagram HDMI 1.4 (1080p/60 Hz) 3.35 Gbps Thru PCB

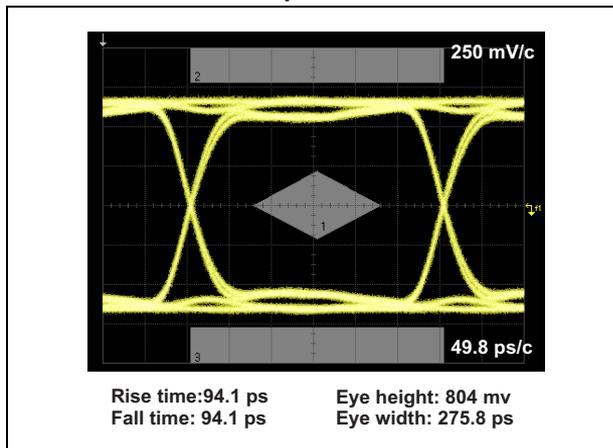


Figure 6. Eye diagram HDMI 1.4 (1080p/60 Hz) 3.35 Gbps ESDAULC5-1BF4

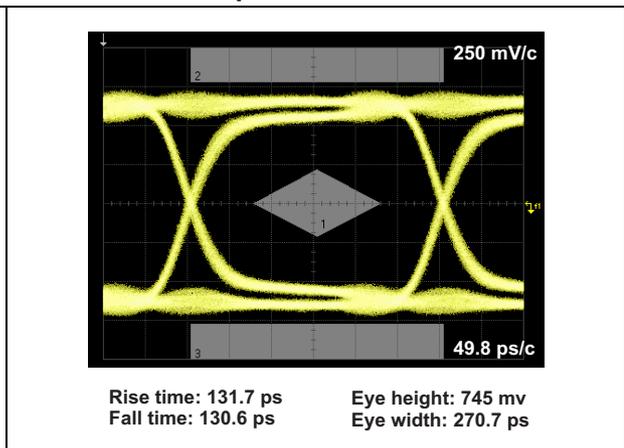


Figure 7. Eye diagram display port HBR 2.7 Gbps Thru PCB

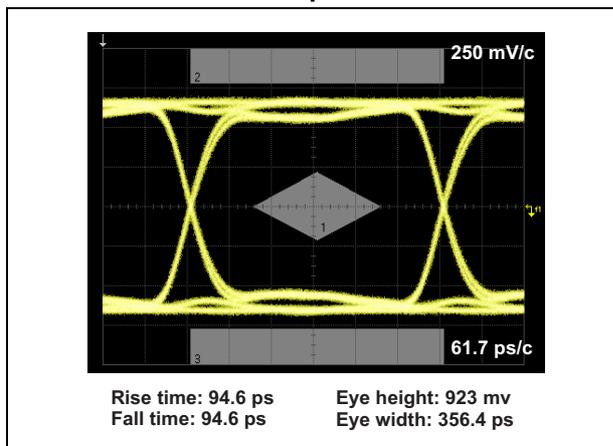


Figure 8. Eye diagram display port HBR 2.7 Gbps ESDAULC5-1BF4

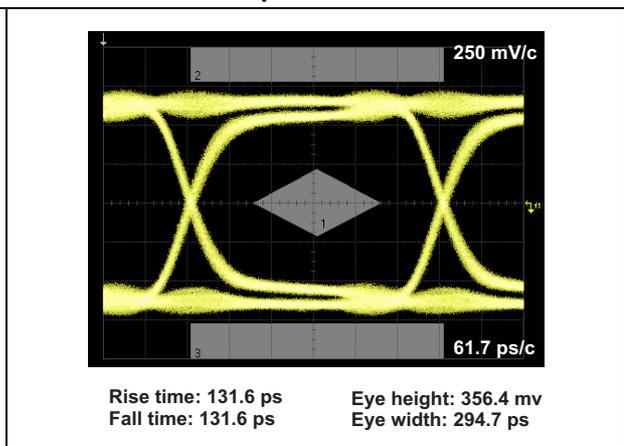
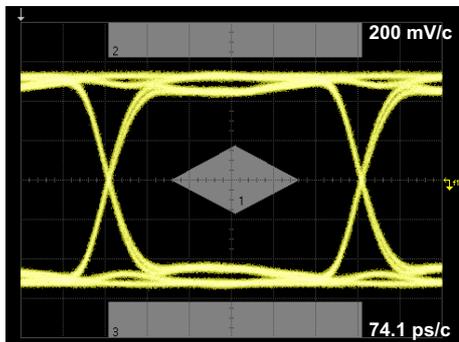
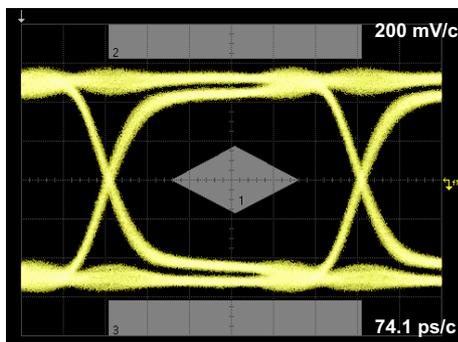


Figure 9. Eye diagram MHL 1.0
2.5 Gbps Thru PCB



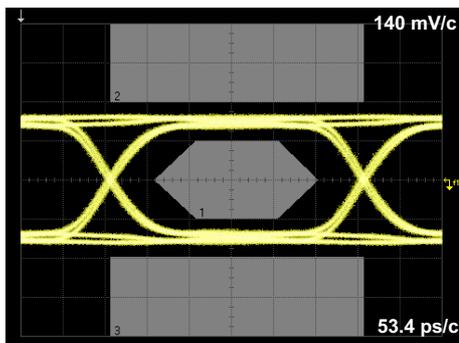
Rise time: 92.2 ps Eye height: 743 mv
Fall time: 90.6 ps Eye width: 430.1 ps

Figure 10. Eye diagram MHL 1.0
2.5 Gbps ESDAULC5-1BF4



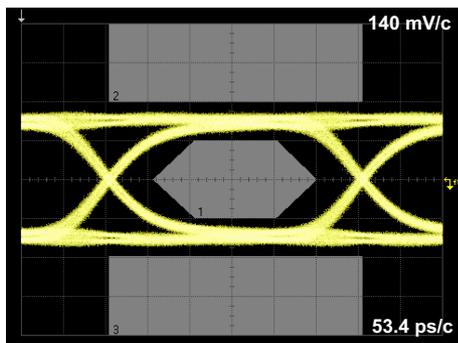
Rise time: 136.7 ps Eye height: 729 mv
Fall time: 133.4 ps Eye width: 418.6 ps

Figure 11. Eye diagram SD4.2,
3.12 Gbps Thru PCB



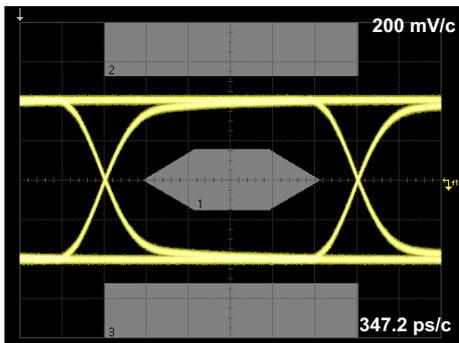
Rise time: 98.5 ps Eye height: 345 mv
Fall time: 96.1 ps Eye width: 299.5 ps

Figure 12. Eye diagram SD4.2,
3.12 Gbps ESDAULC5-1BF4



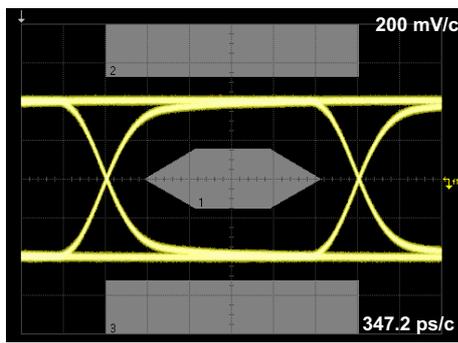
Rise time: 137.7 ps Eye height: 321 mv
Fall time: 138.8 ps Eye width: 294.7 ps

Figure 13. Eye diagram USB2.0,
480 Mbps Thru PCB



Rise time: 532 ps Eye height: 718 mv
Fall time: 532 ps Eye width: 2042 ps

Figure 14. Eye diagram USB2.0,
480 Mbps ESDAULC5-1BF4



Rise time: 556 ps Eye height: 716 mv
Fall time: 548 ps Eye width: 2048 ps

Figure 15. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

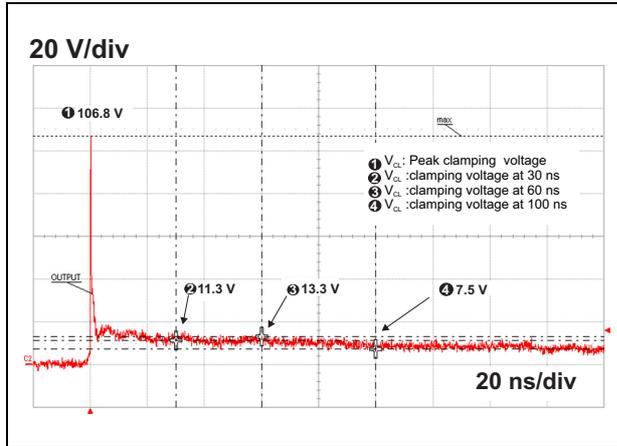


Figure 16. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

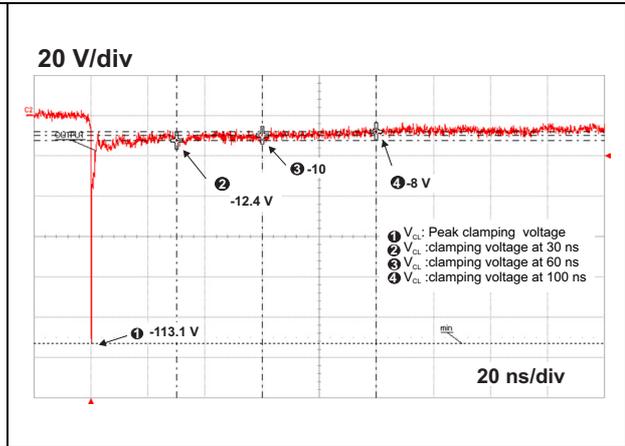
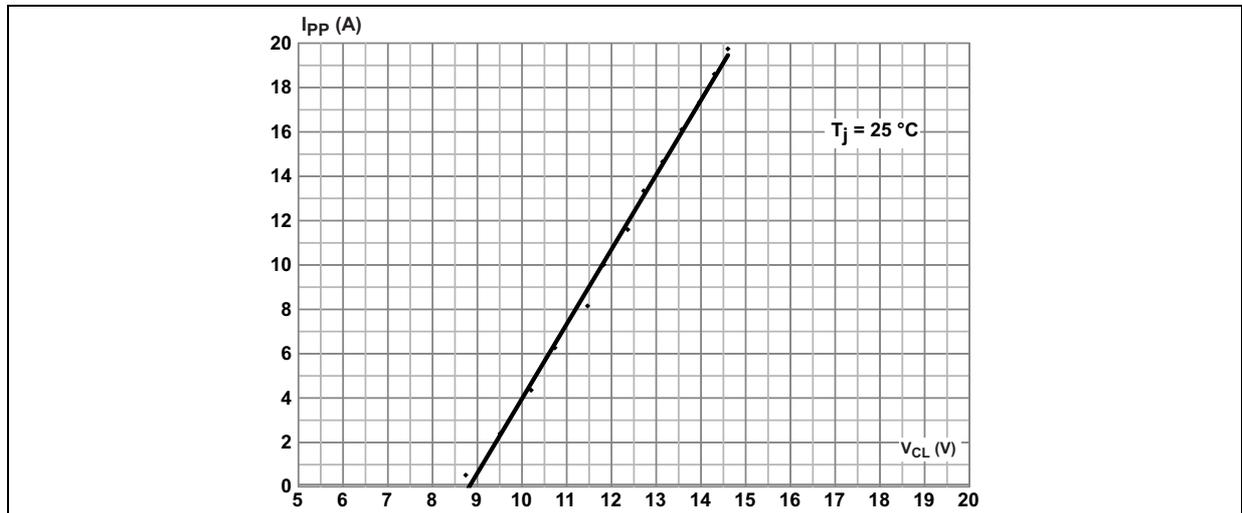


Figure 17. TLP measurements



2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 18. 0201 package dimension definitions

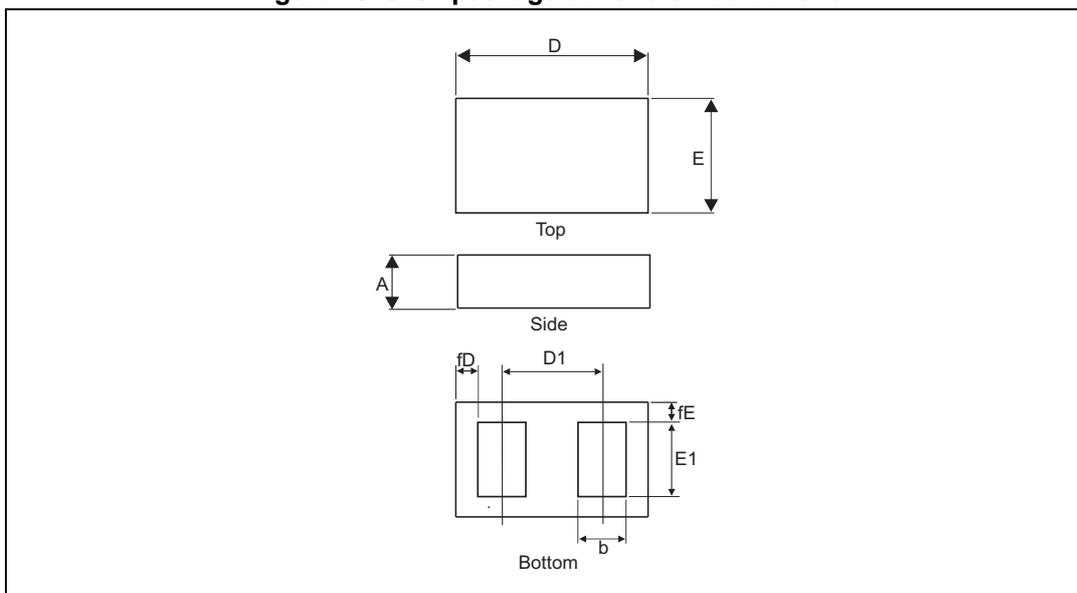


Table 3. 0201 package dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.28	0.3	0.32	0.0110	0.0118	0.0126
b	0.125	0.14	0.155	0.0049	0.0055	0.0061
D	0.57	0.6	0.63	0.0224	0.0236	0.0248
D1		0.35			0.0138	
E	0.27	0.3	0.33	0.0106	0.0118	0.0130
E1	0.175	0.19	0.205	0.0069	0.0075	0.0081
fD	0.065	0.08	0.095	0.0026	0.0031	0.0037
fE	0.11	0.125	0.13	0.0043	0.0049	0.0051

Figure 19. Footprint in mm (inches)

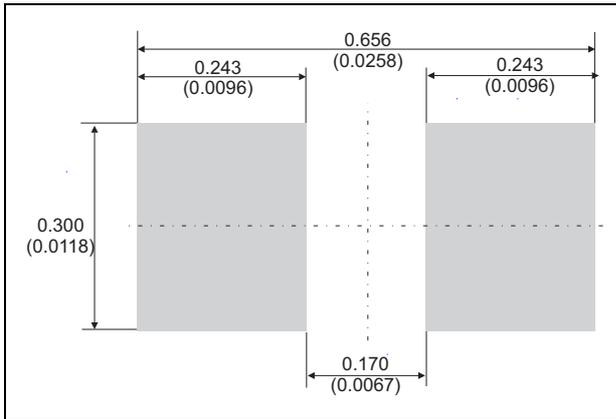
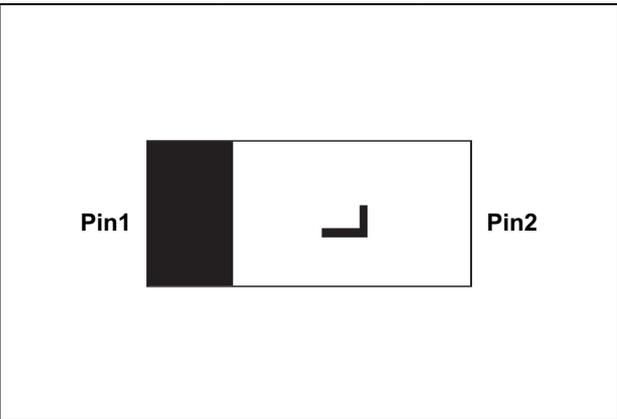
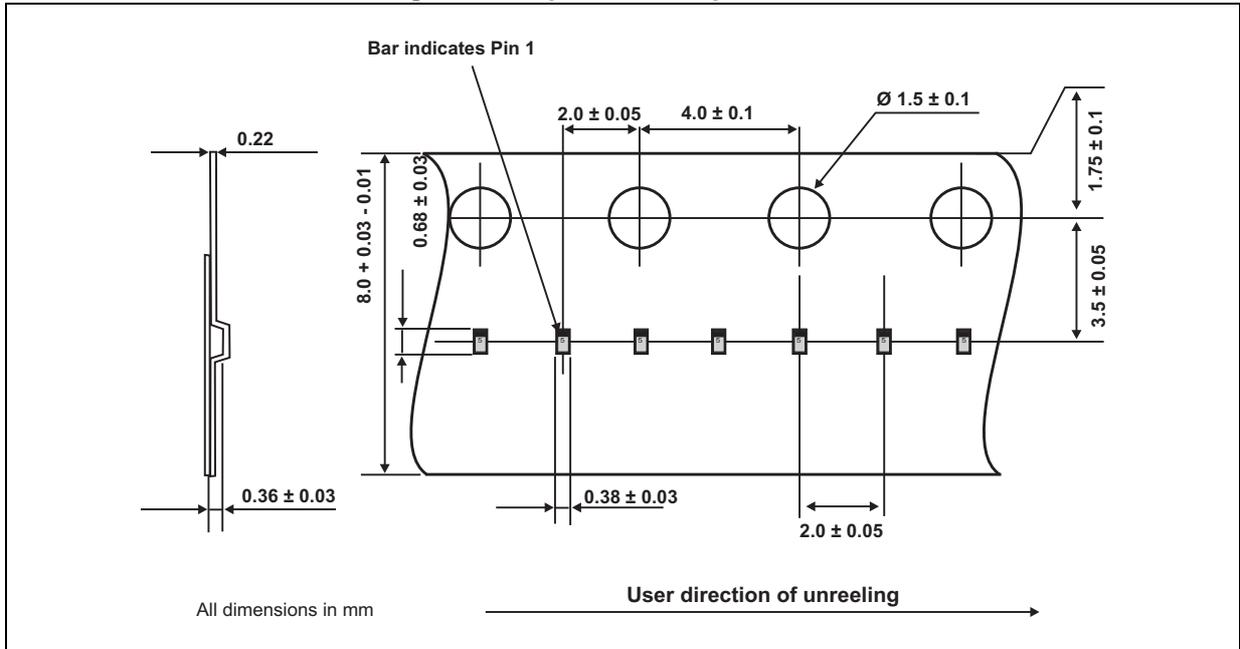


Figure 20. Marking



Note: The marking codes can be rotated by 90° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 21. Tape and reel specification

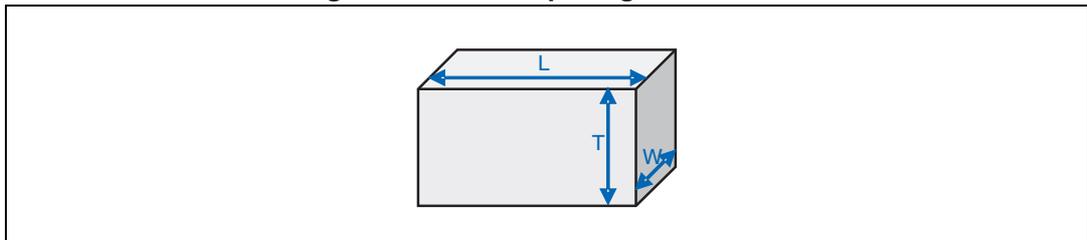


3 Recommendation on PCB assembly

3.1 Stencil opening design

1. General recommendations on stencil opening design
 - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

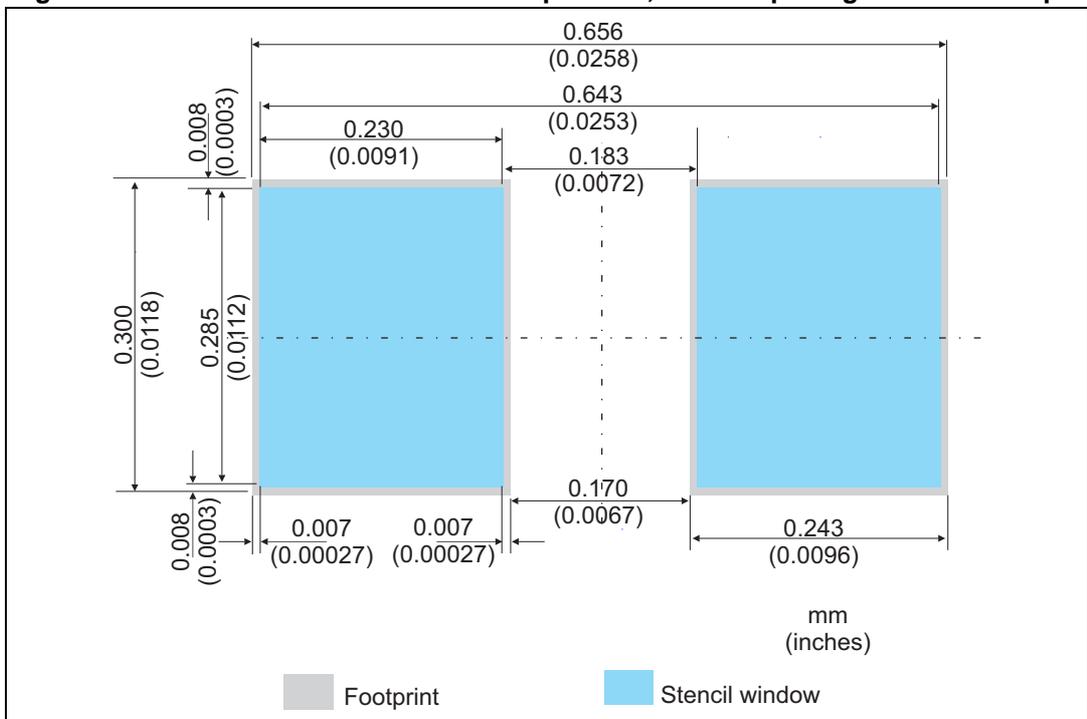
Figure 22. Stencil opening dimensions



- b) General design rule
 - Stencil thickness (T) = 75 ~ 125 μm
 - Aspect Ratio = $\frac{W}{T} \geq 1.5$
 - Aspect Area = $\frac{L \times W}{2T(L + W)} \geq 0.66$

2. Recommended stencil window
 - a) Stencil opening thickness: 80 μm
 - b) Other dimensions: see [Figure 23](#)

Figure 23. Recommended stencil window position, stencil opening thickness: 80 μm



3.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: Type 4 (powder particle size 20-48 μm per IPC J STD-005).

3.3 Placement

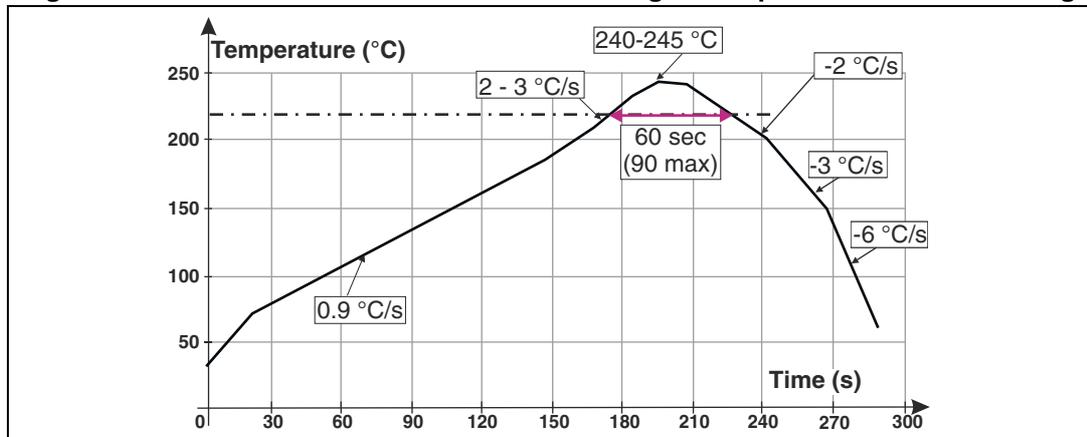
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

3.5 Reflow profile

Figure 24. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

4 Ordering information

Figure 25. Ordering information scheme

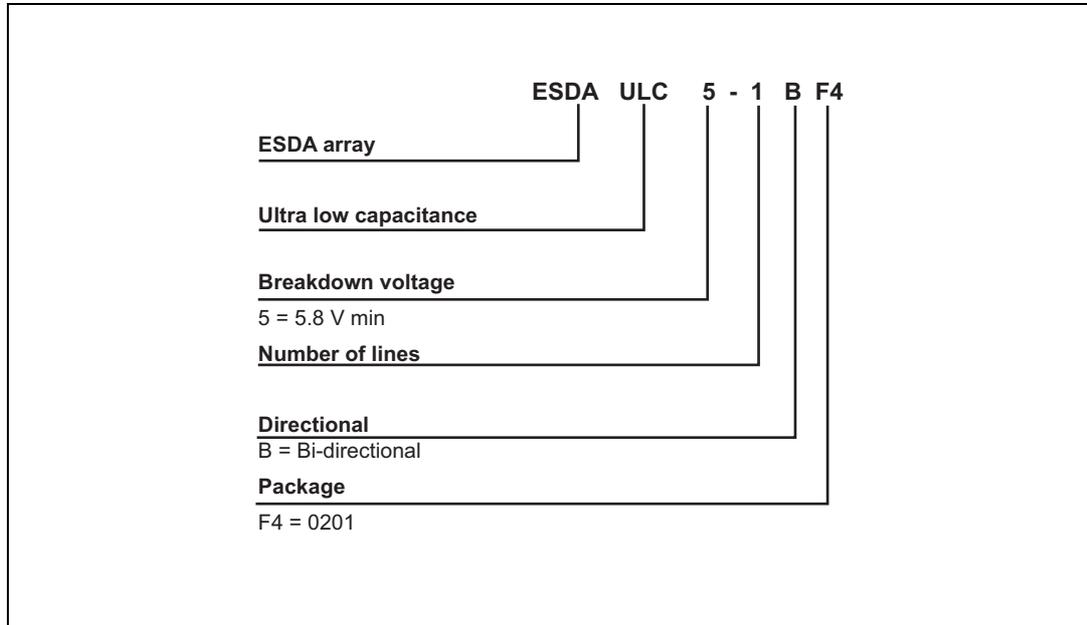


Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDAULC5-1BF4	L ⁽¹⁾	0201	0.116 mg	15000	Tape and reel

1. The marking codes can be rotated by 90° or 180° to differentiate assembly location

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
03-Jun-2014	1	First issue.

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