EVK-THEMIS-ATLAS-Evaluation Board Application Note

Version: 1.3

General description

The EVK-THEMIS-ATLAS evaluation board demonstrates the functionality of a power gate driver circuit using CHT-THEMIS and CHT-ATLAS devices. The board features a gate current output capability of up to 4A total, controllable through 2 distinct channels of 2A each. It is designed and optimized in order to drive external power switch devices that can be either silicon carbide (SiC) MOSFET or normally-On JFET devices (the configuration is selectable by the user at board-level). Other power switch devices can be used, such as normally-Off JFET, as well as IGBTs and even BJTs, but hardware changes could be required. With high switching frequency capability, EVK-THEMIS-ATLAS is the solution of choice for the most advanced silicon carbide or gallium-nitride (GaN) based solutions and high power-density systems. It also allows extending the lifetime of power converters which implement traditional silicon MOSFETs or IGBTs by an order of magnitude, taking advantage of CISSOID high reliability technology, with an estimated lifetime of 20 to 30 years at 125°C operating temperature.

The Evaluation Board can be used as a turnkey gate-driver and can be plugged directly into the user's system and power board or module. The implementation minimizes the propagation delay, the gate transition time and the desaturation detection time, while coping with dV/dt up to 50kV/µs.

The board is populated with CISSOID CHT-THEMIS and CHT-ATLAS integrated circuits in ceramic package form (CSOIC28, guaranteed for -55°C to +225°C). The board being based on a polyimide PCB (rated 200°C), it is suitable for use up to 175°C, with possible short excursions to 225°C for testing.

The EVK-THEMIS-ATLAS evaluation board core components are the CISSOID CHT-THEMIS, CHT-ATLAS and CHT-MOON. The evaluation board is delivered with the complete electrical schematic, the bill of materials including active and passive components, the Gerber files.

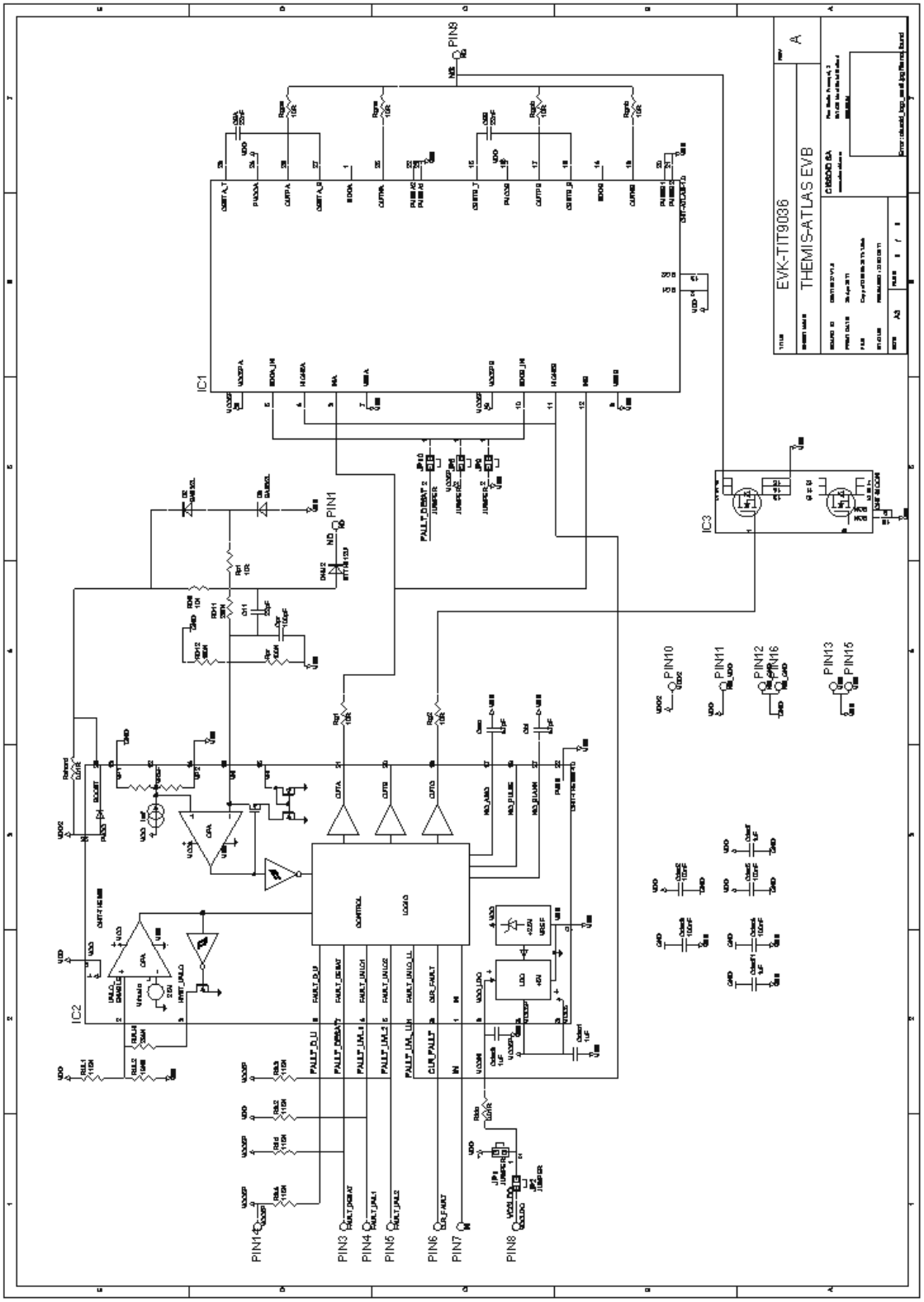
Features

- DC bus voltage: up to 1200V
- Supply Voltage: 5 to 30V
- High common mode transient immunity: 50KV/µS
- Typical switching time: 10ns (with C_{Load}=1nF and V_{CC}=15V)
- Adjustable Under-voltage lockout
- De-saturation detection circuit
- Active Miller clamping (AMC) support
- 100% duty cycle support
- Fault signals (2) generation
  - UVLO
  - DESAT
- Capable to drive normally-On JFET and normally-Off MOSFET SIC devices
- Operating ambient temperature: from -55°C to +175°C
- Active components all qualified from -55 to +225°C (Tj)

Applications

- High density power modules
- Motor drives, battery chargers and DC-DC converters in EV / HEV
- Electrical power conversion, power generation and actuator controls in aeronautics
- Power conversion and motor drive in railway
- Wind turbine power converters
- Solar inverters
- General purpose AC-DC, DC-AC and DC-DC Converters

Detailed Schematic



Bill of Material

Qty	Part Type	Designator	Description	Manufacturer	Part number
1	IC	*IC1*	CHT-ATLAS, Dual Channel Power Transistor Driver	Cissoid	CHT-TIT3345B-CSOIC28-T
1	IC	*IC2*	CHT-THEMIS, Dual Channel Power Transistor Driver	Cissoid	CHT-TIT9570A-CSOIC28-T
1	MOS	*IC3*	CHT-MOON, dual MOSFET N-Channel	Cissoid	CHT-PLA2016A-CSOIC16-T
5	115k	*RUL1, Rflt1, Rflt2, Rflt3, Rflt4*	0805 Thin film resistor, 0.125W 0.1%	Panasonic	ERA6AEB1153V
1	19.6k	*RUL2*	0805 Thin film resistor, 0.125W 0.1%	Panasonic	ERA6AEB1962V
1	294k	*RULH*	0805 Thin film resistor, 0.125W 0.1%	Panasonic	ERA6AEB2943V
2	0.01R	*Rshort1, Rldo*	1206 Metal strip resistor, 0.25W 1%	Vishay Dale	WSL1206R0100FEB
1	160k	*RD12*	0805 Thin film resistor, 0.125W 0.1%	Panasonic	ERA6AEB164V
1	100k	*Rpr*	0805 Thin film resistor, 0.125W 0.1%	Panasonic	ERA6AEB104V
1	267k	*RD11*	0805 Thin film resistor, 0.125W 0.1%	Panasonic	ERA6AEB2673V
1	10k	*RDS*	2512 Thick film resistor, 1W 1%	Yageo (Phycomp)	RC2512FK-0710KL
7	10R	*Rp1, Rg1, Rg2, Rgpa, Rgpb, Rgna, Rgnb*	1206 Thick film resistor, 0.5W 1%	Vishay Draloric	CRCW120610R0FKEAHP
4	1µF	*Cdec1, Cdec7, Cdec71, Cdec8*	1210 X8L capacitor, 50V 10%	Kemet	C1210C105K5NACTU
4	100nF	*Cdec2, Cdec3, Cdec4, Cdec5*	0805 X8R capacitor, 50V 10%	AVX	08055F104KAT2A
2	47pF	*Cbl, Cmc*	1206 C0G/NP0 capacitor, 50V 5%	Vishay Vitramon	VJ1206A470JXAMT
1	22pF	*C11*	1206 C0G/NP0 capacitor, 100V 5%	Vishay Vitramon	VJ1206A220JXBMT
1	100pF	*Cpr*	1206 C0G/NP0 capacitor, 50V 5%	Vishay Vitramon	VJ1206A101JXAMT
2	22nF	*CBA, CBB*	0805 X8R capacitor, 50V 10%	Kemet	C0805C223K5HACTU
1	Diode	*DHV2*	SMB Fast recovery diode, 1200V	STMicroelectronics	STTH112U
2	Diode	*D2, D3*	SOD-80C High speed diode	NXP	BAS32L

Connector Description

Pin #	Pin Name	Pin type	Pin Description
1	ND	Input/Output	Drain of the FET
3	FAULT_DESAT	Output	DESAT fault output signal; open drain output with pull-up on the board; signal referenced between VSS and VCC5P
4	FAULT_UVL1	Output	UVLO fault output signal; open drain output with pull-up on the board; signal referenced between VSS and VDD
5	FAULT_UVL2	Output	UVLO fault output signal; open drain output with pull-up on the board; signal referenced between VSS and VCC5P
6	CLR_FAULT	Input	Clear Fault input; signal to be referenced between VSS and VCC5P
7	IN	Input	PWM input; signal to be referenced between VSS and VCC5
8	VCCLDO	Input power supply	Positive power supply of the THEMIS LDO
9	NG	Output	Gate of the FET
10	VDD2	Input power supply	Positive power supply feeding the DESAT circuit
11	VDD	Input power supply	Positive power supply feeding THEMIS and ATLAS
12	NS	Input/Output	Source of the FET
13	VSS	Input power supply	Negative power supply feeding THEMIS and ATLAS
14	VCC5P	Output power supply	5V (referenced to VSS) output power supply (e.g. to feed CHT-RHEA); max output current: 20 mA
15	VSS	Input power supply	Negative power supply feeding THEMIS and ATLAS
16	NS	Input/Output	Source of the FET

EVK-THEMIS-ATLAS: Absolute Maximum Ratings

Stressing the EVK above these absolute maximum ratings could present permanent damage. Exposure to this maximum rating for extended periods may affect the EVK reliability. These ratings are considered individually (not in combination). If not specified, voltages are related to VSS.

Parameter	Min.	Max.	Units
(VDD-VSS), (VDD2-VSS)	-0.5	30	V
(VCCLDO-VSS)	-0.5	+30	V
Steady Operating Temperature	-55	175	°C

Electrical Characteristics

Unless otherwise stated: T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T_j < +175°C).

Parameter	Condition	Min	Typ	Max	Units
External Power Supply					
External Power Supplies VDD versus VSS VCCLDO versus VSS	EVK is functional (not in under-voltage-lockout)	18		30	V
External Power Supply VCCLDO versus VSS	If the LDO of Themis is supplied through terminal VCCLDO (jumper JP2 closed, JP1 open) In the default configuration of the EVK, this option is not used and terminal VCCLDO is not connected.	7		30	V
External power supply VSS versus NS	Negative supply voltage with respect to the source of the SiC FET. Applicable to MOSFET configuration. Above this value, De-saturation circuit might not work anymore			-2.7	V
VCC quiescent current	Static input signal (IN), LDO supplied by terminal VCC (VCCLDO option not in use)			**2.5**	mA
VCC5P Power Supply					
5V Power Supply (VCC5P) versus VSS	(VCC-VSS) or (VCCLDO-VSS) from 7V to 30V, Iout from 0.25mA to 20mA	**4.75**	5	**5.25**	V
Output Current		**0.25**		**20**	mA
Initial Accuracy	(VCC-VSS)) or (VCCLDO-VSS) = 15V; Iout=2.5mA	-2		+2	%
Drift with temperature	(VCC-VSS)) or (VCCLDO-VSS) = 15V; Iout=2.5mA		0.5		mV/°C
Line Regulation	(VCC-VSS)) or (VCCLDO-VSS) from 7V to 30V; Iout=2.5mA		+/-1		mV/V
Load Regulation	(VCC-VSS)) or (VCCLDO-VSS) = 15V; Iout from 2.5mA to 20mA		0.01		V/mA
Under-voltage Lockout (UVLO)					
Internal UVLO comparator threshold voltage		**2.375**	2.5	**2.625**	V
UVLO upper threshold	Supply voltage (VCC-VSS) above which the undervoltage-lockout is released at power-up	**16.75**	18	**19.25**	V
UVLO lower threshold	Supply voltage (VCC-VSS) below which the undervoltage-lockout is activated at power-down.	**15.75**	17	**18.25**	V
UVLO Hysteresis		**0.98**	1	**1.02**	V
Open-drain transistor ON-Resistance	Note: transistor drain is HYST_UVLO pin		1K		Ω
Delay from UVLO_ENABLE to FAULT_UVLO	500mV overdrive[1]		100		ns
Delay from UVLO_ENABLE	CLoad=0.5nF		100		ns

[1] This delay is obtained for a step from 2V to 3V with a rise time of 10ns at node UVLO_ENABLE. It corresponds to a step from 14.4V to 21.6V at terminal VCC with respect to VSS

Parameter	Condition	Min	Typ	Max	Units
to driver outputs (OUTA and OUTB) when VCC goes low					
Input signal (IN, CLR_FAULT)					
Input start threshold	Wrt to VSS	3.03	3.43	3.83	V
Input stop threshold	Wrt to VSS	1.1	1.39	1.68	V
Hysteresis		1.68	2.04	2.39	V
Active Miller Clamping (AMC) Pre-driver					
AMC delay t_{amc}	C_{mc}=47pF[2], 5%	**250**	313	**380**	ns
FAULT/DESAT comparator					
Desat threshold at the anode of the desat diode DHV2		**5.6**	6.6	**7.6**	V
Desat threshold at the drain (ND) of SiC power device	Supposing 0.6V nominal forward drop across desat diode (STTH112)		6		V
Delay from ND to FAULT_DESAT output	500mV overdrive[3]		100		ns
Blanking time t_{blank}	C_{BLANK}=47pF[4]	**550**	626	**700**	ns
Delay t_{AL_Desat} between FAULT_DESAT pulled down and OUTA forced to ZERO	In case of DESAT Fault event	100	200	300	ns
FAULT Outputs (FAULT_UVLO, FAULT_DESAT)					
Open-drain transistor ON-Resistance		40	60	**120**	Ω
Drivers					
Sink current capability (at node NG)		**4**			A
Source current capability (at node NG)		**4**			A
High state output resistance				**6**	Ω
Low state output resistance				**6**	Ω
Propagation delay when output rising (IN→NG)	Driving MOSFET CMF20120D (see test circuit, 450V, 5A) (VDD-VSS)=25V (50%→ 50%)		70		ns
Propagation delay when output falling (IN→NG)	Driving MOSFET CMF20120D (see test circuit, 450V, 5A) (VDD-VSS)=25V (50%→ 50%)		70		ns
Rise Time (10%-90%)	Driving MOSFET CMF20120D (see test circuit, 450V, 5A) (VDD-VSS)=25V		80		ns
Fall Time (10%-90%)	Driving MOSFET CMF20120D (see test circuit, 450V, 5A) (VDD-VSS)=25V		80		ns

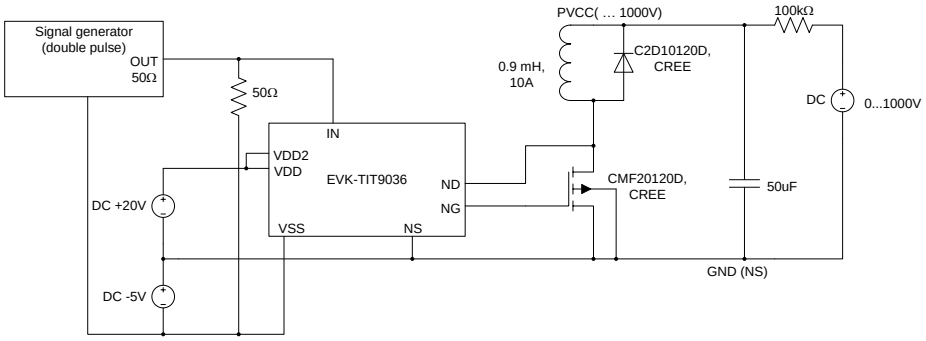
[2] This assumes an external Ceramic COG capacitor with a 50ppm/°C temperature coefficient

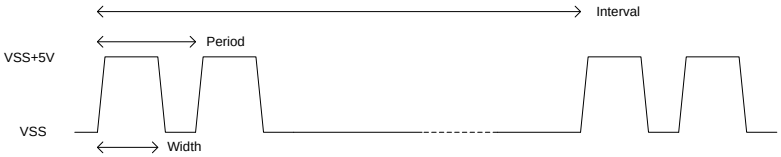
[3] This delay is obtained for a step from 4.9V to 5.9V with a rise time of 10ns at node ND, the effective threshold being 5.4V

[4] This assumes an external Ceramic COG capacitor with a 50ppm/°C temperature coefficient

Typical Characteristics

Description test circuit





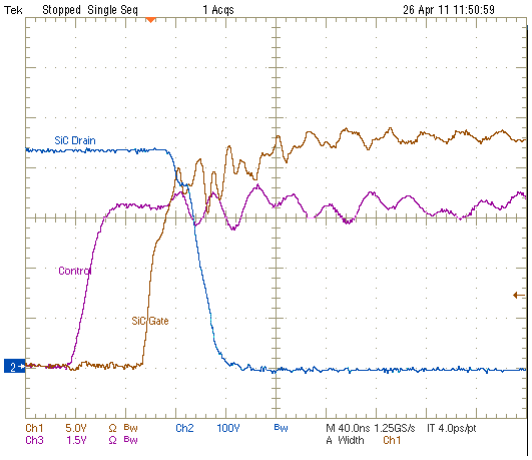


Figure 1: Turn-on of SiC MOSFET CMF20120D at 5A, 450V (Ta= 25°C)

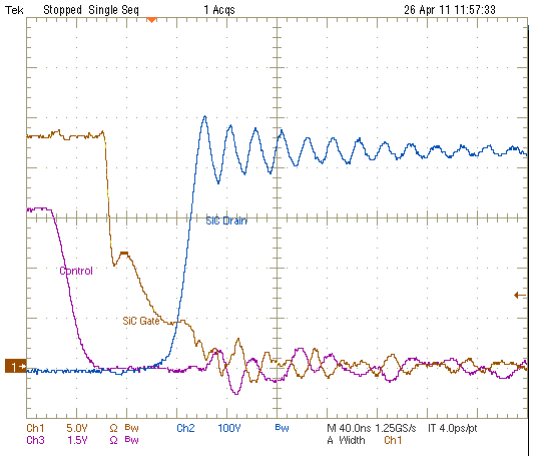


Figure 2: Turn-off of SiC MOSFET CMF20120D at 5A, 450V (Ta= 25°C)

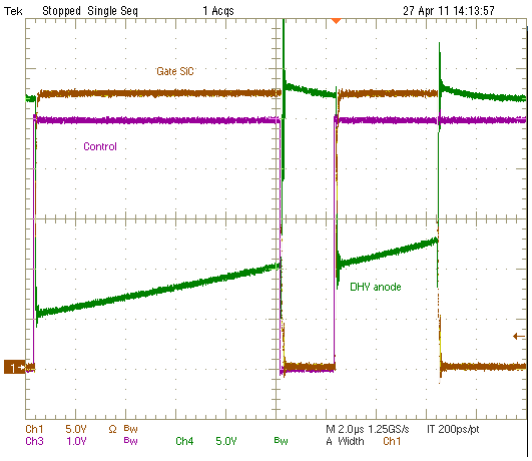


Figure 3: Illustration of a de-saturation fault. 0.5 Ohm is inserted in the drain connection of the MOSFET. As current builds up in the MOSFET, the drain-source voltage increases from 0 to 5V during the first pulse (green line measured at the anode of the desat diode). In the middle of the 2nd pulse, the drain voltage measured after the diode has reached the desat threshold (about 7V) and the MOSFET is turned off while the input control signal is still active (purple line).

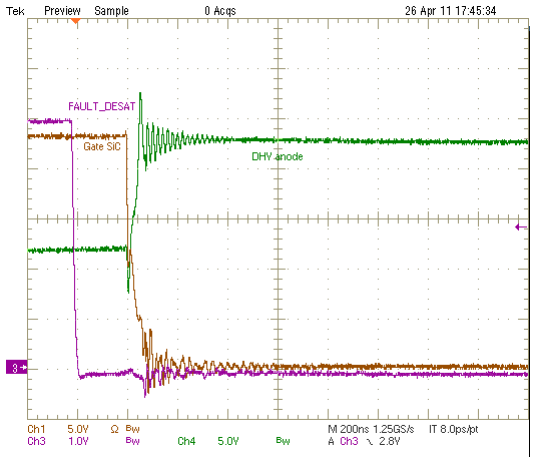


Figure 4: The gate driver is pulled low about 200ns after the de-saturation fault has been asserted.

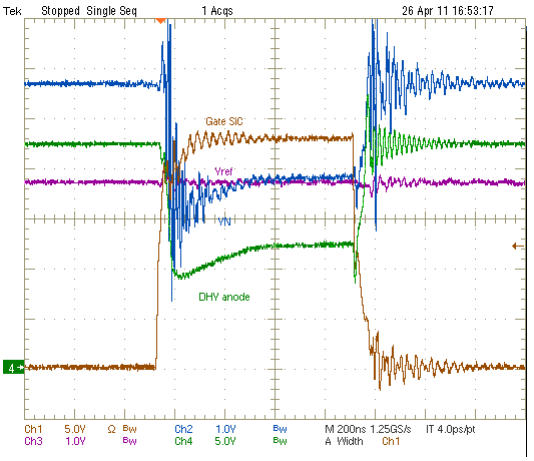


Figure 5: The MOSFET is turned on at high current in the coil, directly causing a de-saturation fault. The delay between turn-on and turn-off by de-saturation detection is about 800ns (600ns blanking time + 200 ns delay).

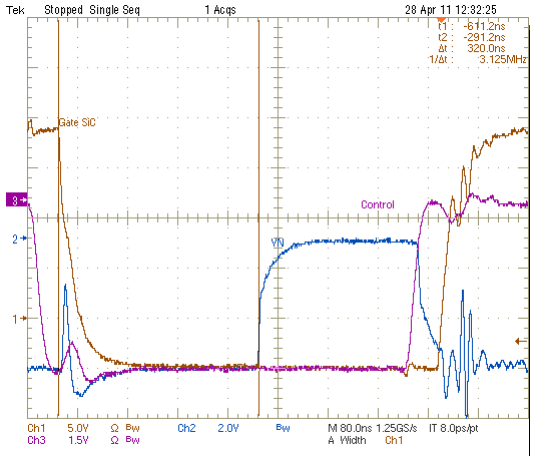


Figure 6: AMC behaviour: the gate of the AMC NMOS is pulled high 320ns after the gate driver has pulled the gate low

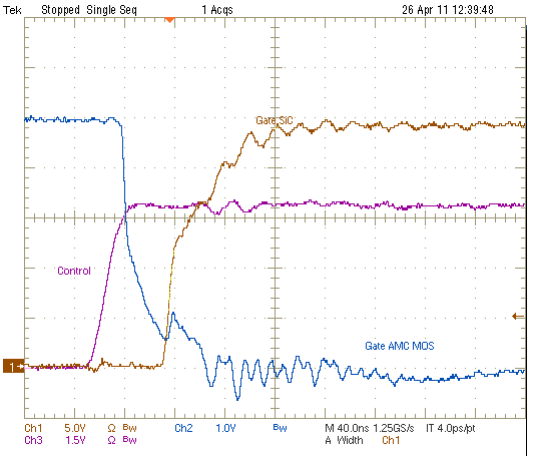


Figure 7: AMC behaviour: the AMC NMOS is turned off before the driver pulls the SiC gate up.

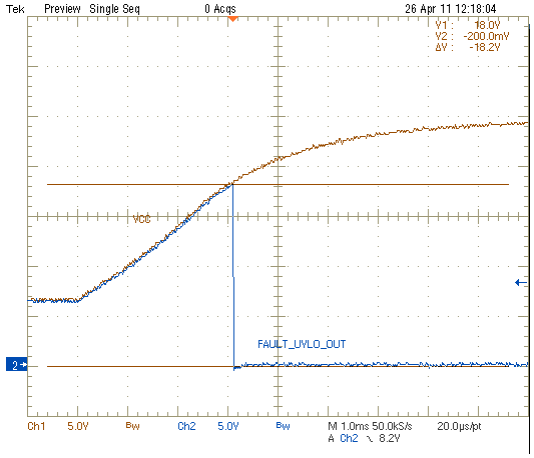


Figure 8: Under Voltage detection

General description

Power Supply configuration

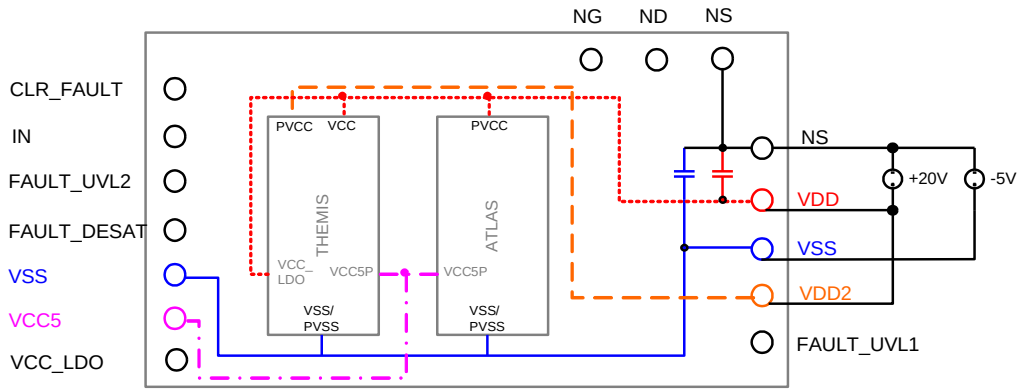


Figure 9: Power supply configuration for driving a SiC MOSFET.

The voltages VDD (+20V) and VSS (-5V) are set as per the datasheet of the CREE CMF20120D MOSFET. To have the de-saturation function working properly, the negative voltage VSS should be lower than -2.7V.

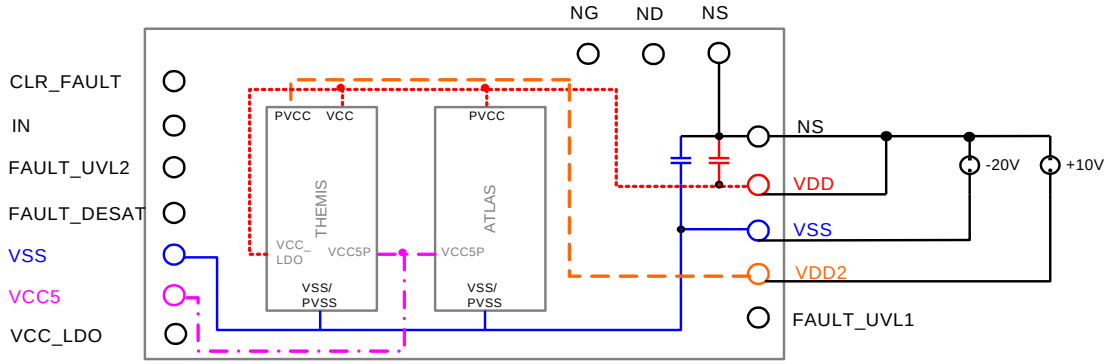


Figure 10: Power supply configuration for driving a normally-off JFET. A positive supply is needed at terminal VDD2 for sensing de-saturation. The evaluation board itself is identical for SiC MOSFET and normally-ON JFET.

The voltage VSS (-20V) is set as per the recommendation of the JFET Normally-On manufacturer (Infineon); it should be set between the threshold and the pinch-off voltage of the JFET. The voltage VDD2 (+10V) is feeding the de-saturation function; it should be set higher than the de-saturation threshold (7V on this Evaluation Board).

Under Voltage Lockout configuration

V_{UHV} : the device operates as soon as the supply voltage (*VCC-VSS*) exceeds that threshold value.

V_{UVL}: the device stops operating when the supply voltage (*VCC-VSS*) drops below that threshold value.

The difference between those two thresholds defines the hysteresis.

$$V_{UVL} = \frac{RUL1 + RUL2}{RUL2}\left(Vref - VSS\right) = \frac{RUL1 + RUL2}{RUL2}\,2.5 \pm 5\%$$

$$V_{UVH} = \frac{RUL1 + RUL2 \,//\, RULH}{RUL2 \,//\, RULH}\left(Vref - VSS\right) = \frac{RUL1 + RUL2 \,//\, RULH}{RUL2 \,//\, RULH}\,2.5 \pm 5\%$$

Choosing *RUL2 and the 2 thresholds*, *RUL1 and RULH* are calculated by:

$$RUL1 = RUL2\,\frac{\left(V_{UVL} - 2.5\right)}{2.5}$$

$$RULH = \frac{2.5\,RUL1 \;\; RUL2}{RUL2\;V_{UVH} - 2.5\left(RUL1 + RUL2\right)}$$

V_{UVH} = 18V
V_{UVL} = 17V

RUL2=20kΩ
RUL1=116kΩ
RULH = 290kΩ

Active Miller Clamp configuration

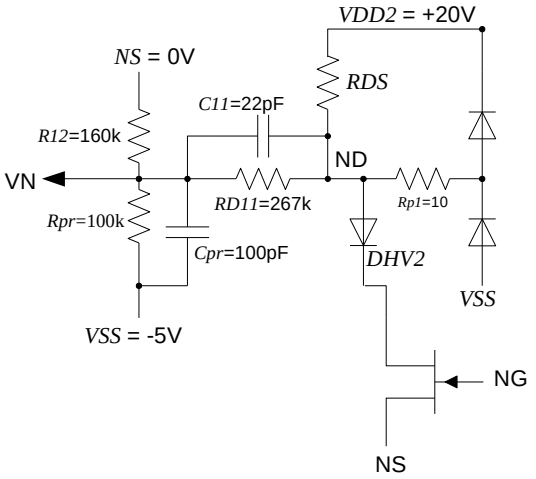
At turn-off of the the SiC device, the Active Miller Clamp NMOS (CHT-MOON) is activated after some delay defined by capacitor *Cmc*.

$$t_{AMC} = 6666\ Cmc$$

With *Cmc*=47pF, the AMC delay is 313ns.

Desat Theshold configuration

Desat detection threshold



When the SiC device is conducting, a current for sensing de-saturation flows from *VDD2* through the SiC device channel via resistor *RDS*.
With *VDD2*=*VDD*=20V and *RDS*=10k, the de-saturation sensing current is *VDD*/*RDS* and power dissipation is VDD^2/RDS = 40mW.
In order to make the de-saturation threshold V(ND) independent from the supply voltage, Rpr, *RD11* and *RD12* must be linked by the relationship $Rpr = RD11 // RD12$.
Choosing the drain de-saturation threshold voltage (sensed after the de-saturation diode DHV2) *V(ND)* = 6.6V and *Rpr* = 100kΩ, component *RD11* and *RD12* can be dimensioned by the following rules

$$RD11 = \frac{Rpr\ RD12}{RD12 - Rpr}$$

$$RD12 = \frac{Rpr\ \left(V(NS) - V(ND)\right)}{2Vref\ - V(VSS) - V(ND)} \text{ with } Vref\ = \frac{V(ND) + V(VSS)}{2} + Iref\ Rref \text{ and } Iref\ Rref \approx 1.25V$$

$$RD12 = \frac{Rpr\ \left(V(ND) - V(NS)\right)}{V(ND) - V(NS) - 2\,Iref\ Rref} = 160\ \text{kΩ}$$

$$RD11 = Rpr\ \frac{\left(V(ND) - V(NS)\right)}{2\,Iref\ Rref} = 267\ \text{kΩ}$$

Because of the independence from the supply voltage, the de-saturation threshold remains unchanged as long as *VSS* is less than -2.7V.

Capacitors *Cpr* and *C*11 have been placed across resistors *Rpr* and *RD*11 in order to form a perfect voltage divider from ND to VN.

$$RD11 \cdot C11 = (Rpr\ //\ RD12) \cdot Cpr$$

At large dV/dT, it is possible that the voltage at node ND drops below the actual drain voltage. The recovery is achieved through resistance *RDS* which could be made smaller in order to speed it up (at the expense of larger power dissipation).

Desat detection delay

Capacitor Cbl defines the so-called blanking time which is the delay allowing for settling of the voltage at the drain of the SiC device before actually detecting de-saturation at turn-on:

$$t_{BLANK} = 13333\ CBL$$

With CBL = 47pF, the blanking time is 626ns.

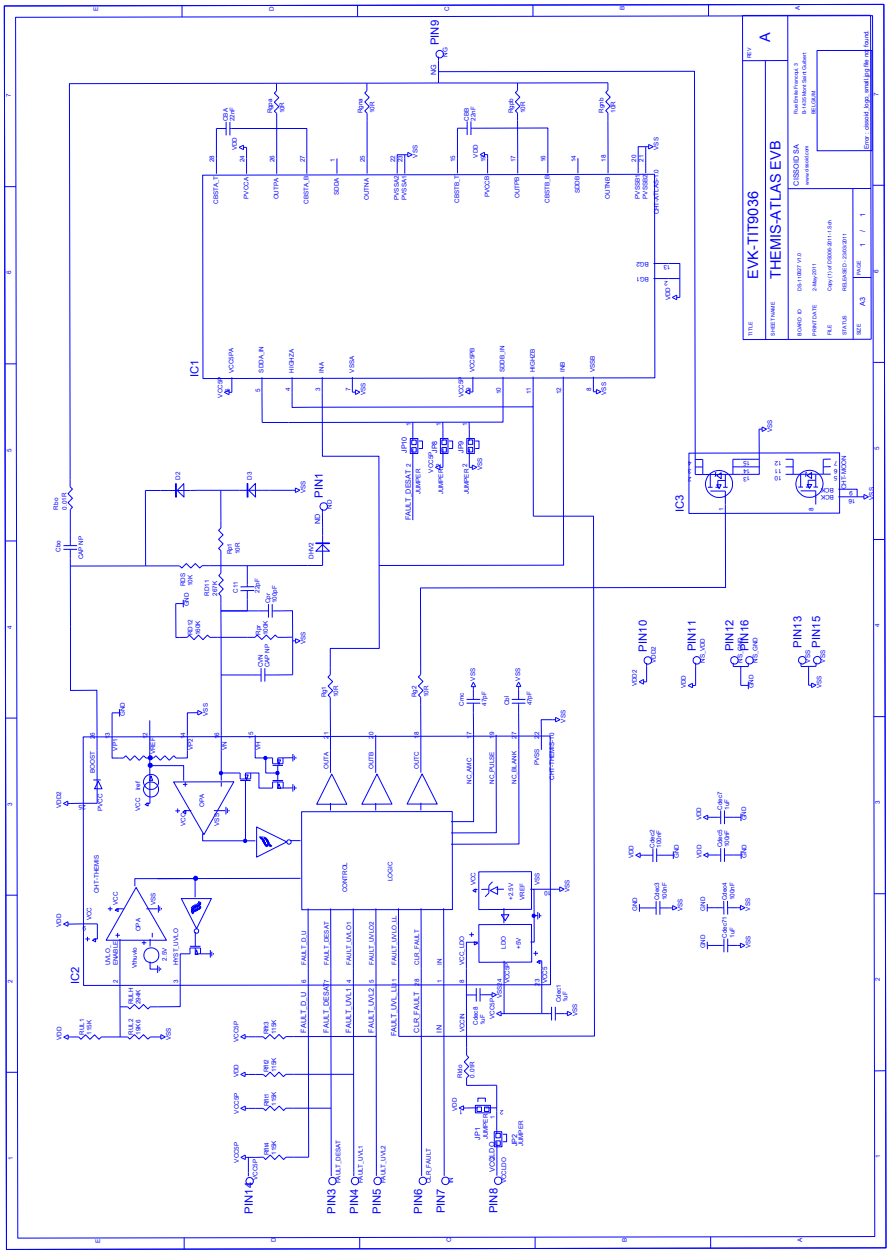
Support of Normally-On JFET

By default, the board configuration is configured to support SiC MOSFET.
With the same configuration, it supports normally-on JFET; only the external supply system must be changed (VSS, VDD, VDD2). In this case, a specific power supply (VDD2) is used to feed the de-saturation circuit.

To support Normally-On JFET and to have the de-saturation circuit being fed by a bootstrap configuration (cfr CHT-THEMIS datasheet for more details) (the positive supply VDD2 not being needed in this case), following items should be changed on the board:

- Resistor Rshort1 is removed
- Rbo = 0.01 ohm is added
- Cbo = 100nF is added

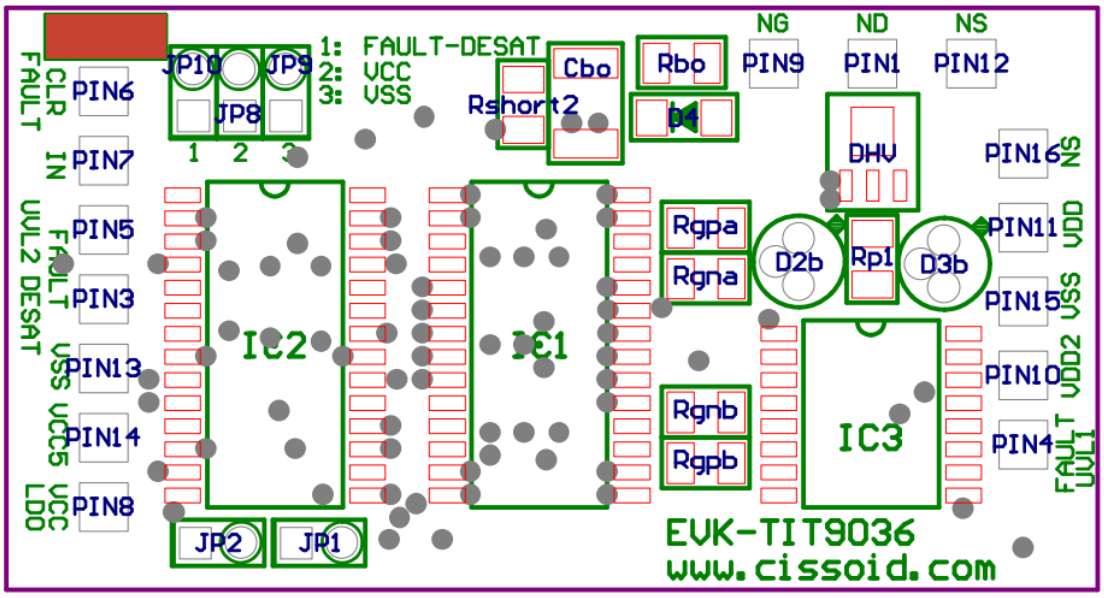
Schematic below illustrates the required changes for this configuration.
Please note that this configuration is still under validation.



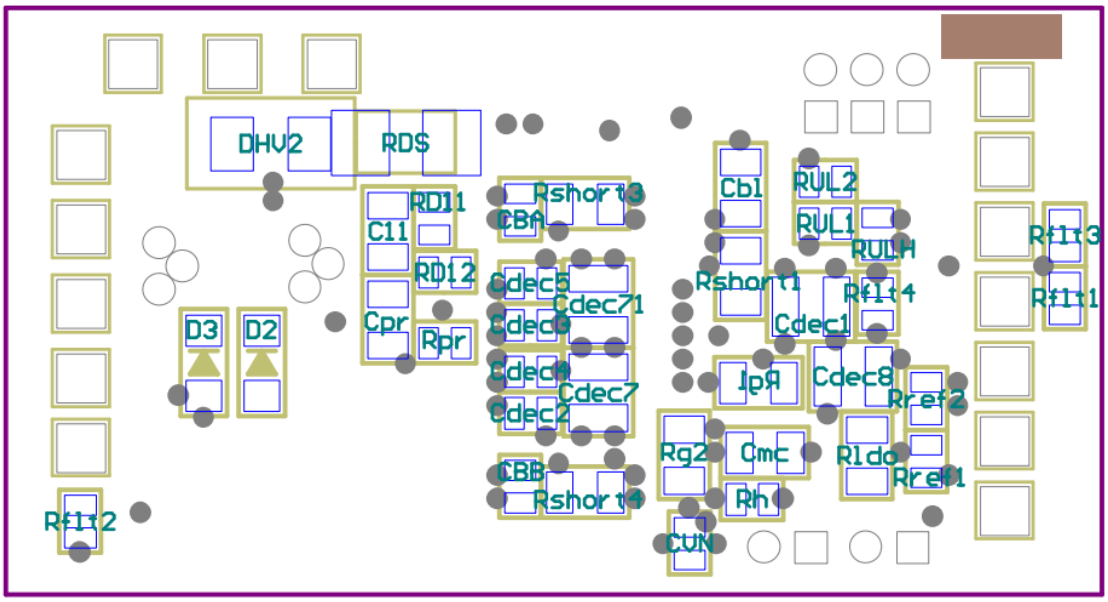
PCB layout

Physical dimensions: 60 mm * 32 mm

Top side



Bottom side



Ordering Information

Product Name	Ordering Reference	Package	Marking
EVK-THEMIS-ATLAS	EVK-TIT9036A	Ceramic	EVK-TIT9036

Contact & Ordering

CISSOID S.A.

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