Downconverters - Packaged

EWD1509YF

May 2010 - Rev 1

Preliminary

Features

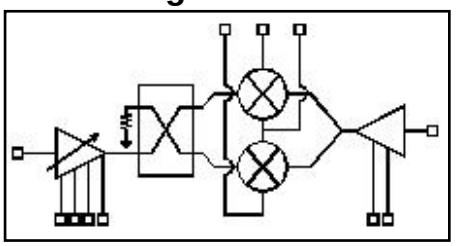
- Extremely high integration
- Includes converter, LO doubler, RF VGA
- Noise figure: 2.5 dB, nominal
- Conversion gain: +15 dB, typical
- Input IP3: +4 dBm, typical
- Image rejection: 15 dB, typical
- Low power consumption : +4.5V @ 220 mA
- HBM Class 1A - ESD Protection Bias Circuitry
- Package: 5 x 5 mm, 32 lead, plastic overmold QFN
- RoHS compliant
- 100% DC and RF tested

Device Photo

Description

The Endwave *EWD1509YF* is an extremely highly integrated MMIC down-converter that includes LO amplification, as well as RF gain adjustability via a unique voltage variable attenuator. The device provides 15 dB of nominal conversion gain with 15 dB of RF gain adjustability, while maintaining +4 dBm input third order intercept over all conditions with 0 dBm of LO input power. This device has integrated ESD protection bias circuitry and can be used for a wide range of applications from defense electronics to commercial communication systems. All parts are 100% DC and RF tested and visually inspected to IPC-A-610.

Block Diagram



Electrical Characteristics (Temperature = +25°C)

Parameter	Min.	Typ.	Max.	Units
Frequency Range, IF	DC		4	GHz
Frequency Range, RF	10		15.4	GHz
Frequency Range, LO	6		19.4	GHz
Conversion Gain (nominal)	10	15		dB
Dynamic Range (Vgc1,2 + 0 vs. -1.5V)		15		dB
Image Rejection		15		dBc
LO Drive Power		0		dBc
Input 3rd-Order Intercept (all gain settings)	+2	+4		dBm
Noise Figure (at maximum gain)		2.5	3	dB
Noise Figure (at minimum gain)			15	dB
IF Return Loss		10		dB
LO Return Loss		10		dB
RF Return Loss		10		dB
Drain Bias Voltages (Vd1, Vd2, Vd3)		+4.5		V
Drain Bias Currents (Id1+Id2+Id3)		220		mA
Gate Bias Voltage (Vg3)		-1.1		V
Gate Bias Voltage (Vg4)		-0.6		V
Gate Control Voltage (Vgc1,2)	-1.5		0	V

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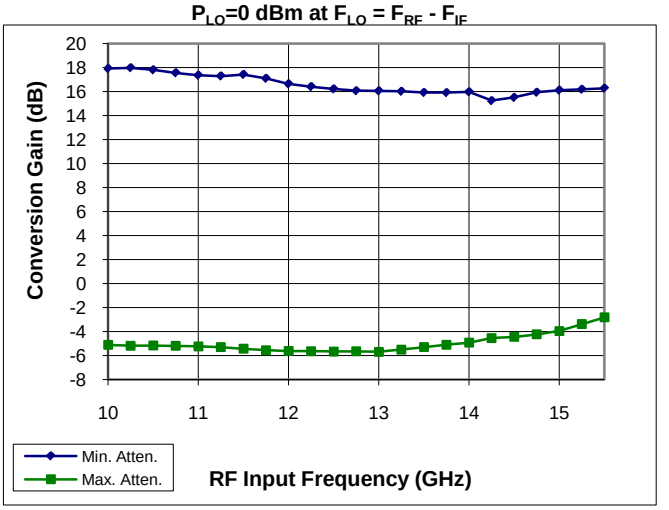
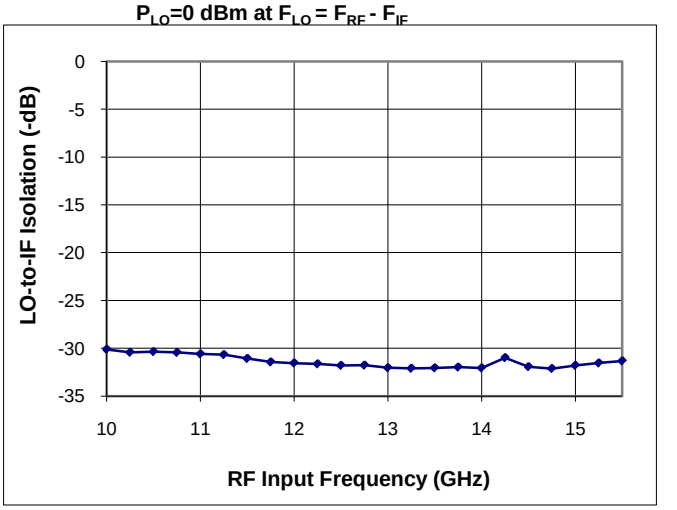
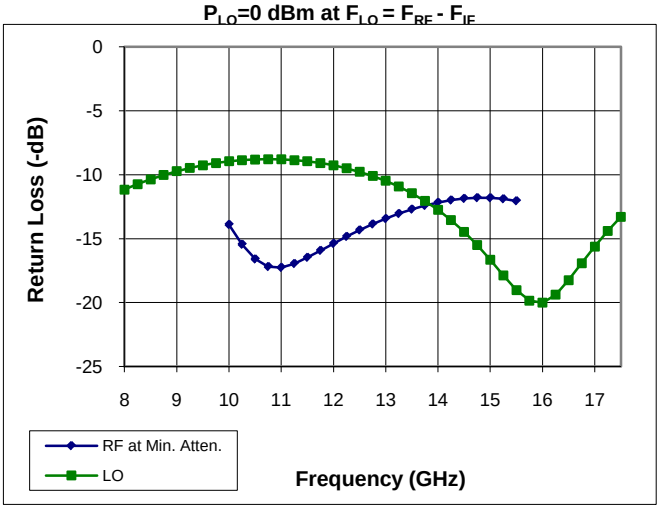
Conversion Gain
VG3=-1.2V, IF=2 GHz from external 90-degree hybrid,
P_{LO}=0 dBm at $F_{LO} = F_{RF} - F_{IF}$



LO-to-IF Isolation
VG3=-1.2V, IF=2GHz from external 90-degree hybrid,
P_{LO}=0 dBm at $F_{LO} = F_{RF} - F_{IF}$



Return Losses
VG3=-1.2V, IF connected to external 90-degree hybrid,
P_{LO}=0 dBm at $F_{LO} = F_{RF} - F_{IF}$



Conversion Gain Dynamic Range
VG3=-1.2V, IF=2GHz from external 90-degree hybrid,
P_{LO}=0 dBm at $F_{LO} = F_{RF} - F_{IF} - F_{IF}$

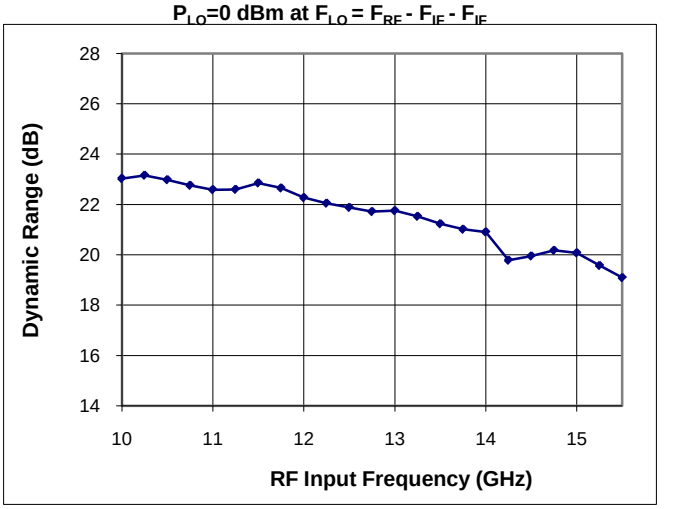
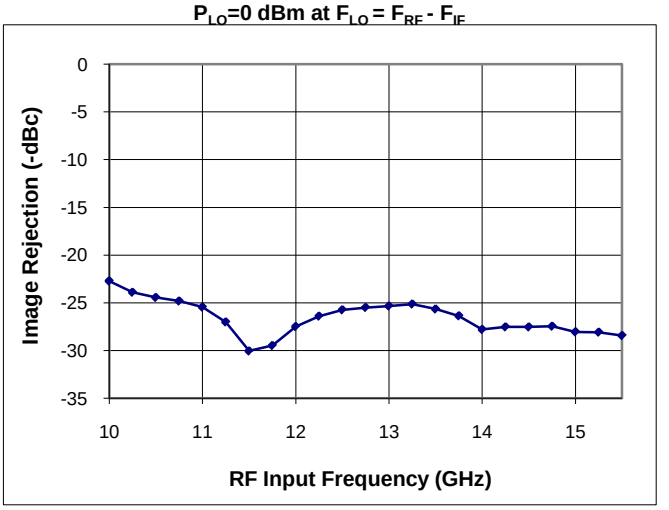
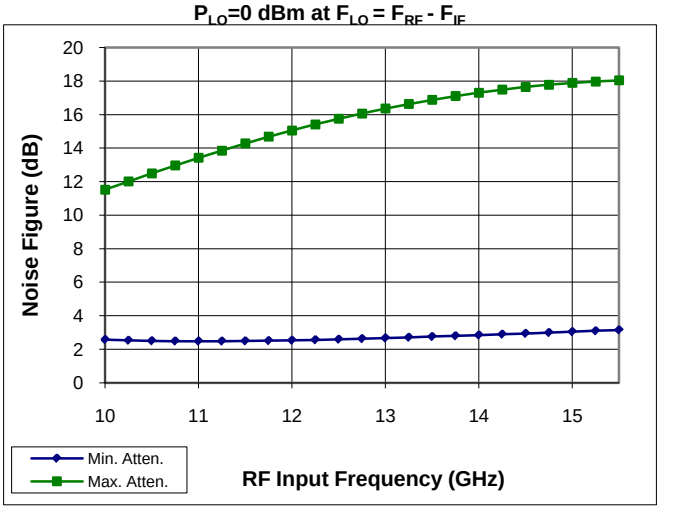


Image Rejection
VG3=-1.2V, IF=2GHz from external 90-degree hybrid,
P_{LO}=0 dBm at $F_{LO} = F_{RF} - F_{IF}$



Noise Figure
VG3=-1.2V, IF=2GHz from external 90-degree hybrid,
P_{LO}=0 dBm at $F_{LO} = F_{RF} - F_{IF}$



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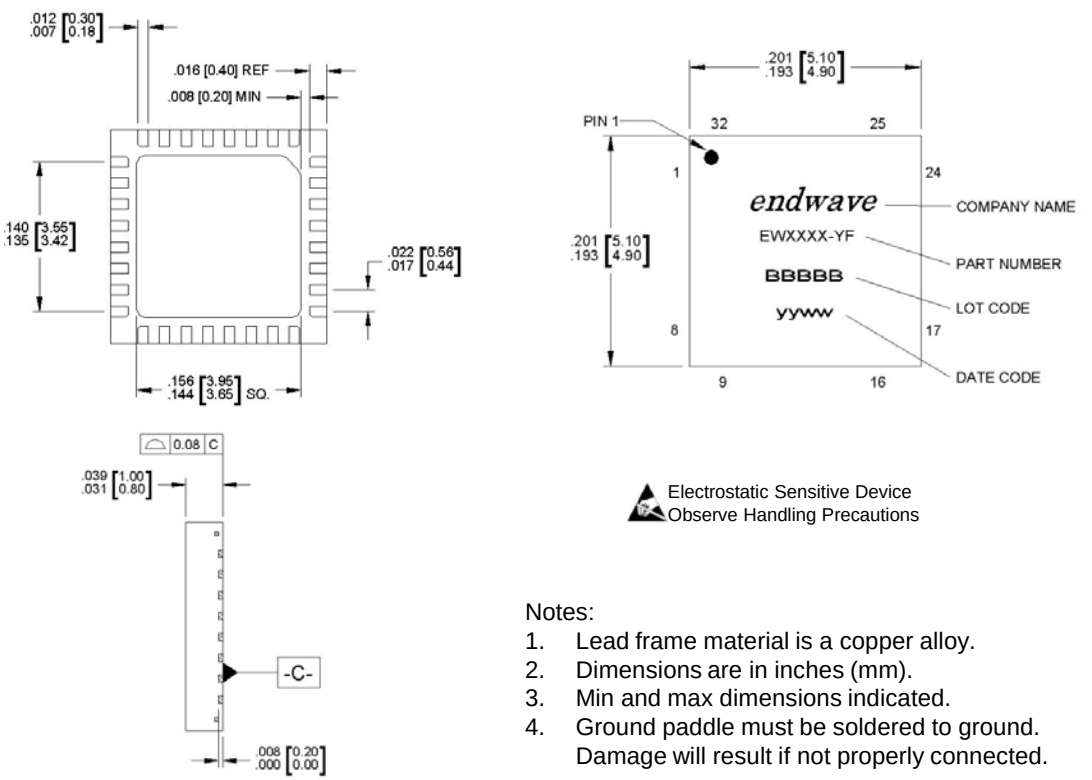
DC & RF Pinout

Pin Number	Function
1-5, 15, 16, 20, 21, 23, 24, 30, 31, 32	No Connection
6, 8, 17, 19, 25, 27, 29	Ground
7	RF Input
9	V_{GC1}
10	V_{GC2}
11	V_{G4} (Note 2)
12	V_{D3} (Note 2)
13	V_{D2} (Note 2)
14	V_{D1} (Note 2)
18	LO Input
22	V_{G3} (mixer bias)
26	IF Output2 (Note 1)
28	IF Output1 (Note 1)

Note 1: Combine IF outputs via external 90-degree hybrid to create image rejection.
Note 2: Place 100pF bypass chip capacitor as close as possible to the pin.

Outline Drawings

"F" Package – 5 x 5mm, 32 lead

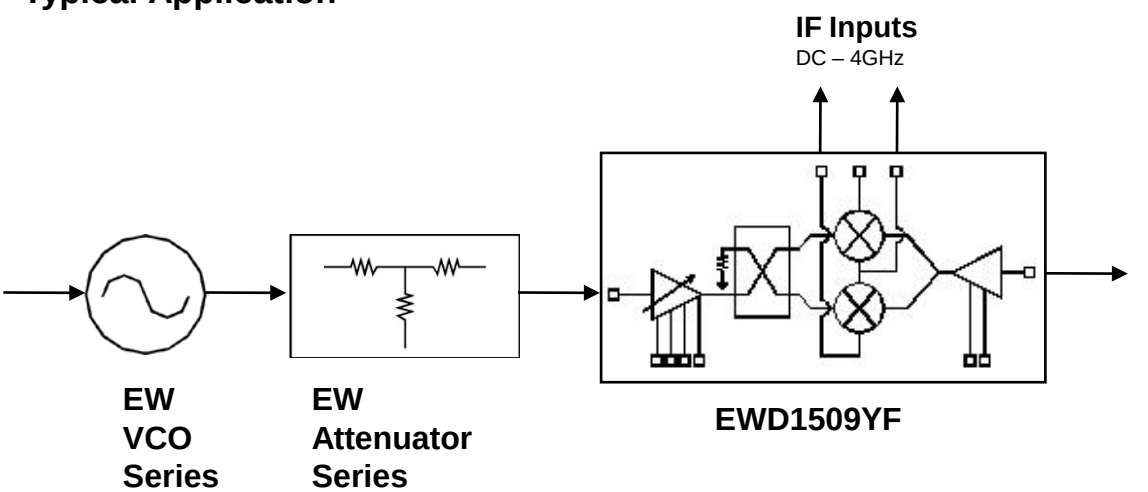


Notes:
1. Lead frame material is a copper alloy.
2. Dimensions are in inches (mm).
3. Min and max dimensions indicated.
4. Ground paddle must be soldered to ground. Damage will result if not properly connected.

Absolute Maximum Ratings

RF Input Power	+10 dBm
LO Input Power	+15 dBm
Supply Voltage (Vd_{total})	+5.5 V
Supply Current (Id_{total})	700 mA
Storage Temperature	-65 to +150 C
Operating Temperature	-40 to +85 C
Channel Temperature	175 C

Typical Application



Support Documentation

Support documentation including Assembly Notes, Application Notes and Qualification Procedures can be found on our website at www.endwave.com.

Ordering Information

Part Number	Description
EWD1509YF	RoHS compliant bare die in waffle or gel packs
EWD1509YF-EV	*EWD1509YF* in a Connectorized Test Fixture