FAIRCHILD

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FAN5909
Multi-Mode Buck Converter with LDO Assist for GSM / EDGE, 3 G/3.5 G and 4 G PAs

Features

- Solution Size < 9.52 mm^2
- 2.7 V to 5.5 V Input Voltage Range
- V_{OUT} Range from 0.40 V to 3.60 V (or V_{IN})
- Single, Small Form-Factor Inductor
- 29 mΩ Integrated LDO
- 100% Duty Cycle for Low-Dropout Operation
- Input Under-Voltage Lockout / Thermal Shutdown
- 1.61 mm x 1.61 mm, 16-Bump, 0.4 mm Pitch WLCSP
- 2.9 MHz PWM Mode
- 6 µs Output Voltage Step Response for early Tx Power-Loop Settling with 14 µF Load Capacitance
- Sleep Mode for ~50 µA Standby Current Consumption
- **Forced PWM Mode**
  - Up to 95% Efficient Synchronous Operation in High Power Conditions
  - 2.9 MHz PWM-Only Mode
- **Auto PFM/PWM Mode**
  - 2.9 MHz PWM Operation at High Power and PFM Operation at Low Power and Low Output Voltage for Maximum Low Current Efficiency

Applications

- Dynamic Supply Bias for Polar or Linear GSM / EDGE PAs and 3 G/3.5 G and 4 G PAs
- Dynamic Supply Bias for GSM / EDGE Quad Band Amplifiers for Mobile Handsets and Data Cards

Description

The FAN5909 is a high-efficiency, low-noise, synchronous, step-down, DC-DC converter optimized for powering Radio Frequency (RF) Power Amplifiers (PAs) in handsets and other mobile applications. Load currents up to 2.5 A are allowed, which enables GSM / EDGE, 3 G/3.5 G, and 4G platforms under very poor VSWR conditions.

The output voltage may be dynamically adjusted from 0.40 V to 3.60 V, proportional to an analog input voltage V_{CON} ranging from 0.16 V to 1.44 V, optimizing power-added efficiency. Fast transition times of less than 6 µs are achieved, allowing excellent inter-slot settling.

An integrated LDO is automatically enabled under heavy load conditions or when the battery voltage and voltage drop across the DC-DC PMOS device are within a set range of the desired output voltage. This LDO-assist feature supports heavy load currents under the most stringent battery and V_{SWR} conditions while maintaining high efficiency, low dropout, and superior spectral performance.

The FAN5909 DC-DC operates in PWM Mode with a 2.9 MHz switching frequency and supports a single, small form-factor inductor ranging from 1.0 µH to 2.2 µH. In addition, PFM operation is allowed at low load currents for output voltages below 1.5 V to maximize efficiency. PFM operation can be disabled by setting MODE pin to LOW.

When output regulation is not required, the FAN5909 may be placed in Sleep Mode by setting V_{CON} below 100 mV nominally. This ensures a very low I_Q (<50 µA) while enabling a fast return to output regulation.

FAN5909 is available in a low profile, small form factor, 16 bump, Wafer-Level Chip-Scale Package (WLCSP) that is 1.61 mm x 1.61 mm. Only three external components are required: two 0402 capacitors and one 2016 inductor.

Ordering Information

Part Number	Output Voltage	Temperature Range	Package	Packing
FAN5909UCX	0.4 V to PVIN	-40°C to +85°C	1.61 mm x 1.61 mm, 16-Bump 0.4 mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)	Tape and Reel

Block Diagrams

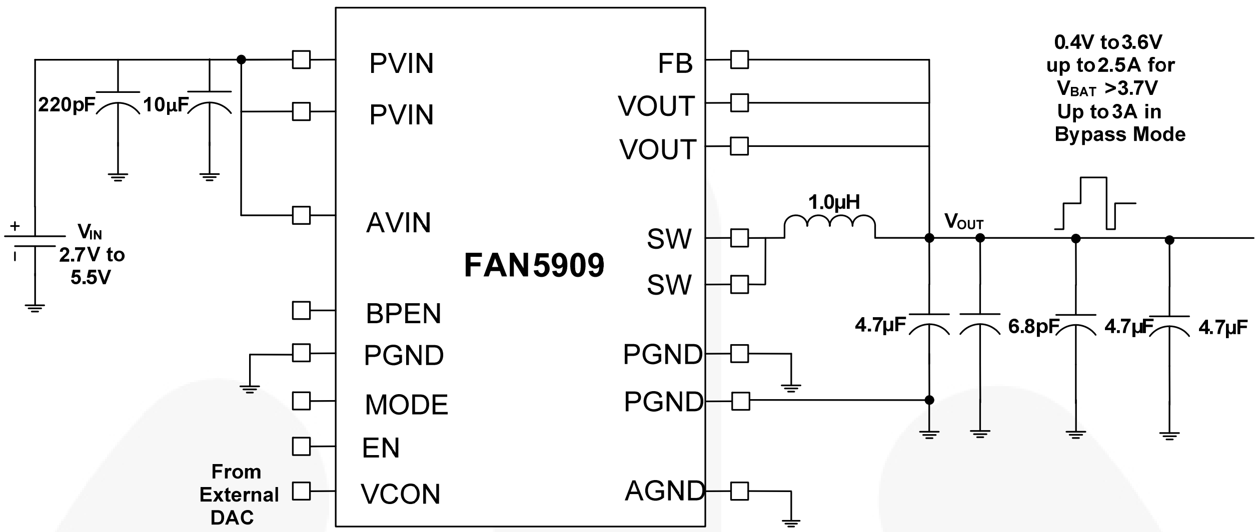


Figure 1. Typical Application

Notes:
1. The three 4.7 µF capacitors include the FAN5909 output capacitor and PA bypass capacitors.
2. Regulator requires only one 4.7 µF; the V_{OUT} bus should not exceed 14 µF capacitance over DC bias and temperature.

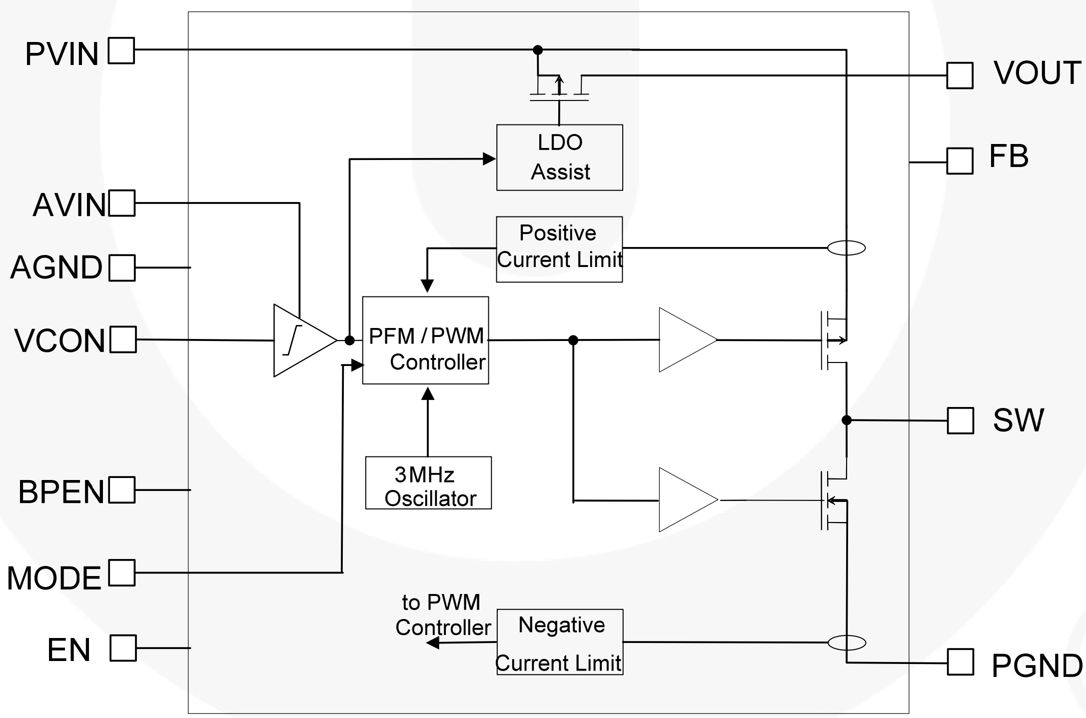


Figure 2. Simplified Block Diagram

Pin Configuration

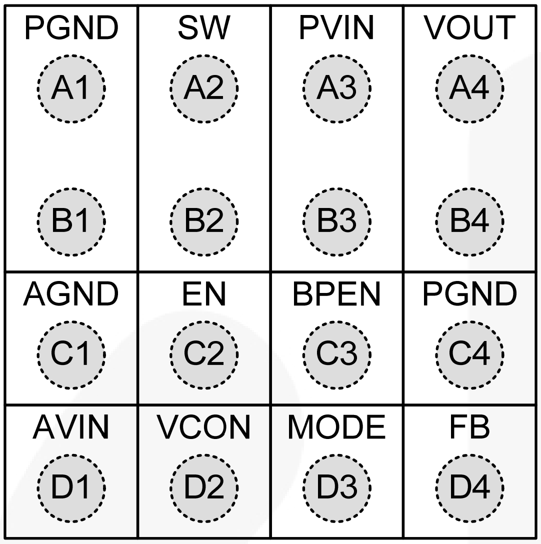


Figure 3. Bumps Face Down – Top-Through View

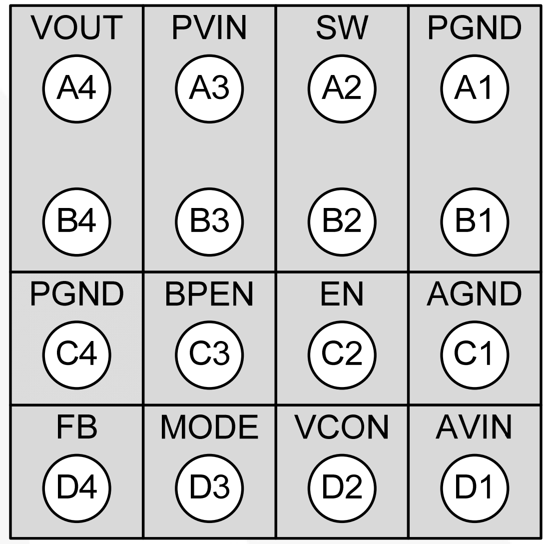


Figure 4. Bumps Face Up

Pin Definitions

Pin #	Name	Description
C1	AGND	Analog ground, reference ground for the IC. Follow PCB routing notes for connecting this pin.
A4, B4	VOUT	Output voltage sense pin. Connect to V_{OUT} to establish feedback path for regulation point. Connect together on PCB.
D4	FB	Feedback pin. Connect to positive (+) pad of C_{OUT} on V_{OUT}.
C2	EN	Enables switching when HIGH; Shutdown Mode when LOW. This pin should not be left floating.
D2	VCON	Analog control pin. Shield signal routing against noise.
D1	AVIN	Analog supply voltage input. Connect to PVIN.
C3	BPEN	Force Bypass Mode when HIGH; Auto Bypass Mode when LOW. This pin should not be left floating.
D3	MODE	When MODE is HIGH, the DC-DC permits PFM operation under low load currents and PWM operation under heavy load currents. When MODE pin is set LOW, the DC-DC operates in forced PWM operation. This pin should not be left floating.
A3, B3	PVIN	Supply voltage input to the internal MOSFET switches. Connect to input power source.
A2, B2	SW	Switching node of the internal MOSFET switches. Connect to output inductor.
A1, B1,C4	PGND	Power ground of the internal MOSFET switches. Follow routing notes for connections between PGND and AGND.

Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Voltage on AVIN, PVIN		-0.3	6.0	V
	Voltage on Any Other Pin		-0.3	AV_{IN} + 0.3	
T_J	Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature		-65	+150	°C
T_L	Lead Soldering Temperature (10 Seconds)			+260	°C
ESD	Electrostatic Discharge Protection Level	Human Body Model, JESD22-A114	2.0		kV
		Charged Device Model, JESD22-C101	1.0		
LU	Latch Up		JESD 78D		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Supply Voltage Range	2.7		5.5	V
V_{OUT}	Output Voltage Range	0.35		$<V_{IN}$	V
I_{OUT_BYPASS}	Output Current in Bypass Mode (100% Duty Cycle)			4.5	A
I_{OUT}	Output Current			3.0	A
L	Inductor		1		μH
C_{IN}	Input Capacitor(3)		10		μF
C_{OUT}	Output Capacitor(4)		4.7		μF
T_A	Operating Ambient Temperature Range	-40		+85	°C
T_J	Operating Junction Temperature Range	-40		+125	°C

Notes:

3. The input capacitor must be large enough to limit the input voltage drop during GSM bursts, bypass transitions, and large output voltage transitions.
4. Regulator requires only one 4.7 μF; the V_{OUT} bus should not exceed 14 μF capacitance over DC bias and temperature.

Dissipation Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
Θ_{JA}	Junction-to-Ambient Thermal Resistance(5)		40		°C/W

Note:

5. Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards with vias in accordance to JESD51- JEDEC standard. Special attention must be paid not to exceed junction temperature $T_{J(MAX)}$ at a given ambient temperature T_A.

Electrical Characteristics, All Modes

Recommended operating conditions, unless otherwise noted, circuit per Figure 1, V_{IN} = 2.7 V to 5.5 V, T_A = -40°C to +85°C. Typical values are given V_{IN} = 3.8 V at T_A = 25°C. L = 1 µH, Toko DFE201610C, C_{IN} = 10 µF 0402 TDK C1005X5R0J106MT, C_{OUT} = 3 x 4.7 µF 0402 TDK C1005X5R0J475KT.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Power Supplies						
V_{IN}	Input Voltage Range	I_{OUT} ≤ 2.5 A	2.7		5.5	V
I_{SD}	Shutdown Supply Current	EN = 0 V, MODE = 0		0.5	3.0	µA
V_{UVLO}	Under Voltage Lockout Threshold	V_{IN} Rising	2.20	2.45	2.60	V
		Hysteresis		250		mV
Logic Control						
V_{IH}	Logic Threshold Voltage; EN, BPEN, MODE	Input HIGH Threshold	1.2			V
V_{IL}		Input LOW Threshold			0.4	V
I_{CTRL}	Logic Control Input Bias Current; EN, BPEN, MODE	V_{IN} or GND		0.01	1.00	µA
Analog Control						
$V_{CON\_LDO\_EN1}$	V_{CON} Forced Bypass Enter(6)	V_{CON} Voltage that Forces Bypass; V_{IN} = 4.0 V – 4.75 V	1.6			V
$V_{CON\_LDO\_EN2}$	V_{CON} Forced Bypass Enter(6)	V_{CON} Voltage that Forces Bypass; $V_{IN} \approx V_{OUT}$		V_{IN}/2.5		V
$V_{CON\_LDO\_EX}$	V_{CON} Forced Bypass Exit	V_{CON} Voltage that Exits Forced Bypass; V_{IN} = 2.70 V – 4.75 V			1.4	V
$V_{con\_SL\_en}$	V_{con} Sleep Enter	V_{CON} Voltage Forcing Low I_Q Sleep Mode	70			mV
$V_{con\_SL\_ex}$	V_{con} Sleep Exit	V_{CON} Voltage that Exits SLEEP Mode			125	mV
I_Q	DC-DC Quiescent Current in Sleep Mode	V_{CON} < 70 mV		50	80	µA
Gain	Gain in Control Range 0.16 V to 1.44 V			2.5		
V_{OUT_ACC}	V_{OUT} Accuracy	Ideal = 2.5 x V_{CON}	-50		+50	mV
LDO						
R_{FET}	LDO FET Resistance			29		mΩ
ΔV_{OUT_LDO}	LDO Dropout(7)	I_{OUT} = 2.0 A		100		mV
Over Temperature Protection						
T_{OTP}	Over-Temperature Protection	Rising Temperature		+150		°C
		Hysteresis		+20		°C
Oscillator						
f_{SW}	Average Oscillator Frequency		2.6	2.9	3.2	MHz
DC-DC						
R_{DSON}	PMOS On Resistance	$V_{IN} = V_{GS}$ = 3.7 V		80		mΩ
	NMOS On Resistance	$V_{IN} = V_{GS}$ = 3.7 V		60		mΩ
I_{LIMp}	P-Channel Current Limit(8)		1.50	1.90	2.30	A
I_{LIMn}	N-Channel Current Limit(8)		1.50	1.90	2.30	A
$I_{Discharge}$	Maximum Transient Discharge Current			3.7	4.5	A
I_{LIMLDO}	LDO Current Limit				4.5	A
V_{OUT_MIN}	Minimum Output Voltage	V_{CON} = 0.16 V	0.35	0.40	0.45	V
V_{OUT_MAX}	Maximum Output Voltage	V_{CON} = 1.44 V, V_{IN} = 3.9 V	3.55	3.60	3.65	V

Electrical Characteristics, All Modes

Recommended operating conditions, unless otherwise noted, circuit per Figure 1, V_{IN} = 2.7 V to 5.5 V, T_A = -40°C to +85°C. Typical values are given V_{IN} = 3.8 V at T_A = 25°C. L = 1 µH, Toko DFE201610C, C_{IN} = 10 µF 0402 TDK C1005X5R0J106MT, C_{OUT} = 3 x 4.7 µF 0402 TDK C1005X5R0J475KT.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DC-DC Efficiency						
η_{Power}	Power Efficiency, Low-Power Auto Mode, V_{IN} = 3.7 V	V_{OUT} = 3.1 V, I_{LOAD} = 250 mA		95		%
		V_{OUT} = 1.8 V, I_{LOAD} = 250 mA		90		
		V_{OUT} = 0.5 V, I_{LOAD} = 10 mA		65		
Output Regulation						
V_{OUT_RLine}	V_{OUT} Line Regulation	3.1 ≤ V_{IN} ≤ 3.7		±5		mV
V_{OUT_RLoad}	V_{OUT} Load Regulation	20 mA ≤ I_{OUT} ≤ 800 mA		±25		mV
V_{OUT_Ripple}	V_{OUT} Ripple	PFM Mode, V_{IN} = 3.7 V, I_{OUT} < 100 mA		11		mV
		PWM Mode, V_{IN} = 3.7 V		4		
Timing						
t_{SS}	Startup Time(9)	V_{IN} = 3.7 V, V_{OUT} from 0 V to 3.1 V, C_{OUT} = 3 x 4.7 µF, 10 V, X5R		50	60	µs
$t_{DC\text{-}DC\_TR}$	V_{CON} Step Response Rise Time(9)	From V_{CON} to 95% V_{OUT}, ΔV_{OUT} ≤ 2.7 V (0.7 V – 3.4 V), R_{LOAD} = 5 Ω, C_{OUT} = 14 µF		6.0	7.3	µs
$t_{DC\text{-}DC\_TF}$	V_{CON} Step Response Fall Time(9)	From V_{CON} to 5% V_{OUT}, ΔV_{OUT} 2.7 V (3.4 V – 0.7 V), R_{LOAD} = 200 Ω, C_{OUT} = 14 µF		6.8	7.6	µs
$t_{DC\text{-}DC\_CL}$	Maximum Allowed Time for Consecutive Current Limit(10)	V_{OUT} < 1 V		1500		µs
t_{DCDC_CLR}	Consecutive Current Limit Recovery Time(10)			4800		µs

Notes:

6. Input voltages nominally exceeding the lesser of V_{IN}/2.5 or 1.6 V force 100% duty cycle.
7. Dropout depends on LDO and DC-DC PFET R_{DSON} and inductor DCR.
8. The current limit is the peak (maximum) current.
9. Guaranteed by design. Maximum values are based on simulation results with 50% C_{OUT} derating; not tested in production. Voltage transient only. Assumes C_{OUT} = 3 x 4.7 µF (1x4.7 µF for regulator and 2x4.7 µF for PA decoupling capacitors).
10. Protects part under short-circuit conditions.

Typical Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7 V, L = 1.0 µH, C_{IN} = 10 µF, C_{OUT} = 3 x 4.7 µF, and T_A = +25°C.

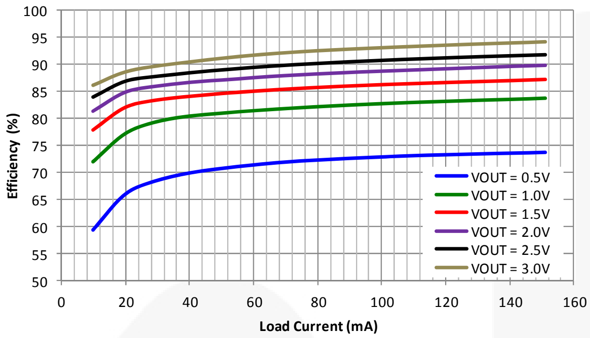


Figure 5. Efficiency vs. Load Current and Output Voltage, V_{IN}=3.8 V, I_{OUT}=10 mA to 150 mA

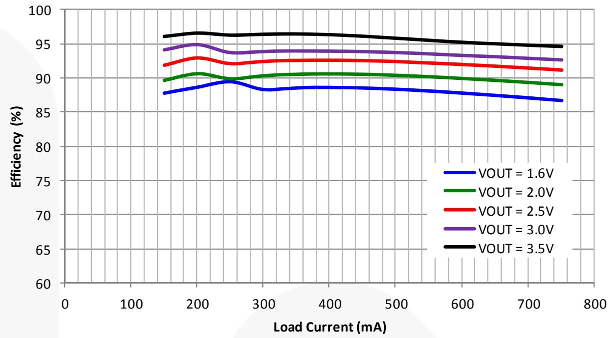


Figure 6. Efficiency vs. Load Current and Output Voltage, V_{IN}=3.8 V, I_{OUT}=150 mA to 750 mA

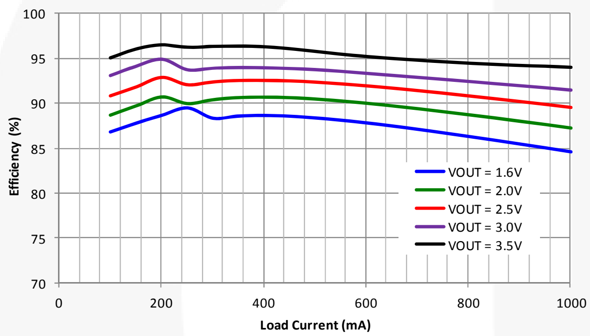


Figure 7. Efficiency vs. Load Current and Output Voltage, V_{IN}=3.8 V, I_{OUT}=100 mA to 1 A

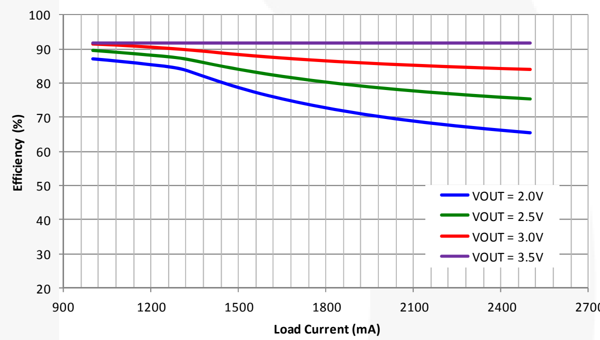


Figure 8. Efficiency vs. Load Current and Output Voltage, V_{IN}=3.8 V, I_{OUT}=1 A to 2.5 A

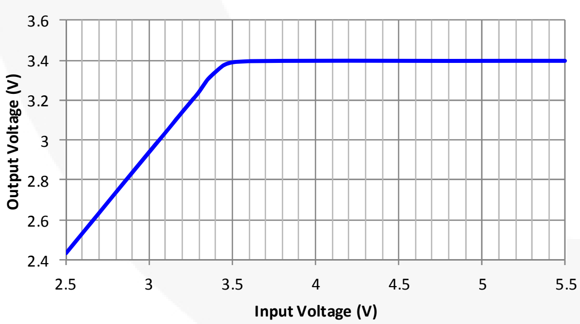


Figure 9. Output Voltage vs. Supply Voltage, V_{OUT}=3.4 V, I_{OUT}=1.5 A, V_{IN}= 4.3 V to Dropout

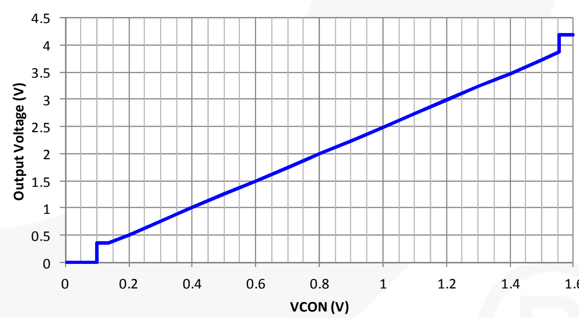


Figure 10. Output Voltage vs. V_{CON} Voltage, V_{IN}= 4.2 V, R_{LOAD}=6.8 Ω, 0.1 V < V_{CON} < 1.6 V

Typical Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7 V, L = 1.0 µH, C_{IN} = 10 µF, C_{OUT} = 3 x 4.7 µF, and T_A = +25°C.

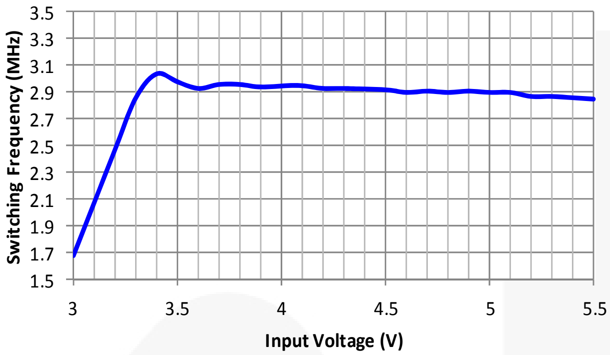


Figure 11. Center-Switching Frequency vs. Supply Voltage, V_{OUT} = 2.5 V, I_{OUT} =700 mA

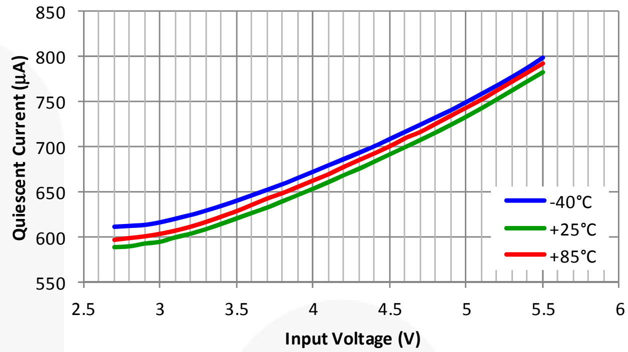


Figure 12. Quiescent Current (PFM) vs. Supply Voltage, V_{OUT} = 1 V, 2.7 V < V_{IN} < 5.5 V (No Load)

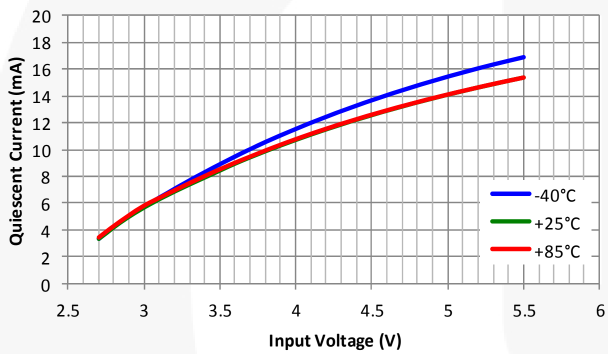


Figure 13. Quiescent Current (PWM) vs. Supply Voltage, V_{OUT} = 2.5 V, 2.7 V < V_{IN} < 5.5 V (No Load)

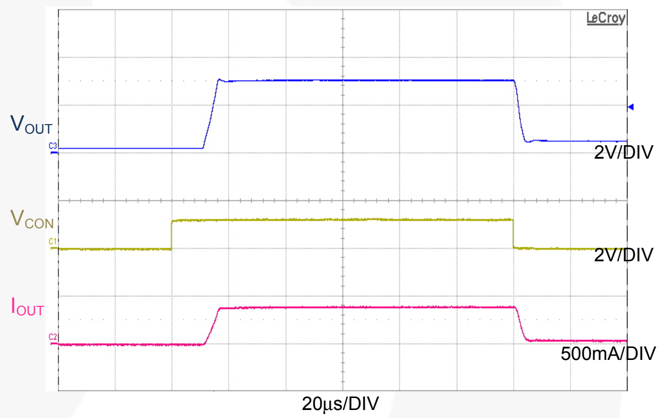


Figure 14. V_{CON} Transient (3 G/4 G), V_{OUT} = 0 V to 3 V, R_{LOAD}=6.8 Ω, V_{IN} = 3.8 V, 100 ns Edge

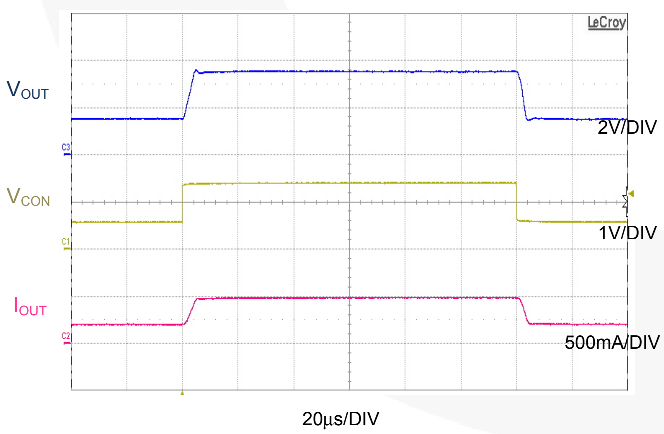


Figure 15. V_{CON} Transient (PFM to PWM), V_{OUT} = 1.4 V to 3.4 V, R_{LOAD}=6.8 Ω, V_{IN} = 3.8 V, 100 ns Edge

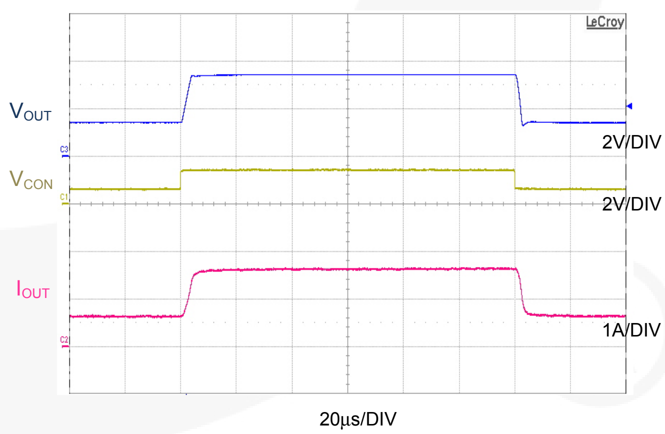


Figure 16. V_{CON} Transient (PWM), V_{OUT} = 1.4 V to 3.4 V, R_{LOAD}=1.9 Ω, V_{IN} = 4.2 V, 100 ns Edge

Typical Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7 V, L = 1.0 µH, C_{IN} = 10 µF, C_{OUT} = 3 x 4.7 µF, and T_A = +25°C.

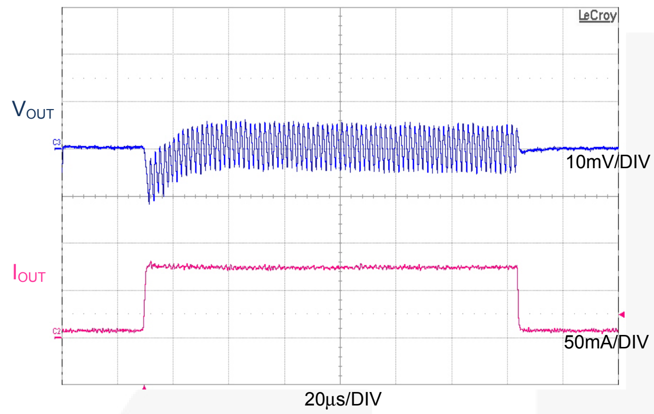


Figure 17. Load Transient in PFM Mode, V_{IN} = 3.6 V, V_{OUT} = 1 V, I_{OUT} = 0 mA to 60 mA, 1 µs Edge

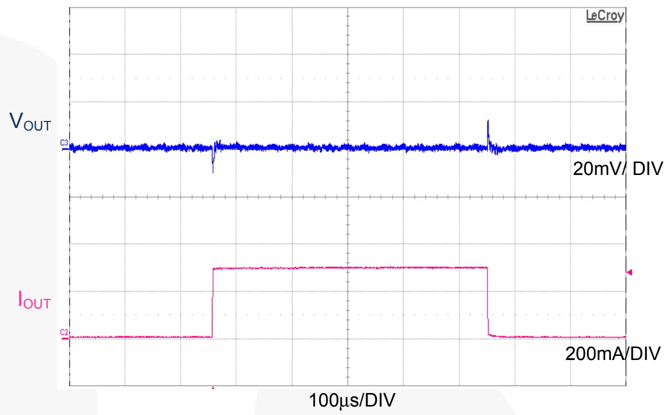


Figure 18. Load Transient in PWM Mode, V_{IN} = 3.8 V, V_{OUT} = 2.5 V, I_{OUT} = 0 mA to 300 mA, 10 µs Edge

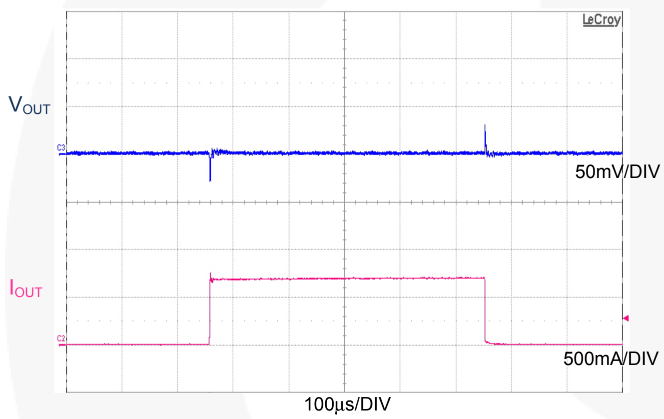


Figure 19. Load Transient in PWM Mode, V_{IN} = 3.8 V, V_{OUT} = 3.0 V, I_{OUT} = 0 mA to 700 mA, 10 µs Edge

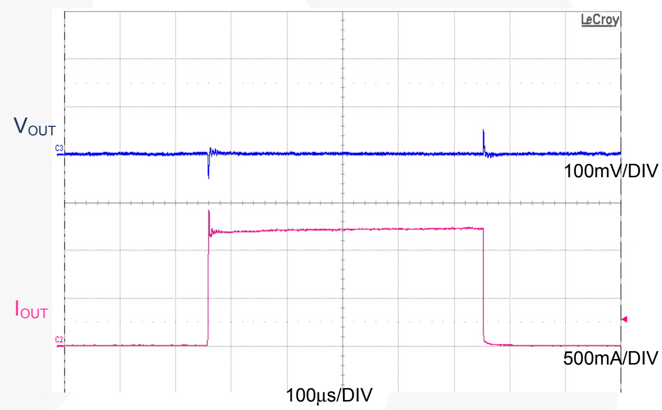


Figure 20. Load Transient in PWM Mode, V_{IN} = 4.2 V, V_{OUT} = 3.0 V, I_{OUT} = 0 mA to 1.2 A, 10 µs Edge

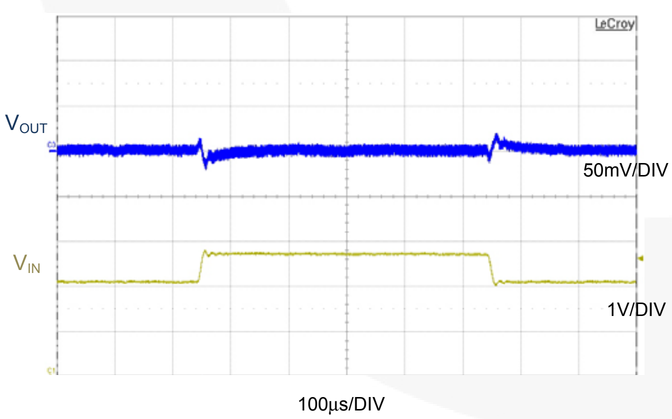


Figure 21. Line Transient, V_{IN} = 3.6 V to 4.2 V, V_{OUT} = 1.0 V, 6.8 Ω Load, 10 µs Edge

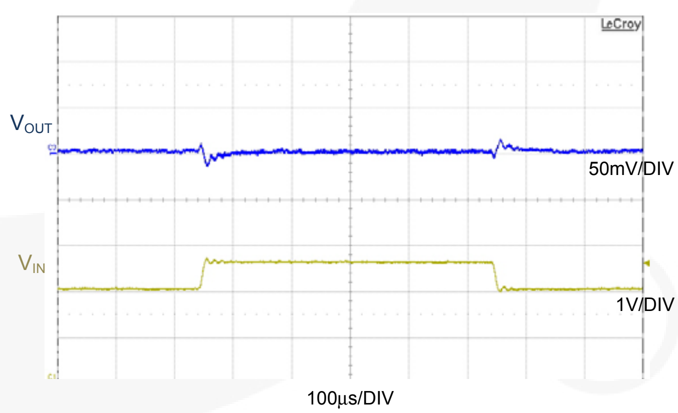


Figure 22. Line Transient, V_{IN} = 3.6 V to 4.2 V, V_{OUT} = 2.5 V, 6.8 Ω Load, 10 µs Edge

Typical Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7 V, L = 1.0 µH, C_{IN} = 10 µF, C_{OUT} = 3 x 4.7 µF, and T_A = +25°C.

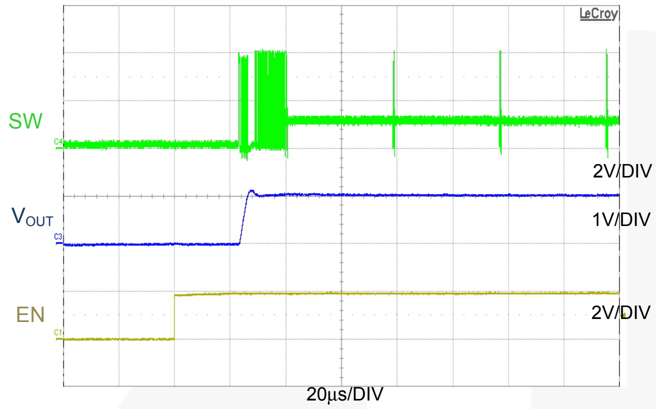


Figure 23. Startup in PFM Mode, V_{IN} = 3.8 V, V_{OUT} = 1.0 V, No Load, EN = LOW to HIGH

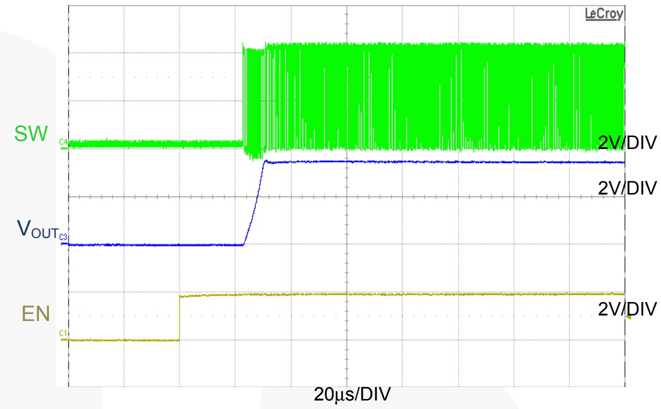


Figure 24. Startup in PWM Mode, V_{IN} = 4.2 V,V_{OUT} = 3.4 V, No Load, EN = LOW to HIGH

Operating Description

The FAN5909 is a high-efficiency, synchronous, step-down converter (DC-DC) with LDO-assist function.

The DC-DC converter operates with current-mode control and supports a wide range of load currents. High-current applications up to a 2.5 A DC output, such as mandated by GSM/EDGE applications, are allowed. Performance degradation due to spurs is removed by spreading the ripple energy through clock dither. A regulated Bypass Mode continues to regulate the output to the desired voltage as V_{IN} approaches V_{OUT}. The LDO offers a dropout voltage of approximately 100 mV under a 2 A load current.

The output voltage V_{OUT} is regulated to 2.5 times the input control voltage, V_{CON}, set by an external DAC. The FAN5909 operates in either PWM or PFM Mode, depending on the output voltage and load current.

In Pulse Width Modulation (PWM) Mode, regulation begins with on-state. A P-channel transistor is turned on and the inductor current is ramped up until the off-state begins. In the off-state, the P-channel is switched off and an N-channel transistor is turned on. The inductor current decreases to maintain an average value equal to the DC load current. The inductor current is continuously monitored. A current sense flags when the P-channel transistor current exceeds the current limit and the switcher is turned back to off-state to decrease the inductor current and prevent magnetic saturation. The current sense flags when the N-channel transistor current exceeds the current limit and redirects discharging current through the inductor back to the battery.

In Pulse Frequency Modulation (PFM) Mode, the FAN5909 operates in a constant on-time mode at low load currents. During on-state, the P-channel is turned on for a specified time before switching to off-state. In off-state, the N-channel switch is enabled until inductor current decreases to 0 A. The switcher enters three-state until a new regulation cycle starts.

PFM operation is allowed only in Low-Power Mode (MODE=1) for output voltages nominally less than 1.5 V. At low load currents, PFM achieves higher efficiency than PWM. The trade-off for efficiency improvement, however, is larger output ripple. Some applications, such as audio, may not tolerate the higher ripple, especially at high output voltages.

Dynamic Output Voltage Transitions

FAN5909 has a complex voltage transition controller that realizes 6 µs transition times with a large output capacitor and output voltage ranges.

The transition controller manages five transitions:

- ΔV_{OUT} positive step
- ΔV_{OUT} negative step
- ΔV_{OUT} transition to or from 100% duty cycle
- ΔV_{OUT} transition at startup

In all cases, it is recommended that sharp V_{CON} transitions be applied, letting the transition controller optimize the output voltage slew rate.

ΔV_{OUT} Positive Step

After a V_{CON} positive step, the FAN5909 enters Current-Limit Mode, where V_{OUT} ramps with a constant slew rate dictated by the output capacitor and the current limit.

ΔV_{OUT} Negative Step

After a V_{CON} negative step, the FAN5909 enters Current Limit Mode where V_{OUT} is reduced with a constant slew rate dictated by the output capacitor and the current limit.

V_{OUT} Transition to or from Forced Bypass

The DC-DC is forced into 100% duty cycle for V_{CON} nominally greater than 1.6 V. This allows the output to be connected to the supply through both the low-resistance DC-DC and the LDO PFETs.

V_{OUT} Transition at Startup

At startup, after the EN rising edge is detected, the system requires 25 µs for all internal voltage references and amplifiers to start before enabling the DC-DC converter function.

MODE Pin

The MODE pin enable Forced PWM Mode or Auto PFM / PWM Mode. When the MODE pin is toggled HIGH (logic 1), the FAN5909 operates in PFM for $V_{OUT} \leq 1.5$ V under light-load conditions and PWM for heavy-load conditions. If the MODE pin is set LOW (logic = 0), it operates in Forced PWM Mode.

Auto PFM / PWM Mode (MODE = 1)

Auto PFM/PWM Mode is appropriate for 3 G/3.5 G and 4 G applications.

Forced PWM Mode (MODE = 0)

Forced PWM Mode is appropriate for applications that demand minimal ripple over the entire output voltage range.

DC-DC – LDO-Assist

The LDO-assist function maintains output regulation when V_{IN} approaches V_{OUT}, enables fast transition times under heavy loads, and minimizes PCB space by enabling a smaller inductor to be employed by using the LDO to provide a portion of the necessary load current.

The LDO-assist function limits the maximum current that the DC-DC may supply by shunting current away from the DC-DC under heavy loads and high duty cycles. In addition, the LDO-assist enables a seamless transition into 100% duty cycle, ensuring both low output ripple and constant output regulation. Since the LDO-assist function limits the maximum current supplied by the DC-DC, PCB area is minimized by enabling a lower current capable, and thus smaller form factor, inductor to be used.

DC-DC – Sleep Mode

The Sleep Mode minimizing current while enabling rapid return to regulation. Sleep Mode is entered when V_{CON} is held below 70 mV for at least 40 µs. In this mode, current consumption is reduced to under 50 µA. Sleep Mode is exited after ~12 µs when V_{CON} is set above 125 mV.

Application Information

Figure 26 illustrates the FAN5909 in a GSM / EDGE / WCDMA transmitter configuration, driving multiple GSM / EDGE and 3 G/3.5 G and 4 G PAs. Figure 27 presents a timing diagram designed to meet GSM specifications.

DC Output Voltage

The output voltage is determined by V_{CON} provided by an external DAC or voltage reference:

$$V_{OUT} = 2.5 \times V_{CON} \quad (1)$$

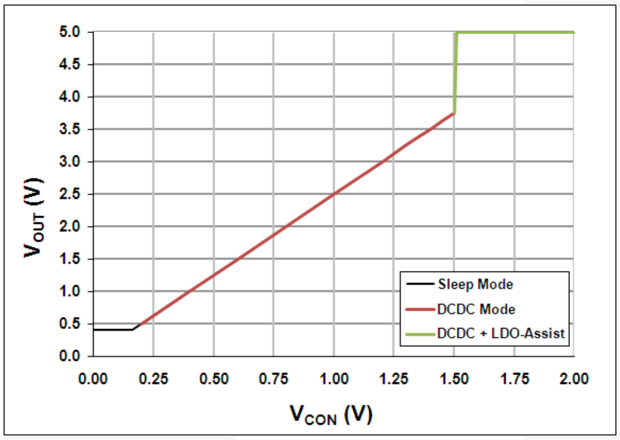


Figure 25. Output Voltage vs. Control Voltage

The FAN5909 provides regulated V_{OUT} only if V_{CON} falls within the typical range from 0.16 V to 1.44 V. This allows V_{OUT} to be adjusted between 0.4 V and 3.6 V. If V_{CON} is less than 0.16 V, V_{OUT} is clamped to 0.40 V. In Auto PFM/PWM Mode, the FAN5909 automatically switches between PFM and PWM. In Forced PWM Mode (MODE = 0), the FAN5909 automatically switches into PWM Mode.

The FAN5909 is designed to support voltage transients of 6 µs when configured for GSM/EDGE applications (MODE=0) and driving a load capacitance of approximately 14 µF. Figure 1 shows a timing diagram for WCDMA applications.

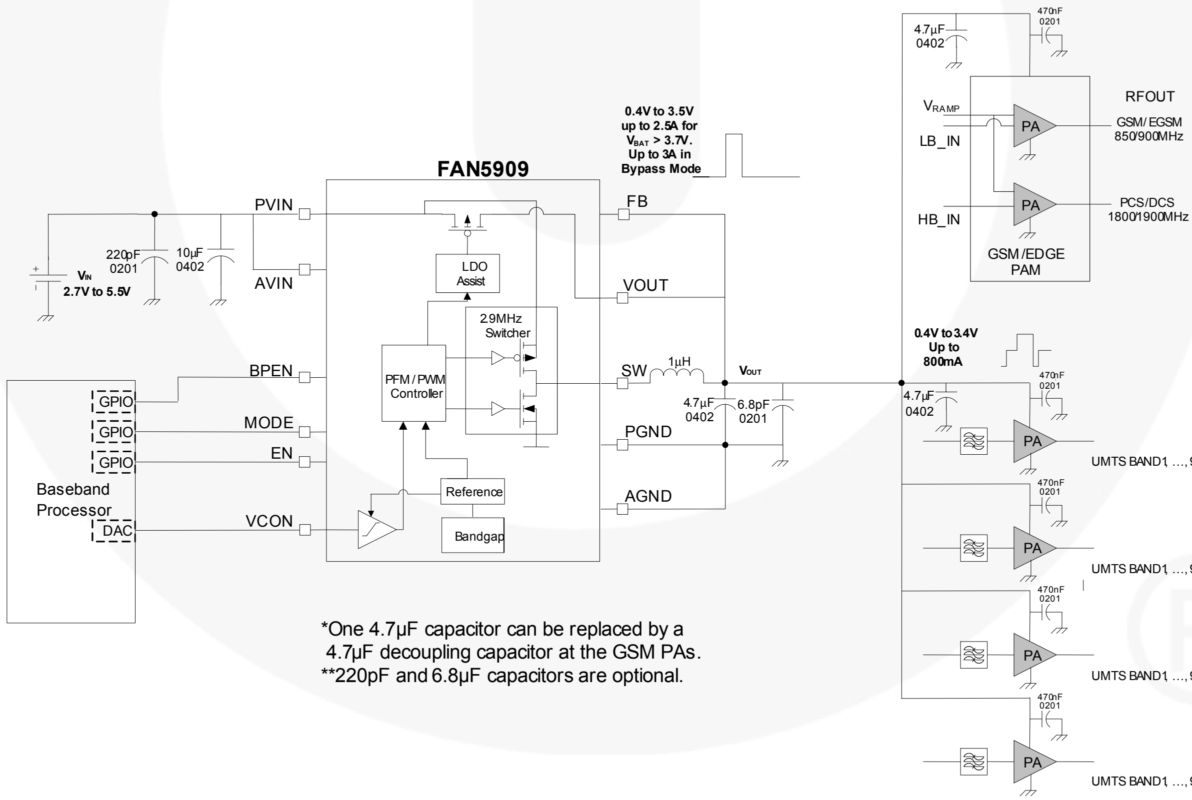


Figure 26. Typical Application Diagram with GSM/EDGE/WCDMA Transmitters

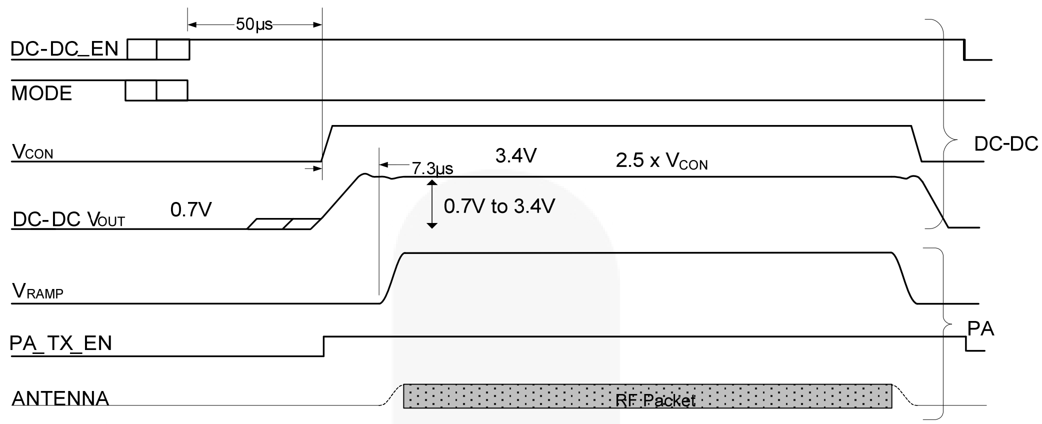


Figure 27. Timing Diagram for GSM/EDGE Transmitters

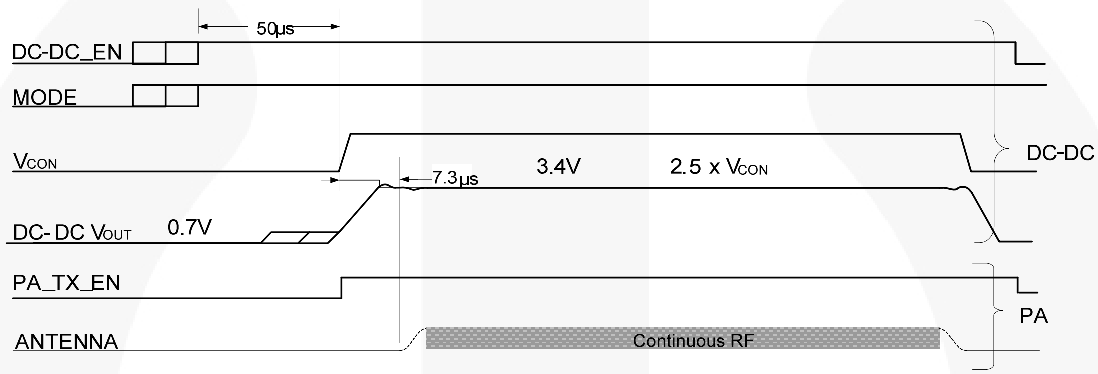


Figure 28. Timing Diagram for WCDMA Transmitters

Inductor Selection

The FAN5909 operates at 2.9 MHz switching frequency, allowing 1.0 µH or 1.5 µH inductors to be used in designs. For applications requiring the smallest possible PCB area, use a 1.0 µH 2012 inductor or a 1.0 µH 2016 inductor for optimum efficiency performance.

Table 1. Recommended Inductors

Inductor	Description
L	1.0 µH, ±20%, 2.1 A, 2012 Case Size Cyntec: PSK20121T-1R0MS-63
	1.0 µH, ±20%, 2.2 A, 2016 Case Size Toko: DFE201610R-H-1R0M

Capacitor Selection

The minimum required output capacitor C_{OUT} should be one (1) 4.7 µF, 6.3 V, X5R with an ESR of 10 mΩ or lower and an ESL of 0.3 nH or lower in parallel after inductor L1. Larger case sizes result in increased loop parasitic inductance and higher noise. One 4.7 µF capacitor should be used as a decoupling capacitor at the GSM/EDGE PA V_{CC} pin and another 4.7 µF capacitor should be placed at V_{CC} pin of the 3 G/4 G PA.

A 6.8 pF capacitor may be added in parallel with C_{OUT} to reduce the capacitor's parasitic inductance.

Table 2. Recommended Capacitor Values

Capacitor	Description
C_{IN}	10 µF, ±20%, X5R, 6.3 V, 0402 (1005 metric) TDK C1005X5R0J106M
C_{OUT}	4.7 µF, ±20%, X5R, 6.3 V, 0402 (1005 metric)TDK C1005X5R0J475K

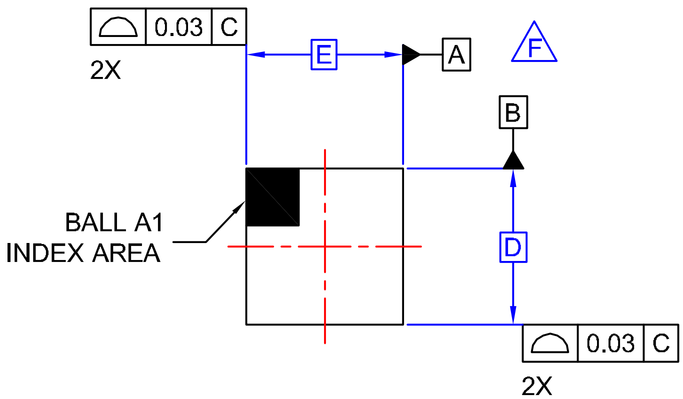
PCB Layout and Component Placement

- The key point in the placement is the power ground (PGND) connection shared between the FAN5909, CIN, and COUT. This minimizes the parasitic inductance of the switching loop paths.
- Place the inductor away from the feedback pins to prevent unpredictable loop behavior.
- Ensure the traces are wide enough to handle the maximum current value, especially in Bypass Mode.
- Ensure the vias are able to handle the current density. Use filled vias if available.
- *Refer to Fairchild's application note:* AN-9726 — The Importance of PCB Design for FAN590x Family.

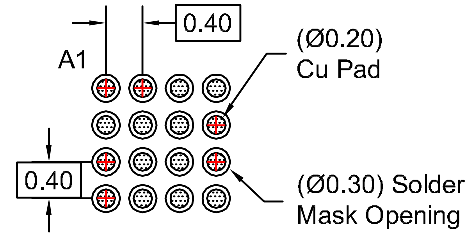
Product Specific Dimensions

D	E	X	Y	Unit
1.615 ± 0.030	1.615 ± 0.030	0.2075	0.2075	mm

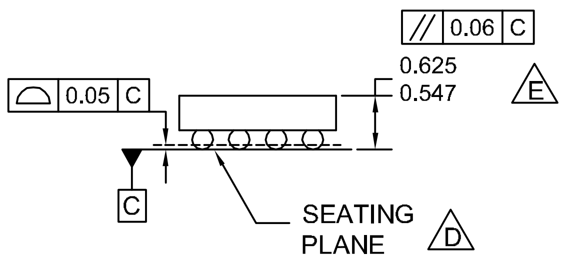
REVISIONS			
REV	DESCRIPTION	DATE	APP'D / SITE
1	Initial drawing release.	3-31-08	L. England
2	Changed land pad solder mask to individual pad openings. Other general updates for drawing consistency.	3-31-08	L. England / FSME

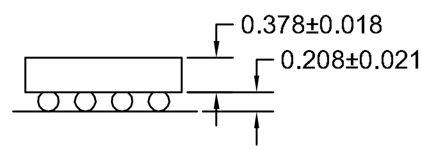


TOP VIEW

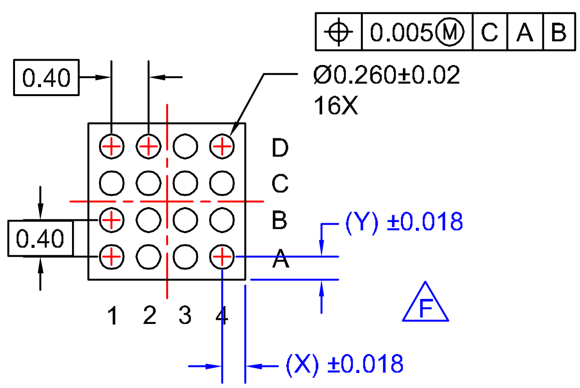


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC016AArev2.

APPROVALS	DATE	FAIRCHILD SEMICONDUCTOR™			
DRAWN L. England	10-26-09	16BALL WLCSP, 4X4 ARRAY 0.4MM PITCH, 250UM BALL			
DFTG. CHK. E. Shacham	10-26-09				
ENGR. CHK.					
PROJECTION INCH [MM]		SCALE N/A	SIZE N/A	DRAWING NUMBER MKT-UC016AA	REV 2
		DO NOT SCALE DRAWING		SHEET 1 of 1	

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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