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September 2010

FAN6747 Highly Integrated Green-Mode PWM Controller

Features

- High-Voltage Startup
- AC-Line Brownout Protection by HV Pin
- Constant Output Power Limit by HV Pin (Full AC-Line Range)
- Built-in 8ms Soft-Start Function
- Two-Level Over-Current Protection (OCP) with 220ms Debounce
- Short-Circuit Protection (SCP) with 15ms Debounce as Output Short
- Peak-Current Mode Operation with Cycle-by-Cycle Current Limiting
- Low Startup Current: 30µA
- Low Operating Current: 1.7mA
- Over-Temperature Protection (OTP) with an External Negative-Temperature-Coefficient (NTC) Thermistor
- PWM Frequency Decreasing at Green-Mode
- V_{DD} Over-Voltage Protection (OVP)
- Internal Latch Circuit for OVP, OTP, SCP, and OCP

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- Power Adapters
- SMPS with Peak-Current Output, such as for Printers, Scanners, Motor Drivers
- AC/DC NB Adapters
- Open-Frame SMPS

Description

The highly integrated FAN6747 PWM controller provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to decrease the switching frequency with load condition.

Under zero-load condition, the power supply enters burst mode and burst frequency can be low to save more power. Green-mode function enables the power supply to meet international power conservation requirements.

The FAN6747 is especially designed for SMPS with peak-current output. It incorporates a cycle-by-cycle current limiting and two-level Over-Current-Protection (OCP) that can handle peak load with a debounce time. Once the current is over the threshold level, it triggers the first counter 15ms and checks if V_{DD} is below 10V; if it is, the PWM latches off for SCP. If V_{DD} is higher than 10V; it keeps counting to 220ms, then the PWM latches off for OCP.

FAN6747 also integrates a frequency-hopping function internally to help reduce EMI emission of a power supply with minimum line filters. Built-in proprietary internal synchronized slope compensation achieves constant output power limit over universal AC line range. The gate output is clamped at 14V to protect the external MOSFET from over-voltage damage.

Other protection functions include AC-line brownout protection with hysteresis and V_{DD} over-voltage protection. For over-temperature protection, an external NTC thermistor can be applied to sense the ambient temperature. When OCP, OVP, SCP, or OTP is activated, an internal latch circuit latches off the controller. The latch is reset when the V_{DD} supply is removed.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6747LMY	-40 to +105°C	8-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, .15-Inch Narrow Body	Tape & Reel

Application Diagram

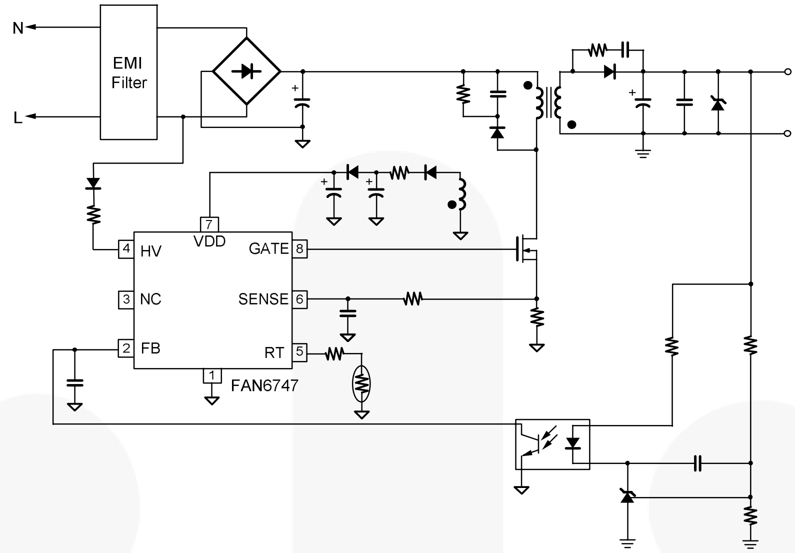


Figure 1. Typical Application

Internal Block Diagram

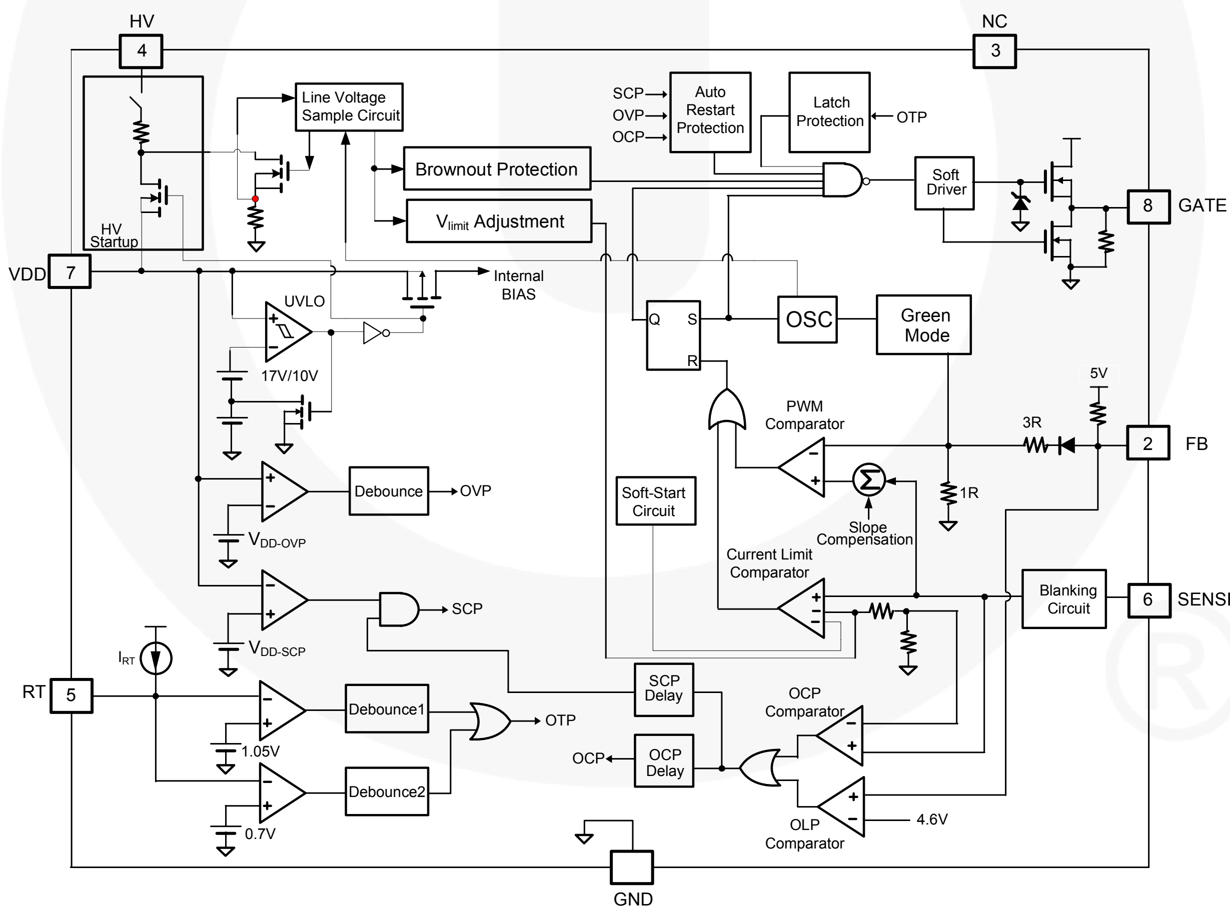
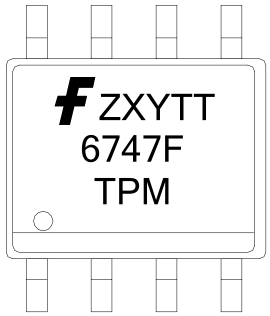


Figure 2. Functional Block Diagram

Marking Information



F: Fairchild Logo
Z: Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
F: L = OCP latch
T: Package Type (N =DIP, M = SOP)
P: Y = Green Compound
M: Manufacturing Flow Code

Figure 3. Top Mark

Pin Configuration

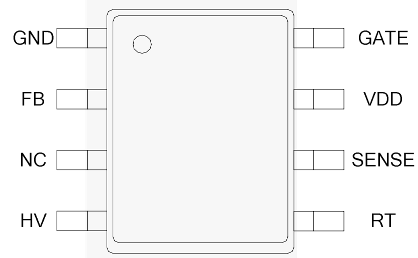


Figure 4. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**. This pin is used for the ground potential of all the pins. A 0.1µF decoupling capacitor placed between VDD and GND is recommended.
2	FB	**Feedback**. The output voltage feedback information from the external compensation circuit is fed into this pin. The PWM duty cycle is determined from this pin and the current-sense signal from Pin 6.
3	NC	**No Connection**.
4	HV	**High-Voltage Startup**. This pin is connected to the line input via diodes and resistors to achieve brownout and high/low line compensation. Once the voltage of the HV pin is lower than the brownout voltage, PWM output is turned off. High/low line compensation dominates the OCP level and cycle-by-cycle current limit, to solves the unequal OCP level and power limit problem under universal input.
5	RT	**Over-Temperature Protection**. For over-temperature protection, an external NTC thermistor is connected from this pin to GND. The impedance of the NTC decreases at high temperatures. Once the voltage of the RT pin drops below the threshold voltage, the controller latches off the PWM. If the RT pin is not connected to the NTC resistor for over temperature protection, it is recommended to connect one 100KΩ resistor to ground to prevent noise interference. This pin is limited by internal clamping circuit.
6	SENSE	**Current Sense**. This pin is used to sense the MOSFET current for the current mode PWM and OCP. If the switching current is higher than OCP threshold and lasts 220ms, the controller latches off the PWM.
7	VDD	**Supply Voltage**. IC operating current and MOSFET driving current are supplied using this pin. This pin is connected to an external bulk capacitor of typically 10µF. The threshold voltages for startup and turn-off are 16.5V and 9V, respectively. The operating current is lower than 2mA.
8	GATE	**Gate Driver Output**. The totem-pole output driver for the power MOSFET. It is internally clamped below 14V.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	DC Supply Voltage			30	V
V_{HV}	Suddenly Input Voltage to HV Pin within 1 Second (Series connect with R_{HV})			640	V
V_L	Input Voltage to FB, SENSE, RT Pin		-0.3	7.0	V
P_D	Power Dissipation (T_A<50°C)			400	mW
Θ_{JA}	Thermal Resistance (Junction-to-Ambient)			150	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability, All Pins Except HV Pin	Human Body Model, JESD22-A114		4.50	kV
		Charge Device Model, JESD22-C101		1.5	

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to the network ground terminal.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature		-40		+105	°C
V_{HV}	Input Voltage to HV Pin				500	V
R_{HV}	HV Startup Resistor		150	200	250	kΩ

Electrical Characteristics

V_{DD}=15V and T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD Section						
V_{OP}	Continuously Operating Voltage				24	V
$V_{DD\text{-}ON}$	Turn-On Threshold Voltage		15.5	16.5	17.5	V
$V_{DD\text{-}OFF}$	PWM Turn-Off Threshold Voltage		8	9	10	V
$V_{DD\text{-}OLP}$	Threshold Voltage on V_{DD} for HV JFET Turn-On in Protection Condition	After Trigger OCP/ SCP/ OVP/ OTP	5.5	6.5	7.5	V
$V_{DD\text{-}LH}$	Threshold Voltage on VDD Pin for Latch-Off Release Voltage		3.5	4.0	4.5	V
$V_{DD\text{-}AC}$	Threshold Voltage on VDD Pin for Disable AC Recovery to Avoid Startup Failed		$V_{DD\text{-}OFF}$ +2.5	$V_{DD\text{-}OFF}$ +3.0	$V_{DD\text{-}OFF}$ +3.5	V
$V_{DD\text{-}SCP}$	Threshold Voltage on VDD Pin for Short-Circuit Protection (SCP)	V_{FB} > V_{FBO}	$V_{DD\text{-}OFF}$ +0.5	$V_{DD\text{-}OFF}$ +1.0	$V_{DD\text{-}OFF}$ +1.5	V
I_{LH}	Holding Current Under Latch-Off Condution	V_{DD}=5V	80	100	120	µA
$I_{DD\text{-}ST}$	Startup Current	$V_{DD\text{-}ON}$ – 0.16V			30	µA
$I_{DD\text{-}OLP}$	Holding Current at PWM-Off Phase	$V_{DD\text{-}OLP}$+0.1V	210	270	330	µA
$I_{DD\text{-}OP1}$	Operating Supply Current when PWM Operating	V_{DD}=20V, V_{FB}=3V Gate Open		1.7	2.0	mA
$I_{DD\text{-}OP2}$	Operating Supply Current when PWM Stop	V_{DD}=20V, V_{FB}=3V Gate Open		1.2	1.5	mA
$V_{DD\text{-}OVP}$	Threshold Voltage on VDD Pin for V_{DD} Over-Voltage Protection (Latch-Off)		24	25	26	V
$t_{D\text{-}OVP}$	V_{DD} OVP Debounce Time	V_{FB} > $V_{FB\text{-}N}$	75	160	245	µs

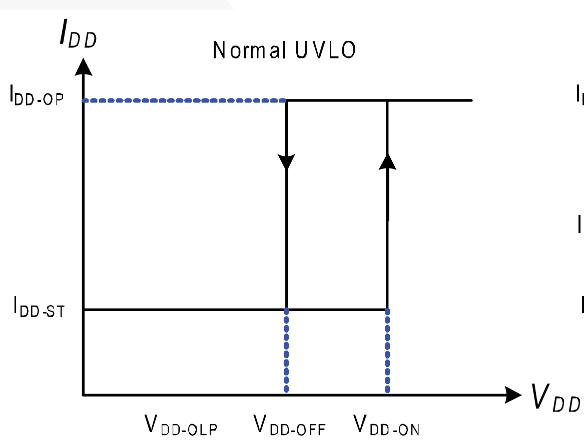


Figure 5. UVLO Specification

Continued on following pages…

Electrical Characteristics

V_{DD}=15V and T_A=25°C, unless otherwise specified.

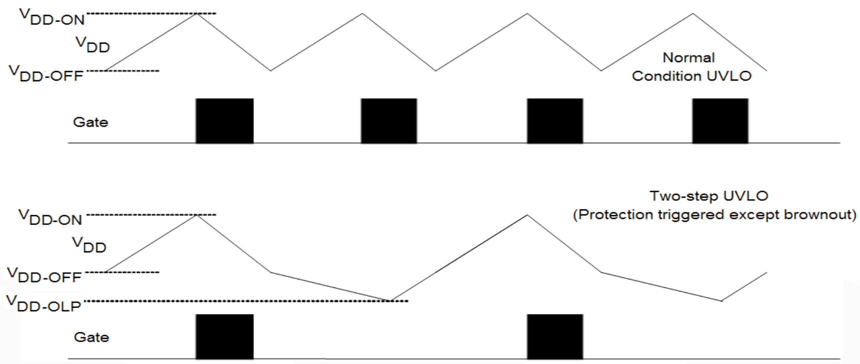


Figure 6. Normal UVLO and Two-Step UVLO Behavior

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
HV Section						
I_{HV}	Supply Current Drawn from HV Pin	V_{HV}=120V, V_{DD}=0V	1.50	2.75	4.00	mA
V_{IN-OFF}	PWM Turn-Off Threshold	DC Source Series R=200k to HV Pin	92	102	112	V
V_{IN-ON}	PWM Turn-On Threshold	DC Source Series R=200k to HV Pin	104	114	124	V
ΔV_{IN}	Change in V_{IN}, V_{IN-ON} - V_{IN-OFF}	DC Source Series R=200k to HV Pin	6	12	18	V
$t_{S-CYCLE}$	Line Voltage Sample cycle	$V_{FB} > V_{FB-N}$	170	205	240	µs
		$V_{FB} < V_{FB-G}$	450	615	780	
t_{S-TIME}	Line Voltage Sample Period			20		µs
$t_{D\_VIN-OFF}$	PWM Turn-Off Debounce Time	$V_{FB} > V_{FB-N}$	65	75	85	ms
		$V_{FB} < V_{FB-G}$	180	235	290	ms

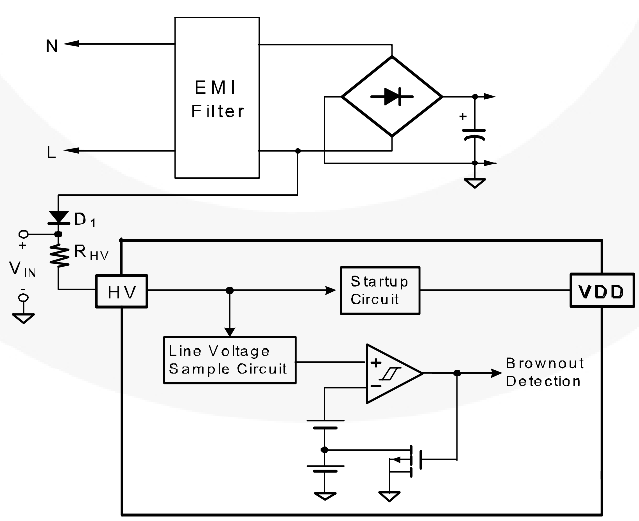


Figure 7. Brownout Circuit

Electrical Characteristics

V_{DD}=15V and T_A=25°C, unless otherwise specified.

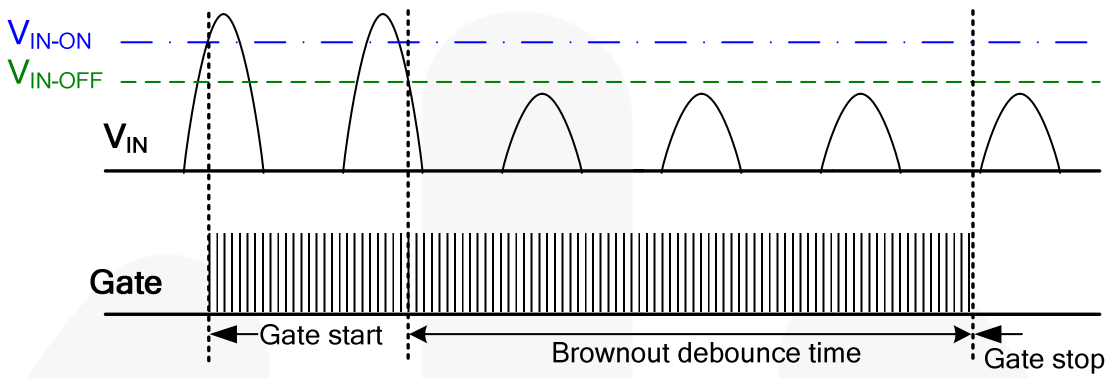


Figure 8. Brownout Behavior

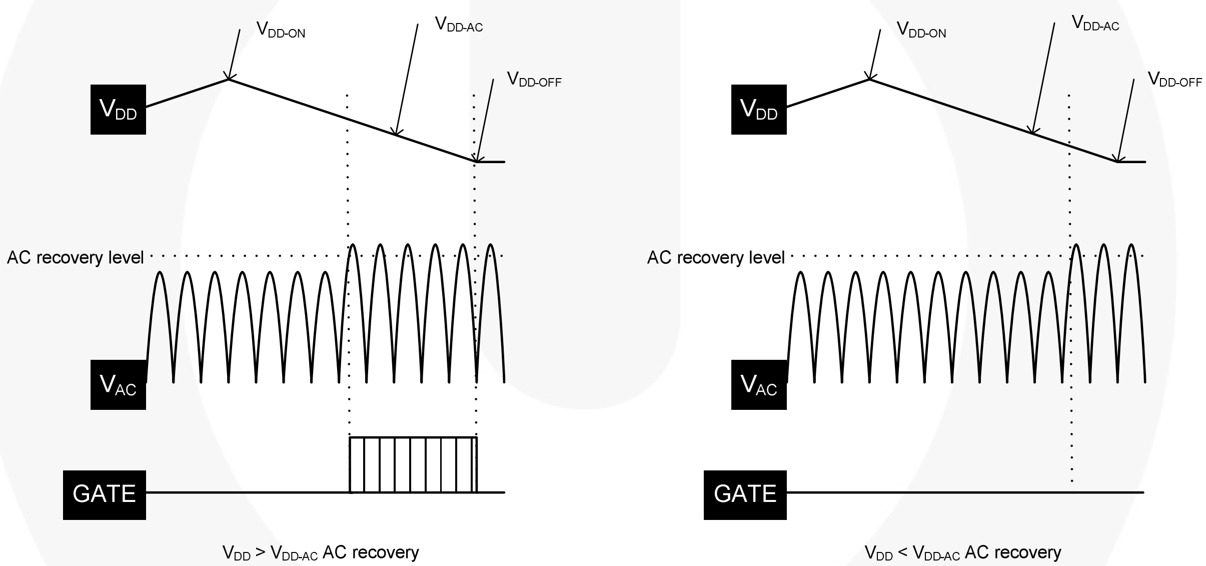


Figure 9. V_{DD-AC} and AC Recovery

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Oscillator Section						
f_{OSC}	Normal PWM Frequency	Center Frequency (V_{FB}>V_{FB-N})	61	65	69	kHz
t_{JTR-1}	Jitter Period 1	V_{FB} > V_{FB-N}	3.9	4.4	4.9	ms
t_{JTR-3}	Jitter Period 3	V_{FB}=V_{FB-G}	10.2	11.5	12.8	ms
f_{OSC-G}	Green-Mode Minimum Frequency		19	22	25	kHz
V_{FB-N}	FB Threshold Voltage for Frequency Reduction Beginning	Pin, FB Voltage (V_{FB}=V_{FB-N}), f_{OSC} – 5KHz	2.6	2.8	3.0	V
		Jitter Range	±3.7	±4.2	±4.7	kHz
V_{FB-G}	FB Threshold Voltage for Turn-Off Jitter and Frequency Reduction Destination	Pin, FB Voltage (V_{FB}=V_{FB-G})	2.1	2.3	2.5	V
		Jitter Range		±1.45		kHz

Electrical Characteristics

V_{DD}=15V and T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{OZ\text{-}ON}$	FB Threshold Voltage for Zero-Duty Recovery		1.6	1.8	2.0	V
$V_{FB\text{-}ZDC}$ ($V_{OZ\text{-}OFF}$)	FB Threshold Voltage for Zero-Duty		1.5	1.7	1.9	V
$V_{OZ\text{-}ON}$ -$V_{OZ\text{-}OFF}$	FB Voltage Hysteresis for $V_{OZ\text{-}ON}$ to $V_{OZ\text{-}OFF}$		50	100	150	mV
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=12V to 22V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-40 to 105°C			5	%

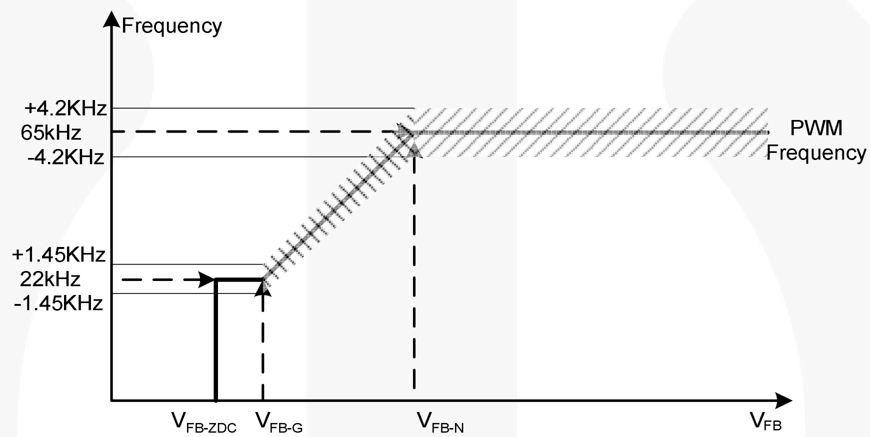


Figure 10. PWM Frequency

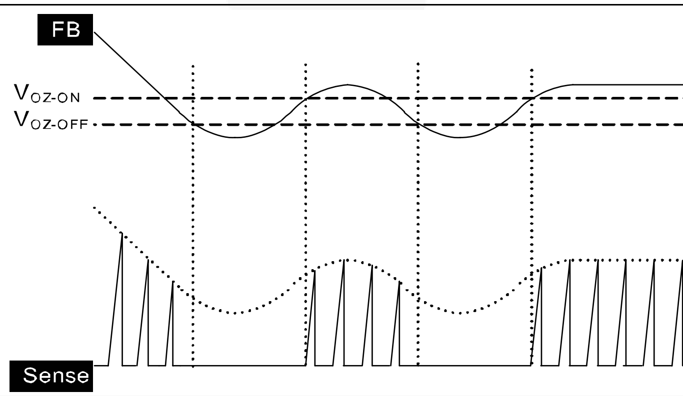


Figure 11. Burst-Mode Diagram

Feedback Input Section

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
A_V	Input-Voltage to Current-Sense Attenuation	V_{FB} < $V_{FB\text{-}G}$	1/4.5	1/4.0	1/3.5	V/V
Z_{FB}	Input Impedance		13.4	15.5	17.6	kΩ
V_{FBO}	FB Pin Open Voltage		4.8	5.0	5.2	V
$V_{FB\text{-}OLP}$	FB Open-Loop Protection Threshold Voltage		4.3	4.6	4.9	V
$t_{D\text{-}OLP}$	Open-Loop Protection Debounce		190	215	240	ms

Electrical Characteristics

V_{DD}=15V and T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Current Sense Section						
t_{PD}	Delay to Output			65	200	ns
t_{LEB}	Leading-Edge Blanking Time		230	270	310	ns
$V_{limit-L}$	Current Limit at Low Line (V_{AC-RMS}=86V)	V_{DC}=122V, Series R=200kΩ to HV	0.790	0.825	0.860	V
$V_{limit-H}$	Current Limit at High Line (V_{AC-RMS}=259V)	V_{DC}=366V, Series R=200kΩ to HV	0.690	0.725	0.760	V
V_{OCP-L}	OCP Trigger Level at Low Line (V_{AC-RMS}=86V)	V_{DC}=122V, Series R=200kΩ to HV	0.450	0.480	0.510	V
V_{OCP-H}	OCP Trigger Level at High Line (V_{AC}=259V)	V_{DC}=366V, Series R=200kΩ to HV	0.390	0.420	0.450	V
$t_{SOFT-START}$	Period During Startup	Startup Time	7	8	9	ms
t_{D-OCP}	Debounce Time for Output OCP	V_{CS}>V_{OCP}	190	215	240	ms
t_{D-SCP}	Debounce Time for Output SCP	V_{CS}>V_{OCP} and V_{DD}< V_{DD-SCP}	12	15	18	ms
PWM Output Section						
DCY_{MAX}	Maximum Duty Cycle		88.0	89.5	91.0	%
V_{OL}	Output Voltage Low	V_{DD}=15V, I_O=50mA			1.5	V
V_{OH}	Output Voltage High	V_{DD}=12V, I_O=50mA	8			V
t_R	Rising Time	GATE=1nF		95		ns
t_F	Falling Time	GATE=1nF		30		ns
V_{CLAMP}	Gate Output Clamping Voltage	V_{DD}=22V	11.0	13.5	16.0	V
Over-Temperature Protection Section						
I_{RT}	Output Current of RT Pin		92	100	108	μA
$V_{OTP-LATCH-OFF}$	Threshold Voltage for Over-Temperature Protection		1.00	1.05	1.10	V
$t_{D\_OTP-LATCH}$	Over-Temperature Latch-Off Debounce	V_{FB} > V_{FB-N}	14	16	18	ms
		V_{FB} < V_{FB-G}	40	51	62	ms
$V_{OTP2-LATCH-OFF}$	Second Threshold Voltage for Over-Temperature Protection		0.65	0.70	0.75	V
$t_{D\_OTP2-LATCH}$	Second Over-Temperature Latch-Off Debounce	V_{FB} > V_{FB-N}	110	185	260	μs
		V_{FB} < V_{FB-G}	320	605	890	

Typical Performance Characteristics

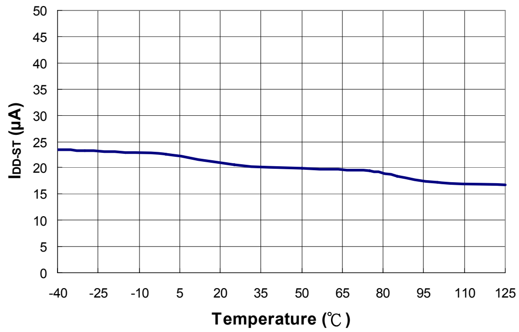


Figure 12. Startup Current (I_{DD-ST}) vs. Temperature

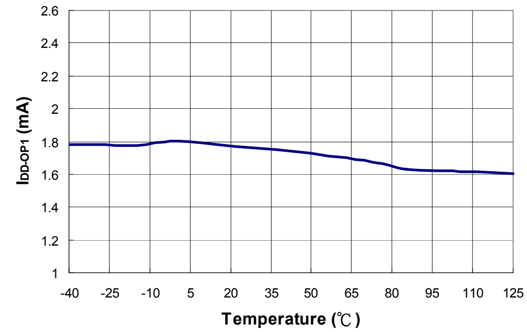


Figure 13. Operation Supply Current (I_{DD-OP1}) vs. Temperature

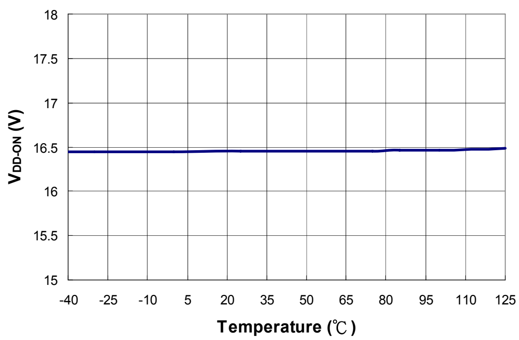


Figure 14. Start Threshold Voltage (V_{DD-ON}) vs. Temperature

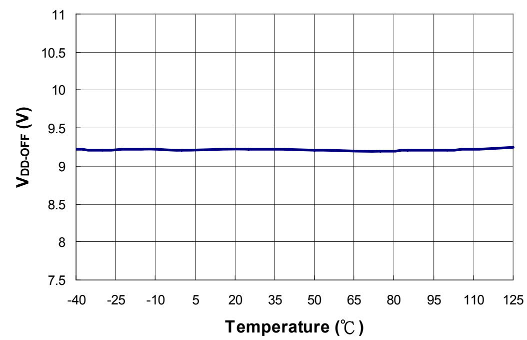


Figure 15. Minimum Operating Voltage (V_{DD-OFF}) vs. Temperature

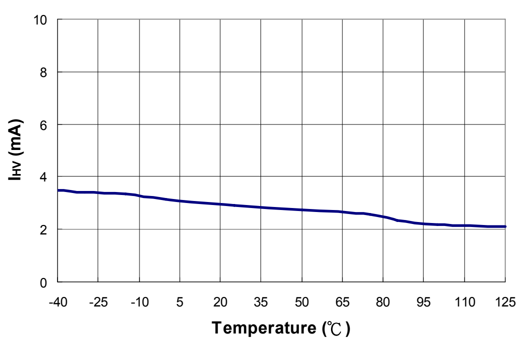


Figure 16. Supply Current Drawn from HV Pin (I_{HV}) vs. Temperature

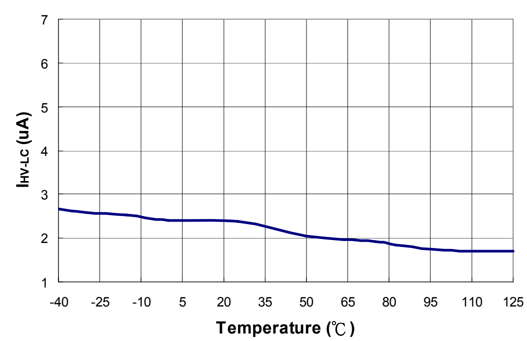


Figure 17. HV Pin Leakage Current After Startup (I_{HV-LC}) vs. Temperature

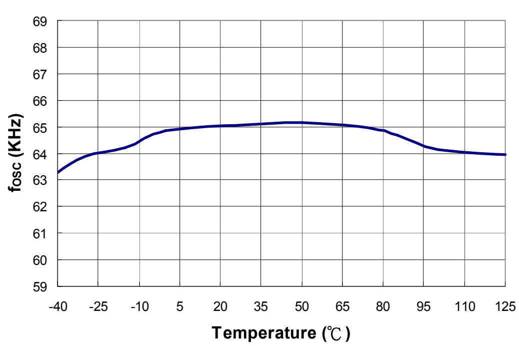


Figure 18. Frequency in Normal Mode (f_{OSC}) vs. Temperature

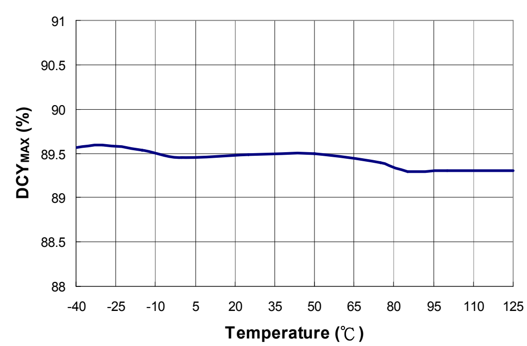


Figure 19. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

Typical Performance Characteristics

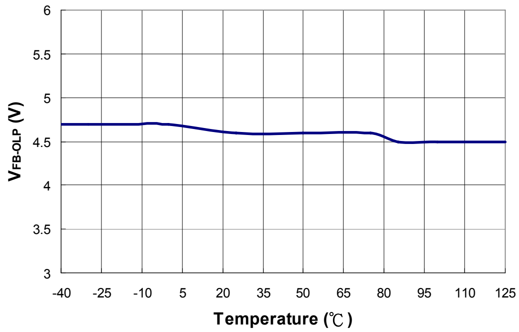


Figure 20. FB Open-Loop Trigger Level (V_{FB-OLP}) vs. Temperature

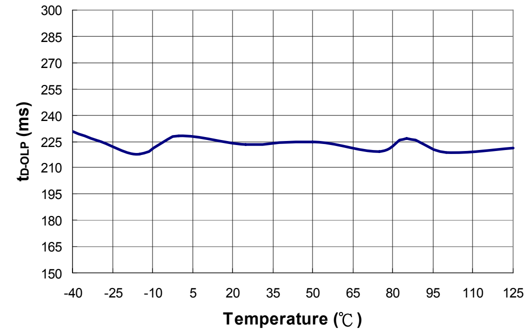


Figure 21. Debounce Time of FB Pin Open-Loop Protection (t_{D-OLP}) vs. Temperature

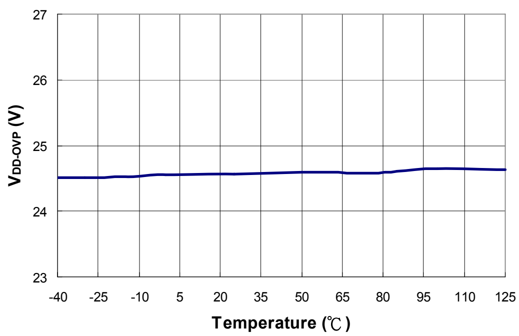


Figure 22. V_{DD} Over-Voltage Protection (V_{DD-OVP}) vs. Temperature

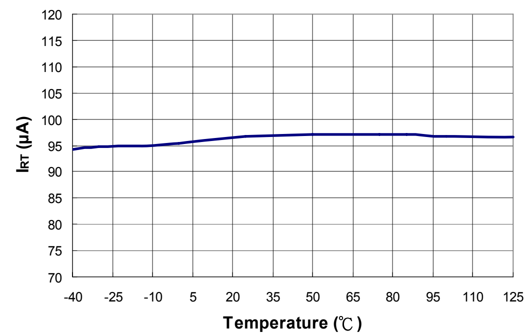


Figure 23. Output Current from RT Pin (I_{RT}) vs. Temperature

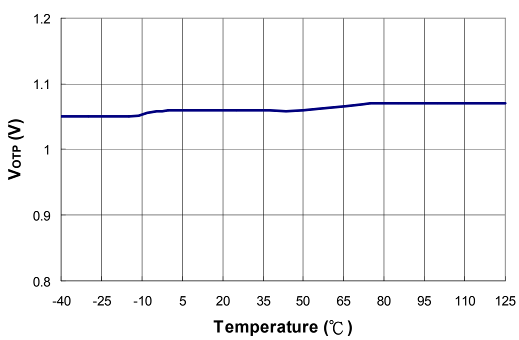


Figure 24. Over-Temperature Protection Threshold Voltage (V_{OTP}) vs. Temperature

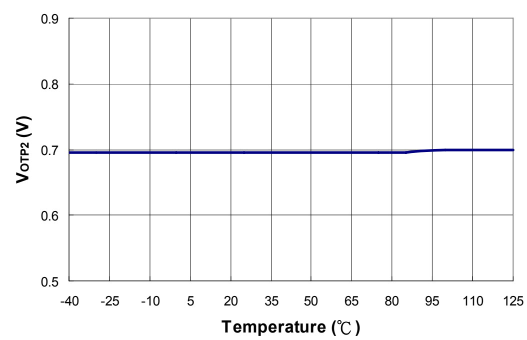


Figure 25. Over-Temperature Protection Threshold Voltage (V_{OTP2}) vs. Temperature

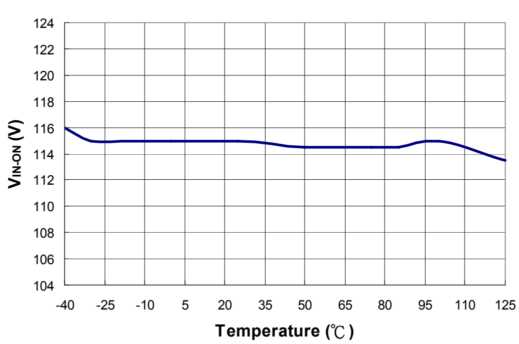


Figure 26. Brown-In (V_{IN-ON}) vs. Temperature

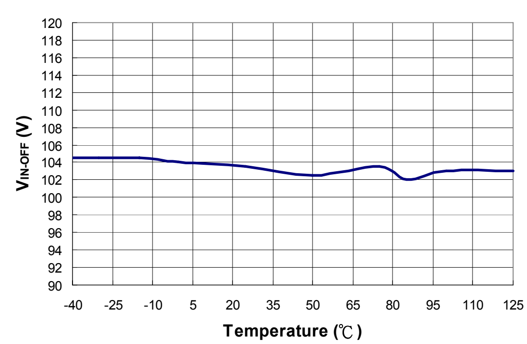


Figure 27. Brownout (V_{IN-OFF}) vs. Temperature

Operation Description

Startup Current

For startup, the HV pin is connected to the line input through an external diode and resistor, R_{HV}, (1N4007 / 200KΩ recommended). Peak startup current drawn from the HV pin is ($V_{AC} \times \sqrt{2}$)/R_{HV} and charges the hold-up capacitor through the diode and resistor. When the V_{DD} capacitor level reaches $V_{DD\text{-}ON}$, the startup current switches off. At this moment, the V_{DD} capacitor only supplies the FAN6747 to maintain the V_{DD} before the auxiliary winding of the main transformer provides the operating current.

Operating Current

Operating current is around 2mA. The low operating current enables better efficiency, power saving, and reduces the requirement of V_{DD} hold-up capacitance.

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to reduce the switching frequency in light-load and no-load conditions. V_{FB}, which is derived from the voltage feedback loop, is taken as the reference. Once V_{FB} is lower than the threshold voltage, switching frequency is continuously decreased to the minimum green-mode frequency of around 22KHz.

Two-Level Over-Current Protection (OCP)

The cycle-by-cycle current limiting shuts down the PWM immediately when the sense voltage is over the limited threshold voltage (0.825V at low line). Additionally, when the sense voltage is higher than the OCP threshold (0.48V at low line), the internal counter counts for 220ms, then latches off PWM. When OCP occurs, PWM output is turned off and V_{DD} begins decreasing.

When V_{DD} goes below the turn-off threshold (~9V), the controller is totally shut down. V_{DD} continues to discharge below $V_{DD\text{-}OLP}$ by $I_{DD\text{-}OLP}$. Then V_{DD} is charged up to the turn-on threshold voltage of 16.5V through the startup resistor. When V_{DD} is charged to 16.5V, it cycles again. This phenomenon is called two-level UVLO.

Brownout and Constant Power Limited HV Pin

Unlike previous PWM controllers, FAN6747's HV pin isn't only used for startup; it can also detect the AC line voltage to perform brownout function and set the current limit level. Through a fast diode and startup resistor to sample the AC line voltage, the peak value refreshes and stores in register at each sampling cycle. When internal update time is met, this peak value is used to for brownout and current-limit level judgment. Equations 1 and 2 can be used to calculate out the level of brown-in or brownout converted to RMS value. For power saving, FAN6747 enlarges the sampling cycle to lower the power loss from HV sampling at light-load condition.

$$V_{AC-ON}(RMS) = (0.9 \times \frac{R_{HV} + 1.6}{1.6}) / \sqrt{2} \qquad (1)$$

$$V_{AC-OFF}(RMS) = (0.81 \times \frac{R_{HV} + 1.6}{1.6}) / \sqrt{2} \qquad (2)$$

; the unit of R_{HV} is kΩ

Short-Circuit Protection (SCP)

This protection is used to handle the huge output demand if the power supply output is suddenly shorted to ground. If V_{DD} drops under 10V and the sensed voltage is higher than the limited threshold voltage, SCP is triggered and PWM output is latched off. This latch condition is reset only if V_{DD} is discharged under 4V or by unplugging AC power line.

Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16.5V and 9V, respectively. During startup, the hold-up capacitor must be charged to 16.5V through the startup resistor to enable the IC. The hold-up capacitor continues to supply V_{DD} before the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 9V during startup. This UVLO hysteresis window ensures that the hold-up capacitor is adequate to supply V_{DD} during startup.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and can not switch off the gate driver.

Gate Output / Soft Driving

The BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 13.5V Zener diode to protect power MOSFET transistors against undesirable gate over voltage. A soft driving waveform is implemented to minimize EMI.

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection is built in to prevent damage due to abnormal conditions. If the V_{DD} voltage is over the over-voltage protection voltage ($V_{DD\text{-}OVP}$) and lasts for $t_{D\text{-}OVP}$, the PWM pulses are disabled until the V_{DD} voltage drops below 4V, then restarts again.

Soft-Start

For many applications, it is necessary to minimize the inrush current at startup. The built-in 8ms soft-start circuit significantly reduces the startup current spike and output voltage overshoot.

Built-In Slope Compensation

The sensed voltage across the current-sense resistor is used for peak-current-mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillation. FAN6747 inserts a synchronized, positive-going, ramp at every switching cycle.

Constant Output Power Limit

When the SENSE voltage across sense resistor R_S reaches the threshold voltage, the output GATE drive is turned off after a small delay, t_{PD}. This delay introduces an additional current proportional to $t_{PD} \cdot V_{IN} / L_P$. Since the delay is nearly constant regardless of the input voltage V_{IN}, higher input voltage results in a larger additional current and the output power limit is higher than under low input line voltage. To compensate this variation for a wide AC input range, a power-limiter is controlled by HV pin to solve the unequal power-limit problem. The power limiter is fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line input than at low-line input.

Over-Temperature Protection (OTP)

A NTC thermistor, R_{NTC}, in series with a resistor, R_A, is connected from the RT pin to GND pin. A constant current I_{RT} is output from this pin. The voltage of the RT pin can be expressed as $V_{RT} = I_{RT} \cdot (R_{NTC} + R_A)$, where I_{RT} is 100µA, the headroom of V_{RT} is limited at around 5V by internal circuitry. As high ambient temperatures occur, R_{NTC} is smaller, such that the V_{RT} decreases. When V_{RT} is less than 1.05V(V_{OTP}) but over 0.7V, the PWM turns off after $t_{D\_OTP\text{-}LATCH}$. The other threshold, V_{DD} under 0.7V, is used for fast shut down of FAN6747 after a short time. If the RT pin is not connected to the NTC resistor for over temperature protection, it is recommended to connect one 100KΩ resistor to ground to prevent noise interference. This pin is limited by internal clamping circuit.

Noise Immunity

Noise on the current sense or control signal may cause significant pulse-width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN6747, and increasing the power MOS gate resistance improve performance.

Physical Dimensions

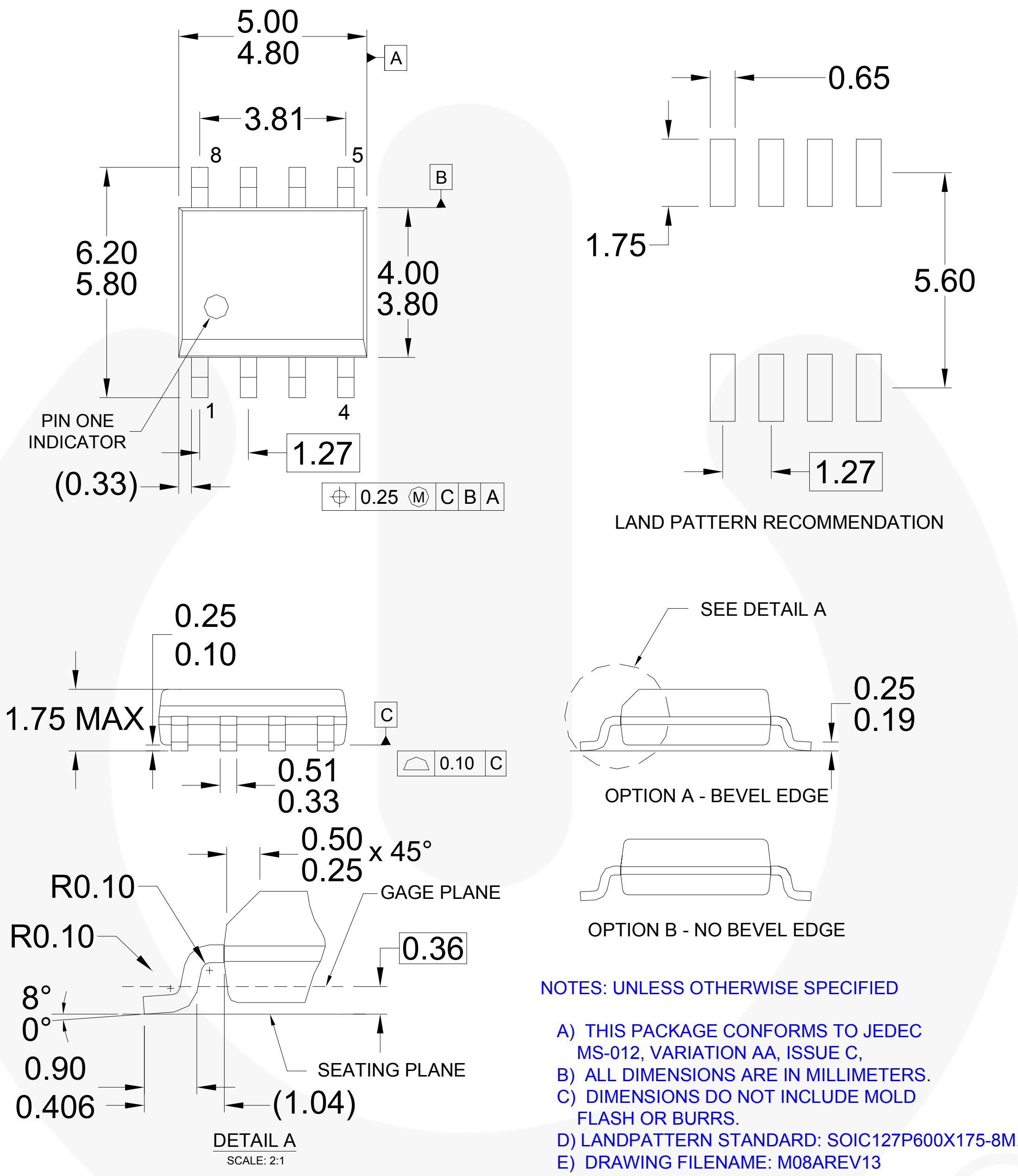


Figure 28. 8-Lead, Small Outline Integrated Circuit (SOIC) Package

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