



Is Now Part of



**ON Semiconductor®**

To learn more about ON Semiconductor, please visit our website at

[www.onsemi.com](http://www.onsemi.com)

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.



# FAN6749

## Highly Integrated Ultra Green-Mode PWM Controller

### Features

- High-Voltage Startup
- Low Operating Current: 1.8 mA
- Linearly Decreasing PWM Frequency to 24 kHz
- Proprietary Frequency Hopping to Reduce EMI
- Two-Level Over-Current Protection (OCP), 1400 ms Delay for Normal Peak Load
- Two-Level OCP, 56 ms Delay for Super Peak Load
- Output Short-Circuit Protection (SCP)
- Peak-Current Mode Operation with Cycle-by-Cycle Current Limiting
- HV Pin Brown-in/out Protection with Hysteresis
- Constant Power Limit by HV Sampling
- Internal FB Open-Loop Protection (OLP)
- GATE Output Maximum Voltage Clamp: 14.5V
- V<sub>DD</sub> Over-Voltage Protection (OVP)
- Programmable Over-Temperature Protection (OTP)
- Integrated 6ms Soft-Start Function
- Internal Latch Circuit (OVP, OTP, OCP, OLP, SCP)
- Internal OTP Sensor with Hysteresis

### Applications

General-Purpose Switched-Mode Power Supplies and Flyback Power Converters, including:

- Power Adapters
- Open-Frame SMPS; Specifically for SMPS with Surge-Current Output, such as for Printer, Scanner, Motor Drivers

### Description

The FAN6749 highly integrated PWM controller enhances the performance of flyback converters. To minimize standby power consumption, a proprietary Green-Mode function continuously decreases the switching frequency under light-load conditions. Under zero-load conditions, the power supply enters Burst Mode and completely shuts off PWM output. Green Mode helps power supplies meet international power conservation requirements.

The FAN6749 is designed for SMPS with surge-current output and incorporates a two-level Over-Current Protection (OCP) function. Besides the cycle-by-cycle current limiting, two-level OCP can handle peak loading within a specified delay time.

FAN6749 also integrates a frequency-hopping function that helps reduce EMI emission of a power supply with minimum line filters. Built-in synchronized slope compensation helps achieve stable peak-current control. To keep constant output power limit over universal AC input range, the current limit and OCP threshold voltage are adjusted according to AC line voltage detected by the HV pin. Gate output is clamped at 14.5 V to protect the external MOSFET from over-voltage damage.

Other protection functions include: AC input brownout protection with hysteresis, Short-Circuit Protection (SCP) for output-short condition, and V<sub>DD</sub> Over-Voltage Protection (OVP). For over-temperature protection, an external NTC thermistor can be applied to sense the ambient temperature. When OLP, OCP, SCP, V<sub>DD</sub> OVP, or OTP is activated, an internal latch circuit latches off the controller. The latch resets when V<sub>DD</sub> is removed.

OVP	OCP	OLP	OTP	SCP
Latch	Latch	Latch	Latch	Latch

There are three differences from FAN6748 to FAN6749:

- Over-current protection debounce time is extended to 1400 ms.
- Brown-out debounce time is extended to 100 ms.
- No SENSE short-circuit protection function.

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6749MLM	-40 to +105°C	8-Pin Small Outline Package (SOP)	Reel & Tape

### Application Diagram

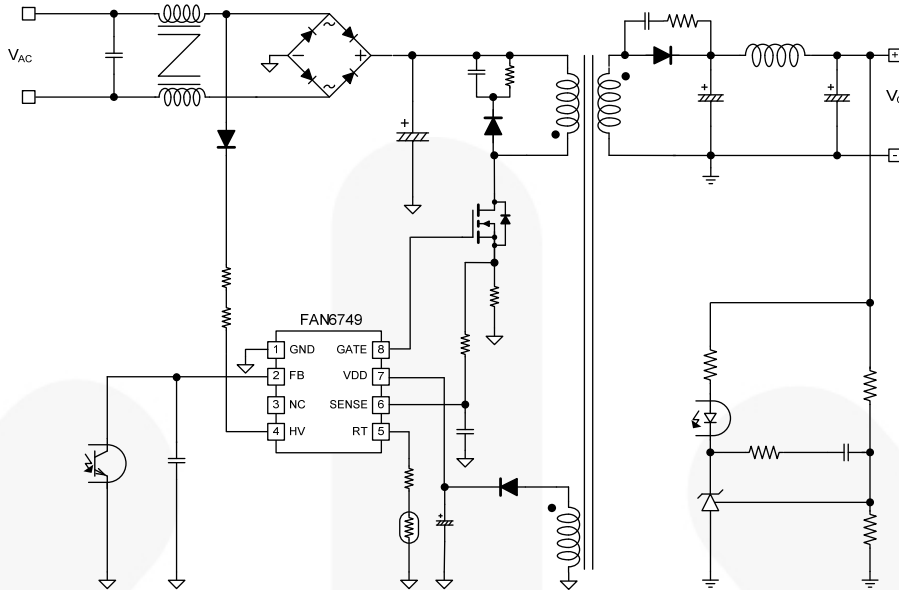


Figure 1. Typical Application

### Internal Block Diagram

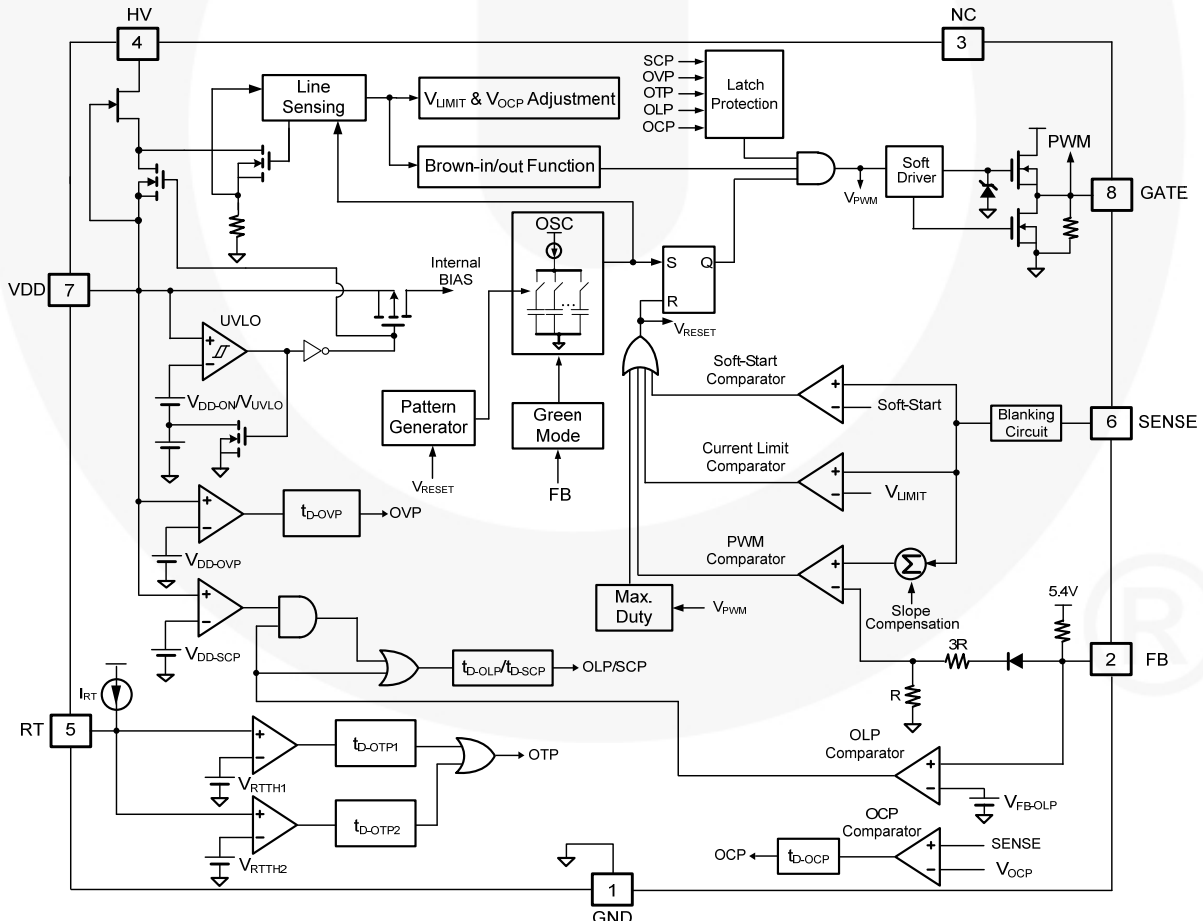
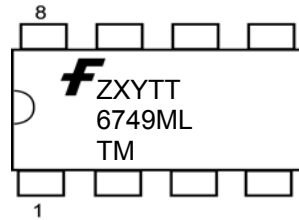


Figure 2. Functional Block Diagram

## Marking Information



**F** - Fairchild Logo  
**Z** - Plant Code  
**X** - 1-Digit Year Code  
**Y** - 1-Digit Week Code  
**TT** - 2-Digit Die Run Code  
**T** - Package Type (M=SOP)  
**M** - Manufacture Flow Code

Figure 3. Top Mark

## Pin Configuration

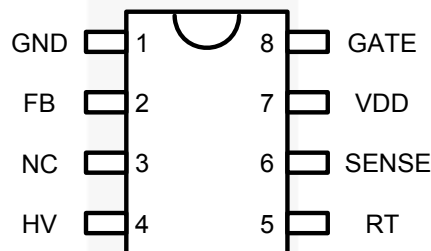


Figure 4. Pin Configuration (Top View)

## Pin Definitions

Pin #	Name	Description
1	GND	<b>Ground Pin.</b> A 0.1 $\mu$ F decoupling capacitor between VDD and GND is recommended.
2	FB	<b>Feedback Pin.</b> The output voltage feedback information from the external compensation circuit is fed into this pin. The PWM duty cycle is determined by comparing the FB signal with current-sense signal from the SENSE pin.
3	NC	No Connection
4	HV	<b>High-Voltage Startup.</b> The HV pin is typically connected to the AC line input through an external diode and a resistor ( $R_{HV}$ ). This pin is used not only to charge $V_{DD}$ capacitor during startup, but also to sense the line voltage. The line voltage information is used for brown-out protection and power limit line compensation.
5	RT	<b>Over-Temperature Protection.</b> An external NTC thermistor is connected from this pin to the GND pin. Once the voltage of the RT pin drops below the threshold voltage, the controller latches off the PWM. The RT pin also provides external latch protection. If the RT pin is not connected to an NTC resistor for over-temperature protection, place a 100 k $\Omega$ resistor to ground to prevent noise interference.
6	SENSE	<b>Current Sense.</b> The sensed voltage is used for peak-current-mode control, over-current protection, short-circuit protection, and cycle-by-cycle current limiting.
7	VDD	<b>Power Supply of IC.</b> A holdup capacitor typically connects from this pin to ground. A rectifier diode in series with the transformer auxiliary winding connects to this pin to supply bias during normal operation.
8	GATE	<b>Gate Drive Output.</b> The totem-pole output driver for the power MOSFET; internally limited to $V_{GATE-CLAMP}$ .

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit	
$V_{DD}$	DC Supply Voltage <sup>(1,2)</sup>		30	V	
$V_{FB}$	FB Pin Input Voltage	-0.3	7.0	V	
$V_{SENSE}$	SENSE Pin Input Voltage	-0.3	7.0	V	
$V_{RT}$	RT Pin Input Voltage	-0.3	7.0	V	
$V_{HV}$	Continuous Input Voltage		500	V	
	Pulse Input Voltage <sup>(3)</sup>		640		
$P_D$	Power Dissipation ( $T_A < 50^\circ\text{C}$ )		400	mW	
$\Theta_{JA}$	Thermal Resistance (Junction-to-Air)		150	$^\circ\text{C}/\text{W}$	
$T_J$	Operating Junction Temperature	-40	+125	$^\circ\text{C}$	
$T_{STG}$	Storage Temperature Range	-55	+150	$^\circ\text{C}$	
$T_L$	Lead Temperature (Wave Soldering or IR, 10 Seconds)		+260	$^\circ\text{C}$	
ESD	Human Body Model <sup>(4)</sup> , JEDEC:JESD22-A114	All Pins Except HV Pin		6	kV
	Charged Device Model <sup>(4)</sup> , JEDEC:JESD22-C101	All Pins Except HV Pin		2	kV

### Notes:

1. All voltage values, except differential voltages, are given with respect to the network ground terminal.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Duration of pulse input voltage is less than or equal to  $\leq 1$  second.
4. ESD with the HV pin CDM=1000 V and HBM=500 V.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{HV}$	HV Startup Resistor	150	200	250	$\text{k}\Omega$

## Electrical Characteristics

$V_{DD}=15\text{ V}$  and  $T_A=25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>V<sub>DD</sub> Section</b>						
V <sub>OP</sub>	Continuously Operating Voltage	Limited by V <sub>DD</sub> OVP			25	V
V <sub>DD-ON</sub>	Threshold Voltage to Startup	V <sub>DD</sub> Rising	16	17	18	V
V <sub>DD-OFF</sub>	Threshold Voltage to Stop Switching in Protection Mode	V <sub>DD</sub> Falling	10	11	12	V
V <sub>DD-OLP</sub>	Threshold Voltage to Turn On HV Startup in Protection Mode	V <sub>DD</sub> Falling	6.5	7.5	8.5	V
V <sub>UVLO</sub>	Threshold Voltage to Stop Switching in Normal Mode	V <sub>DD</sub> Falling	6.0	6.5	7.0	V
V <sub>RESTART</sub>	Threshold Voltage to Enable HV Startup to Charge V <sub>DD</sub> in Normal Mode	V <sub>DD</sub> Falling	4.5	5.0	5.5	V
V <sub>DD-LH</sub>	Threshold Voltage to Release Latch Mode	V <sub>DD</sub> Falling	3.5	4.0	4.5	V
V <sub>DD-AC</sub>	Threshold Voltage on VDD Pin for Disable Brown-in to Avoid Startup Failure		V <sub>UVLO</sub> +2.5	V <sub>UVLO</sub> +3	V <sub>UVLO</sub> +3.5	V
V <sub>DD-SCP</sub>	Threshold Voltage on VDD Pin for Short-Circuit Protection (SCP)	V <sub>FB</sub> > V <sub>FB-OLP</sub>	V <sub>DD-OFF</sub> +1.0	V <sub>DD-OFF</sub> +1.5	V <sub>DD-OFF</sub> +2.0	V
t <sub>D-SCP</sub>	Debounce Time for SCP	V <sub>FB</sub> > V <sub>FB-OLP</sub> & V <sub>DD</sub> < V <sub>DD-SCP</sub>	12	17	22	ms
I <sub>DD-ST</sub>	Startup Current	V <sub>DD-ON</sub> - 0.16 V			30	μA
I <sub>DD-OP1</sub>	Supply Current in PWM Operation	V <sub>DD</sub> =20 V, V <sub>FB</sub> = 3 V Gate Open		1.8	2.4	mA
I <sub>DD-OP2</sub>	Supply Current when PWM Stops	V <sub>DD</sub> =15 V, V <sub>FB</sub> < 1.4 V		1.0	1.9	mA
I <sub>LH</sub>	Operating Current when V <sub>DD</sub> < V <sub>DD-OFF</sub> in Protection Mode	V <sub>DD</sub> = 5 V	100	120	140	μA
I <sub>DD-OLP</sub>	Internal Sink Current	V <sub>DD-OLP</sub> +0.1 V	265	325	385	μA
V <sub>DD-OVP</sub>	Threshold Voltage for V <sub>DD</sub> Over-Voltage Protection		28.5	29.0	29.9	V
t <sub>D-VDDOVP</sub>	V <sub>DD</sub> Over-Voltage Protection Debounce Time		160	200	240	μs

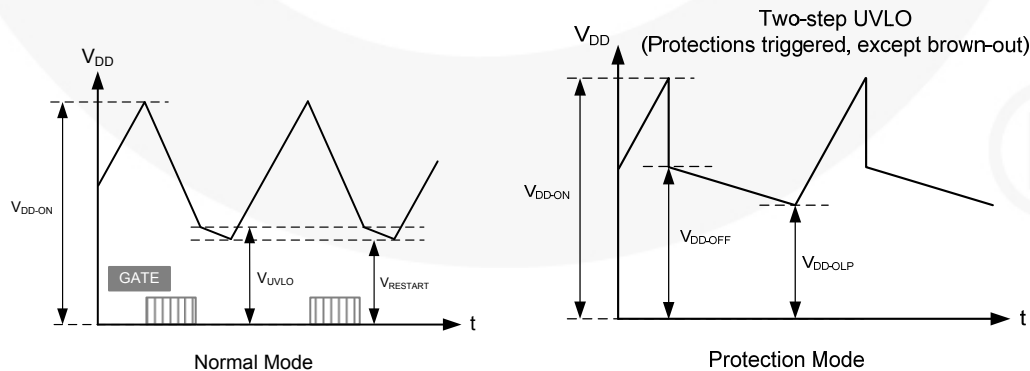
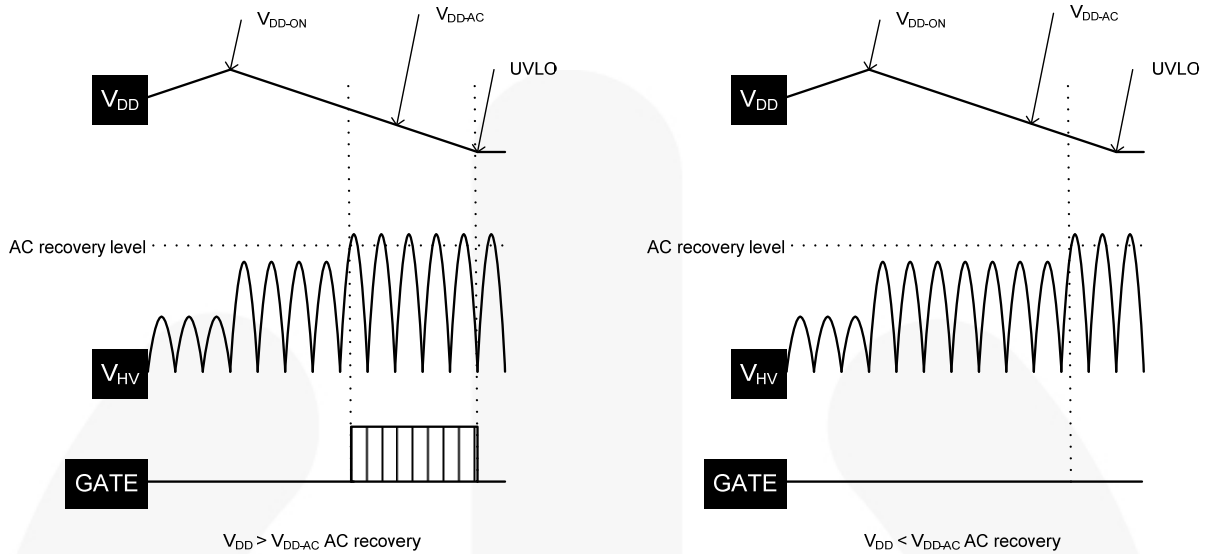


Figure 5. V<sub>DD</sub> Behavior

Continued on the following page...

### Electrical Characteristics (Continued)

$V_{DD}=15\text{ V}$  and  $T_A=25^\circ\text{C}$  unless otherwise noted.



**Figure 6.  $V_{DD-AC}$  & AC Recovery**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>HV Section</b>						
$I_{HV}$	Supply Current from HV Pin	$V_{DC}=120\text{ V}$ , $V_{DD}=0\text{ V}$	2.0	3.5	5.0	mA
$I_{HV-LC}$	Leakage Current after Startup	$HV=500\text{ V}$ , $V_{DD}=V_{DD-OFF}+1\text{ V}$		1	20	$\mu\text{A}$
$V_{AC-OFF}$	Threshold Voltage for Brownout	DC Source Series $R=200\text{ k}\Omega$ to HV Pin	90	100	110	V
$V_{AC-ON}$	Threshold Voltage for Brown-In	DC Source Series $R=200\text{ k}\Omega$ to HV Pin	100	110	120	V
$\Delta V_{AC}$	$V_{AC-ON} - V_{AC-OFF}$	DC Source Series $R=200\text{ k}\Omega$ to HV Pin	8	10	17	V
$t_{S-CYCLE}$	Line Voltage Sample Cycle <sup>(7)</sup>	$V_{FB} > V_{FB-N}$	170	200	230	$\mu\text{s}$
		$V_{FB} < V_{FB-G}$	400	520	640	
$t_{H-TIME}$	Line Voltage Hold Period <sup>(7)</sup>		18	23	28	$\mu\text{s}$
$t_{UPDATE}$	Peak Line Voltage Data Update Cycle for High / Low Line Compensation <sup>(7)</sup>	$V_{FB} > V_{FB-N}$	20	24	28	ms
		$V_{FB} = V_{FB-G}$	64	72	80	
$t_{D-AC-OFF}$	Debounce Time for Brownout		70	100	130	ms
<b>Oscillator Section</b>						
$f_{OSC}$	Switching Frequency when $V_{FB} > V_{FB-N}$	Center Frequency	62	65	68	kHz
		Hopping Range	$\pm 3.5$	$\pm 4.0$	$\pm 4.5$	
$t_{HOP}$	Hopping Period		16	20	24	ms
$f_{OSC-G}$	Switching Frequency When $V_{FB} < V_{FB-G}$	Center Frequency	20	24	28	kHz
		Hopping Range	$\pm 1.25$	$\pm 1.55$	$\pm 1.85$	
$f_{DV}$	Frequency Variation vs. $V_{DD}$ Deviation	$V_{DD}=11\text{ V}$ to $22\text{ V}$			5	%
$f_{DT}$	Frequency Variation vs. Temperature Deviation	$T_A=-40$ to $105^\circ\text{C}$			5	%

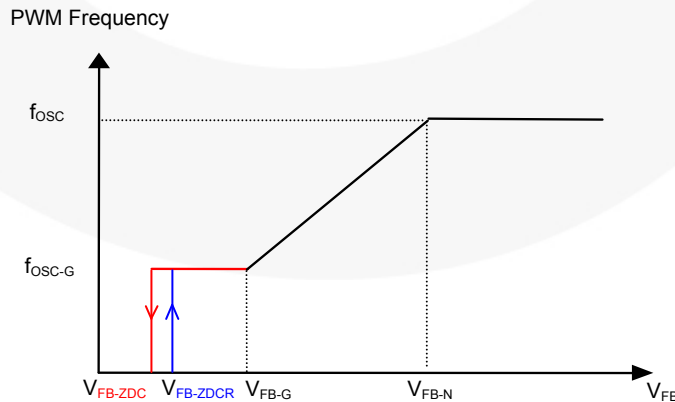
Continued on the following page...

**Electrical Characteristics** (Continued)

$V_{DD}=15\text{ V}$  and  $T_A=25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Feedback Input Section</b>						
$A_V$	Input Voltage to Current-Sense Attenuation		1/4.5	1/4.0	1/3.5	V/V
$Z_{FB}$	FB Internal Pull-High Impedance		15	17	19	k $\Omega$
$V_{FB-OPEN}$	FB internal Biased Voltage	FB Pin Open	5.2	5.4	5.6	V
$V_{FB-OLP}$	Threshold Voltage for OLP		4.3	4.6	4.9	V
$t_{D-OLP}$	Debounce Time for OLP		40	56	72	ms
$V_{FB-N}$	Threshold Voltage for Maximum Switching Frequency	Pin, FB Voltage( $V_{FB}=V_{FB-N}$ )	2.5	2.7	2.9	V
$V_{FB-G}$	Threshold Voltage for Minimum Switching Frequency	Pin, FB Voltage( $V_{FB}=V_{FB-G}$ )	2.05	2.25	2.45	V
$S_G$	Slope for Green-Mode Modulation			85		Hz/mV
$V_{FB-ZDCR}$	Threshold Voltage for Zero Duty Cycle Recovery		1.9	2.1	2.3	V
$V_{FB-ZDC}$	Threshold Voltage for Zero Duty Cycle		1.8	2.0	2.2	V
$V_{FB-ZDCR} - V_{FB-ZDC}$	Zero Duty Cycle Hysteresis		0.05	0.10	0.15	V
<b>Current-Sense Section</b>						
$t_{PD}$	Delay to Output			65	200	ns
$t_{LEB}$	Leading-Edge Blanking		230	270	310	ns
$V_{LIMIT-L}$	Current Limit Level at Low Line ( $V_{AC-RMS}=86\text{ V}$ )	$V_{DC}=122\text{ V}$ , Series R=200 k $\Omega$ to HV	0.790	0.825	0.860	V
$V_{LIMIT-H}$	Current Limit Level at High Line ( $V_{AC-RMS}=259\text{ V}$ )	$V_{DC}=366\text{ V}$ , Series R=200 k $\Omega$ to HV	0.690	0.725	0.760	V
$V_{OCP-L}$	OCP Trigger Level at Low Line ( $V_{AC-RMS}=86\text{ V}$ )	$V_{DC}=122\text{ V}$ , Series R=200 k $\Omega$ to HV	0.45	0.48	0.51	V
$V_{OCP-H}$	OCP Trigger Level at High Line ( $V_{AC-RMS}=259\text{ V}$ )	$V_{DC}=366\text{ V}$ , Series R=200 k $\Omega$ to HV	0.39	0.42	0.45	V
$t_{SS}$	Soft-start time	Startup Time	4.5	6.0	7.5	ms
$t_{D-OCP}$	Debounce Time for OCP	$V_{SENSE}>V_{OCP}$	1000	1400	1800	ms

Continued on the following page...



**Figure 7.  $V_{FB}$  vs. PWM Frequency**



**Electrical Characteristics** (Continued) $V_{DD}=15\text{ V}$  and  $T_A=25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>GATE Section</b>						
$D_{MAX}$	Maximum Duty Cycle		80	85	90	%
$V_{GATE-L}$	Gate Low Voltage	$V_{DD}=15\text{ V}$ , $I_O=50\text{ mA}$			1.5	V
$V_{GATE-H}$	Gate High Voltage	$V_{DD}=12\text{ V}$ , $I_O=50\text{ mA}$	8			V
$t_r$	Gate Rising Time (20-80%)	$V_{DD}=15\text{ V}$ , $C_L=1\text{ nF}$	60	75	90	ns
$t_f$	Gate Falling Time (80-20%)	$V_{DD}=15\text{ V}$ , $C_L=1\text{ nF}$	15	25	35	ns
$I_{GATE-SINK}$	Gate Sink Current <sup>(7)</sup>	$V_{DD}=15\text{ V}$	300			mA
$I_{GATE-SOURCE}$	Gate Sourcing Current <sup>(7)</sup>	$V_{DD}=15\text{ V}$ , $GATE=6\text{ V}$	250			mA
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	$V_{DD}=22\text{ V}$	11.0	14.5	18.0	V
<b>RT Section</b>						
$I_{RT}$	Output Current of RT Pin		90	100	110	$\mu\text{A}$
$V_{RTTH1}$	Threshold Voltage for Over-Temperature Protection	$0.7\text{ V} < V_{RT} < 1.05\text{ V}$ , After 14 ms Latch Off	1.015	1.050	1.085	V
$V_{RTTH2}$	Threshold Voltage for Latch Triggering	$V_{RT} < 0.7\text{ V}$ , After 165 $\mu\text{s}$ Latch Off	0.65	0.70	0.75	V
$R_{OTP}$	Maximum External Resistance of RT Pin to Trigger Latch Protection		9.66	10.50	11.34	k $\Omega$
$t_{D-OTP1}$	Debounce Time for Over-Temperature Protection Triggering	$V_{RTTH2} < V_{RT} < V_{RTTH1}$	11	14	18	ms
$t_{D-OTP2}$	Debounce Time for Latch Triggering	$V_{RT} < V_{RTTH2}$	90	165	240	$\mu\text{s}$
<b>Over-Temperature Protection Section (OTP)</b>						
$T_{OTP}$	Protection Junction Temperature <sup>(6,7)</sup>		+135			$^\circ\text{C}$
$T_{Restart}$	Restart Junction Temperature <sup>(6,7)</sup>		$T_{OTP}-25$			$^\circ\text{C}$

**Notes:**

5. When activated, the output is disabled and the latch is turned off.
6. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.
7. Guaranteed by design.

## Typical Performance Characteristics

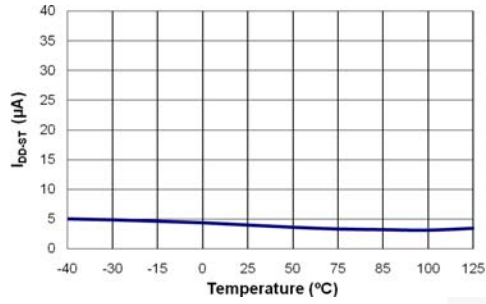


Figure 8. Startup Current ( $I_{DD-ST}$ ) vs. Temperature

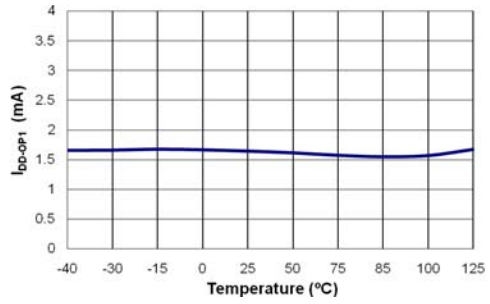


Figure 9. Operation Supply Current ( $I_{DD-OP1}$ ) vs. Temperature

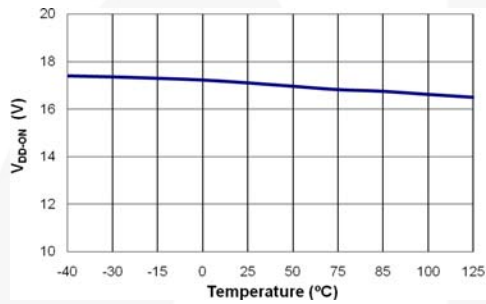


Figure 10. Start Threshold Voltage ( $V_{DD-ON}$ ) vs. Temperature

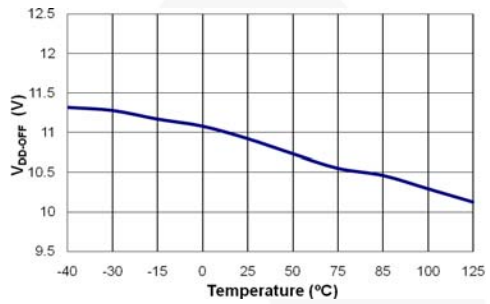


Figure 11. Minimum Operating Voltage ( $V_{DD-OFF}$ ) vs. Temperature

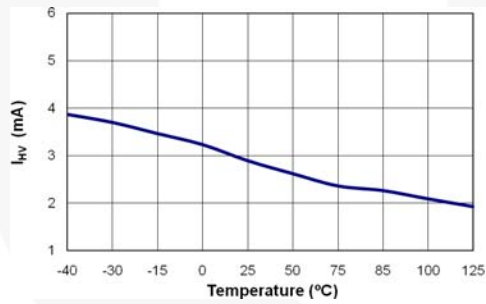


Figure 12. Supply Current Drawn from HV Pin ( $I_{HV}$ ) vs. Temperature

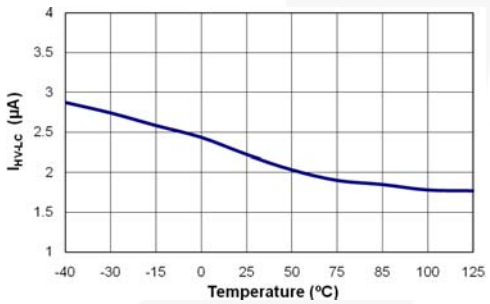


Figure 13. HV Pin Leakage Current After Startup ( $I_{HV-LC}$ ) vs. Temperature

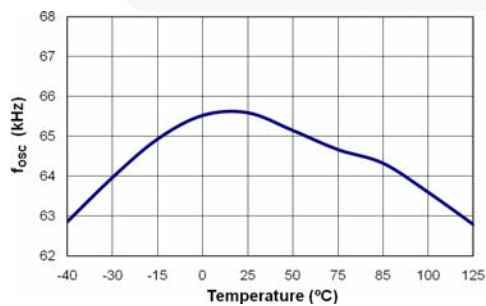


Figure 14. Frequency in Normal Mode ( $f_{osc}$ ) vs. Temperature

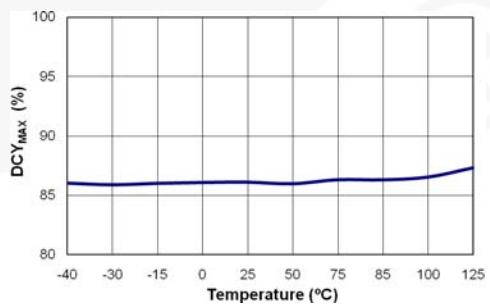


Figure 15. Maximum Duty Cycle ( $DCY_{MAX}$ ) vs. Temperature

## Typical Performance Characteristics

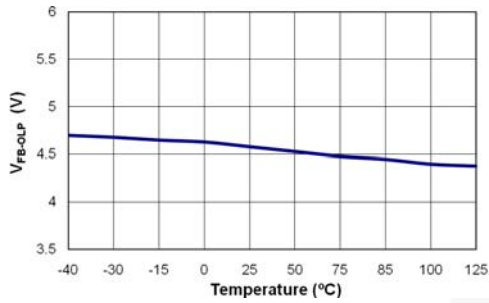


Figure 16. FB Open-Loop Trigger Level (V<sub>FB-OLP</sub>) vs. Temperature

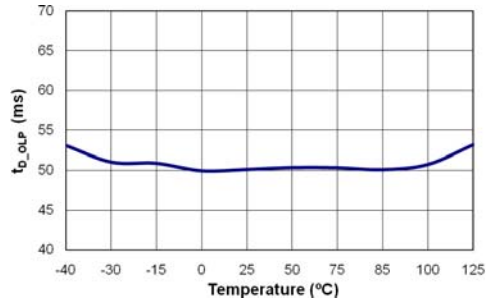


Figure 17. Delay of FB Pin Open-Loop Protection (t<sub>D-OLP</sub>) vs. Temperature

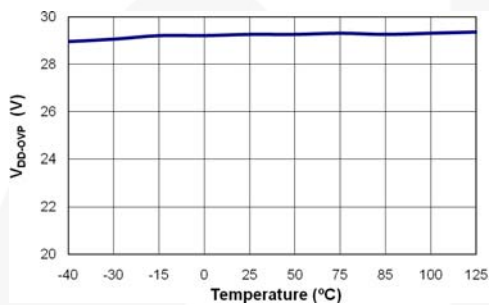


Figure 18. V<sub>DD</sub> Over-Voltage Protection (V<sub>DD-OVP</sub>) vs. Temperature

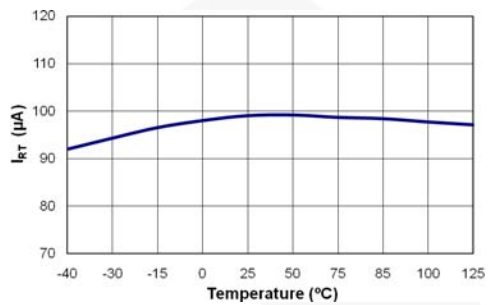


Figure 19. Output Current from RT Pin (I<sub>RT</sub>) vs. Temperature

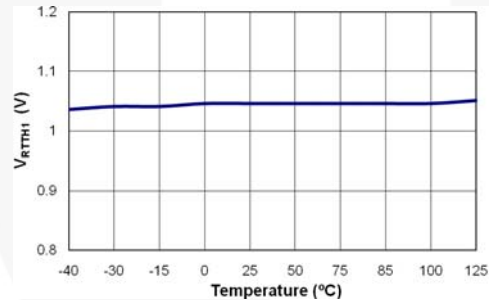


Figure 20. Over-Temperature Protection Threshold Voltage (V<sub>RTTH1</sub>) vs. Temperature

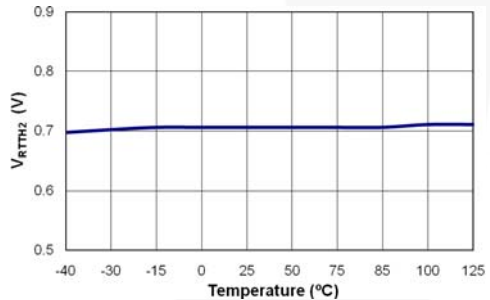


Figure 21. Over-Temperature Protection Threshold Voltage (V<sub>RTTH2</sub>) vs. Temperature

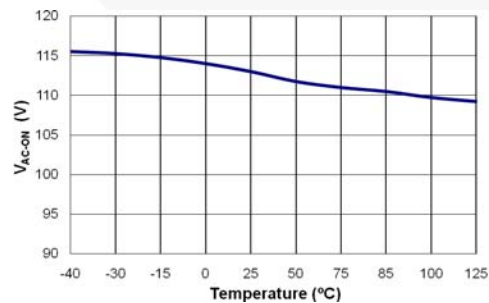


Figure 22. Brown-in (V<sub>AC-ON</sub>) vs. Temperature

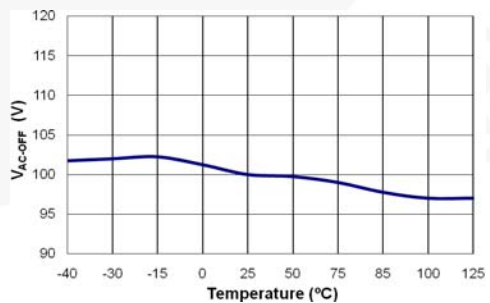


Figure 23. Brown-out (V<sub>AC-OFF</sub>) vs. Temperature

## Functional Description

### Current Mode Control

FAN6749 employs peak current mode control, as shown in Figure 24. An opto-coupler (such as the H11A817A) and a shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the  $R_{sense}$  resistor makes it possible to control the switching duty cycle. The built-in slope compensation stabilizes the current loop and prevents sub-harmonic oscillation.

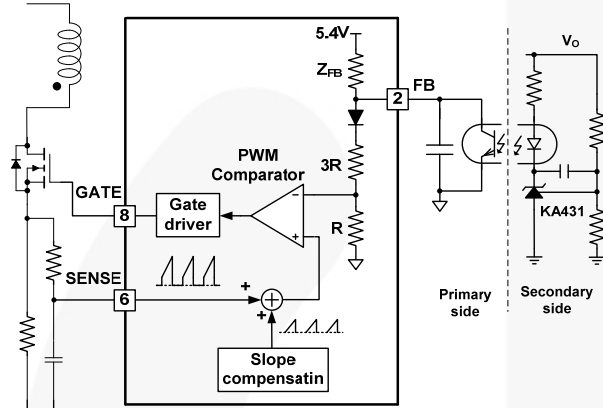


Figure 24. Current Mode Control Circuit Diagram

### Green-Mode Operation

FAN6749 modulates the PWM frequency as a function of the FB voltage to improve the medium- and light-load efficiency, as shown in Figure 25. Since the output power is proportional to the FB voltage in current mode control, the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is fixed at 65 kHz. Once  $V_{FB}$  decreases below  $V_{FB-N}$  (2.7 V), the PWM frequency starts linearly decreasing from 65 kHz to 24 kHz to reduce switching losses. As  $V_{FB}$  drops to  $V_{FB-G}$  (2.25 V), where switching frequency is decreased to 24 kHz, the switching frequency is fixed to avoid acoustic noise.

When  $V_{FB}$  falls below  $V_{FB-ZDC}$  (2.0 V) as load decreases further, FAN6749 enters Burst Mode, where PWM switching is disabled. Then the output voltage starts to drop, causing the feedback voltage to rise. Once  $V_{FB}$  rises above  $V_{FB-ZDCR}$  (2.1 V), switching resumes. Burst Mode alternately enables and disables switching, thereby reducing switching loss for lower power consumption, as shown in Figure 26

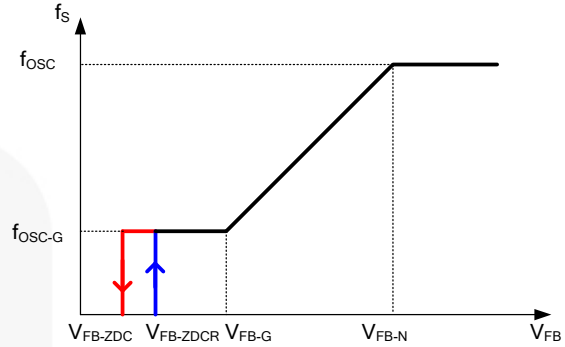


Figure 25.  $V_{FB}$  vs. PWM Frequency

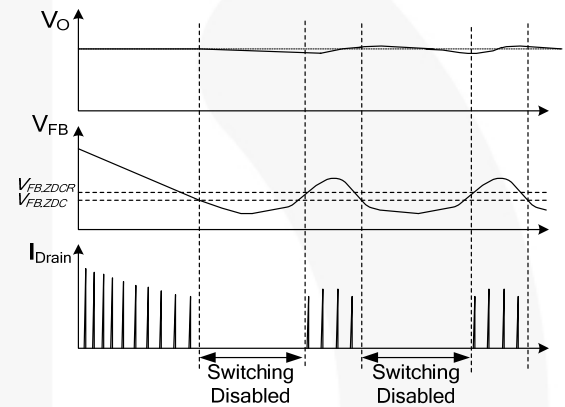


Figure 26. Burst Switching in Green Mode

### Operating Current

In normal condition, operating current is around 1.8 mA ( $I_{DD-OP1}$ ); when  $V_{FB} < 1.4$  V, operating current is further reduced to 1 mA ( $I_{DD-OP2}$ ) by disabling several blocks of FAN6749. The low operating current improves light-load efficiency and reduces the requirement of  $V_{DD}$  hold-up capacitance.

### High-Voltage Startup and Line Sensing

The HV pin is typically connected to the AC line input through an external diode and a resistor ( $R_{HV}$ ), as shown in Figure 27. When AC line voltage is applied, the  $V_{DD}$  hold-up capacitor is charged by the line voltage through the diodes and resistor. After  $V_{DD}$  voltage reaches the turn-on threshold voltage ( $V_{DD-ON}$ ), the startup circuit charging  $V_{DD}$  capacitor is switched off and  $V_{DD}$  is supplied by the auxiliary winding of the transformer. Once FAN6749 starts up, it continues operation until  $V_{DD}$  drops below 6.5 V ( $V_{UVLO}$ ). The IC startup time with a given AC line input voltage is given as:

$$t_{STARTUP} = R_{HV} \cdot C_{DD} \cdot \ln \frac{V_{AC-IN} \cdot \frac{\sqrt{2}}{\pi}}{V_{AC-IN} \cdot \frac{\sqrt{2}}{\pi} - V_{DD-ON}} \quad (1)$$

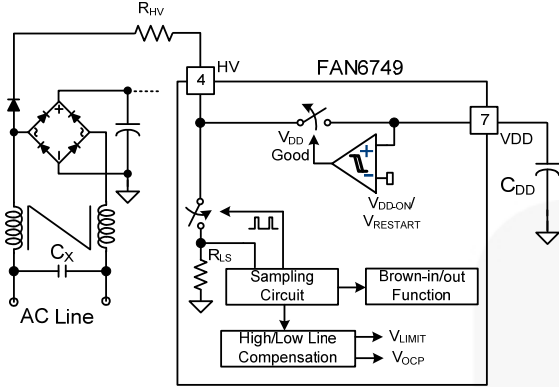


Figure 27. Startup Circuit

The HV pin detects the AC line voltage using a switched voltage divider that consists of external resistor ( $R_{HV}$ ) and internal resistor ( $R_{LS}$ ), as shown in Figure 27. The internal line-sensing circuit detects line voltage using a sampling circuit and a peak-detection circuit. Since the voltage divider causes power consumption when it is switched on, the switching is driven by a signal with a very narrow pulse width to minimize power loss. The sampling frequency is adaptively changed according to the load condition to minimize the power consumption in the light-load condition.

Based on the detected line voltage, brown-in and brown-out thresholds are determined as:

$$V_{BROWN-IN} (RMS) = \frac{R_{HV}}{200k} \cdot \frac{V_{AC-ON}}{\sqrt{2}} \quad (2)$$

$$V_{BROWN-OUT} (RMS) = \frac{R_{HV}}{200k} \cdot \frac{V_{AC-OFF}}{\sqrt{2}} \quad (3)$$

Since the internal resistor ( $R_{LS}=1.62 \text{ k}\Omega$ ) of the voltage divider is much smaller than  $R_{HV}$ , the thresholds are given as a function of  $R_{HV}$ .

Note that  $V_{DD}$  must be larger than  $V_{DD-AC}$  to start up, even though sensed line voltage satisfies Equation 2.

### High/Low Line Compensation for Constant Power Limit

FAN6749 has cycle-by-cycle current limit, as shown in Figure 28, which limits the maximum input power with a given input voltage. If the output consumes beyond this maximum power, the dropping output voltage triggers the overload protection.

As shown in Figure 28, the high/low line compensation block adjusts the current limit level,  $V_{LIMIT}$ , based on the line voltage. Figure 29 shows how the cycle-by-cycle current-limit level changes with the line voltage for different  $R_{HV}$  resistors. To maintain the constant output power limit regardless of line voltage, the cycle-by-cycle current limit level,  $V_{LIMIT}$ , decreases as line voltage increases. The current-limit level is also proportional to the  $R_{HV}$  resistor value and power limit level can be tuned using different  $R_{HV}$  resistors.

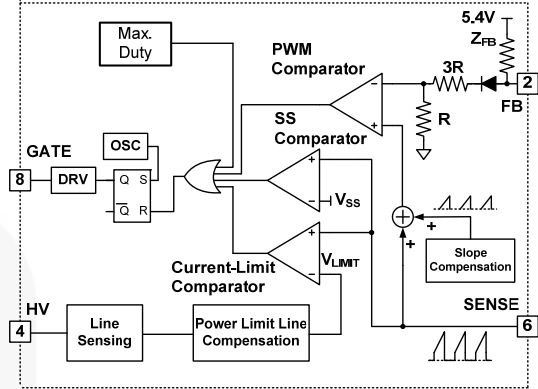


Figure 28. Cycle-by-Cycle Current-Limit Circuit

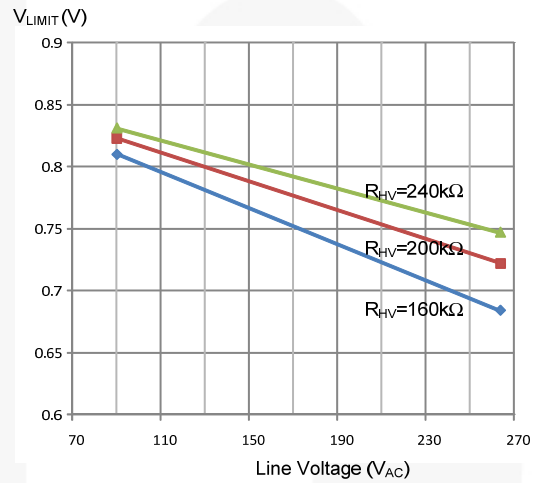


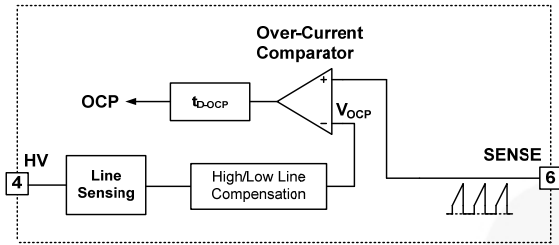
Figure 29. Current Limit vs. Line Voltage

### Two-Level Over-Current Protection (OCP)

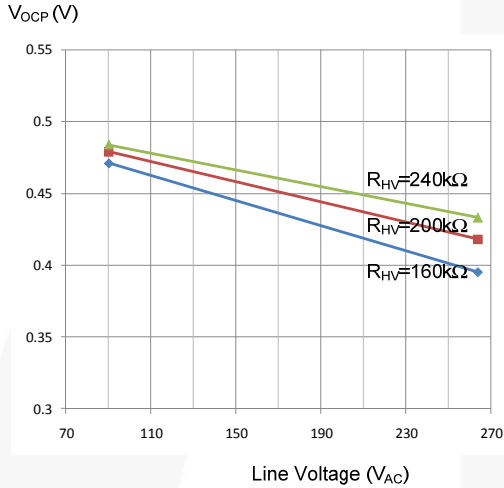
Other than cycle-by-cycle current limiting, FAN6749 applies another threshold voltage,  $V_{OCP}$ , for current sense. As shown in Figure 28, when peak of  $V_{SENSE}$  exceeds  $V_{OCP}$  at each pulse for a period of time,  $t_{D-OCP}$ ; over-current protection (OCP) is triggered. This protection is designed for applications with surge-current outputs. If a peak load is present for less than  $t_{D-OCP}$ , the controller operates as usual. If the peak load continues longer than  $t_{D-OCP}$ , GATE output is stopped to protect the converter from overload condition.

Like  $V_{LIMIT}$ , the  $V_{OCP}$  is adjusted by high/low line compensation block to maintain a constant over-current protection level, regardless of line voltage. Figure 31 shows how  $V_{OCP}$  changes with the line voltage with different  $R_{HV}$  resistors.

When OCP is triggered, it is recommended to have  $V_{FB} > V_{FB-N}$  for whole AC input range.  $V_{FB} > V_{FB-N}$  ensures switching frequency is fixed at 65 kHz. If OCP is triggered in the frequency-reduction region ( $V_{FB} < V_{FB-N}$ ), output current is reduced due to lower switching frequency. It causes the difference of OCP-triggering point between high and low AC input voltages.



**Figure 30. Over-Current Protection Circuit**



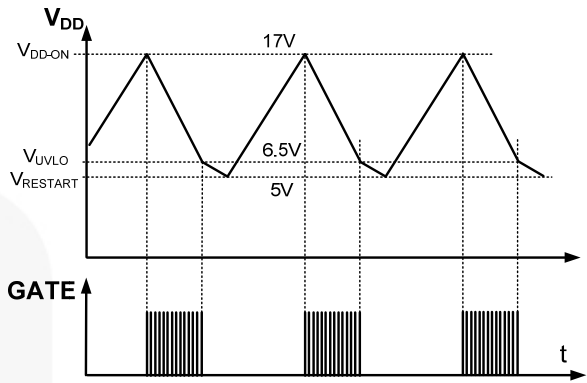
**Figure 31. V<sub>OCP</sub> vs. Line Voltage**

### Short Circuit Protection (SCP)

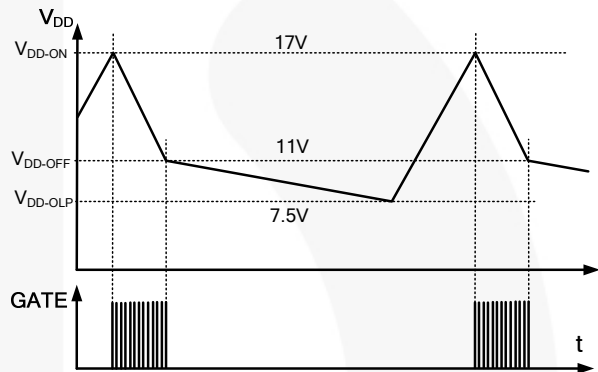
The  $V_{DD}$  voltage decreases every time the output of the power supply is shorted because the impedance at secondary windings becomes far lower than at auxiliary winding and currents choose the low-impedance path. When  $V_{FB}$  is larger than  $V_{FB-OLP}$  over a debounce time of  $t_{D-SCP}$ ; if  $V_{DD}$  is lower than  $V_{DD-SCP}$ , PWM output is latched off.

### Under-Voltage Lockout (UVLO)

As shown in Figure 32, as long as protection is not triggered, the turn-off threshold of  $V_{DD}$  is fixed internally at  $V_{UVLO}$  (6.5 V). When a protection is triggered, the  $V_{DD}$  level to terminate PWM gate switching is changed to  $V_{DD-OFF}$  (11 V), as shown in Figure 33. When  $V_{DD}$  drops below  $V_{DD-OFF}$ , the switching is terminated and the operating current from  $V_{DD}$  is reduced to  $I_{DD-OLP}$ , to slow down the discharge of  $V_{DD}$  until  $V_{DD}$  reaches  $V_{DD-OLP}$ . This delays restart after shutdown by protection to minimize the input power and voltage/current stress of switching devices during fault condition.



**Figure 32. V<sub>DD</sub> UVLO in Normal Mode**



**Figure 33. V<sub>DD</sub> UVLO in Protection Mode**

### Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs on the sense resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time,  $t_{LEB}$ , is introduced. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

### Gate Output / Soft Driving

The BiCMOS output stage has a fast totem-pole gate driver. The output driver is clamped by an internal 14.5 V Zener diode to protect power MOSFET gate from over voltage. A soft driving is implemented to minimize electromagnetic interference (EMI) by reducing the switching noise.

### V<sub>DD</sub> Over-voltage Protection (OVP)

$V_{DD}$  over-voltage protection prevents IC damage from over-voltage exceeding the IC voltage rating. When the  $V_{DD}$  voltage exceeds 29 V, the protection is triggered. This protection is typically caused by an open circuit in the secondary-side feedback network.

### Soft-Start

FAN6749 has an internal soft-start circuit that progressively increases the cycle-by-cycle current limit level of the MOSFET for 6 ms during startup to establish the correct working conditions for transformers and capacitors to operate.

### Over-Temperature Protection (OTP)

The RT pin provides adjustable Over-Temperature Protection (OTP) and an external latch-triggering function. For OTP application, an NTC thermistor,  $R_{NTC}$ , usually in series with a resistor,  $R_A$ , is connected between the RT pin and ground. The internal current source,  $I_{RT}$ , (100  $\mu$ A) introduces voltage on RT as:

$$V_{RT} = I_{RT} \cdot (R_{NTC} + R_A) \quad (4)$$

At high ambient temperature,  $R_{NTC}$  decreases, which reduces  $V_{RT}$ . When  $V_{RT}$  is lower than  $V_{RTTH1}$  (1.050 V) for longer than  $t_{D-OTP1}$  (14 ms), the protection is triggered and FAN6749 enters Latch Mode protection.

The OTP can be also triggered by pulling down the RT pin voltage using an opto-coupler or transistor. Once  $V_{RT}$  is less than  $V_{RTTH2}$  (0.7 V) for longer than  $t_{D-OTP2}$  (165  $\mu$ s), the protection is triggered and FAN6749 enters Latch Mode protection.

When  $V_{FB}$  falls below 1.9 V, the RT pin function is disabled for lower power consumption. If OTP is not used, place a 100 k $\Omega$  resistor between this pin and ground to prevent noise interference.

### Noise Immunity

Noise on the current sense or control signal may cause significant pulse-width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN6749, and increasing the power MOS gate resistance improve performance.

Physical Dimensions

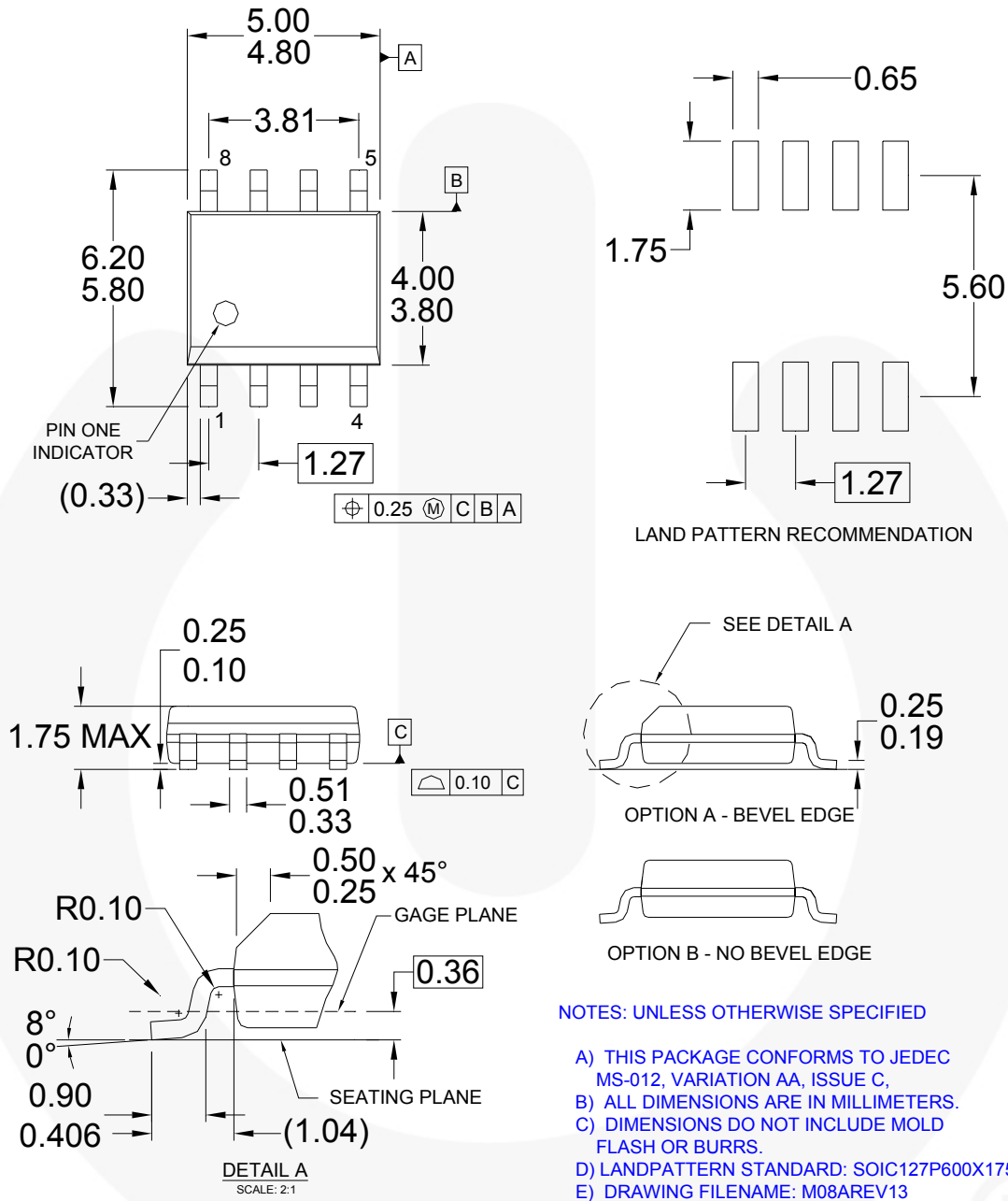


Figure 34. 8-Pin SOP-8 Package

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
<http://www.fairchildsemi.com/packaging/>.





**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |   |  |   |   |
|---|--|---|---|
| 2Cool™  | F-PFS™   | PowerTrench®  | The Power Franchise®  |
| AccuPower™  | FRFET®   | PowerXS™  | the Power Franchise®  |
| AX-CAP™*  | Global Power Resource™                         | Programmable Active Droop™  | <b>Power Franchise</b>  |
| BitSiC™   | GreenBridge™                                   | QFET®   | TinyBoost™  |
| Build it Now™   | Green FPS™                                     | QS™   | TinyBuck™   |
| CorePLUS™   | Green FPS™ e-Series™                           | Quiet Series™   | TinyCalc™   |
| CorePOWER™  | Gmax™  | RapidConfigure™   | TinyLogic®  |
| CROSSVOLT™  | GTO™   |  | TINYOPTO™   |
| CTL™  | IntelliMAX™                                    | Saving our world, 1mW/WkW at a time™  | TinyPower™  |
| Current Transfer Logic™   | ISOPLANAR™                                     | SignalWise™   | TinyPWM™  |
| DEUXPEED®   | Making Small Speakers Sound Louder and Better™ | SmartMax™   | TinyWire™   |
| Dual Cool™  | MegaBuck™                                      | SMART START™  | TransiC™  |
| EcoSPARK®   | MICROCOUPLER™                                  | Solutions for Your Success™   | TriFault Detect™  |
| EfficientMax™   | MicroFET™                                      | SPM®  | TRUECURRENT®*   |
| ESBC™   | MicroPak™                                      | STEALTH™  | µSerDes™  |
|  | MicroPak2™                                     | SuperFET®   |  |
| Fairchild®  | MillerDrive™                                   | SuperSOT™-3   | UHC®  |
| Fairchild Semiconductor®  | MotionMax™                                     | SuperSOT™-6   | Ultra FRFET™  |
| FACT Quiet Series™  | mWSaver™                                       | SuperSOT™-8   | UniFET™   |
| FACT®   | OptoHi™  | SupreMOS®   | VcX™  |
| FAST®   | OPTOLOGIC®                                     | SyncFET™  | VisualMax™  |
| FastvCore™  | OPTOPLANAR®                                    | Sync-Lock™  | VoltagePlus™  |
| FETBench™   |  |  | XS™   |
| FlashWriter®*   |  |   |   |
| FPS™  |  |   |   |

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I62

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative