

# DATA SHEET

**FBL2041**

**FBL2041I**

3.3V BTL 7-bit Futurebus+ transceiver  
(standard A-port)

Product specification  
Supersedes data of 1998 May 11  
IC23 Data Handbook

1999 Apr 27

## 3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

**FBL2041**  
**FBL2041I**

### FEATURES

- 7-bit BTL transceiver
- Separate I/O on TTL A-port
- Inverting
- Three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low  $I_{CC}$  current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack
- 5V compatible I/O on A-port
- Industrial temperature range option available as FBL2041I

### DESCRIPTION

The FBL2041/FBL2041I is a 7-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FBL2041 is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The FBL2041/FBL2041I is pin and function compatible with FB2041 but operates at a 3.3V supply voltage, greatly reducing power consumption.

The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

There are three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement. The TTL/BTL output drivers for bit 0 are enabled with  $OEA1/\overline{OEB1}$ , output drivers for bits 1–2–3 are enabled with  $OEA2/\overline{OEB2}$  and output drivers for bits 4–5–6 are enabled with  $OEA3/\overline{OEB3}$ .

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when  $OEA_n$  goes High after an extra 6ns delay which is built in to provide a break-before-make function. When  $OEA_n$  goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when  $V_{CC}$  is below 1.3V.

The B-port has an output enable,  $OEB0$ , which affects all seven drivers. When  $OEB0$  is High and  $\overline{OEBn}$  is Low the output driver will be enabled. When  $OEB0$  is Low or if  $\overline{OEBn}$  is High, the B-port drivers will be inactive and at the level of the backplane signal.

To support live insertion,  $OEB0$  is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 3.3V level while  $V_{CC}$  is Low. If live insertion is not a requirement, the BIAS V pin should be tied to a  $V_{CC}$  pin.

The LOGIC GND and BUS GND pins are isolated in the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble-shoot.

JTAG boundary scan functionality is provided as an option with signals TMS, TCK, TDI and TDO. When this option is not present, TMS and TCK are no-connects (no bond wires) and TDI and TDO are shorted together internally.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay AIn to $\overline{Bn}$	4.2 3.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay $\overline{Bn}$ to AOn	4.8 4.9	ns
$C_{OB}$	Output capacitance ( $\overline{B0}$ - $\overline{B6}$ only)	6	pF
$I_{OL}$	Output current ( $\overline{B0}$ - $\overline{B6}$ only)	100	mA
$I_{CC}$	Supply Current	Standby	5.2
		AIn to $\overline{Bn}$ (outputs Low or High)	3.2
		$\overline{Bn}$ to AOn (outputs Low)	13.5
		$\overline{Bn}$ to AOn (outputs High)	10.7

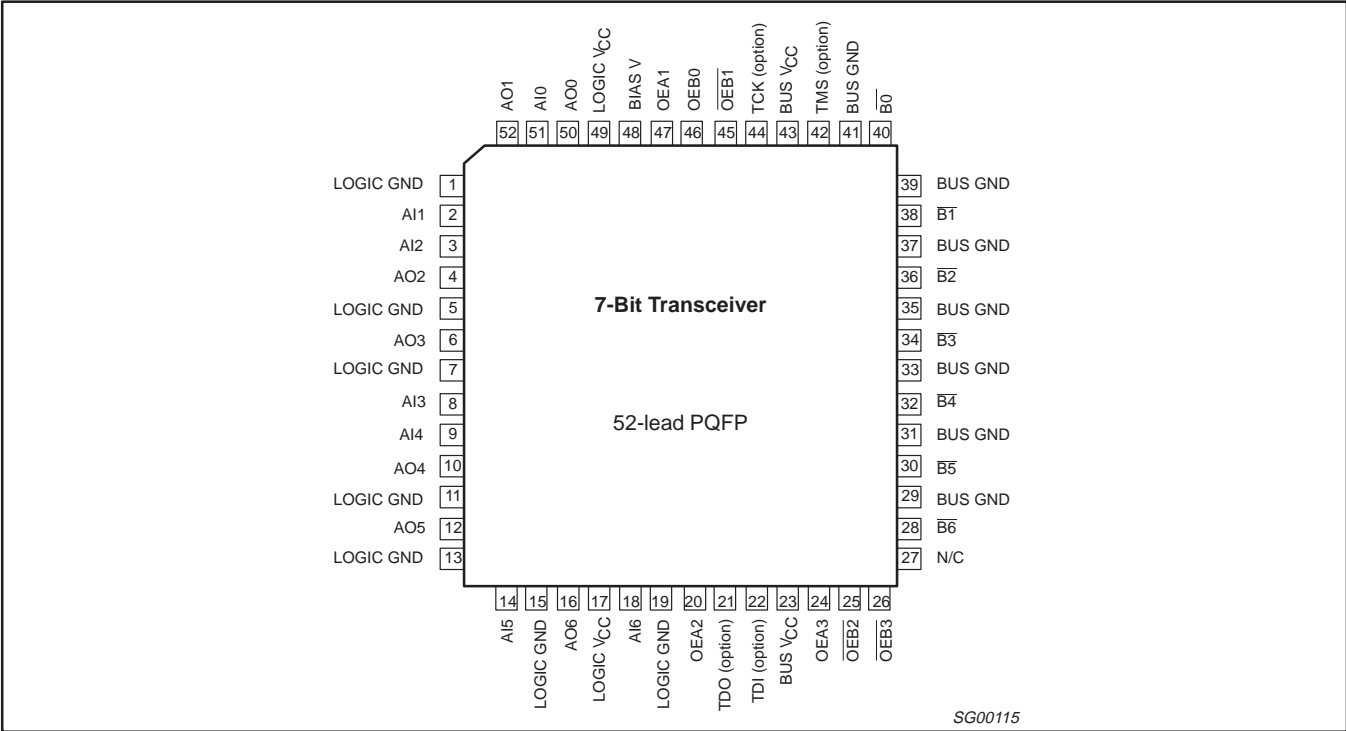
### ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE $V_{CC} = 3.3V \pm 10\%$ ; $T_{amb} = 0$ to $+70^\circ C$	INDUSTRIAL RANGE $V_{CC} = 3.3V \pm 10\%$ ; $T_{amb} = -40$ to $+85^\circ C$	DWG No.
52-pin Plastic Quad Flatpack	FBL2041 BB	FBL2041I BB	SOT379-1

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PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI6	51, 2, 3, 8, 9, 14, 18	Input	Data inputs (TTL)
AO0 – AO6	50, 52, 4, 6, 10, 12, 16	Output	3-State outputs (TTL)
$\overline{B0} - \overline{B6}$	40, 38, 36, 34, 32, 30, 28	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the Bn outputs when High
$\overline{OEB1}$	45	Input	Enables the B0 output when Low
$\overline{OEB2}$	25	Input	Enables the B1 – B3 outputs when Low
$\overline{OEB3}$	26	Input	Enables the B4 – B6 outputs when Low
OEA1	47	Input	Enables the A0 outputs when High
OEA2	20	Input	Enables the A1 – A3 outputs when High
OEA3	24	Input	Enables the A4 – A6 outputs when High
BUS GND	41, 39, 37, 35, 33, 31, 29	GND	Bus ground (0V)
LOGIC GND	1, 5, 7, 11, 13, 15, 19	GND	Logic ground (0V)
BUS V <sub>CC</sub>	23, 43	Power	Positive supply voltage
LOGIC V <sub>CC</sub>	17, 49	Power	Positive supply voltage BAND GAP
BIAS V	48	Power	Positive supply voltage
TMS	42	Input	Test Mode Select (no-connect)
TCK	44	Input	Test Clock (no-connect)
TDI	22	Input	Test Data In (shorted to TDO)
TDO	21	Output	Test Data Out (TDI)
N/C	27	—	Not connected

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## FUNCTION TABLE

MODE	INPUTS									OUTPUTS	
	AIn	Bn*	OEB0	OEB1	OEB2	OEB3	OEA1	OEA2	OEA3	AOn	Bn*
AIn to Bn	L	—	H	L	L	L	L	L	L	Z	H**
	H	—	H	L	L	L	L	L	L	Z	L
	L	—	H	L	L	L	H	H	H	L	H**
	H	—	H	L	L	L	H	H	H	H	L
AI0 to B0	L	—	H	L	X	X	L	L	L	Z	H**
	H	—	H	L	X	X	L	L	L	Z	L
	L	—	H	L	X	X	H	H	H	L	H**
	H	—	H	L	X	X	H	H	H	H	L
AI1 – AI3 to B1 – B3	L	—	H	X	L	X	L	L	L	Z	H**
	H	—	H	X	L	X	L	L	L	Z	L
	L	—	H	X	L	X	H	H	H	L	H**
	H	—	H	X	L	X	H	H	H	H	L
AI4 – AI6 to B4 – B6	L	—	H	X	X	L	L	L	L	Z	H**
	H	—	H	X	X	L	L	L	L	Z	L
	L	—	H	X	X	L	H	H	H	L	H**
	H	—	H	X	X	L	H	H	H	H	L
Disable Bn outputs	X	X	L	X	X	X	X	X	X	X	H**
	X	X	X	H	H	H	X	X	X	X	H**
Disable B0 outputs	X	X	H	H	X	X	X	X	X	X	H**
Disable B1 – B3 outputs	X	X	H	X	H	X	X	X	X	X	H**
Disable B4 – B6 outputs	X	X	H	X	X	H	X	X	X	X	H**
Bn to AOn	X	L	L	X	X	X	H	H	H	H	Input
	X	H	L	X	X	X	H	H	H	L	Input
	X	L	X	H	H	H	H	H	H	H	Input
	X	H	X	H	H	H	H	H	H	L	Input
B0 to AO0	X	L	L	X	X	X	H	X	X	H	Input
	X	H	L	X	X	X	H	X	X	L	Input
	X	L	X	H	H	H	H	X	X	H	Input
	X	H	X	H	H	H	H	X	X	L	Input
B1 – B3 to AO1 – AO3	X	L	L	X	X	X	X	H	X	H	Input
	X	H	L	X	X	X	X	H	X	L	Input
	X	L	X	H	H	H	X	H	X	H	Input
	X	H	X	H	H	H	X	H	X	L	Input
B4 – B6 to AO4 – AO6	X	L	L	X	X	X	X	X	H	H	Input
	X	H	L	X	X	X	X	X	H	L	Input
	X	L	X	H	H	H	X	X	H	H	Input
	X	H	X	H	H	H	X	X	H	L	Input
Disable AOn outputs	X	X	X	X	X	X	L	L	L	Z	X
Disable AO0 outputs	X	X	X	X	X	X	L	X	X	Z	X
Disable AO1 – AO3 outputs	X	X	X	X	X	X	X	L	X	Z	X
Disable AO4 – AO6 outputs	X	X	X	X	X	X	X	X	L	Z	X

## NOTES:

H = High voltage level

L = Low voltage level

X = Don't care

Z = High-impedance (OFF) state

— = Input not externally driven

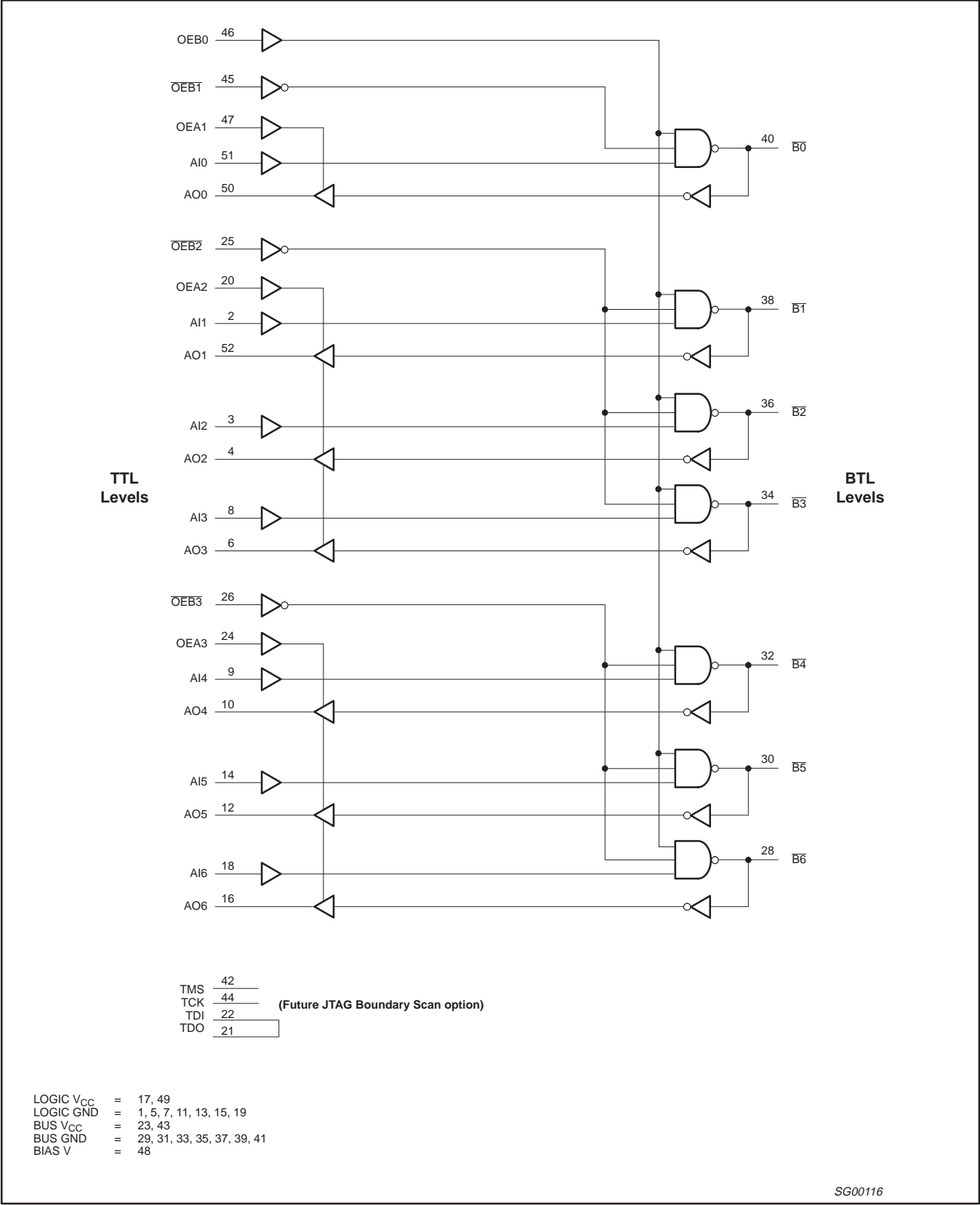
H\*\* = Goes to level of pull-up voltage

B\* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

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LOGIC DIAGRAM



## 3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

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## ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
$V_{CC}$	Supply voltage		-0.5 to +4.6	V
$V_{IN}$	Input voltage	AI0 – AI6, OEB0, $\overline{OEBn}$ , OEAn	-0.5 to +7.0	V
		$\overline{B0} - \overline{B6}$	-0.5 to +3.5	
$I_{IN}$	Input current	$V_{IN} < 0$	-50	
$V_{OUT}$	Voltage applied to output in High output state		-0.5 to +7.0	V
$I_{OUT}$	Current applied to output in Low output state/High output state	AO0 – AO6	64, -64	mA
		$\overline{B0} - \overline{B6}$	200	
$T_{STG}$	Storage temperature		-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		COMMERCIAL LIMITS $V_{CC} = 3.3V \pm 10\%$ ; $T_{amb} = 0 \text{ to } +70^\circ\text{C}$			INDUSTRIAL LIMITS $V_{CC} = 3.3V \pm 10\%$ ; $T_{amb} = -40 \text{ to } +85^\circ\text{C}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage		3.0	3.3	3.6	3.0	3.3	3.6	V
$V_{IH}$	High-level input voltage	Except $\overline{B0} - \overline{B6}$	2.0			2.0			V
		$\overline{B0} - \overline{B6}$	1.62	1.55		1.62	1.55		
$V_{IL}$	Low-level input voltage	Except $\overline{B0} - \overline{B6}$			0.8			0.8	V
		$\overline{B0} - \overline{B6}$			1.47			1.47	
$I_{IK}$	Input clamp current				-18			-18	mA
$I_{OH}$	High-level output current	AO0 – AO6			-32			-32	mA
$I_{OL}$	Low-level output current	AO0 – AO6			+32			+32	mA
		$\overline{B0} - \overline{B6}$			100			100	
$C_{OB}$	Output capacitance on B port			6	7		6	7	pF
$T_{amb}$	Operating free-air temperature range		0		+70	-40		+85	°C

## LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	TYP	MAX	
$V_{BIASV}$	Bias pin voltage	Voltage difference between the Bias voltage and $V_{CC}$ after the PCB is plugged in.	-	-	0.5	V
$I_{BIASV}$	Bias pin ( $I_{BIASV}$ ) input DC current	$V_{CC} = 0 \text{ V}$ , Bias $V = 3.6 \text{ V}$			1.2	mA
		$V_{CC} = 3.3 \text{ V}$ , Bias $V = 3.6 \text{ V}$			10	μA
$\overline{V_{Bn}}$	Bus voltage during prebias	$\overline{B0} - \overline{B8} = 0 \text{ V}$ , Bias $V = 3.3 \text{ V}$	1.62		2.1	V
$I_{LM}$	Fall current during prebias	$\overline{B0} - \overline{B8} = 2 \text{ V}$ , Bias $V = 1.3 \text{ to } 2.5 \text{ V}$			1	μA
$I_{HM}$	Rise current during prebias	$\overline{B0} - \overline{B8} = 1 \text{ V}$ , Bias $V = 3 \text{ to } 3.6 \text{ V}$	-1			μA
$\overline{I_{BnPEAK}}$	Peak bus current during insertion	$V_{CC} = 0 \text{ to } 3.3 \text{ V}$ , $\overline{B0} - \overline{B8} = 0 \text{ to } 2.0 \text{ V}$ , Bias $V = 2.7 \text{ to } 3.6 \text{ V}$ , OEB0 = 0.8V, $t_r = 2 \text{ ns}$			10	mA
$I_{OLOFF}$	Power up current	$V_{CC} = 0 \text{ to } 3.3 \text{ V}$ , OEB0 = 0.8V			100	μA
		$V_{CC} = 0 \text{ to } 1.2 \text{ V}$ , OEB0 = 0 to 5V			100	
$t_{GR}$	Input glitch rejection	$V_{CC} = 3.3 \text{ V}$	1.0	1.35		ns

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## DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT
				MIN	TYP <sup>2</sup>	MAX	
$I_{OH}$	High level output current	$\overline{B0} - \overline{B6}$	$V_{CC} = \text{MAX}$ , $V_{IL} = \text{MAX}$ , $V_{OH} = 1.9\text{V}$			100	$\mu\text{A}$
$I_{OFF}$	Power-off output current	$\overline{B0} - \overline{B6}$	$V_{CC} = 0\text{V}$ , $V_{IL} = \text{MAX}$ , $V_{OH} = 1.9\text{V}$			100	$\mu\text{A}$
			$V_{CC} = 0\text{V}$ , $V_{IL} = \text{MAX}$ , $V_{OH} = 1.9\text{V}$ @ $85^\circ\text{C}$			300	$\mu\text{A}$
$V_{OH}$	High-level output voltage	AO0 – AO6 <sup>3</sup>	$V_{CC} = \text{MIN to MAX}$ ; $I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$			V
			$V_{CC} = \text{MIN}$ ; $I_{OH} = -8\text{mA}$	2.4			V
			$V_{CC} = \text{MIN}$ ; $I_{OH} = -32\text{mA}$	2.0			V
$V_{OL}$	Low-level output voltage	AO0 – AO6 <sup>3</sup>	$V_{CC} = \text{MIN}$ ; $I_{OL} = 16\text{mA}$			0.4	V
			$V_{CC} = \text{MIN}$ ; $I_{OL} = 32\text{mA}$			0.5	V
		$\overline{B0} - \overline{B6}$	$V_{CC} = \text{MIN}$ , $I_{OL} = 4\text{mA}$	0.5			V
			$V_{CC} = \text{MIN}$ , $I_{OL} = 100\text{mA}$	0.75	1.0	1.20	V
$V_{IK}$	Input clamp voltage		$V_{CC} = \text{MIN}$ , $I_I = I_{IK} = -18\text{mA}$		-0.85	-1.2	V
$I_I$	Input leakage current	Control pins	$V_{CC} = 3.6\text{V}$ ; $V_I = V_{CC}$ or GND			$\pm 1.0$	$\mu\text{A}$
		Control/ AI0 – AI6	$V_{CC} = 0\text{V}$ or $3.6\text{V}$ ; $V_I = 5.5\text{V}$			10	
		AI0 – AI6	$V_{CC} = 3.6\text{V}$ ; $V_I = V_{CC}$			1	
		Note 4	$V_{CC} = 3.6\text{V}$ ; $V_I = 0\text{V}$			-5	
$I_{IH}$	High-level input current	$\overline{B0} - \overline{B6}$	$V_{CC} = \text{MAX}$ , $V_I = 1.9\text{V}$			100	$\mu\text{A}$
			$V_{CC} = \text{MAX}$ , $V_I = 3.5\text{V}$ , note 5	100			$\text{mA}$
			$V_{CC} = \text{MAX}$ ; $V_I = 3.75\text{V}$ @ $-40^\circ\text{C}$	100			$\text{mA}$
$I_{IL}$	Low-level input current	$\overline{B0} - \overline{B6}$	$V_{CC} = \text{MAX}$ , $V_I = 0.75\text{V}$			-100	$\mu\text{A}$
$I_{OZH}$	Off-state output current	AO0 – AO6	$V_{CC} = \text{MAX}$ , $V_O = 3\text{V}$			5	$\mu\text{A}$
$I_{OZL}$	Off-state output current	AO0 – AO6	$V_{CC} = \text{MAX}$ , $V_O = 0.5\text{V}$			-5	$\mu\text{A}$
$I_{CC}$	Supply current (total)	$I_{CCZ}$	$V_{CC} = \text{MAX}$		5.2	13.5	$\text{mA}$
		$I_{CCB}$	$V_{CC} = \text{MAX}$ , outputs Low or High		3.2	9.0	
		$I_{CCL}$	$V_{CC} = \text{MAX}$ , outputs Low		13.5	19.5	
		$I_{CCH}$	$V_{CC} = \text{MAX}$ , outputs High		10.7	16.0	

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
- All typical values are at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^\circ\text{C}$ .
- Due to test equipment limitations, actual test conditions are  $V_{IH} = 1.8\text{V}$  and  $V_{IL} = 1.3\text{V}$  for the B side.
- Unused pins are at  $V_{CC}$  or GND.
- For B port input voltage between 3 and 5 volt;  $I_{IH}$  will be greater than 100mA but the part will continue to function normally (clamping circuit is active).

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS								UNIT
			$T_{amb} = +25^{\circ}\text{C}$ , $V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pf}$ , $R_L = 500\Omega$			FBL2041 COMMERCIAL		FBL2041I INDUSTRIAL			
						$T_{amb} = 0 \text{ to } +70^{\circ}\text{C}$ , $V_{CC} = 3.3\text{V}\pm 10\%$ , $C_L = 50\text{pF}$ , $R_L = 500\Omega$		$T_{amb} = -40 \text{ to } +85^{\circ}\text{C}$ , $V_{CC} = 3.3\text{V}\pm 10\%$ , $C_L = 50\text{pF}$ , $R_L = 500\Omega$			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
$t_{PLH}$ $t_{PHL}$	Propagation delay, $\overline{Bn}$ to AOn	Waveform 1, 2	3.9 4.0	4.8 4.9	5.8 6.0	3.7 3.8	6.4 6.7	2.8 2.7	6.9 7.0	ns	
$t_{PZH}$ $t_{PZL}$	Output enable time, OEA to AOn	Waveform 4, 5	5.3 2.4	6.6 4.4	8.0 8.0	5.0 2.1	8.6 8.5	4.5 1.1	9.0 9.0	ns	
$t_{PHZ}$ $t_{PLZ}$	Output disable time, OEA to AOn	Waveform 4, 5	3.5 2.3	4.8 3.1	6.0 3.9	3.4 2.2	6.5 4.3	2.7 1.4	7.0 4.7	ns	
$t_{TLH}$ $t_{THL}$	Transition time, AOn Port (10% to 90% or 90% to 10%)	Test Circuit and Waveforms	0.7 0.5	1.8 1.6	3.0 2.0	0.7 0.5	3.0 2.0	0.7 0.5	3.0 2.0	ns	
$t_{SK(o)}$	Output skew between receivers in same package <sup>1</sup>	Waveform 3		0.7	1.5		1.5		1.5	ns	
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS								UNIT
			$T_{amb} = +25^{\circ}\text{C}$ , $V_{CC} = 3.3\text{V}$ , $C_D = 30\text{pF}$ , $R_U = 9\Omega$			$T_{amb} = 0 \text{ to } +70^{\circ}\text{C}$ , $V_{CC} = 3.3\text{V}\pm 10\%$ , $C_D = 30\text{pF}$ , $R_U = 9\Omega$		$T_{amb} = -40 \text{ to } +85^{\circ}\text{C}$ , $V_{CC} = 3.3\text{V}\pm 10\%$ , $C_D = 30\text{pF}$ , $R_U = 9\Omega$			
$t_{PLH}$ $t_{PHL}$	Propagation delay, $A_{In}$ to $\overline{Bn}$	Waveform 1, 2	3.3 2.7	4.2 3.5	5.2 4.5	2.9 2.5	6.0 5.0	1.8 1.7	6.7 5.6	ns	
$t_{PLH}$ $t_{PHL}$	Enable/disable time, $OEB_0$ to $\overline{Bn}$	Waveform 2	4.0 3.4	4.9 4.3	5.8 5.3	3.6 3.1	6.6 6.0	2.8 2.5	7.1 6.4	ns	
$t_{PLH}$ $t_{PHL}$	Enable/disable time, $\overline{OEB_1}$ to $\overline{Bn}$	Waveform 1	4.2 2.9	5.1 3.8	6.1 4.7	3.9 2.6	6.9 5.5	2.9 1.9	7.3 6.0	ns	
$t_{TLH}$ $t_{THL}$	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.2 0.4	2.4 0.9	3.0 1.5	1.2 0.4	3.0 1.5	1.2 0.4	3.0 1.5	ns	
$t_{SK(o)}$	Output skew between drivers in same package <sup>1</sup>	Waveform 3			1.5		1.5		1.5	ns	
SYMBOL	PARAMETER	TEST CONDITION	$R_U = 16.5\Omega$			$R_U = 16.5\Omega$		$R_U = 16.5\Omega$		UNIT	
$t_{PLH}$ $t_{PHL}$	Propagation delay, $A_{In}$ to $\overline{Bn}$	Waveform 1, 2	3.3 2.7	4.2 3.6	5.1 4.5	3.0 2.5	6.0 5.0	1.8 1.7	6.7 5.6	ns	
$t_{PLH}$ $t_{PHL}$	Enable/disable time, $OEB_0$ to $\overline{Bn}$	Waveform 2	4.0 3.4	4.9 4.3	5.8 5.3	3.6 3.1	6.6 6.0	2.7 2.5	7.1 6.4	ns	
$t_{PLH}$ $t_{PHL}$	Enable/disable time, $\overline{OEB_1}$ to $\overline{Bn}$	Waveform 1	4.2 2.9	5.1 3.8	6.1 4.7	3.9 2.6	6.8 5.5	3.0 1.9	7.3 6.0	ns	
$t_{TLH}$ $t_{THL}$	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.2 0.4	2.4 0.9	3.0 1.5	1.2 0.4	3.0 1.5	1.2 0.4	3.0 1.5	ns	
$t_{SK(o)}$	Output skew between drivers in same package <sup>1</sup>	Waveform 3			1.5		1.5		1.5	ns	

## NOTES:

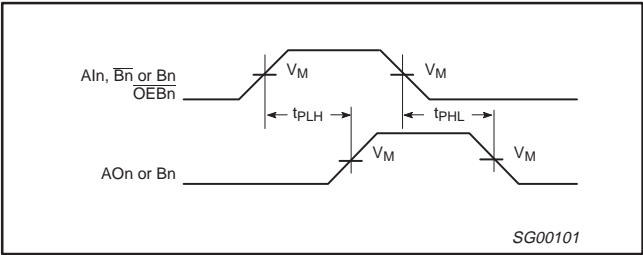
- $|t_{PNactual} - t_{PMactual}|$  for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature,  $V_{CC}$ , loading, etc.).



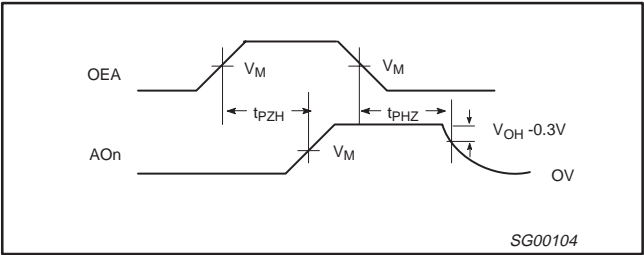
3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL2041  
FBL2041I

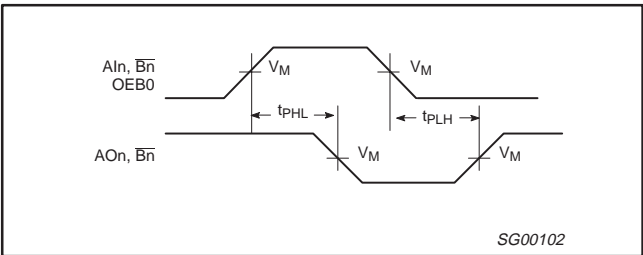
**AC WAVEFORMS**  
 $V_M = 1.55V$  for  $\overline{Bn}$ ,  $V_M = 1.5V$  for all others.



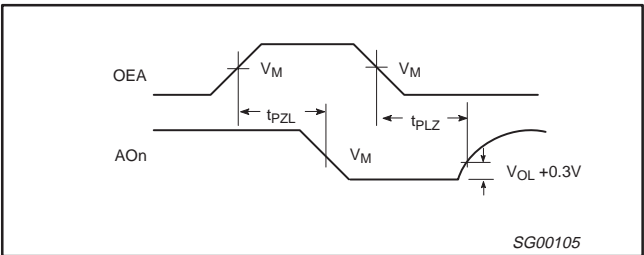
**Waveform 1.** Propagation Delay for Data or Output Enable to Output



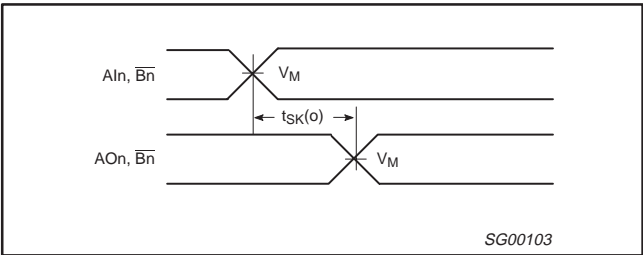
**Waveform 4.** 3-State Output Enable Time to High Level and Output Disable Time from High Level



**Waveform 2.** Propagation Delay for Data or Output Enable to Output



**Waveform 5.** 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

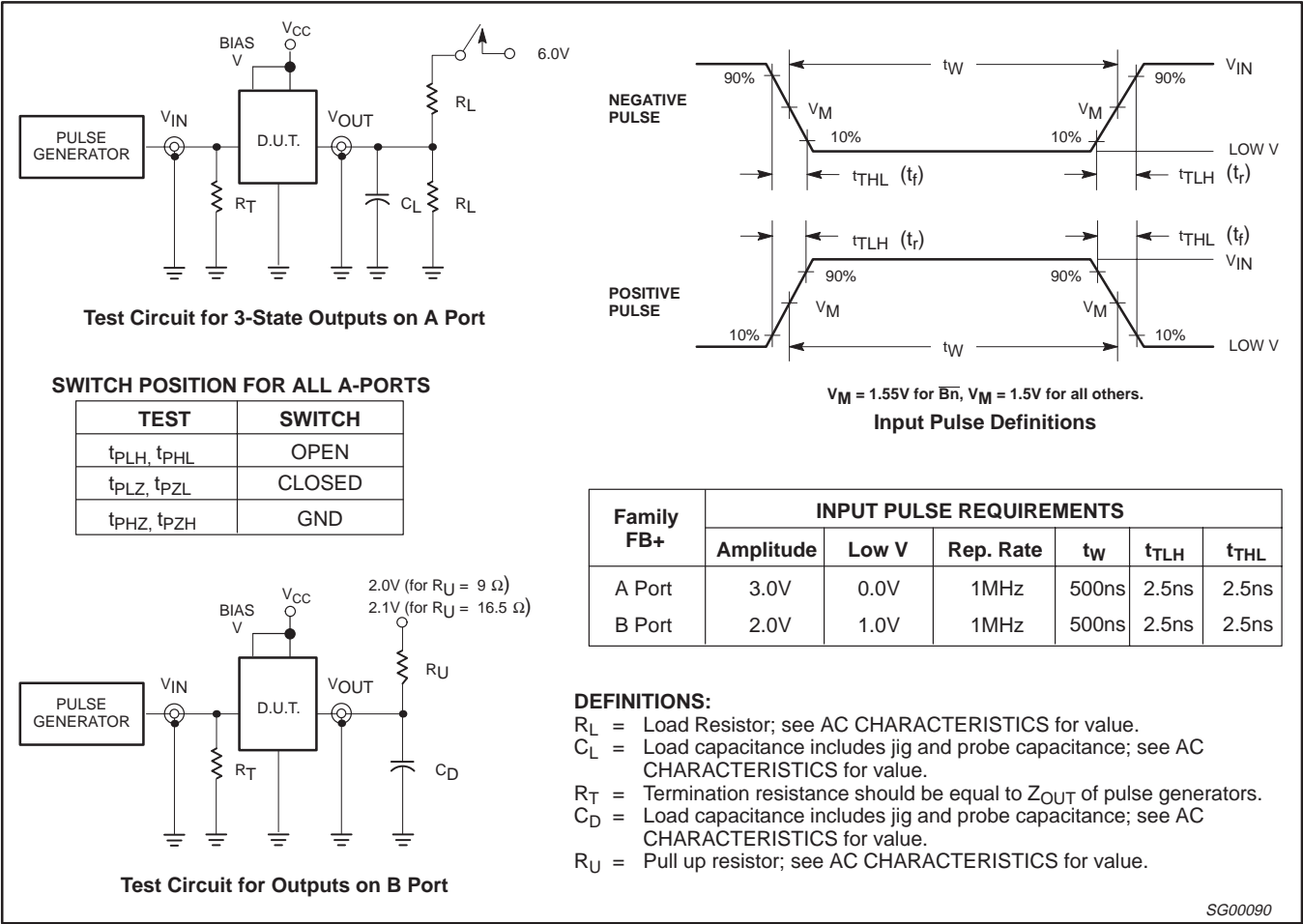


**Waveform 3.** Output Skews

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL2041  
FBL2041I

TEST CIRCUIT AND WAVEFORMS



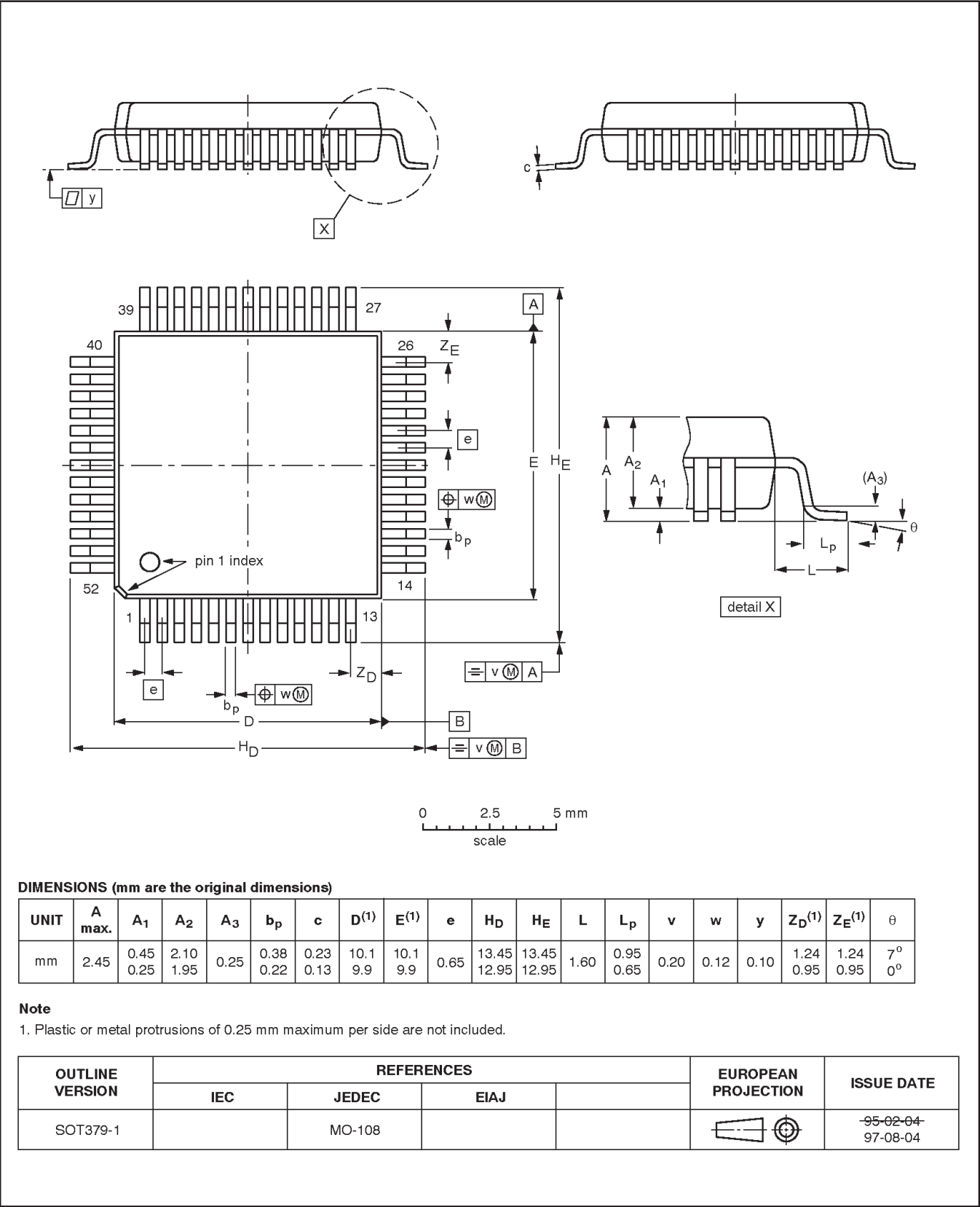
SG00090

3.3V BTL 7-bit Futurebus+ transceiver (standard A port)

FBL2041  
FBL2041I

QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm

SOT379-1



## 3.3V BTL 7-bit Futurebus+ transceiver (standard A port)

FBL2041  
FBL2041I

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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