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WL-CSP
(Wafer Level Chip Size Package)
Application Notes

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■ Applicable Products of this Application Note

The purpose of this Application Note is to provide important notes and a better understanding of mounting Wafer Level CSP's, and is not a guarantee of a perfect SMT assembly result. Needless to say, the results may differ depending on the machine capability, atmosphere, material , etc.,, but these notes should help in means of limiting any unexpected failures. Applicable products for this document is as listed below. For any product not listed, kindly contact your local sales office or send an inquiry through our URL stated on the last page. Before proceeding to the context, please confirm the Package Code corresponding with your product in interest.

Category	Package Code	Applicable Product
Schottky Barrier Diode (SBD)	(DCSP0402010-N1)	-
	DCSP0603010-N1	DB2L32300L, *DB2L32400L, *DB2L21100L *DB2L21200L,*DB2L10300L, *DB2L10400L
	DCSP1006020-N1	DB2G41000L
	(DCSP1006020-N2)	-
	(DCSP1006010-N1)	-
Zener Diode (ZND)	(DCSP0402010-N1)	-
	DCSP0603010-N1	-
	DCSP1006020-N1	-
	(DCSP1006020-N2)	-
	(DCSP1006010-N1)	-
MOSFET	(ALGA004-W-0606-RA)	-
	XLGA004-W-0808-RA	FK4B01100L, *FJ4B01100L
	ULGA004-W-1010-RA	*FK4B01120L, *FJ4B01120L
	ULGA004-W-1212	FC4B21080L
	MLGA006-W-1726-RA	FC6B22090L, FC6B22100L
	MLGA006-W-1727-RA	FC6B21100L, FC6B21230L

*1 Package codes in ( ) are currently undergoing development, therefore all related information is strictly for reference

*2 Products marked with * indicates new product under development as of July 12, 2013, but the recommended condition included in this application note is applicable.

*3 ZND includes Voltage Regulator Diodes, Surge Protection Diodes, and Transient Voltage Suppressor (TVS) diodes. As of July 2013, no ZND in these packages have been commercially released.

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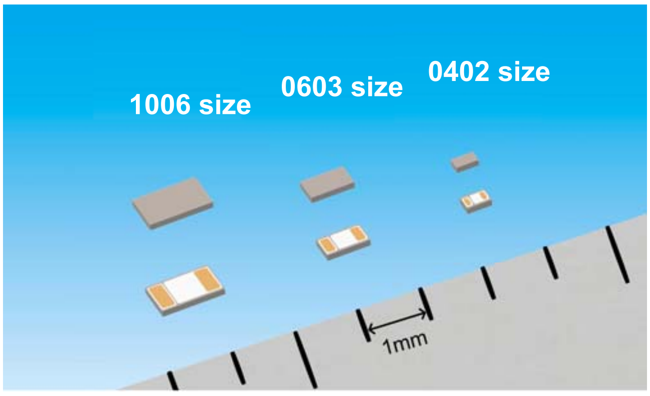
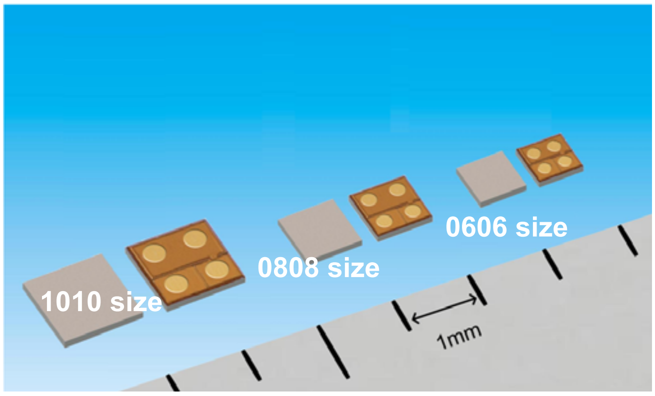
■ **Section 1 Preface**

1.1 Introduction

In recent years, as represented by Smart Phones and tablet PCs, mobile electronic products are constantly improving with more functions and applications squeezed into thin, compact and lightweight designs. Such features mean all components also need to enhance their performance as well as downsizing.



WL-CSP Diode Series



WL-CSP Single Type MOSFET Series

In order to respond to these needs, PANASONIC introduced a dual type MOSFET in a Wafer-Level Chip-Size Package (hereafter WL-CSP) in 2011, specifically for Lithium-Ion battery protection purposes, in Smart Phones. Starting from a 1.67mm square WL-CSP in a Ball Grid Array (hereafter BGA) form, PANASONIC continued with a 1.11mm square WL-CSP in a Land Grid Array (hereafter LGA) form, where the know-how and technology was later utilized to the developments of 0808 (0.8mm square) size single-type MOSFETs, for load switch purposes. Coming in October 2013, 1010 (1.0mm square) size will also be released. This Technology was also transferred to developments of Diodes, such as Schottky Barrier Diodes (hereafter SBD) and Zener Diodes (hereafter ZND) announcing products in industry leading 1006 and 0603 sizes.

Panasonic is further planning to introduce the industry's smallest size WL-CSP such as 0606 size for MOSFETs, and 0402 size for Diodes within the 2013 fiscal year. PANASONIC aims to contribute through their cut-edge chip process technology to support customer applications that continue to evolve “smaller” and “better”.

In general, it can be said that smaller devices, therefore narrower pitches of leads/pads, would require even more high-tech mounting technology to get a sufficient bonding or junction. Based on PANASONIC’s vast know-how and experience of board mounting, this application note has been compiled to support PCB designing such as solder stencils and land patterns to help improve and maintain assembly productivity and reliability.

*The design examples and recommendations stated in this application note are for reference and may/will need adjustments, depending on the environment/equipment of the assembly line.

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1.2 Features of WL-CSP

WL-CSP offers three major advantages in comparison to conventional mold packages. The First advantage is that WL-CSP increases the device/function ratio per the semiconductor size/area, resulting in an overall improvement in performance. A molded type package consists of four basic components, a semiconductor chip, mold resin, metal wires, and the lead frame. These components are designed to build up a semiconductor according to design rules that require a minimal amount of assembly process tolerance. For this reason, despite the fact that the chip size determines the performance of the device, molded products naturally have a limit in comparison to a WL-CSP type product with the same size. Needless to say, since a WL-CSP consists of only a semiconductor chip, and no excess components, it can maximize the size/area for better performance. Ultimately, this means the user has a choice of either using a better device with the same size, or using a smaller device with the same performance by choosing a WL-CSP type product.

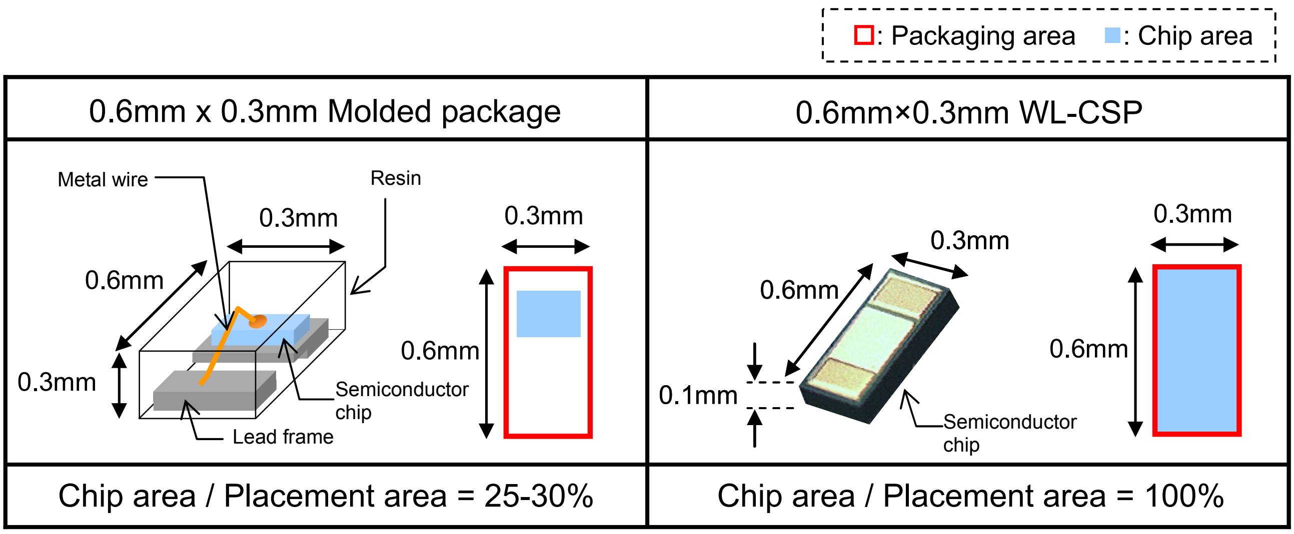

Figure 1: Internal structure of a conventional package and comparison of occupied area by semiconductor chip with WL-CSP

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The Second advantage is its thermal performance. Figure 2 indicates thermal resistance characteristics of a mold package type SBD and WL-CSP type SBD, both in 0603 size. All conditions such as package size, PCB board material/wiring, and voltage applications were conducted under the same conditions. Figure 2 shows that because the WL-CSP type has better thermal resistance characteristics, the heat dissipation is superior throughout the ultra-short pulse range to the saturation range. Figure 3 shows the difference in heat distribution for both package types, under the same IF=0.5A condition.

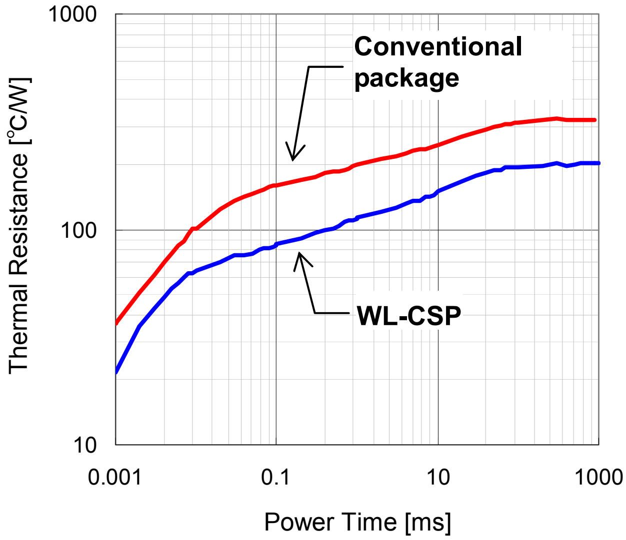

Figure 2: Comparison of thermal resistance between conventional package and WL-CSP

Semiconductor suppliers will always have to work with 1) the package, to improve thermal performance, and 2) the semiconductor chip, to improve the performance and reduce heat generation. For conventional mold type packages, it can be seen in Figure 3 that although the leadframe with the semiconductor chip distributes the heat to the PCB, the other lead frame without the chip and only wire connection, has little or no function in means of releasing heat. On the other hand, for WL-CSP, the direct source of heat is attached directly to the PCB, which enables a more efficient dissipation of heat to the board. And its' symmetrical design gives a more balanced heat generation in comparison to non-symmetrical type packages. Also as mentioned before, WL-CSP are superior to mold type packages since the size of the device is maximized, and directly results to less power consumption. This provides a more user-friendly product to all application engineers especially with thermal management concerns. To combine this with PANASONIC's ultra fine fabrication technology, it is safe to say WL-CSPs are the next generation solution for all applications.

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<table>
<tr><td rowspan="2"></td><td rowspan="2">Heat generation condition at
IF = 0.5A</td><td colspan="2">Image of heat generation/radiation</td></tr>
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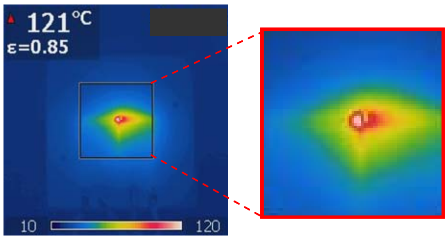
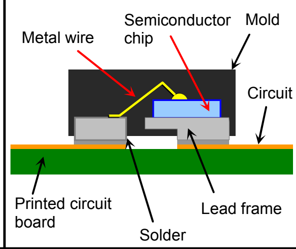
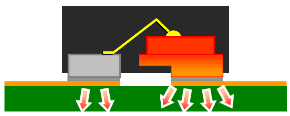
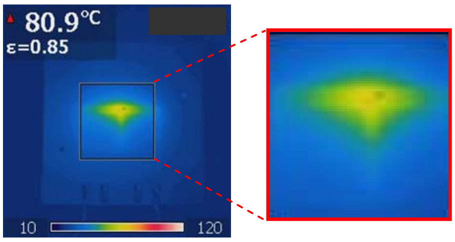
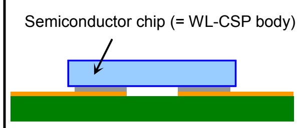
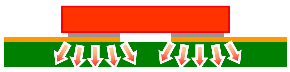
<tr><td>Mold type package</td><td></td><td></td><td></td></tr>
<tr><td>WL-CSP</td><td></td><td></td><td></td></tr>
</table>

Figure 3: Comparison of heat generation/dissipation between conventional packages and WL-CSPs

*Circuit board used for experiment is FR4 material in size 25.4mm × 25.4mm × 1.0mmt with copper foil 108mm^2, 36μmt

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■ Section 2 Panasonic WL-CSP Package Sizes and Pad Designs

This section presents the lineup of Panasonic WL-CSP and pad layout for each package. Table 1 presents WL-CSP diode packages, and Table 2 presents WL-CSP MOSFET packages.

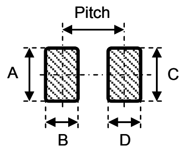
Package Code	Pin count	Pin type	Outline size [mm]			Pad design [mm]					Pad layout
			X	Y	Z	Pitch	A	B	C	D	
DCSP0402010-N1	2	LGA	0.4	0.2	0.1	0.265	0.125	0.06	0.125	0.06	
DCSP0603010-N1	2	LGA	0.6	0.3	0.1	0.4	0.215	0.115	0.215	0.115	
DCSP1006020-N1	2	LGA	1.0	0.6	0.2	0.57	0.39	0.32	0.5	0.23	
DCSP1006020-N2	2	LGA	1.0	0.6	0.2	0.66	0.47	0.21	0.47	0.21	
DCSP1006010-N1	2	LGA	1.0	0.6	0.1						

Table 1: WL-CSP Diode series package lineup and pad layout

*Note: **DCSP0402010-N1, DCSP1006020-N2, DCSP1006010-N1** are under development as of July 2013.

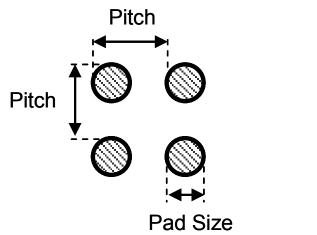
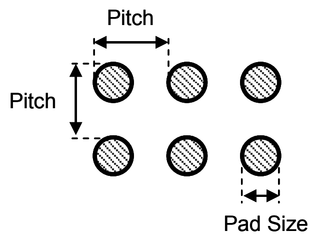
Package Code	Pin count	Pin type	Outline size [mm]			Pad design [mm]		Pad layout
			X	Y	Z	Pitch	Pad Size	
ALGA004-W-0606-RA	4	LGA	0.6	0.6	0.1	0.3	0.15	
XLGA004-W-0808-RA	4	LGA	0.8	0.8	0.1	0.4	0.2	
ULGA004-W-1010-RA	4	LGA	1.0	1.0	0.1	0.5	0.25	
ULGA004-W-1212	4	LGA	1.11	1.11	0.1			
MLGA006-W-1726-RA	6	LGA	2.56	1.67	0.1	0.65	0.3	
MLGA006-W-1727-RA	6	LGA	2.67	1.67	0.1			

Table 2: WL-CSP MOSFET series package lineup and pad layout

*Note: **ALGA004-W-0606-RA** is under development as of July 2013.

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■ Section 3 Notes for PCB Designs

In this section, we would like to provide an overview of, (1) Solder Resist designs, (2) Land Pattern designs, and (3) Solder Stencil designs.

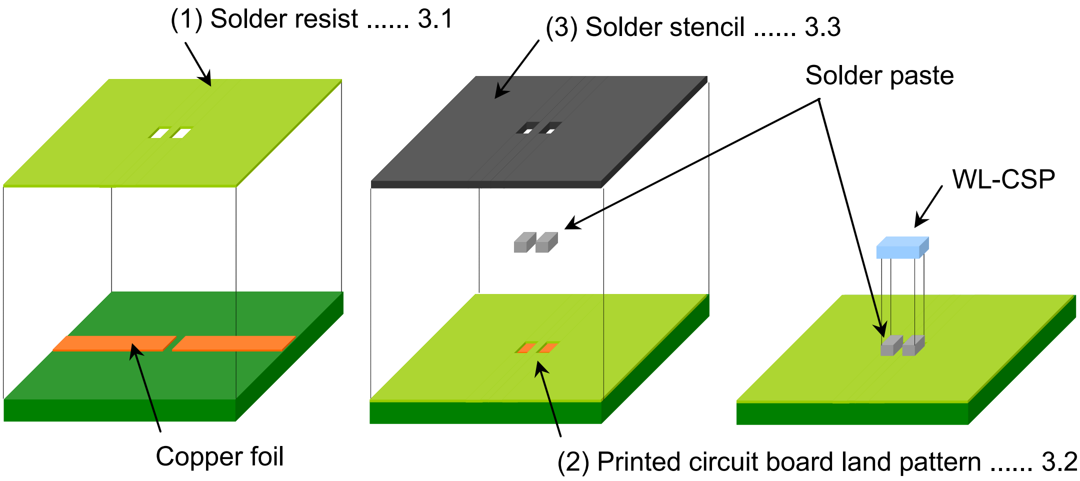

Figure 4: Materials used for circuit manufacturing

3.1 Solder Resist Designing

There are two types of solder resist designing. Solder Mask Defined (SMD) and Non Solder Mask Defined (NSMD). As shown in Figure 5, SMD is a method of designing the solder resist to partially overlap the wiring pattern of the PCB, whereas for NSMD designs have space between the solder resist and the wiring pattern of the PCB.

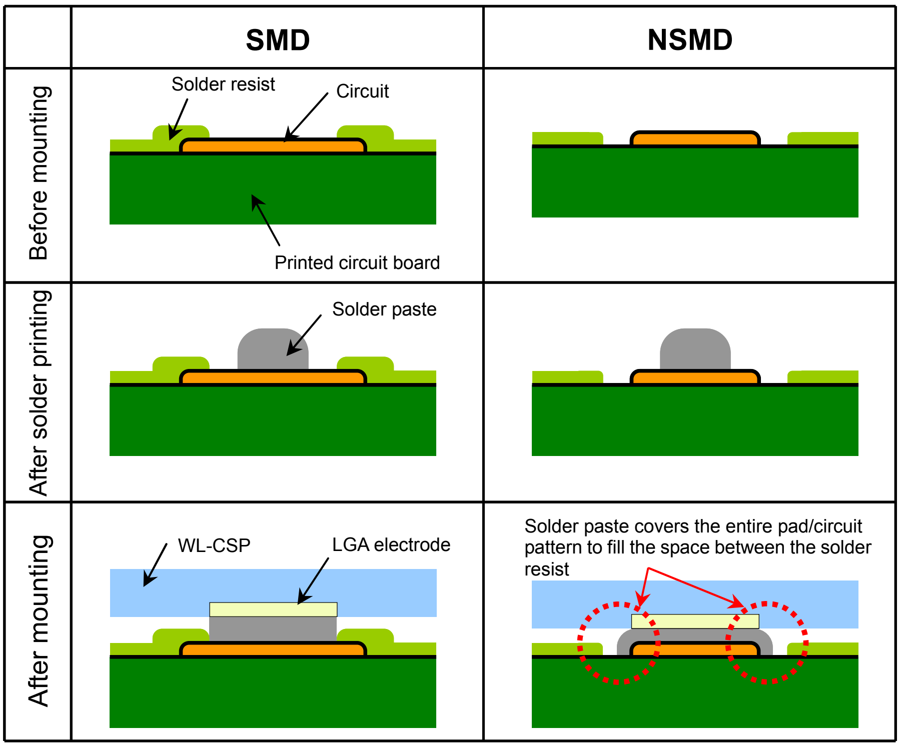

Figure 5: Comparison of SMD and NSMD

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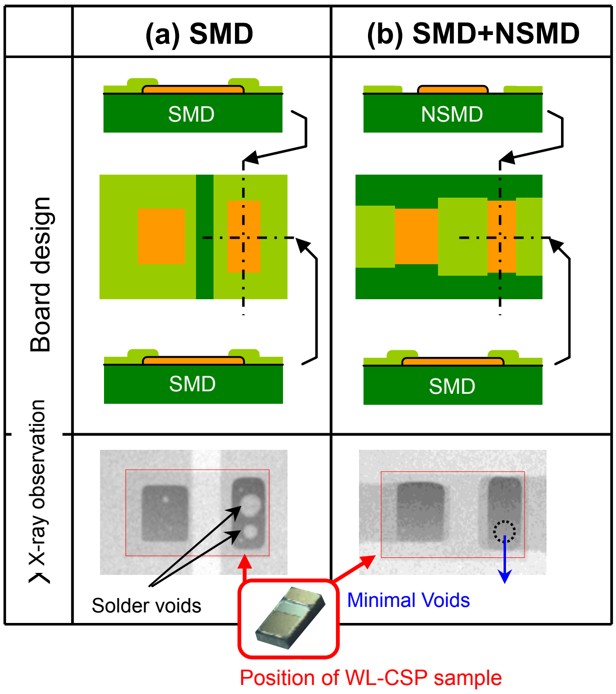

Figure 6: Comparison of solder resist designs

NSMD type solder resist allows the solder paste to cover the entire pad/circuit pattern of the PCB, making the solder joint stronger and temperature life cycle longer in comparison to SMD designs.
Figure 6 shows a comparison of the difference of void generation between the two methods. (a) A PCB with SMD type solder resist design covering each pad, and (b) A PCB with SMD type design on two sides, and NSMD type design on to the other two sides of the pad. Both were observed under conditions to generate voids intentionally (*1). Board (b), which combines SMD and NSMD methods, keeps open space between the pad/circuit pattern and allows flux gas, which in general is the main cause of voids, to escape, thereby reducing the percentage of solder void to occur, whereas SMD designs tend to trap flux gas in the solder to increase the possibilities of voids.
However for NSMD designs, uncovered portions of the pad/circuit, especially edges or corners, at the "neck" tend to peel off easier due to mechanical stress. Therefore, the PCB designer must consider both pros and cons upon designing the pattern and apply the more appropriate solder resist type according to the target application and board design.

*1: Refer to Section 5 for solder void.

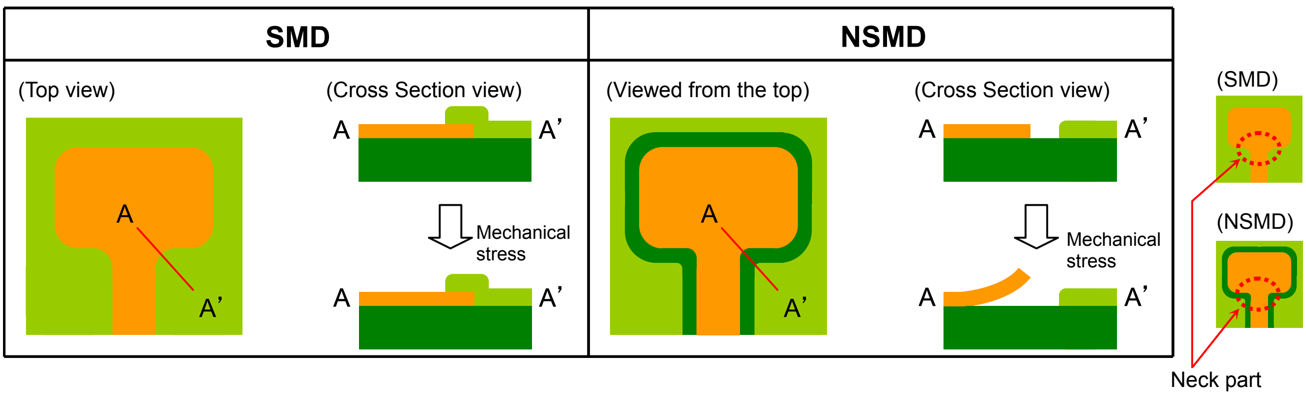

Figure 7: Pad/Circuit peeling

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3.2 Land Pattern Designing

All WL-CSP with pins on the bottom surface of the device, will require reflow soldering (*2) in order to bond to the PCB. Upon reflow soldering, some cases can be seen where the device is placed offset due to misalignment of the machine, and result in a solder joint to a position unintended. The risk of this kind of improper bonding can be reduced by designing a land pattern with a ratio of 1:1 to the pin size. By designing the land pattern this way, it will help the device self-align during the reflow soldering process and reset the position into its original or intended position. For this reason, we recommend the land pattern on the circuit board to be designed 1:1 to the device pin size.

However, when the device size gets small as a 2-pin 0603 WL-CSP (ex: DCSP0603010-N1), because of the decrease in solder joint area, the bond strength also tends to decrease. In order to maintain a certain strength, designing a pad size larger than that of the pin size should also be considered. It should also be noted that because self-alignment occurs by the surface tension of solder, the land pattern should be designed so center of the pad is aligned with the corresponding LGA pins of the device.

*2: Refer to Section 4 for reflow soldering method.

3.3 Solder Stencil Designing

Solder stencil designs are very important in obtaining a sufficient solder joint and also closely related to any unwanted solder balls (*3). Excessive solder will increase the risk of creating solder balls, and any deficiency of solder paste will result in connection failures. To prevent either defects, solder stencils need to be carefully designed to control the output amount of solder paste. PANASONIC has studied a variety of combinations of PCB's, solder stencil designs and materials, and listed in Table 3 and Figure 8 are recommendations of some combinations that have shown good results. Please refer to Table 3 for Stencil thickness recommendations, and Figure 8 for land pattern and stencil designs. These reference designs should be evaluated together with also the actual assembly environment and characteristics of the solder paste.

Package Code	Solder stencil thickness (recommendation)	Fig. 8 Ref No.
DCSP0603010-N1	**80 µm**	**#01**
DCSP1006020-N1	**100 µm**	**#02**
XLGA004-W-0808-RA	**80 µm**	**#03**
ULGA004-W-1010-RA	**100 µm**	**#04**
ULGA004-W-1212		
MLGA006-W-1726-RA	**100 µm**	**#05**
MLGA006-W-1727-RA		

Table 3: Solder stencil thickness recommendation for each type of WL-CSP

*3: Refer to Section 5 for solder balls.

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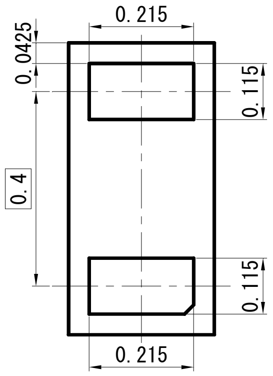
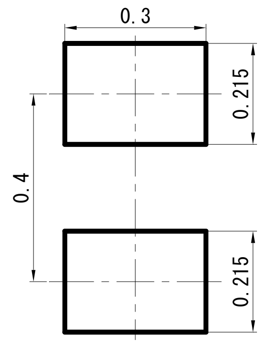
#01 DCSP0603010-N1

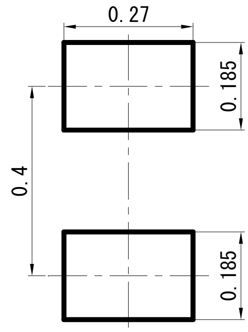
Device Outline



Land Pattern

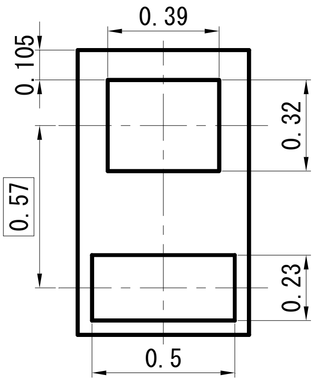


Solder Stencil Pattern

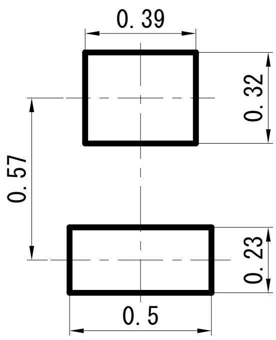


#02 DCSP1006020-N1

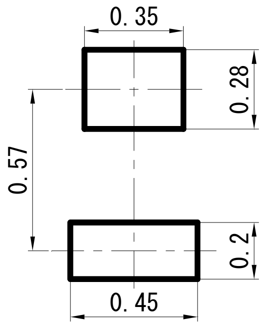
Device Outline



Land Pattern

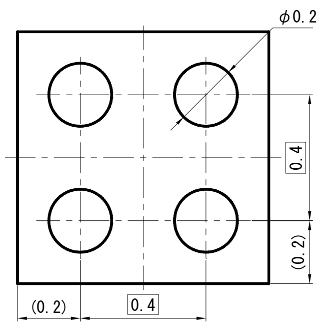


Solder Stencil Pattern

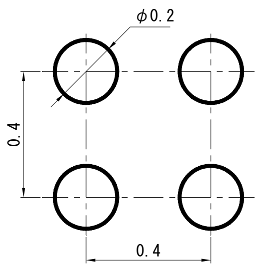


#03 XLGA004-W-0808-RA

Device Outline



Land Pattern



Solder Stencil Pattern

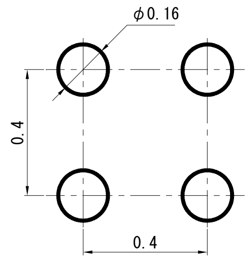


Figure 8: Design recommendations of land patterns and stencils (Unit: mm)

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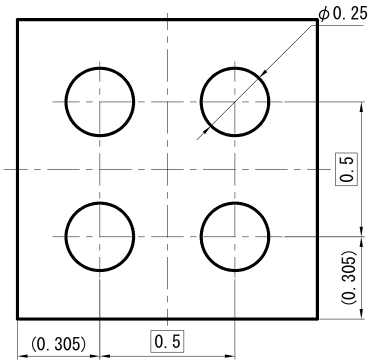
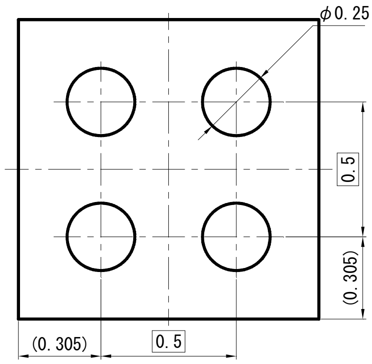
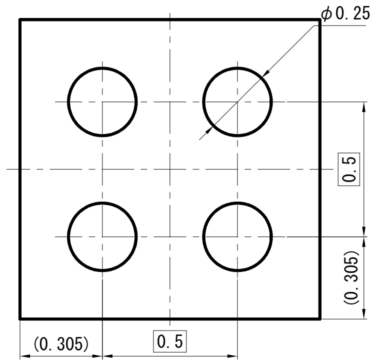
<td></td>
<td></td>
<td></td>
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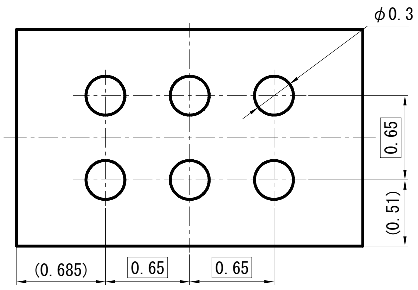
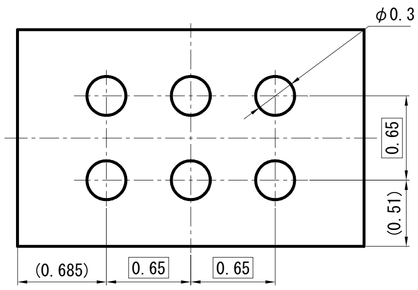
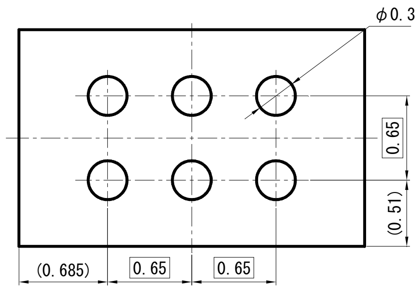
<td></td>
<td></td>
<td></td>
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<tr><td></td><td></td><td></td></tr>
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Figure 8: Design Recommendations of land patterns and stencils (Unit: mm)

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■ Section 4 PCB Mounting Conditions

This section discusses the key factors of gaining a satisfactory finish, form Solder printing to Mounting and Reflow. Figure 9 shows an overview of the said process. Please use as reference for sections 4.1 and after.

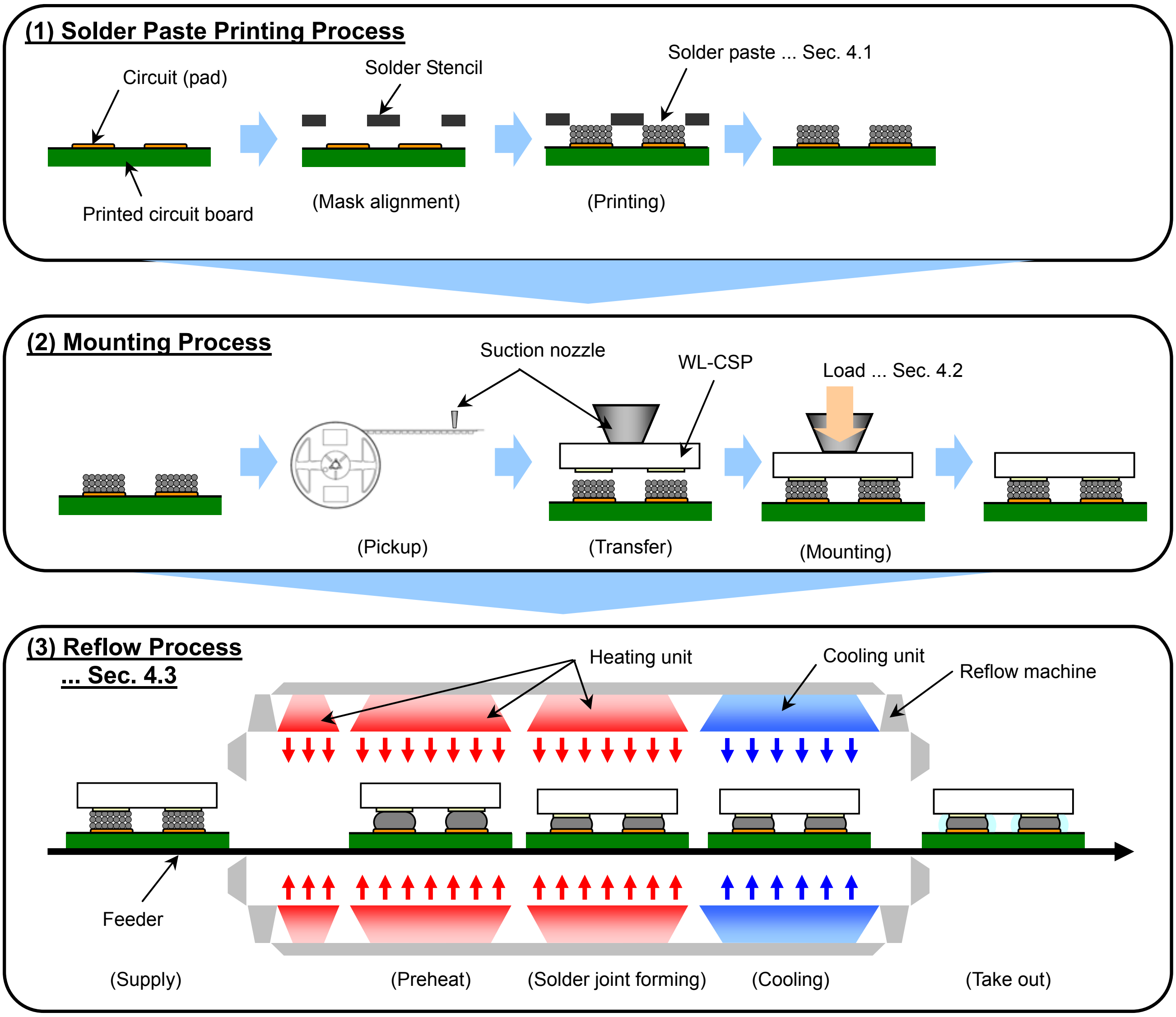

Figure 9: Overview of Chip bonding process

4.1 Solder Paste

The principal substances of Solder paste is Solder powder and Flux. The most general type Solder paste contains approximately 80 to 95wt% of Solder powder. The ratio of Solder powder will determine the viscosity of the paste, and the viscosity will directly affect the thickness and solder wetting after reflow. Also as shown in Table 4, there is a variety of grain size for Solder powder. The smaller the grain size, the amount of Solder powder will increase per unit area in the Solder paste. Therefore, in any case excessive Solder paste should be

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printed on the PCB, the possibilities of solder balls should become higher in comparison to Solder paste with larger grain size. For reference, PANASONICs recommendation of Solder grain size for each type of WL-CSP is shown in Table 5.

It should be noted that oxidation of Solder powder will cause higher risk of solder balls, solder voids and also poor die bonding due to insufficient wetting. Also, since smaller grain size tend to be affected more by surface oxidation, extra caution is required for handling and storage of the said solder paste. For this reason, it can be said that the selection of solder paste is as important to designing solder stencils to achieve quality mounting results and reliability.

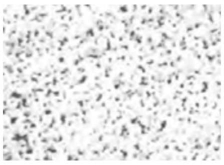
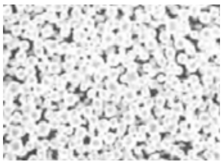
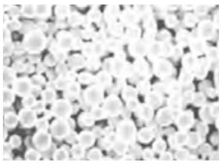
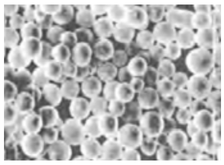
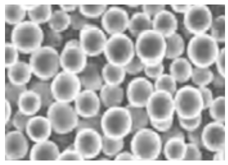
Grain size of solder powder				
5-15 µm	15-25 µm	25-38 µm	24-45 µm	38-53 µm
				

Table 4: Solder Powder Grain size in Solder Paste

*Latest Electronics Packaging [Part 2], Ch. 5. Sec.4 0603 Chip Component Assembly Technology, by Technical Information Institute Co. Ltd.

	Recommended Stencil Thickness	Recommended grain size of solder powder				
		5-15 µm	15-25 µm	25-38 µm	24-45 µm	38-53 µm
DCSP0603010-N1	80 µm			○		
DCSP1006020-N1	100 µm			○		
XLGA004-W-0808-RA	80 µm		○			
ULGA004-W-1010-RA	100 µm		○			
ULGA004-W-1212						
MLGA006-W-1726-RA	100 µm			○		
MLGA006-W-1727-RA						

Table 5: List of solder powder grain size recommended for each type of WL-CSP

4.2 Pick and Place

As shown in Figure 10, the Pick and Place procedure is determined by two parameters. 1) the mounting speed and 2) the placement force. The placement force stated herein is defined as "the depth from where the chip touches the solder paste is put as ±0, to how far the chip is pushed into the solder paste".

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Adjusting the mounter to a slower speed will incur less stress on the device, thus obtaining more stable results. For the placement force, evaluations show that in general the smaller the package, smaller placement force should be applied to the device. Refer to Table 6.

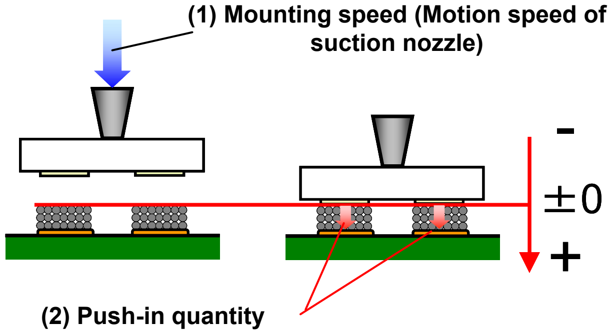

Figure 10: Relationship of mounting load, push-in quantity and mounting speed

Package Code	Recommended push-in quantity
DCSP0603010-N1	+0.3mm
DCSP1006020-N1	+0.5mm
XLGA004-W-0808-RA	+0.2mm
ULGA004-W-1010-RA	
ULGA004-W-1212	
MLGA006-W-1726-RA	+0.5mm
MLGA006-W-1727-RA	

Table 6: Recommended push-in quantity

The said placement force should be carefully evaluated in order not to increase the risk of solder balls. This is also in close relation to the solder paste amount on the PCB and reflow temperature, and need to be carefully controlled likewise. Refer to 5.2.2 for more details.

4.3 Reflow

4.3.1 Methods of Reflow Process

Reflow is the process to bond the device to the PCB. The device is first placed on the PCB and then put through a heating process in an oven to form a solder joint between the device pin and PCB pad. The said oven is a carefully tuned oven in which the temperature is controlled depending on the stage of the process from pre-heating to cooling, as shown in Figure 9. There are two major methods of Reflow, Infrared Reflow method and Convection Reflow method. Figure 12 illustrates the differences of each method.

Infrared Reflow heats the devices by infrared radiant heat. Although this method has advantages of low operating cost and easier maintenance, controlling the temperature may need some experience since the material and shape of the components react differently to the radiant heat. Also, with Infrared Reflow, the pins will not be directly heated and only conductive heat through the PCB will heat the part. Uneven temperature may be caused because of this, therefore result in weaker joint strength.

Convection Reflow performs soldering by heated air and/or nitrogen. In comparison to Infrared, Convection reflow takes longer heating time but because both convection and conductive heat will heat the pins and solder paste, a more even finish can be expected. Based on this reason, we recommend convection reflow method for WL-CSP devices.

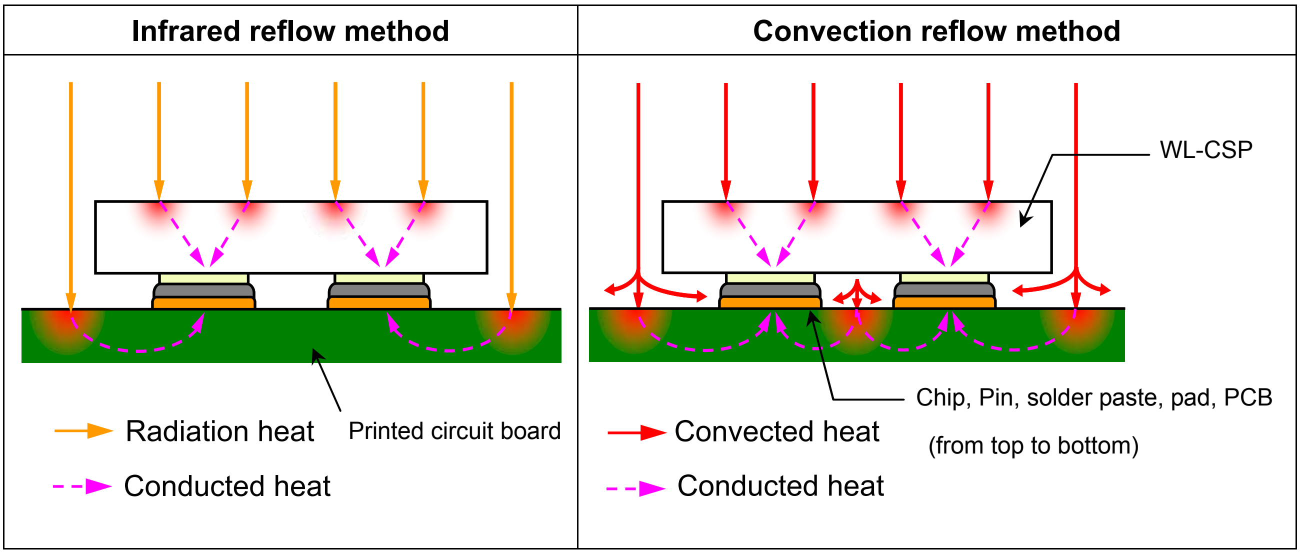

Figure 12: Heat transmission path of infrared reflow method and convection reflow method

4.3.2 Reflow Temperature and Limit count of Reflow runs

All PANASONIC WL-CSP products have been reliability tested, performed accordingly with IPC/JEDEC J-STD-020C specifications. Exposed to pre-moisturing and five reflow runs at the maximum temperature of 260°C, but no issues could be confirmed. Although the parts can withstand five reflow processes, as the IPC/JEDEC J-STD-020C guideline states, it is preferred to limit the process within three times, and lower the risk of thermal shock and deterioration. This must be especially put into consideration for two sided boards and reworking. The Solder paste and manufacturing environment and/or equipment are key factors in deciding the number of runs in this process.

4.3.3 Temperature Profiling

Upon the production of this application note, Panasonic has performed several evaluations with a variety of Solder paste. Shown in Figure 13 is the temperature profile which provided stable results of the said Solder pastes. This data can be used for reference upon determining the most suitable temperature profile for each manufacturing conditions.

Reflow processing with an inappropriate temperature profile may result in generation of solder balls and solder voids, thereby reducing solder joint quality. When determining the reflow process temperature profile, it is recommended to limit the thermal stress on the device as much as possible. Listed below are the items from Figure 13 which should be carefully evaluated upon determining the temperature profile.

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Preheating

The difference of thermal mass of each component or device on the PCB's, due to the difference in size, naturally will cause unevenness of temperature. To prevent the said unevenness, the oven temperature must be Preheated to equalize the temperature through conduction before the actual Heating Time. This will improve the solder joint finish, and help evaporate volatile material that is the major cause of Voids, and also help reduce surface oxidation.

Along with temperature, time is also an important factor in Preheating. If the temperature is set too low or the time too short, the Flux material will remain until the Heating time, causing voids and/or solder balls as a result of Flux boiling. On the other hand, when the Preheating temperature is too high or the time too long, the solder wetting is affected and may lead to poor, weak bonding.

When mounting Panasonic WL-CSP, the preheating time should be set in between 65 to 85 sec (74 sec is recommended) and the average temperature at 165°C. In this case, the "Preheating time" is defined as the time span the temperature rises from 150°C to 170°C.

Critical Zone

The Critical zone, shown in Figure 13, is the temp zone in which Sn (tin) - Ag (silver) lead-free solder melts. Generally, it is defined as the time in between 210°C to 221°C. In PANASONIC, the Critical zone is defined as the time at and above 217°C. Since excessively long and high temperature exposure will result in weaker solder joint and connection failures as discussed in 4.3.2., the Critical zone should be limited to approximately 23 sec, and peak temperature at around 245°C.

Temperature Ramp Rate

The temperature ramp rate, from the Preheat zone to the Critical zone, must also be controlled. A gradual rise is recommended, whereas the Ramp rate should be best at around 1-3°C/sec (1.9°C/sec is most recommended). An immediate and sudden rise in the temp will apply thermal shock to the device and raise the risks of cracks, but also will cause boiling, or in the worst case, explosions of volatile component of flux gas, resulting in Voids or Solder Balls.

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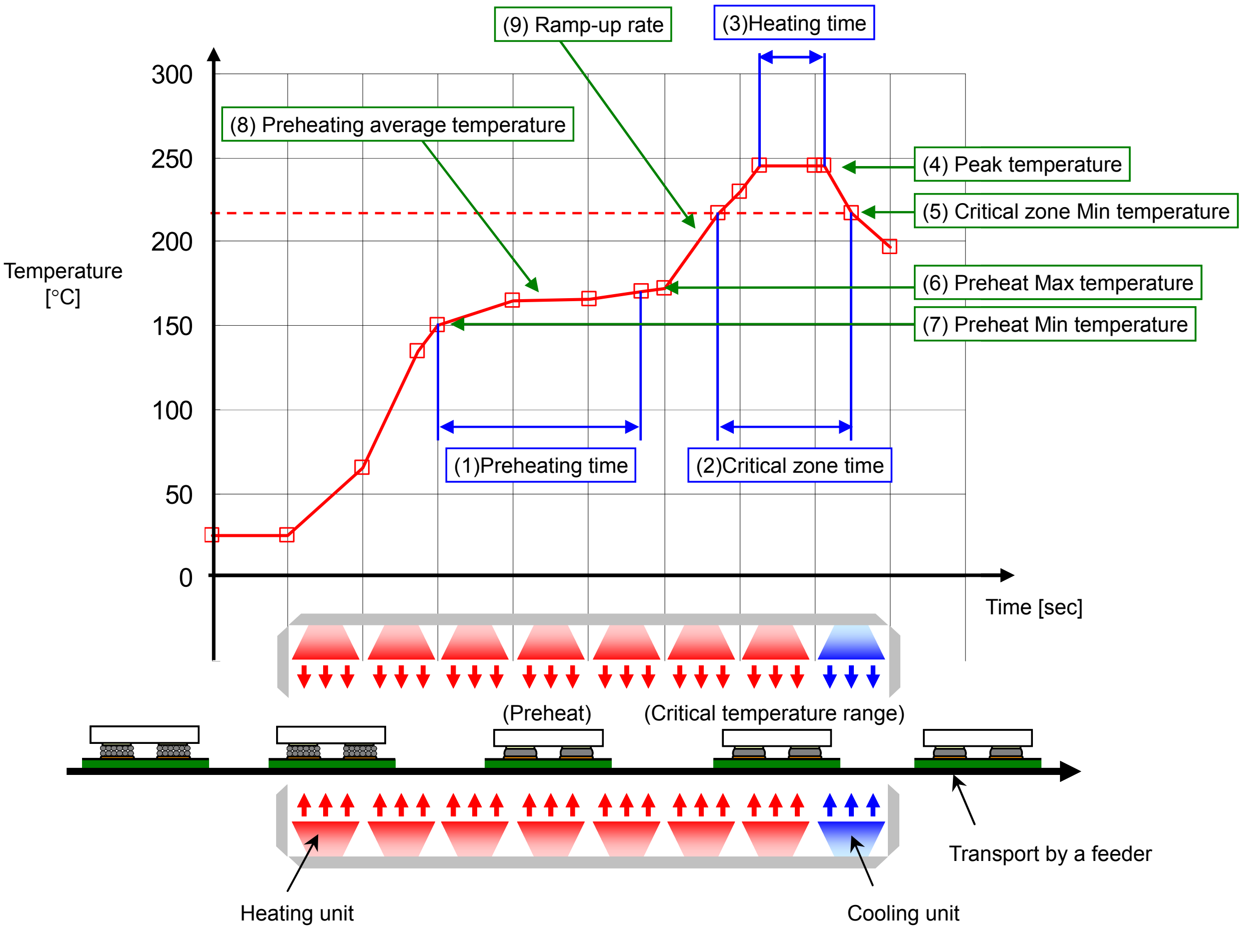

(1)	Preheating time	74 [sec]	(6)	Preheat Max temperature	170 [°C]
(2)	Critical temperature zone time	48 [sec]	(7)	Preheat Min temperature	150 [°C]
(3)	Heating time	23 [sec]	(8)	Preheating average temperature	165 [°C]
(4)	Peak temperature	245 [°C]	(9)	Ramp rate	1.9 [°C/sec]
(5)	Min temperature in critical zone	217 [°C]			

Figure 13: Temperature Profile Example of Reflow Processing

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■ Section 5 Common Failures and Corrective Actions

As discussed up to this point, optimizing the land pattern and solder stencil design, and also evaluating reflow conditions with the combination of solder pastes are the keys to success. However, before reaching the ideal conditions, it is most likely that many problems or abnormalities will be encountered through many evaluations. In this section, some abnormalities and failures most commonly seen have been described to provide a better understanding of perfecting the process.

5.1 Examples of Good and Defective Solder Joints

Shown in Figure 14 is an X-ray photo of a good sample. The red square in dotted line indicates the outline of the WL-CSP, and the black circular objects being the solder joints of the device and PCB. The gray area is the circuit pattern of the PCB. In Table 7, listed are some samples of Solder joints that are Good and Unacceptable.

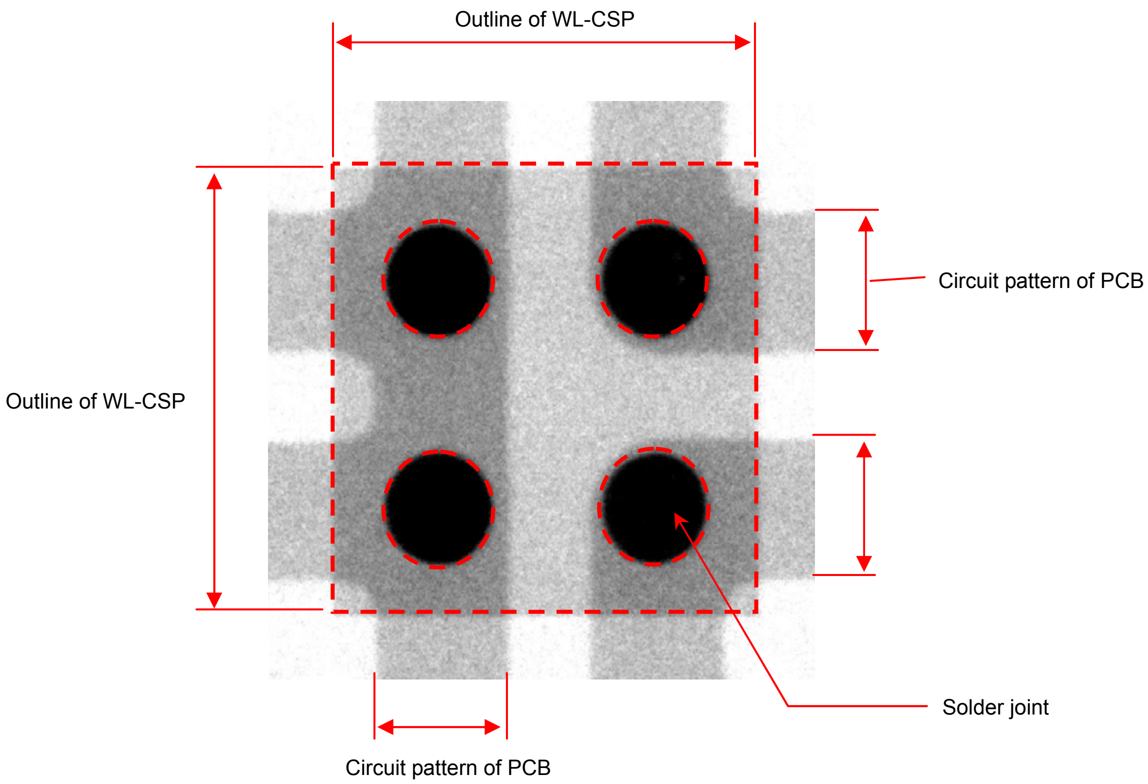

Figure 14: Good sample

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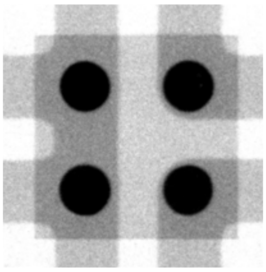
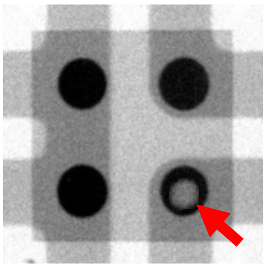
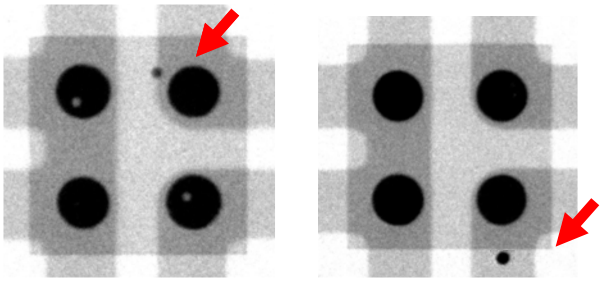
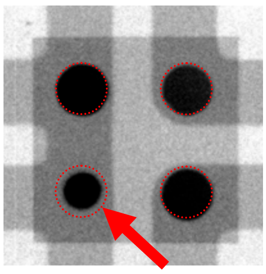
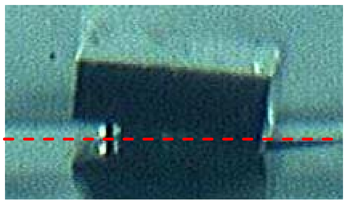
Condition	Example	Reference
Good sample		Figure 14
Void		Sec. 5.2.1
Solder ball		Sec. 5.2.2
Non-wetting		Sec. 5.2.3
Tilting		Sec. 5.2.4

Table 7: Examples of good and defective solder joints

***Note: Defective samples were produced intentionally strictly for explanatory purposes for the use of this application note.**

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5.2 Common Abnormalities

5.2.1 Voids

Figure 15 is an X-ray photo showing a Void that can be seen in the lower right solder joint, circled in red. In most cases the said Voids are caused by remainders of flux-gas trapped inside the solder paste. These type of Solder voids happen randomly but can be minimized by optimizing the Reflow temperature profile (Refer to "4.3.3 Temperature Profiling" for details). Voids can also be avoided by allowing the gas to escape by designing the PCB with a combination of SMD and NSMD patterns (Refer to "3.1 Solder Resist Designing", Figure 6).

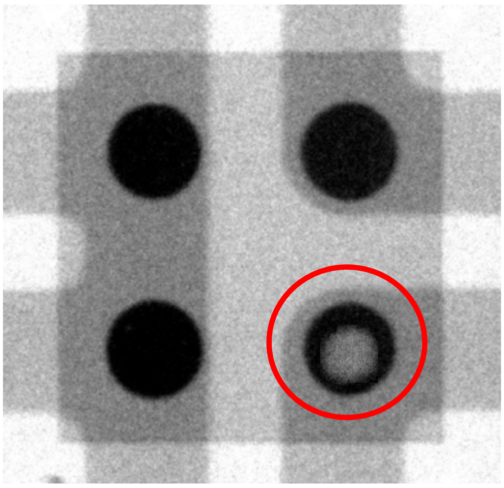

Figure 15: Solder void

In Figure 16, the behavior of Solder voids can be observed during the five Reflow processes the device was put into. This Void, which intentionally generated, in the 1st reflow process is fairly small but continues to grow until the 3rd Reflow run. After the 4th run, the Void cannot be seen, and has basically disintegrated. No changes can be confirmed in the 5th run, where as there are no Voids. The mechanism of the phenomenon is shown in Figure 17. As the diameter of the Void grows during the heating process, the edge of the Void will eventually reach the end of the pad, and finally allow the gas to escape from the solder paste. Based on this evaluation, it must be stressed again that correct Preheating and carefully designed circuit pattern can be extremely effective in minimizing the occurrence of any unwanted Voids. According to many industry standards such as IPC-A-610, the tolerance for void is stated, "less than 25%" of each solder joint area. And with the same standards, PANASONIC has performed evaluations of electrical characteristics, thermal characteristics, and reliability evaluations both with and without Void parts, and have concluded the same. Upon X-ray visual inspections, the defect limit should be, as stated above, all solder voids to be smaller than 25% of solder joint area of each pin/pad.

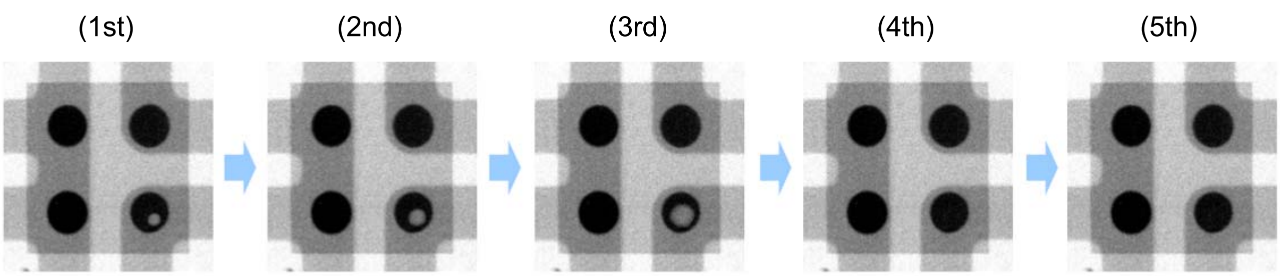

Figure 16: Void evaluation

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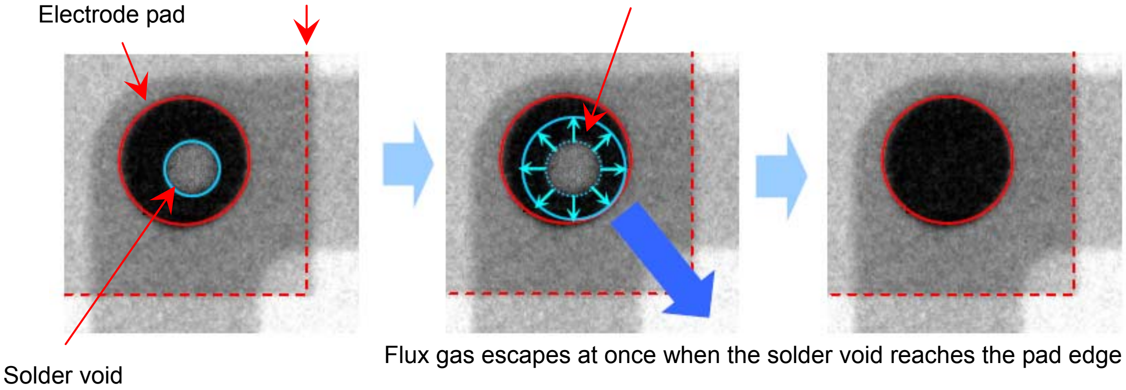

Figure 17: Thermal history by reflow process and solder void growth

Other than flux gas remainders, there are other possibilities that could cause Voids. The combination of PCB pattern contamination, and oxidization of Solder are some examples. In some cases the combination of these could lead to gas generation, likewise resulting in Solder voids.

That said, precautions of keeping the PCB safe from contamination is also an important factor, along with preventing Solder paste oxidization.

5.2.2 Solder Balls

The red circles highlighted in Figure 18 show circular objects near the solder joints, which are called Solder Balls.

Following are a more illustrative description of the three most common reasons why and how Solder balls happen, mentioned briefly in the earlier pages.

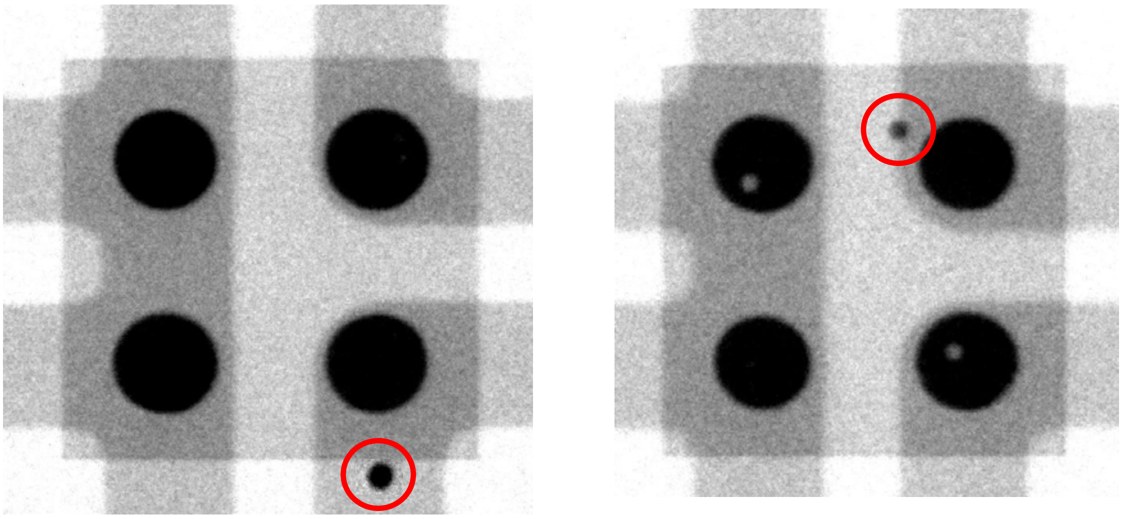

Figure 18: Solder balls

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Case (1)

When the solder paste quantity is excessive. naturally, the excess solder is pushed out of the pad during reflow process by the weight of the device itself and hardens into a spherical shape near the land pattern. This can be corrected by a more appropriate solder stencil design. Refer to 3.3 Solder Stencil Designing.

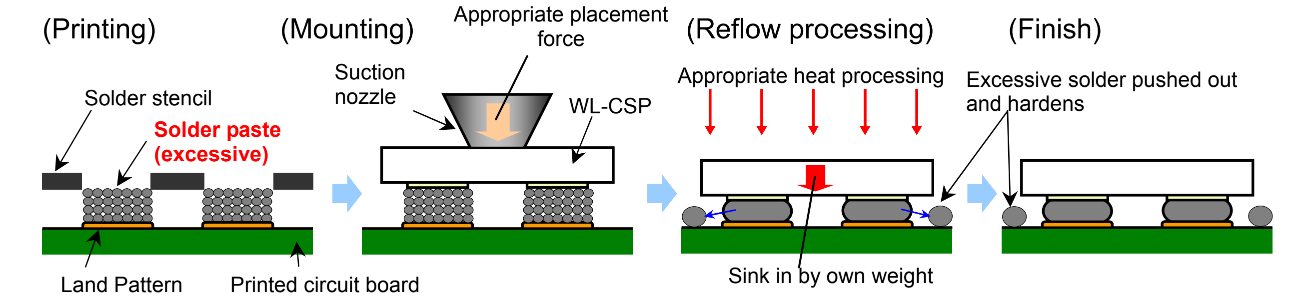

Figure 19: Solder ball generation mechanism (1)

Case (2)

When the placement force is too strong. The outcome is the same as in Case (1). Refer to 4.2 Pick and Place for corrective actions.

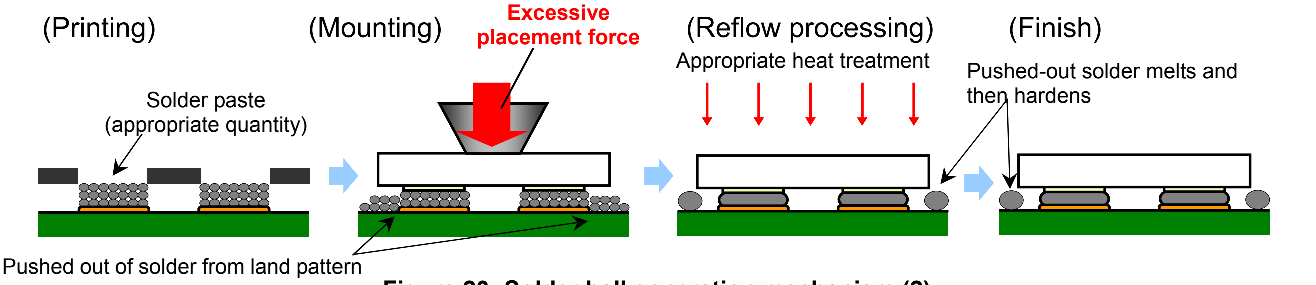

Figure 20: Solder ball generation mechanism (2)

Case (3)

When the temperature profile is inappropriate. As explained previously, excessively high temperature at Preheat and/or excessively high ramp-up rate can lead to a boiling or explosion of flux and other gases. Refer to 4.3.3 Temperature profiling for details.

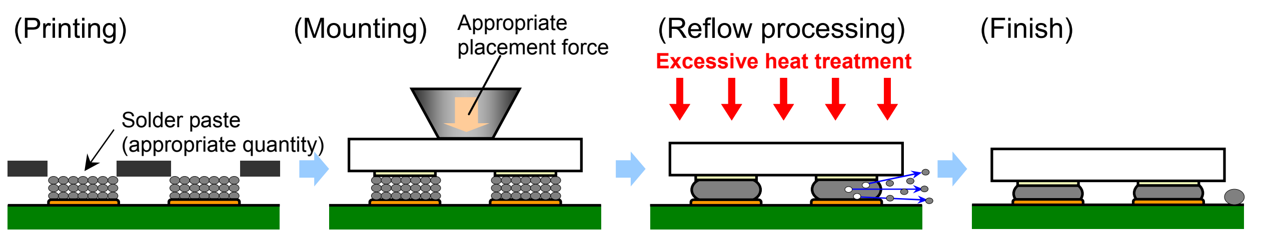

Figure 21: Solder ball generation mechanism (3)

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Although Solder balls do not always affect the function and reliability in a critical way, “foreign objects” are not desirable and should be controlled as much as possible. In the worst case, Solder balls can form a bridge between the pins and may cause short-circuits. Electrical characteristic tests are recommended to screen out such bridge formings.

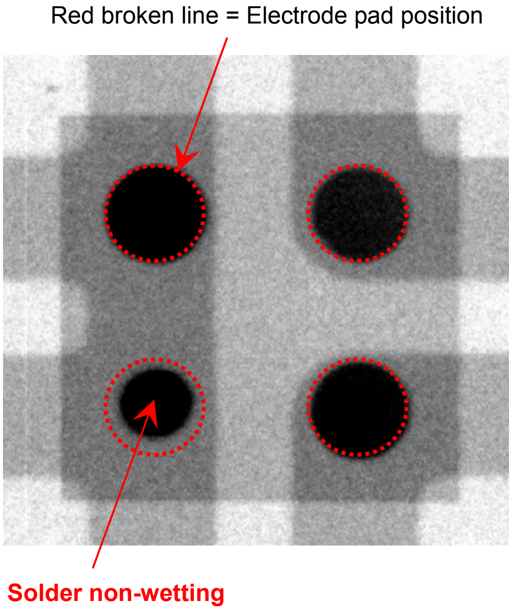

Figure 22: Solder non-wetting

5.2.3 Solder Non-Wetting

In Figure 22, the dotted red circles indicate the area of the pin/pad, which if properly processed should be covered with solder and look entirely “Black” in the X-ray photo. Although three of the four pins have a sufficient finish, the pin on the lower left hand has a smaller “Black” area, covering only a portion of the said pin. This is called Non-wetting . Non-wetting will most likely cause poor reliability performance, as well as increase the risk of open failures. Non-wetting can occur in many cases. For example, when the solder stencil opening is designed too small limiting the solder output amount. Clogging of the stencil opening or solder paste related issues may also be root causes for poor solder printing. For corrective actions, the solder stencil design and solder paste type, especially the grain size of the solder powder should be reevaluated. For the stencil design, please refer to Section 3.3, Solder Stencil Designing. For the solder paste and grain size, please refer to Section 4.1, Solder Paste as well as Table 5. Along with designing issues and selection of material, maintenance issues should not be overlooked. Keeping the equipment clean, namely the stencil, will go a long way to improve the finish and reliability.

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5.2.4 Tilting

Tilting is a condition in where the device is tilted to one side and not level to the board, as shown in Figure 23. Although not as critical as Voids or Solder balls, this abnormality is more commonly seen in smaller devices with two bottom side pins in a rectangular outline. Needless to say this two pin type package is somewhat more unstable in comparison to 4pin square types. The device showed in Figure 23 is a two pin 1.0mm x 0.6mm size package, that was intentionally tilted for evaluation purposes. Unlike larger type devices (mold type products), where in some cases the solder would pull the device to stand up on the end, also known as Tombstoning, this phenomenon does not occur with WL-CSP's, but rather tilt on either short side of the component. See Figure 24.

There are primarily three reasons for this.

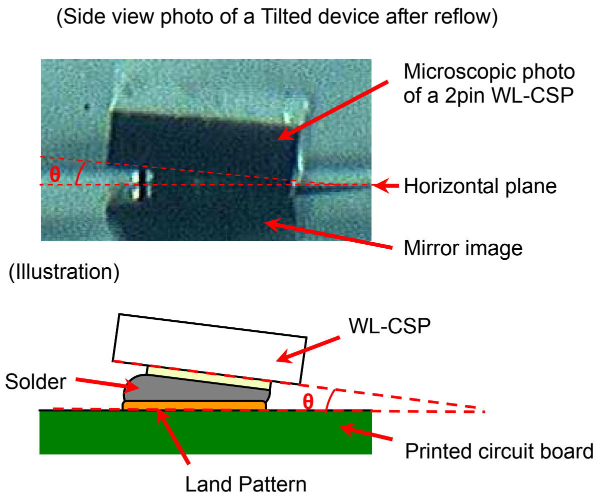

Figure 23: Tilting

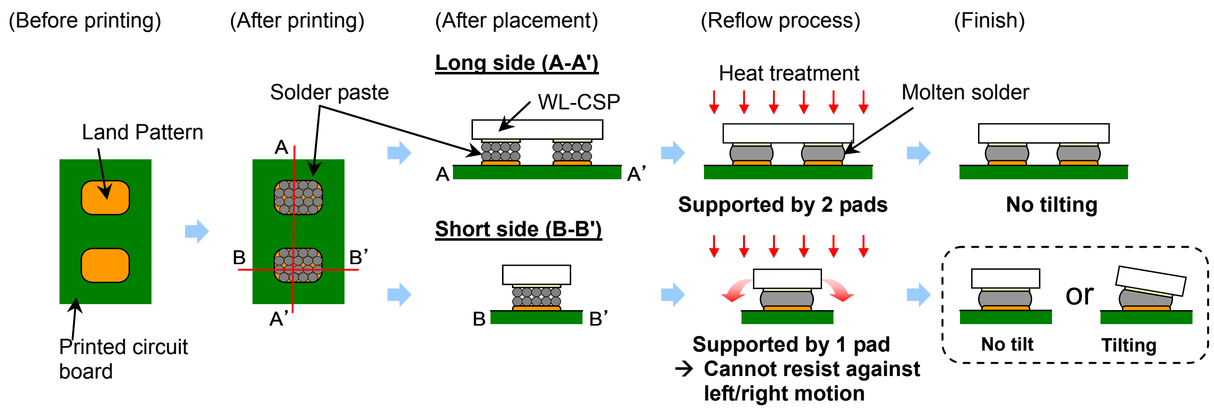

Figure 24: Example of device tilt with a 2-pad type WL-CSP

Case (1)

When the WL-CSP device is affected by the air flow in the oven

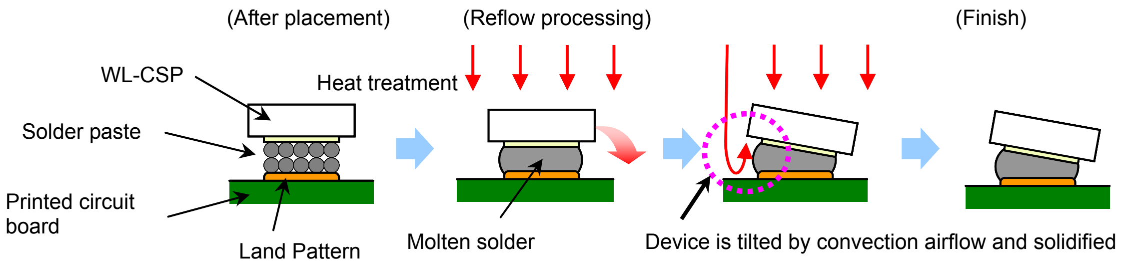

Figure 25: Cause of device tilt in the short side of a 2-pad type device (1)

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Case (2)

When a differential occurs in the solder melting time, due to the board layout density

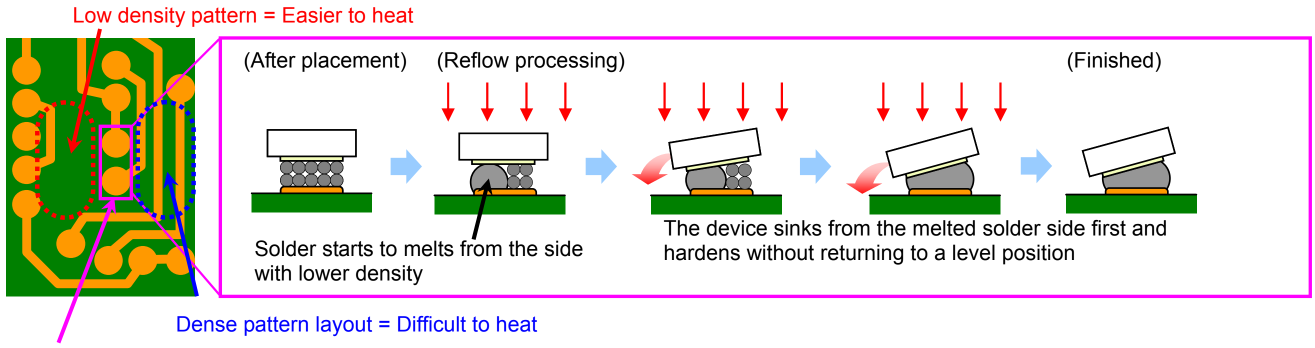

Figure 26: Cause of device tilt in the short side of a 2-pad type device (2)

Case (3)

When the PCB warps

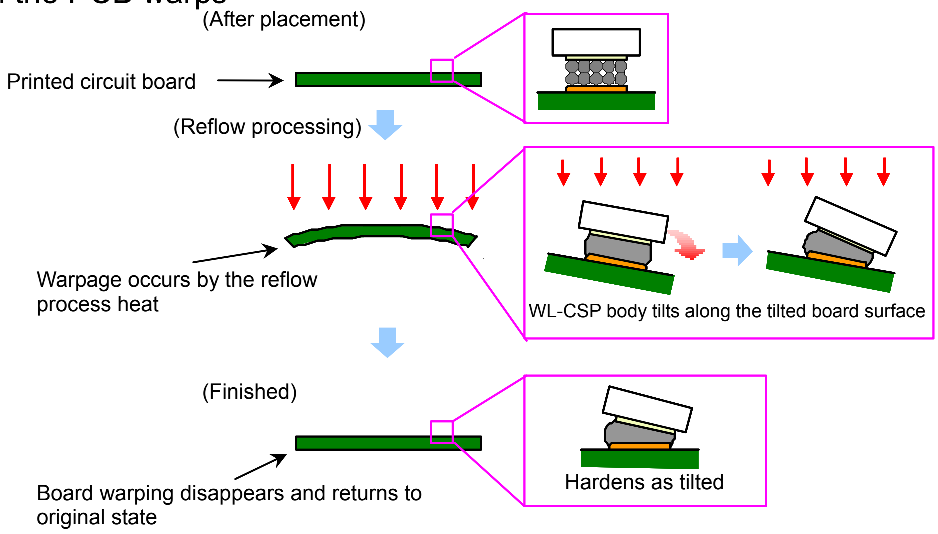

Figure 27: Cause of device tilt in the short side of a 2-pad type device (3)

Tilting is usually caused by the three factors mentioned above, and has a very close relation to the solder amount. Limiting the solder amount, and also controlling the output by reviewing the solder stencil design and solder stencil thickness should be very effective for corrective actions.

Regardless if the package is molded or not, tilting is a phenomenon commonly seen for devices with small outlines and bottom-side two pin devices. But, despite the shaky outlook, tilting does not necessarily affect the performance or reliability of the said device, and through various evaluations and reliability tests, no issues related to tilting could be confirmed. However, it is still recommended to keep the tilting angle less than 10°. Again, in any case tilting is to occur, reevaluating the solder stencil design is recommended. Also refer to Section

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3.3 Solder Stencil Designing. For screening tests, θ>10° should be a good place to start. Because of its balanced structure, device tilt will rarely occur on the long side of a 2-pin type WL-CSP, and 4-pin, 6-pin type WL-CSP likewise. In any rare case such abnormality should occur, the most likely cause would be due to issues in solder printing, such as clogging. Refer to Figure 28. To prevent minor issues like this, fixing a maintenance flow chart, especially cleaning procedures, should also be effective.

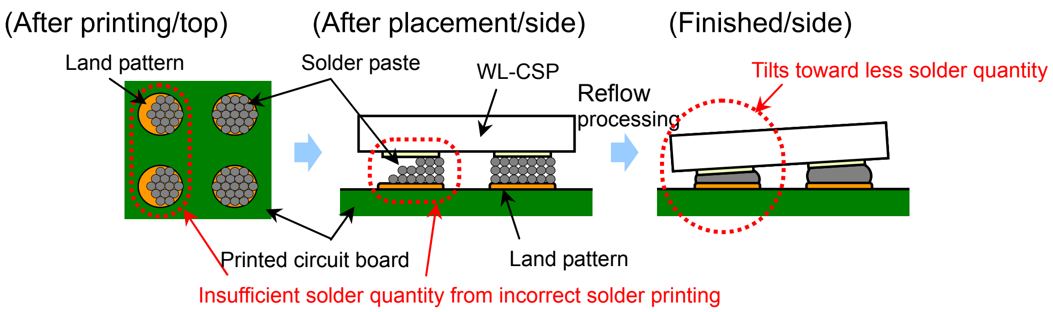

Figure 28: Example of device tilt with a 4-pad type WL-CSP

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■ Section 6 Design Recommendation Chart

Table8 is for SBD and ZND devices. Table9 is for MOSFET devices.

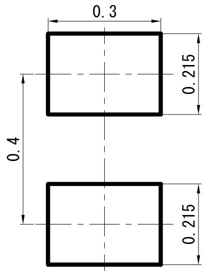
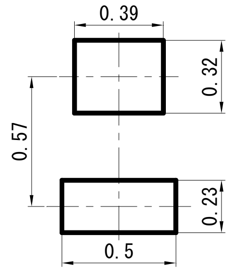
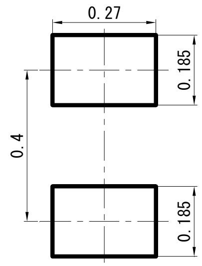
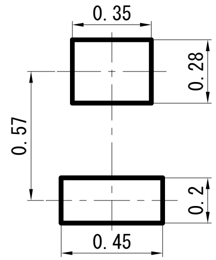
Package Code	**DCSP0603010-N1**	**DCSP1006020-N1**		
Land Pattern (3.2 Land Pattern Designing)				
Solder Stencil Pattern (3.3 Solder Stencil Designing)				
Stencil Thickness (3.3 Solder Stencil Designing)	80μm	100μm		
Solder Paste Grain Size (4.1Solder Paste)	25～38μm	25～38μm		
Push in Quantity(4.2 Pick and Place)	+0.3mm	+0.5mm		
Reflow profiling(4.3.3 Temperature Profiling)	Refer to Figure13			

Table8: WL-CSP "SBD & ZND" Design Recommendation Chart

*The recommendations stated in this chart are for reference and may/will need adjustments, depending on the environment/equipment of the assembly line.

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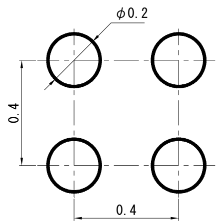
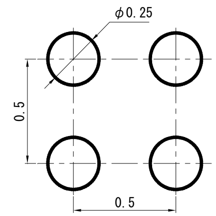
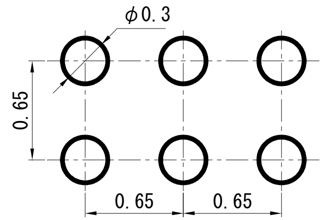
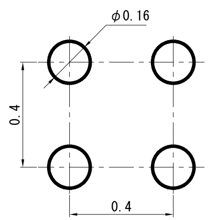
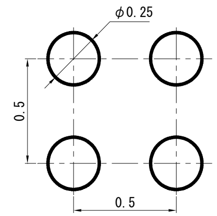
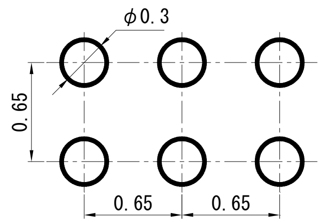
Package Code	XLGA004-W-0808-RA	ULGA004-W-1010-RA ULGA004-W-1212	MLGA006-W-1726-RA MLGA006-W-1727-RA	
Land Pattern (3.2 Land Pattern Designing)				
Solder Stencil Pattern (3.3 Solder Stencil Designing)				
Stencil Thickness (3.3 Solder Stencil Designing)	80μm	100μm	100μm	
Solder Paste Grain Size (4.1Solder Paste)	15～25μm	15～25μm	25～38μm	
Push in Quantity(4.2 Pick and Place)	+0.2mm	+0.2mm	+0.5mm	
Reflow profiling(4.3.3 Temperature Profiling)	Refer to Figure13			

Table9: WL-CSP “MOSFET” Design Recommendation Chart

*The recommendations stated in this chart are for reference and may/will need adjustments, depending on the environment/equipment of the assembly line.

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WL-CSP Application Notes

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Panasonic

Semiconductor Business Division
Automotive & Industrial Systems Company
Panasonic Corporation
1 Kotari-yakemachi, Nagaokakyo, Kyoto 617-8520, Japan
Tel. +81-75-951-8151
http://www.semicon.panasonic.co.jp/en