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May 2016

FCH041N65EFL4

N-Channel SuperFET® II FRFET® MOSFET

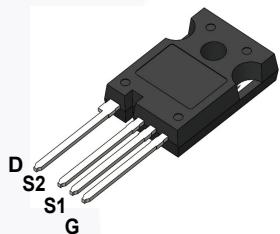
650 V, 76 A, 41 mΩ

Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 36 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 229 \text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(\text{eff.})} = 631 \text{ pF}$)
- 100% Avalanche Tested
- RoHS Compliant

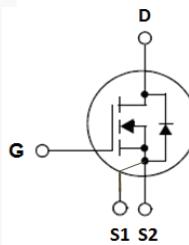
Applications

- LCD / LED / PDP TV
- Solar Inverter
- Telecom / Server Power Supplies
- AC - DC Power Supply



Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



S1: Kelvin Source
S2: Power Source

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		FCH041N65EFL4	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	- DC	± 20	V
		- AC ($f > 1 \text{ Hz}$)	± 30	
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	76	A
		- Continuous ($T_C = 100^\circ\text{C}$)	48.1	
I_{DM}	Drain Current	- Pulsed	(Note 1)	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	mJ
I_{AR}	Avalanche Current		(Note 1)	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt		(Note 3)	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	595	W
		- Derate Above 25°C	4.76	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FCH041N65EFL4	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.21	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH041N65EFL4	FCH041N65EF	TO-247 4L	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 10 \text{ mA}$, $T_J = 25^\circ\text{C}$	650	-	-	V
		$V_{GS} = 0 \text{ V}$, $I_D = 10 \text{ mA}$, $T_J = 150^\circ\text{C}$	700	-	-	
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = 10 \text{ mA}$, Referenced to 25°C	-	0.72	-	$\text{V}/^\circ\text{C}$
		$V_{DS} = 650 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	10	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 520 \text{ V}$, $T_C = 125^\circ\text{C}$	-	145	-	μA
		$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-	± 100	
I_{GSS}	Gate to Body Leakage Current					nA

On Characteristics

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 7.6 \text{ mA}$	3	-	5	V
$R_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 38 \text{ A}$	-	36	41	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}$, $I_D = 38 \text{ A}$	-	71.7	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	9446	12560	pF
C_{oss}	Output Capacitance		-	366	490	pF
C_{rss}	Reverse Transfer Capacitance		-	35	-	pF
C_{oss}	Output Capacitance	$V_{DS} = 380 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	197	-	pF
$C_{oss(\text{eff.})}$	Effective Output Capacitance	$V_{DS} = 0 \text{ V}$ to 400 V , $V_{GS} = 0 \text{ V}$	-	631	-	pF
$Q_{g(\text{tot})}$	Total Gate Charge at 10V	$V_{DS} = 380 \text{ V}$, $I_D = 38 \text{ A}$, $V_{GS} = 10 \text{ V}$	-	229	298	nC
Q_{gs}	Gate to Source Gate Charge		-	50	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	90	-	nC
ESR	Equivalent Series Resistance	$f = 1 \text{ MHz}$	-	0.6	-	Ω

Switching Characteristics

$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = 380 \text{ V}$, $I_D = 38 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_g = 4.7 \Omega$	-	55	120	ns
	Turn-On Rise Time		-	25	60	ns
	Turn-Off Delay Time		-	169	348	ns
	Turn-Off Fall Time		(Note 4)	18	46	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	76	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	228	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 38 \text{ A}$	-	-	1.2
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$, $I_{SD} = 38 \text{ A}$, $dI_F/dt = 100 \text{ A}/\mu\text{s}$	-	207	-
Q_{rr}	Reverse Recovery Charge		-	1.5	μC

Notes:

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. $I_{AS} = 15 \text{ A}$, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 38 \text{ A}$, $dI/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq 380 \text{ V}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

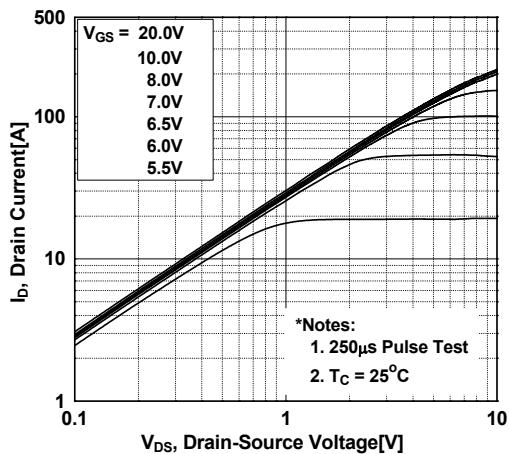


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

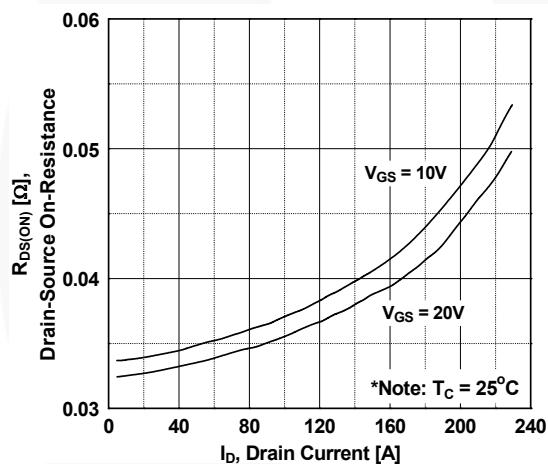


Figure 5. Capacitance Characteristics

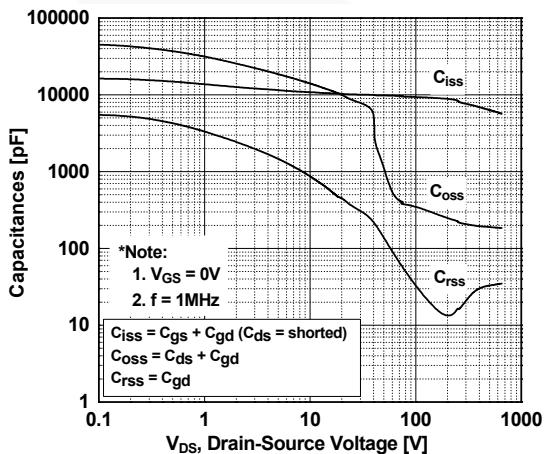


Figure 2. Transfer Characteristics

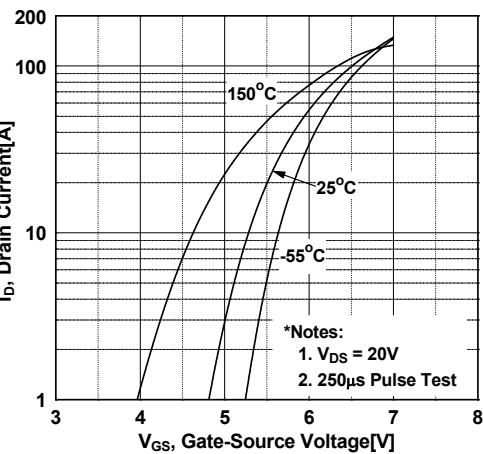


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

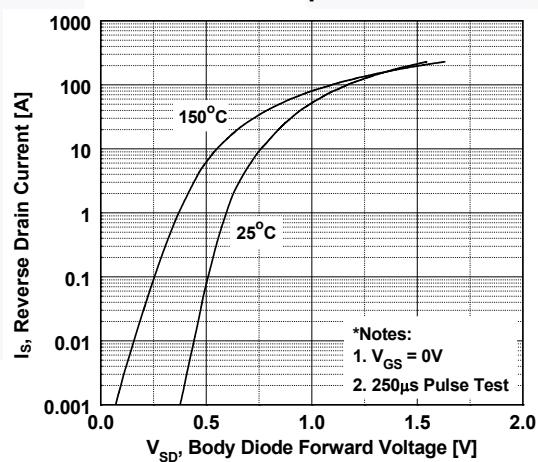
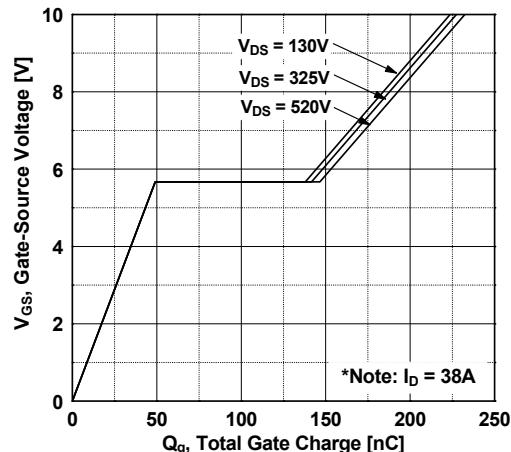


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

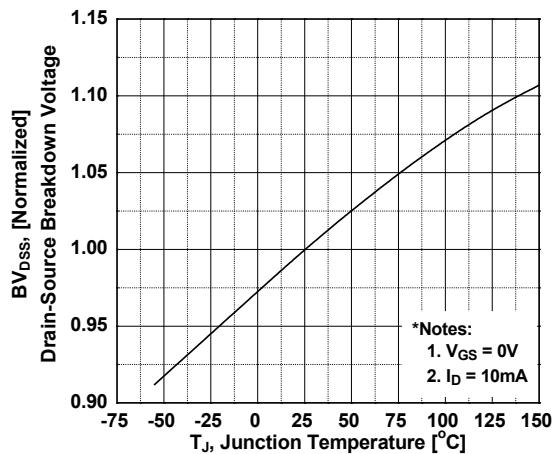


Figure 8. On-Resistance Variation vs. Temperature

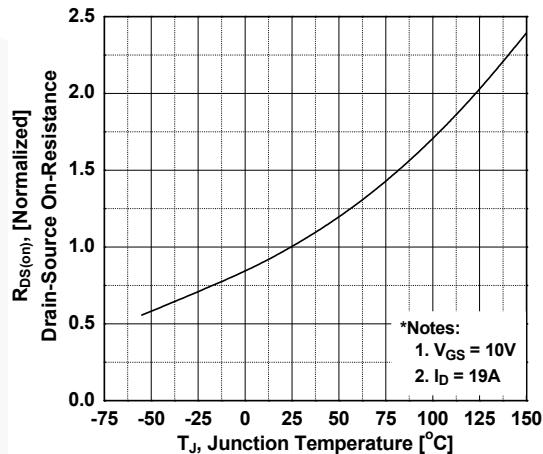


Figure 9. Maximum Safe Operating Area

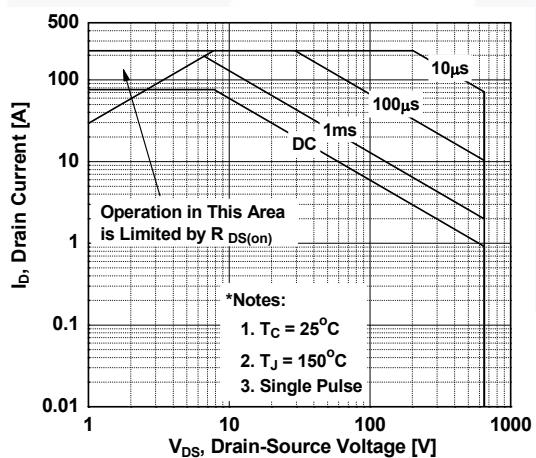


Figure 10. Maximum Drain Current vs. Case Temperature

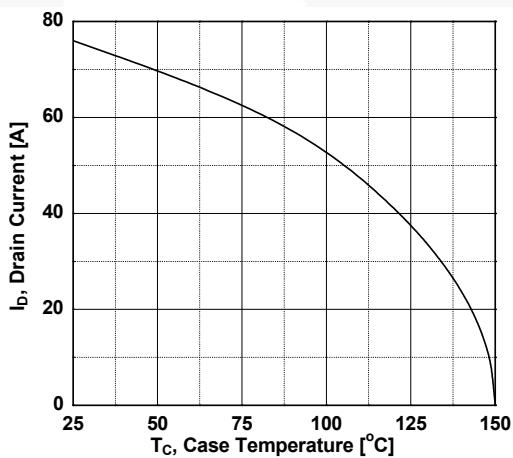
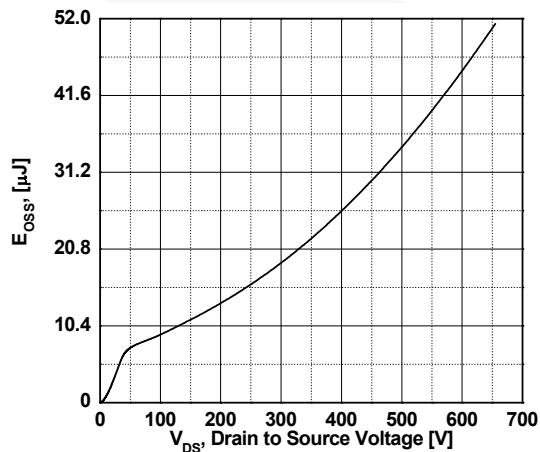
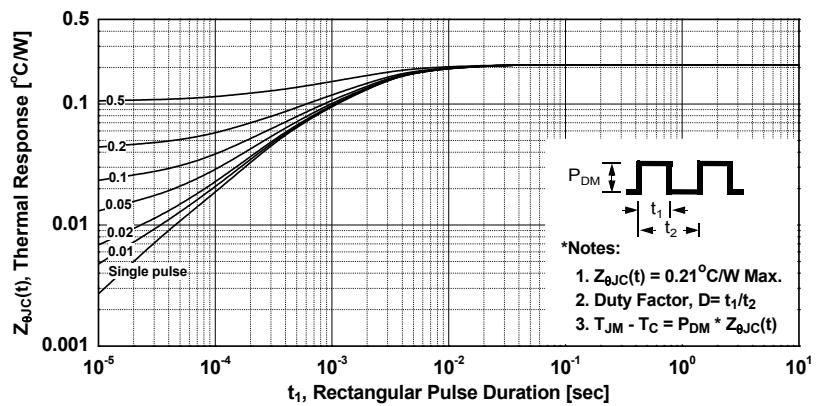


Figure 11. E_{OSS} vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



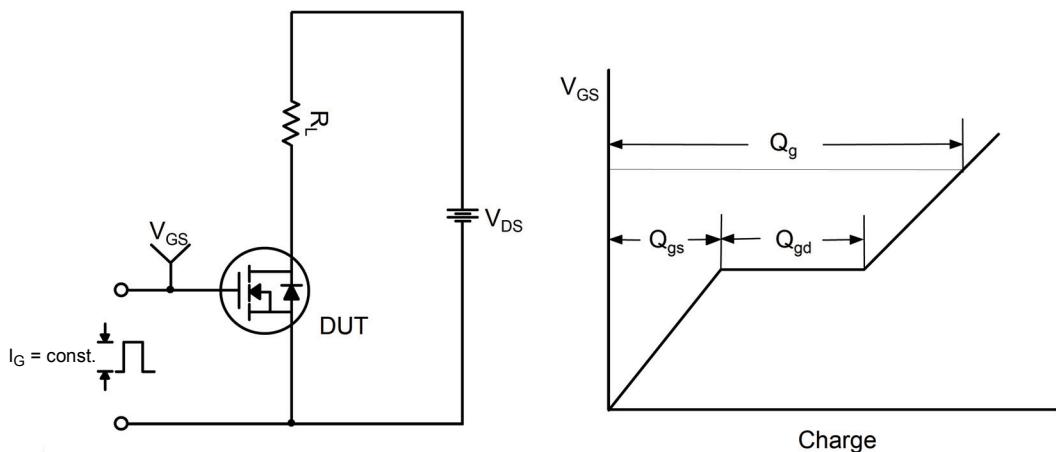


Figure 15. Gate Charge Test Circuit & Waveform

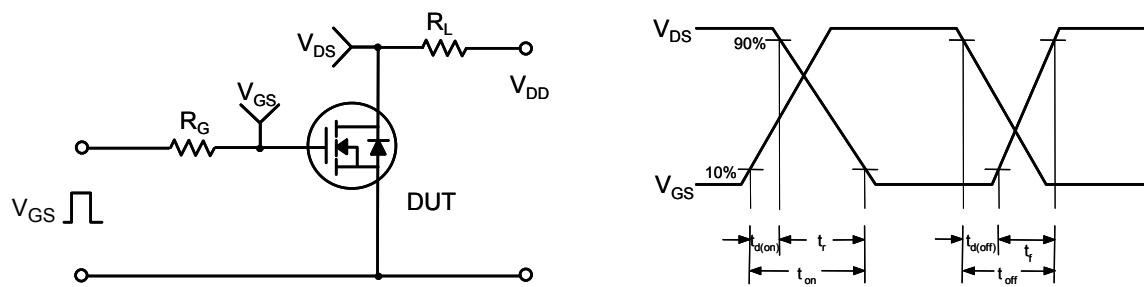


Figure 16. Resistive Switching Test Circuit & Waveforms

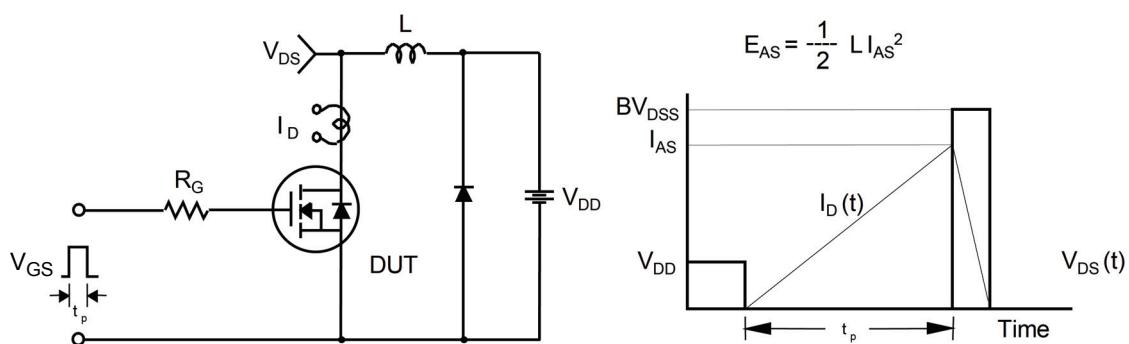


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

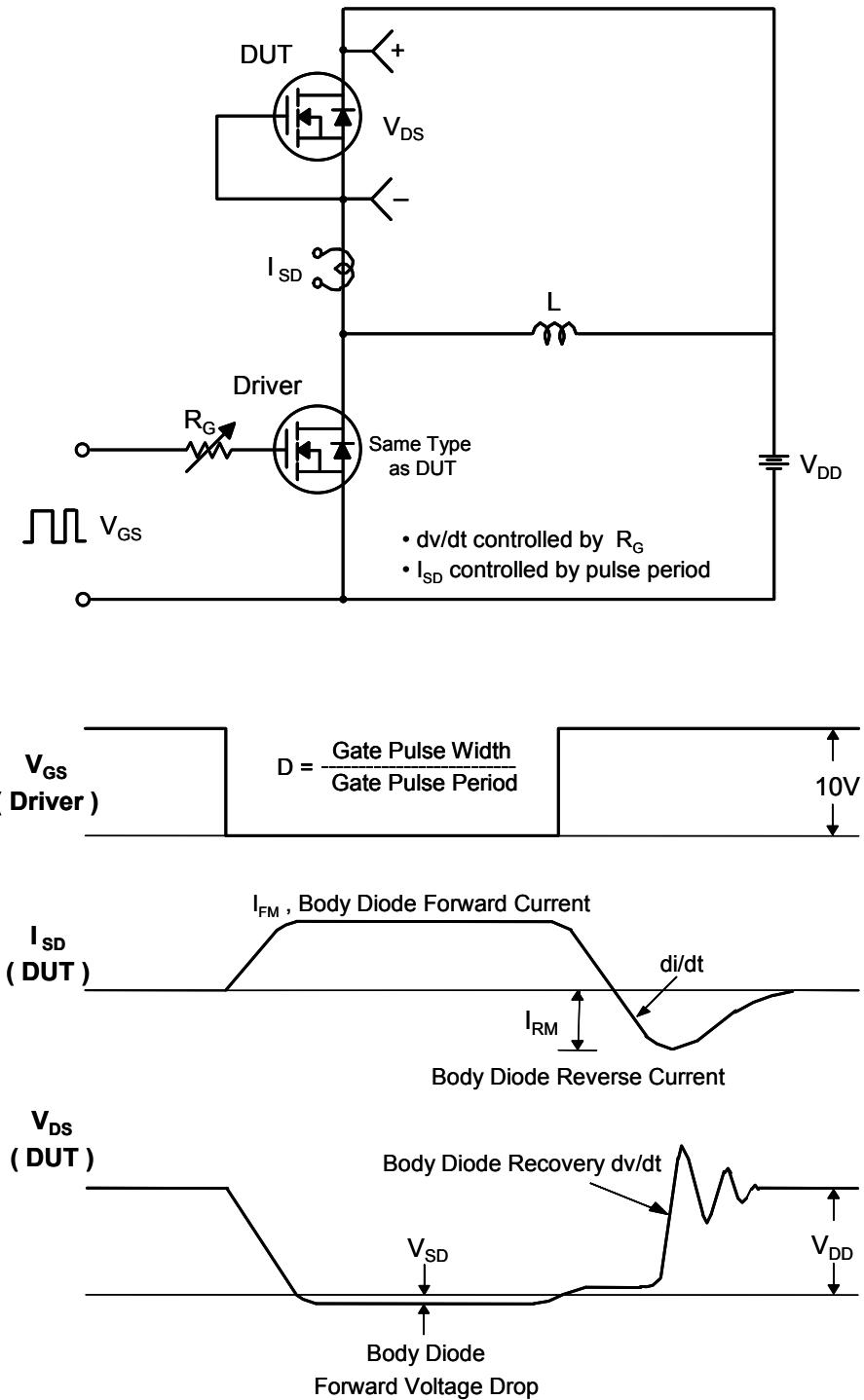
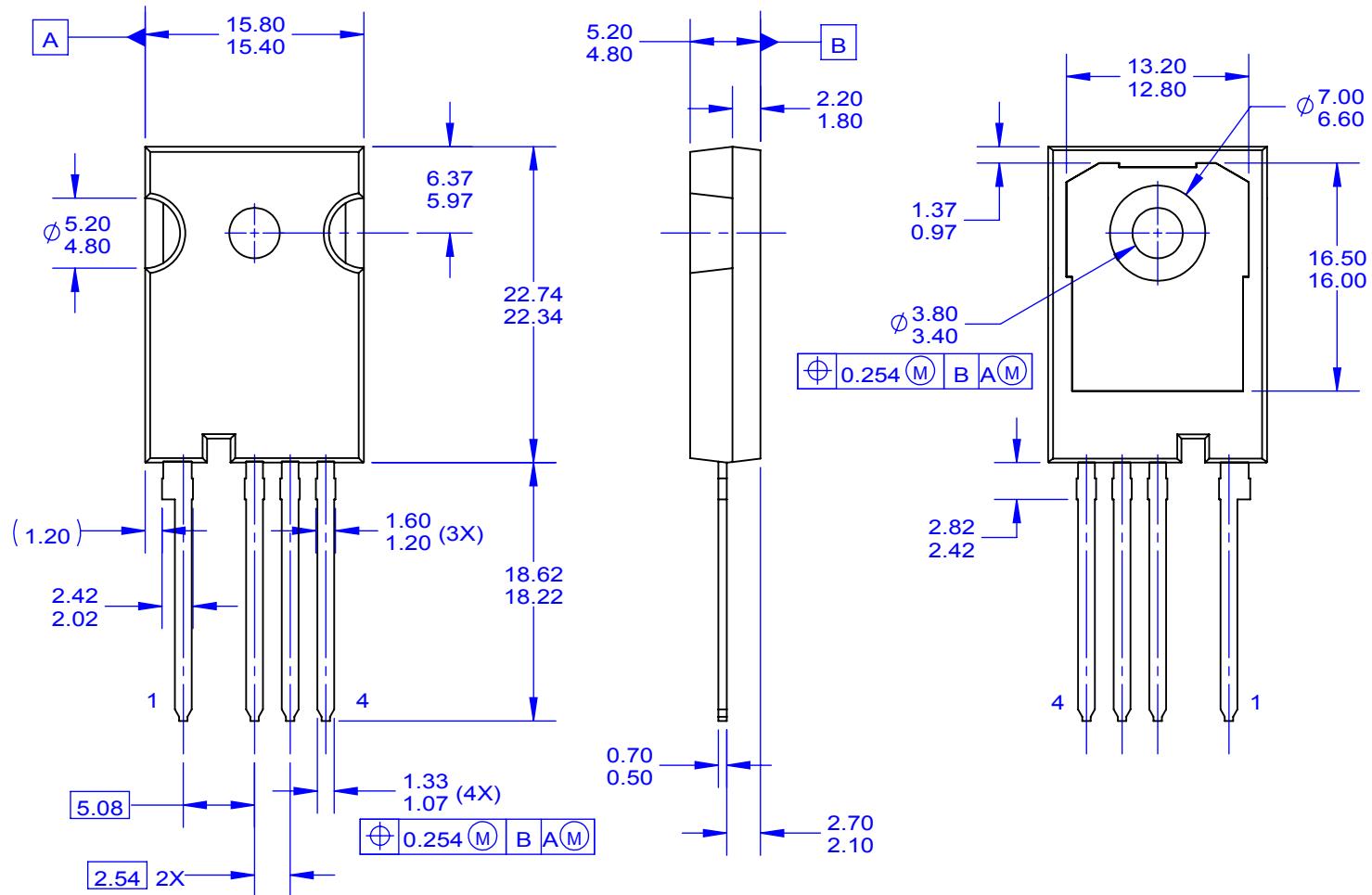


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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