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AN-8202
FCM8531 User Manual Hardware Description

1. Summary

The FCM8531 is an application-specific parallel-core processor for motor control that consists of an Advanced Motor Controller (AMC) processor and a MCS®51-compatible MCU processor. The AMC is the core processor specifically designed for motor control, and more particularly it integrates a configurable processing core and peripheral circuits to perform Sensorless Field-Oriented Control (FOC) motor control. System control, user interface, communication interface, and input/output interface can be programmed through the embedded MCS®51 for different motor applications.

The advantage of FCM8531's parallel-core processors is that the two processors can work independently and complement each other. The AMC is dedicated for motor control applications, such as motor control algorithms, PWM control, current sensing, real-time over-current protection, and motor angle calculation. The embedded MCU provides motor control commands to the AMC to control motors through a communication interface. This approach reduces software burdens and simplifies control system programs because complex motor-control algorithms are executed in the AMC. Fairchild provides the Motor Control Development System (MCDS) IDE and MCDS Programming Kit for users to develop software, execute In System Programming (ISP), and perform online debugging.

Figure 1 shows a typical application of the FCM8531.

Advanced Motor Controller (AMC)

- Configurable Processing Core
  - Sensorless FOC with Speed Integral Method
  - Sensorless FOC with Sliding Mode
  - Hall Interface
- Space Vector Modulation (SVM)
- Sine-Wave and Square-Wave Generator
- Programmable Current Leading Phase Control
- Programmable Dead Time

Embedded MCU

- MCS®51 Compatible
- 63% of Instructions' Execution Cycle < 3 System Clocks (3T)
- Memory Size:
  - 12K Bytes Flash Program Memory
  - 256 +1K Bytes SRAM Data Memory
- Extended 16-Bit Multiplication / Division Unit (MDU)
- ≤17 General-Purpose Input / Output (GPIO) Pins
- Full Duplex Serial Interface (UART)
- I^2C Interface
- Serial Peripheral Interface (SPI)
- Three External Interrupts
- Three 16-Bit Timers
- Programmable 15-Bit Watchdog Timer (WDT)
- Built-in Power-On Reset (POR)
- Built-in Clock Generator
- Two-Level Program Memory Lock

ADC and DAC

- 8-Channel, 10-Bit ADC
  - Auto-Trigger Sample and Hold
  - Four Trigger Mode Selections
  - Three Pre-Amp Gain Selections
- 1 Channel, 8-Bit DAC

Protections

- Three-Level Over-Current Protection (OCP)

Power Management

- IDLE Mode, STOP Mode, and SLEEP Mode

Development Supports

- In System Programming (ISP)
- On-Chip Debug Support (OCDS)

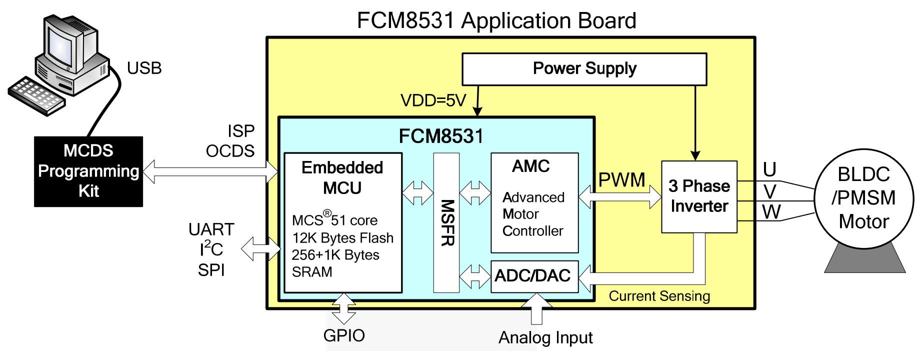

Figure 1. Application Block Diagram

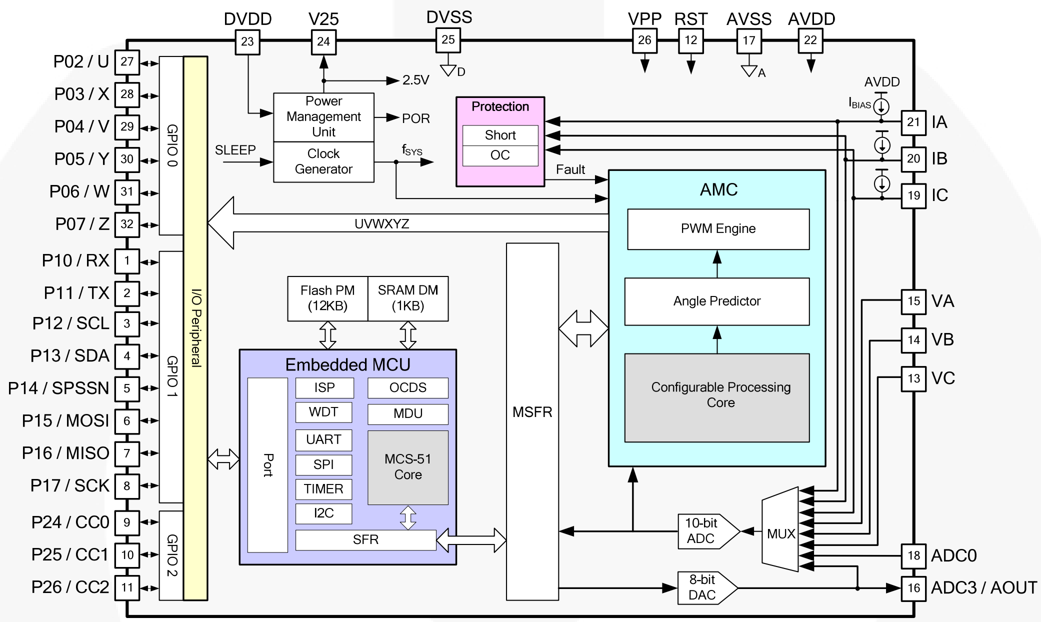

Figure 2. Block Diagram

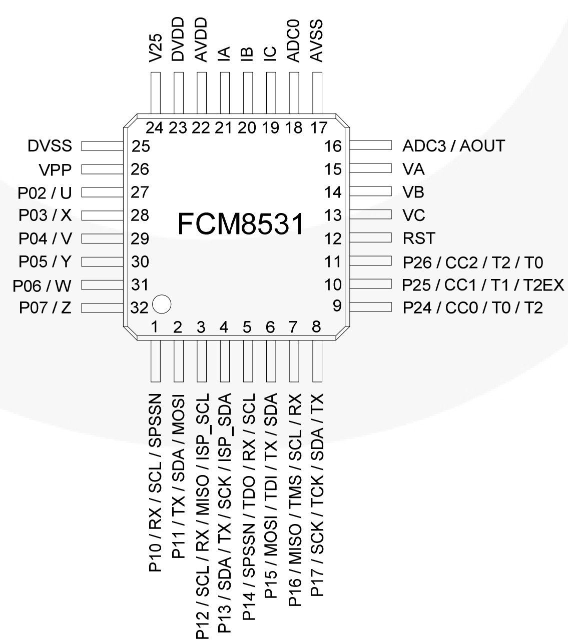

Figure 3. Pin Configuration

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2. MSFRs (Motor Special Function Registers)

MSFRs are registers used exclusively for motor control modules; those are accessed through SFRs.

Parameters such as motor control, Hall signal configure, waveform type, PWM engine, and over-current protection level can be set in MSFRs.

The Analog-to-Digital Converter (ADC) and controller statuses; such as Fault status, Hall status, and PWM status; can be obtained via MSFRs.

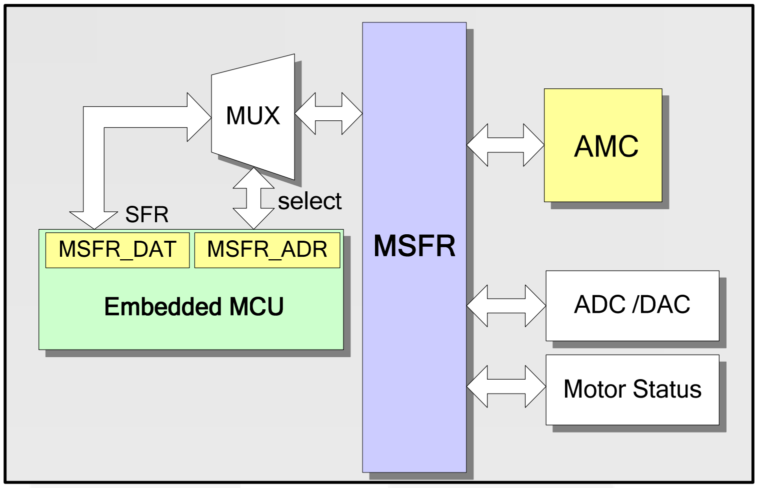

Figure 4. MSFR Block Diagram

2.1. MSFRs Map

Table 1. MSFRs Map

Hex	X000	X001	X010	X011	X100	X101	X110	X111	Hex
40	Reserved	Reserved	Reserved	SLEEP	OCH	OCL	SHORT	DACO	47
38	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ANGLE	MSTAT	3F
30	ADC0L	ADC0H					ADC3L	ADC3H	37
28	VAL	VAH	VBL	VBH	VCL	VCH	ADCINX	Reserved	2F
20	IAL	IAH	IBL	IBH	ICL	ICH	OCCNTL	OCSTA	27
18	HALMXU	HALFLT	HALSTA	HALINT	HPERL	HPERM	HPERH	ADCCFG	1F
10	Reserved	Reserved		Reserved	Reserved	Reserved	Reserved	Reserved	17
08	PWMCFG	SAWCNTL	SPRDL	SPRDH	Reserved	Reserved	Reserved	Reserved	0F
00	MCNTL	ANGCTL	AS	ANGDET	DUTYAL	DUTYA	Reserved	Reserved	07

2.2. MSFRs Description

Table 2. Motor Special Function Registers (MSFRs)

Byte Name	Address	Reset	Bit	Type	Name	Description
MCNTL	00h	00h	Motor Control			
			7	W	Reserved	Must Be Set to 0
			6	R/W	AMC_RST	Reset AMC Core, Active HIGH
			5	R/W	SIN_TBL	Sine-Wave Table Select 0: Default Sine-Wave Table 1: User-Defined Table
			4	R/W	SQU_TBL	Square-Wave Table Select 0: Default Square-Wave Table 1: User-Defined Table
			3:2	W	Reserved	Must Be Set to 0
			1	R/W	CW	Rotation Direction 0: CCW 1: CW
			0	R/W	ST/FREE	FREE or START 0: FREE 1: START
ANGCTL	01h	00h	Angle Control			
			7		Reserved	Must Be Set to 0
			6	R/W	ARNG	Angle Predictor Range 0: Low-Speed 1: Normal
			5	W	Reserved	Must Be Set to 0
			4:0	N/A	N/A	N/A
AS	02h	00h	Angle Shift			
			7	N/A	N/A	N/A
			6:0	R/W	ANG	Shift Angle 0 - 127 Mapping to 0 – 120°
ANGDET	03h	00h	Angle Predictor Configuration			
			7	R/W	SIN_MAU	Sine-Wave Enable Mode 0: Automatically 1: Enabled by SIN_EA
			6	R/W	SIN_EA	Sine-Wave Enable 0: Disabled 1: Enabled
			5	N/A	N/A	N/A
			4:0	W	Reserved	Must Be Set to 0
DUTYAL	04h	00h	DUTY Control			
			7:5	R/W	DUTY[2:0]	Square-Wave Mode: DUTY[2:0] Sine-Wave Mode: DUTY[2]
			4	N/A	N/A	N/A
			3	W	Reserved	Must Be Set to 0
			2	W	Reserved	Must Be Set to 0
			1	W	Reserved	Must Be Set to 0
			0	W	Reserved	Must Be Set to 0
DUTYA	05h	00h	DUTY			
			7:0	R/W	DUTY[10:3]	DUTY[10:3]
PWMCFG	08h	00h	PWM Configuration			
			7:6	R/W	Reserved	Must Be Set to 0
			5:4	R/W	DT[1:0]	Dead Time Setting

Byte Name	Address	Reset	Bit	Type	Name	Description
						00: 12 × t_{SYS} (0.4 μs at 30 MHz) 01: 36 × t_{SYS} (1.2 μs at 30 MHz) 10: 60 × t_{SYS} (2.0 μs at 30 MHz) 11: 96 × t_{SYS} (3.2 μs at 30 MHz)
			3	R/W	Reserved	Must Be Set to 0
			2	R/W	SYNCOFF	Synchronous Rectification (SR) 0: Enabled 1: Disabled
			1	R/W	WMC	Leading Angle Function in Square-Wave Mode 0: Disabled 1: Enabled
			0	W	Reserved	Must Be Set to 0
SAWCNTL	09h	00h	SAW Configuration			
			7	R/W	ASCAL	Auto-scale 0: Disabled 1: Enabled
			6:5	R/W	SAWMOD	SAW Mode 00: Disable 01: UP-DOWN Mode 10: UP Mode 11: DOWN Mode
			4:3	R/W	PRESCAL	SAW Clock Pre-Scale 00: f_{SYS} 01: $f_{SYS}/2$ 10: $f_{SYS}/4$ 11: $f_{SYS}/8$
			2:0	R/W	POSTCAL	SAW Clock Post-Scale 000: 1 001: 1/2 010: 1/3 011: 1/4 100: 1/5 101: 1/6 110: 1/7 111: 1/8
SPRDL	0Ah	E0h	SAW Period			
			7:5	R/W	SPRD[2:0]	SAW Period[2:0]
			4:0	N/A	N/A	N/A
SPRDH	0Bh	FFh	SAW Period			
			7:0	R/W	SPRD[10:3]	SAW Period[10:3]
Reserved	0Ch - 11h	00h		W	Reserved	Must Be Set to 0
Reserved	13h - 17h	00h		W	Reserved	Must Be Set to 0
HALMUX	18h	00h	Hall Signal Inversion			
			7	N/A	N/A	N/A
			6	W	Reserved	Must Be Set to 1
			5	R/W	HC_INV	Hall C Input Invert 0: Non-invert 1: Invert
			4	R/W	HB_INV	Hall B Input Invert 0: Non-invert 1: Invert
			3	R/W	HA_INV	Hall A Input Invert 0: Non-invert 1: Invert

Byte Name	Address	Reset	Bit	Type	Name	Description
			2:0	W	Reserved	Must Be Set to 0
HALFLT	19h	00h	Hall Configuration			
			7	R/W	HAL_REG	Hall Regulation 0: Disabled 1: Enabled
			6:4	R/W	HAL_BNK	Hall Blanking Time 000: Disable 001: (5 - 6) × 1024 t_{SYS} (170.7 - 204.8 μs at 30 MHz) 010: (9 - 10) × 1024 t_{SYS} 011: (17 - 18) × 1024 t_{SYS} 100: (33 - 34) × 1024 t_{SYS} 101: (65 - 66) × 1024 t_{SYS} 110: (129 - 130) × 1024 t_{SYS} 111: (257 - 258) × 1024 t_{SYS}
			3	R/W	HAL_AVG	Hall Period Average Mode 0: Disabled 1: Enabled
			2:0	R/W	HAL_DEB	Hall Debounce Time 000: Disabled (2 - 3 t_{SYS}) 001: (2 - 3) × 64 t_{SYS} (4.3 - 6.3 μs at 30 MHz) 010: (2 - 3) × 128 t_{SYS} 011: (2 - 3) × 256 t_{SYS} 100: (2 - 3) × 512 t_{SYS} 101: (2 - 3) × 1024 t_{SYS} 110: (2 - 3) × 2048 t_{SYS} 111: (2 - 3) × 4096 t_{SYS}
HALSTA	1Ah	00h	Hall State			
			7:3		Reserved	Reserved
			2	R	HALL C_IN	Hall C Status In Angle Predictor
			1	R	HALL B_IN	Hall B Status In Angle Predictor
			0	R	HALL A_IN	Hall A Status In Angle Predictor
HALINT	1Bh	00h	Hall Interrupt Configuration			
			7:4	N/A	N/A	N/A
			3:2	R/W	HTMR_OUT	Hall Period Interrupt (EX8) 00: Disabled 01: If Hall Counter [17] = 1 10: If Hall Counter [18] = 1 11: If Hall Counter [19] = 1
			1:0	R/W	HALL_INT	Hall Edge Interrupt (EX10) 00: Disabled 01: Rise/Fall Edge 10: Rise Edge 11: Fall Edge
HPERL	1Ch	00h	Hall Period			
			7:0	R	HPER [7:0]	Hall Period [7:0]
HPERM	1Dh	00h	Hall Period			
			7:0	R	HPER [15:8]	Hall Period [15:8]
HPERH	1Eh	00h	Hall Period			
			7:4	N/A	N/A	N/A
			3:0	R	HPER[19:16]	Hall Period [19:16]

Byte Name	Address	Reset	Bit	Type	Name	Description
ADCCFG	1Fh	00h	ADC Configuration			
			7	W	ADC_ST	ADC Signal Trigger Enable, ADC_TR= Timer Mode Only 0: N/A 1: ADC Convert Trigger (One Shot, Auto Clear)
			6	N/A	N/A	N/A
			5	R/W	DAC_EA	DAC Output (To AOUT Pin) 0: Disabled 1: Enabled
			4	R/W	AD_CK	ADC Clock 0: $f_{SYS}/16$ 1: $f_{SYS}/32$
			3:2	R/W	FS_DIV	Sampling Rate Divider 00: 1 01: 1/2 10: 1/4 11: 1/8
			1:0	R/W	ADC_TR	ADC Trigger Mode Select 00: SAW Top 01: SAW Bottom 10: TMR0 Overflow
IAL	20h	0Ch	ADC IA Configuration and ADC IA[1:0]			
			7:6	R	IA [1:0]	ADC IA [1:0]
			5:4	N/A	N/A	N/A
			3	W	Reserved	Must Be Set to 1
			2	R/W	Bias_A0	Bias Current 0: Disabled 1: Enabled
			1:0	R/W	GIA	Pre-Amp Gain 00: ×1 01: ×2 10: ×4
IAH	21h	00h	ADC IA[10:2]			
			7:0	R	IA [10:2]	ADC IA [10:2]
IBL	22h	0Ch	ADC IB Configuration and ADC IB[1:0]			
			7:6	R	IB [1:0]	ADC IB [1:0]
			5:4	N/A	N/A	N/A
			3	W	Reserved	Must Be Set to 1
			2	R/W	Bias_B0	Bias Current 0: Disabled 1: Enabled
			1:0	R/W	GIB	Pre-Amp Gain 00: ×1 01: ×2 10: ×4
IBH	23h	00h	ADC IB[10:2]			
			7:0	R	IB [10:2]	ADC IB [10:2]
ICL	24h	0Ch	ADC IC Configuration and ADC IC[1:0]			
			7:6	R	IC [1:0]	ADC IC [1:0]
			5:4	N/A	N/A	N/A
			3	W	Reserved	Must Be Set to 1
			2	R/W	Bias_C0	Bias Current 0: Disabled 1: Enabled

Byte Name	Address	Reset	Bit	Type	Name	Description
			1:0	R/W	GIC	Pre-Amp Gain 00: ×1 01: ×2 10: ×4
ICH	25h	00h	ADC IC[10:2]			
			7:0	R	IC [10:2]	ADC IC [10:2]
OCCNTL	26h	00h	Over-Current Protection Control Register			
			7:6	R/W	OC_DEB	OC Protection Debounce Time 00: 600 - 900 ns 01: 900 – 1200 ns 10: 1200 - 1500 ns 11: 1500 - 1800 ns
			5	R/W	OCCH_EA	Phase C OCH Protection 0: Disabled 1: Enabled
			4	R/W	OCBH_EA	Phase B OCH Protection 0: Disabled 1: Enabled
			3	R/W	OCAH_EA	Phase A OCH Protection 0: Disabled 1: Enabled
			2	R/W	OCCL_EA	Phase C OCL Protection 0: Disabled 1: Enabled
			1	R/W	OCBL_EA	Phase B OCL Protection 0: Disabled 1: Enabled
			0	R/W	OCAL_EA	Phase A OCL Protection 0: Disabled 1: Enabled
OCSTA	27h	00h	OC Protection State			
			7:6	N/A	N/A	N/A
			5	R	OCCH	Phase C OCH Flag, Auto Clear after Read
			4	R	OCBH	Phase B OCH Flag, Auto Clear after Read
			3	R	OCAH	Phase A OCH Flag, Auto Clear after Read
			2	R	OCCL	Phase C OCL Flag, Auto Clear after Read
			1	R	OCBL	Phase B OCL Flag, Auto Clear after Read
			0	R	OCAL	Phase A OCL Flag, Auto Clear after Read
VAL	28h	00h	ADC VA Configuration and ADC VA[1:0]			
			7:6	R	VA [1:0]	ADC VA[1:0]
			5:2	N/A	N/A	N/A
			1:0	R/W	GVA	Pre-Amp Gain 00: ×1 01: ×2 10: ×4
VAH	29h	00h	ADC VA[10:2]			
			7:0	R	VA [10:2]	ADC VA[10:2]
VBL	2Ah	00h	ADC VB Configuration and ADC VB[1:0]			
			7:6	R	VB [1:0]	ADC VB[1:0]
			5:2	N/A	N/A	N/A

Byte Name	Address	Reset	Bit	Type	Name	Description
			1:0	R/W	GVB	Pre-Amp Gain 00: ×1 01: ×2 10: ×4
VBH	2Bh	00h	ADC VB[10:2]			
			7:0	R	VB [10:2]	ADC VB [10:2]
VCL	2Ch	00h	ADC VC Configuration and ADC VC[1:0]			
			7:6	R	VC [1:0]	ADC VC [1:0]
			5:2	N/A	N/A	N/A
			1:0	R/W	GVC	Pre-Amp Gain 00: ×1 01: ×2 10: ×4
VCH	2Dh	00h	ADC VC[10:2]			
			7:0	R	VC [10:2]	ADC VC [10:2]
ADCINX	2Eh	00h	ADC Index			
			7:4		Reserved	Reserved
			3:2	R	AD_INX[3:2]	Current ADC Channel Index 00: VA 01: VB 10: VC 11: ADC0 or ADC3 (need check AD_INX[1:0])
			1:0	R	AD_INX[1:0]	Index of ADC0/ADC3 00: ADC0 01: Reserved 10: Reserved 11: ADC3
Reserved	2Fh				Reserved	Reserved
ADC0L	30h	00h	ADC0 Configuration and ADC0[1:0]			
			7:6	R	ADC0[1:0]	ADC0[1:0]
			5:2	N/A	N/A	N/A
			1:0	R/W	GADC0	Pre-Amp Gain 00: ×1 01: ×2 10: ×4
ADC0H	31h	00h	ADC0[10:2]			
			7:0	R	ADC0[10:2]	ADC0[10:2]
ADC3L	36h	00h	ADC3 Configuration and ADC3[1:0]			
			7:6	R	ADC3[1:0]	ADC3[1:0]
			5:2	N/A	N/A	N/A
			1:0	R/W	GADC3	Pre-Amp Gain 00: ×1 01: ×2 10: ×4
ADC3H	37h	00h	ADC3 [10:2]			
			7:0	R	ADC3 [10:2]	ADC3 [10:2]
Reserved	38h - 3Dh	00h			Reserved	Reserved

Byte Name	Address	Reset	Bit	Type	Name	Description
ANGLE	3Eh	00h	Angle Predictor Result			
			7:0	R	ANGLE	0 - 191 Mapping to 0 – 360°
MSTAT	3Fh	00h	Motor Status			
			7	R	VDD_TEST	For Internal Testing
			6	R	H_SLOW	Hall Period Overflow
			5	R	SHORT_A	IA SHORT
			4	R	SHORT_B	IB SHORT
			3	R	SHORT_C	IC SHORT
			2	R	H_ERR	Hall Error (HA/HB/HC = 1/1/1 or 0/0/0)
			1	R	S_ACT	Operating Mode 0: Square-Wave 1: Sine-Wave
			0	R	DIR	Hall Direction
Reserved	40 - 42h	00h	Reserved			
SLEEP	43h	00h	SLEEP Mode			
			7:3	N/A	N/A	N/A
			2	W	Reserved	Must Be Set to 1
			1	W	Reserved	Must Be Set to 0
			0	R/W	Sleep	SLEEP Mode 0: Disabled 1: Enabled
OCH	44h	FFh	Positive OC Protection Level			
			7:0	R/W	OCH	Positive OC Protection Level (00h - FFh mapping to 0 – 4 V)
OCL	45h	10h	Negative OC Protection Level			
			7:0	R/W	OCL	Negative OC Protection Level (00h - FFh Mapping to 0 - 4 V)
SHORT	46h	FFh	SHORT Detection Level			
			7:0	R/W	SHORT	SHORT Detection Level (00h - FFh Mapping to 0 - 4 V)
DACO	47h	00h	AOUT Output Level			
			7:0	R/W	DACO	AOUT Output Level (00h - FFh Mapping to 0 - 4 V)

3. Advanced Motor Controller

The Advanced Motor Controller (AMC) is used for driving motors that consist of several motor control modules, such as configurable processing core, PWM engine, and angle predictor. Depending on the application, the configurable processing core can be configured with suitable AMC library to perform different motor control algorithms, such as FOC and sensorless control.

For example, if the Sensorless library is used as the control algorithm, the configurable processing core obtains the motor current via the internal ADC to estimate the rotor angle. After that, the PWM engine provides PWM output drive signals to set the correct rotor angle.

If the configurable processing core is configured with the Hall Interface library, the rotor position information is inputted through the GPIO and the rotor angle is estimated by the angle predictor. The PWM engine can provide the appropriate PWM output drive signals for driving motors.

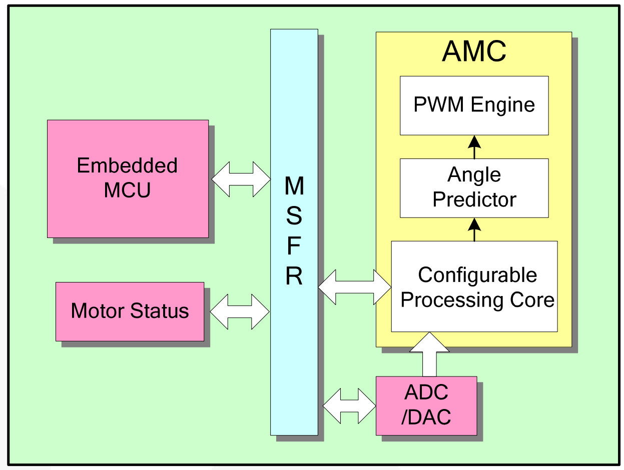

Figure 5. AMC Block Diagram

3.1. Reset

The AMC_RST bit of MSFR MCNTL (00h) is used to reset the AMC processing core. Resetting the AMC processing core in the initial stage is recommended.

3.2. Angle Predictor

When the Hall Interface library is used for Sine-wave control, the Hall signal is used to accurately predict the rotor angle of the motor. This predicted angle provides the Space Vector Modulation (SVM) to generate space vector pulses. The angle predictor includes a Hall signal filter, Phase-Lock Loop (PLL), leading angle shifter, and angle encoder.

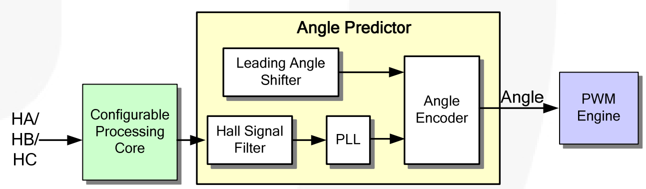

Figure 6. Angle Block Diagram

Table 3. Angle Predictor Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
ANGCTL (01h)	Reserved	ARNG	Reserved	N/A					00h
AS (02h)	N/A	ANG							00h
ANGDET (03h)	SIN_MAU	SIN_EA	N/A	Reserved					00h
HALMUX (18h)	N/A	Reserved	HC_INV	HB_INV	HA_INV	Reserved			00h
HALFLT (19h)	HAL_REG	HAL_BNK			HAL_AVG	HAL_DEB			00h
HALSTA (1Ah)	Reserved					HALL_IN			00h
HALINT (1Bh)	N/A				HTMR_OUT		HALL_INT		00h
HPERL (1Ch)	HPER[7:0]								00h
HPERM (1Dh)	HPER[15:8]								00h
HPERH (1Eh)	N/A				HPER[19:16]				00h
ANGLE (3Eh)	ANGLE								00h

3.2.2 Hall Signal Filter

Functions of the Hall signal filter, set by the MSFR HALFLT (19h), include the debounce, blanking, Hall signal regulation, Hall signal average, and Hall signal inversion.

Debounce:
Noises or bounces may be involved in input signals, usually resulting in incorrect angle prediction. The MSFR HALFLT (19h) can set the debounce time to filter out the involved noises. While the input signal is changing, the debounce function holds the signal for a debounce time until the change is confirmed *(see Figure 7)*.

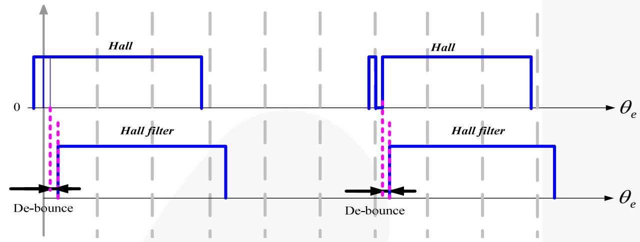

Figure 7. Hall Filter Debounce

Blanking:
Users can set the blanking time through the HALFLT. Hall signals are not allowed to be updated for a blanking time once a change in the Hall signal is confirmed *(see Figure 8)*.

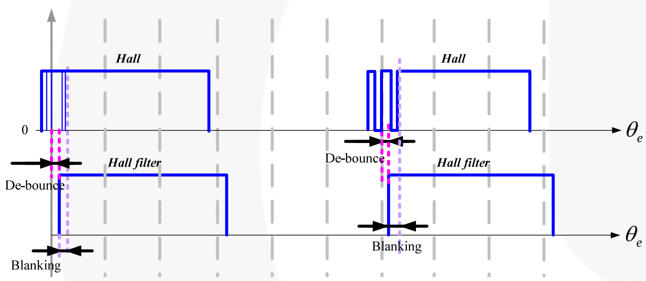

Figure 8. Hall Filter Blanking

Regulation:
This feature makes PWM outputs remain its current state if the Hall signals return to its previous state.

Without Hall regulation; when Hall signals the return to the previous states (*see Figure 9*), the PWM output returns to previous state (corresponding to Hall state), so the PWM U output is off. However, with the Hall regulation, the PWM U remains in the current state and keeps outputting the PWM signal.

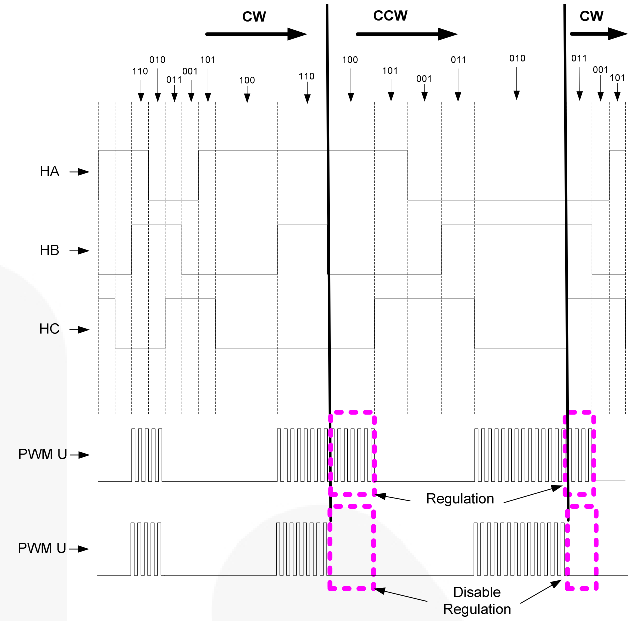

Figure 9. Hall Regulation

Average:
The value stored in the Hall period register represents the time of the most recent 60-degree electrical angle based on the system clock. A digital filter is enabled by the average function to reduce the variation of periods. It is invoked by setting MSFR HALFLT (19h)[3].

Invert:
Set MSFR HALMUX (18h)[5:3] to invert the Hall signal before entering the PLL (*see Figure 10*).

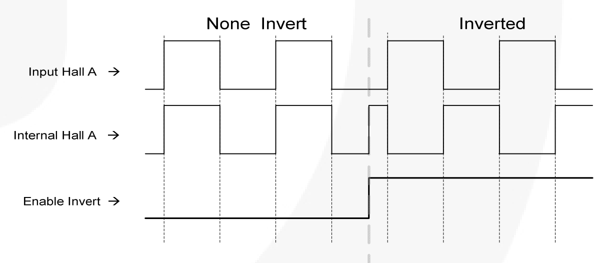

Figure 10. Hall Invert

3.2.3 Phase-Lock Loop (PLL)

The PLL uses Hall signals as input signals and detects changes in every 60-degree electrical angle to predict the rotor position. The motor starts in Square-Wave Mode then enters Sine-Wave Mode once the PLL locks the Hall signals.

There are two modes for entering the Sine-wave driving.

Automatic Mode (Default):
MSFR ANGDET (03h)[7:6] = b'00. Once the rotation speed is stable and higher than the required minimum speed, the PWM drive signal is automatically changed from Square-Wave Mode to Sine-Wave Mode. If the rotation speed is unstable or is below the required minimum speed, it exits Sine-Wave Mode. The enter/exit condition can be set by MSFR ANGDET (03h)[4:0].

Manual Mode:
MSFR ANGDET (03h)[7:6] = b'11. The PWM signal is forced to drive in Sine-Wave Mode. This mode is not recommended.

There are two selectable frequency ranges for the Hall signal input: Low-Speed Mode (PLL clock = f_{SYS}/64) and Normal Mode (PLL clock = f_{SYS}/4). Fairchild recommends using Normal Mode for general motor applications. Low-Speed Mode can be selected for very low-speed operations.

Table 4. Angle Predictor Range (f_{SYS} = 30 MHz)

ANGCTL (01h)[6]	Mode	Hall Frequency
0	Low-Speed	0.1 – 360 Hz
1	Normal	1.5 – 1200 Hz

The conversion between Hall frequency and motor speed is defined in the following formula:

$$\mathrm{RPM} = \frac{120 \times \text{Hall freq.}}{\text{Poles}} \quad (1)$$

where poles is number of magnetic poles in the motor.

The Hall Period register is a 20-bit counter that represents the time of the last 60-degree electrical angle based on the system clock. MSFR HPERL (1Ch) stores bits 0 - 7; MSFR HPERM (1Dh) stores bits 8 - 15; MSFR HPERH (1Eh) stores bits 16 - 19. An example is given below to show how a Hall period is converted to real rotation speed in RPM.

Example: Hall Period Register = 000515h, System Clock = 30 MHz, Motor-Pole = 4

Hall Frequency Range = Low Speed Mode

PLL Clock Period → 64 / (30 × 106) = 2.133 (μ s)

Hall Period Register → 000515h = 1301 (Hexadecimal to Decimal)

1301 × 2.133 = 2.775033 (ms / 60°), 2.775033 × 6 = 16.650198 (ms / 360°)

1 / 16.65 ≈ 60 (Hz), Hall Frequency = 60 (Hz)

$$\mathrm{RPM} = \frac{120 \times 60}{4} = 1800\ (\mathrm{RPM})$$

The resolution could be insufficient while the motor is rotating at very high speed; however, switching the frequency mode to the Normal Mode improves it by using higher PLL clock frequency. An example is given below to show the difference between the two modes.

Example: System Clock=30 MHz, Hall Frequency = 350 Hz

When Hall Frequency Range=Low Speed Mode

PLL Clock Period → 64 / (30 × 106)=2.133 (μ s)

Hall Period = 1 / 350=2.857 (ms / 360°), 2.857 / 6=0.476 (ms / 60°)

(0.476 ms) / (2.133 μ s)=223.16 (0000DFh)

HPERH(1Eh)	HPERM(1Dh)	HPERL(1Ch)	
00	00	DF	Register data

Figure 11. Hall Period Register - 1

When Hall Frequency Range = Normal Mode

PLL Clock Period → 4 / (30 × 106) = 0.133 (μ s)

(0.476 ms) / (0.133 μ s) = 3578.94 (000DFAh)

HPERH(1Eh)	HPERM(1Dh)	HPERL(1Ch)	
00	0D	FA	Register data

Figure 12. Hall Period Register – 2

3.2.4 Leading Angle Shifter

As the motor is rotating, a phase lag (Δθ) between current and Back Electromotive Force (BEMF) may occur because of the motor's winding inductance. Generally, the phase lag gets larger as the speed increases and the phase lag affects motor efficiency. Usually, the best performance is achieved once the current and the BEMF are in phase *(see Figure 13).*

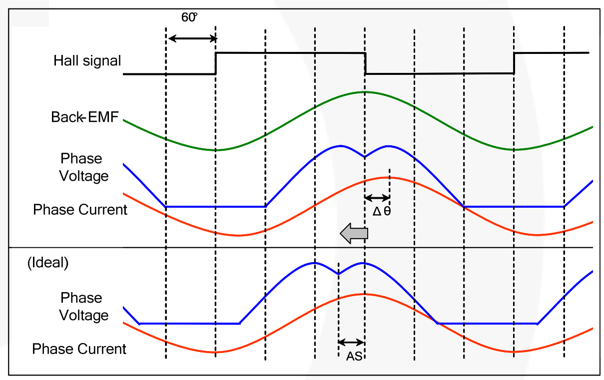

Figure 13. Phase Shift

The leading angle shifter is capable of compensating the phase lag by shifting PWM ahead. MSFR AS (02h) is a 7-bit register that can set the leading angle shifting from 0 to 120° ahead.

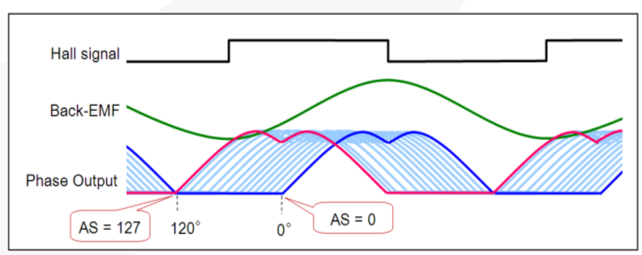

Figure 14. Angle Shift

3.2.5 Angle Encoder

The PWM engine outputs PWM signals according to the angle encoder. The angle encoder sums the PLL calculation results and the leading angle shifter setting in one angle, MSFR ANGLE (3Eh).

3.3. PWM Engine

The PWM engine includes four circuit modules: SAW generator, square-wave PWM generator, sine-wave PWM generator, and PWM MUX.

The motor starts in Square-Wave Mode, and then enters into Sine-Wave Mode once the PLL locks the Hall signals. By setting the MSFR ANGDET (03h), users can determine whether the PWM engine is working in Square-Wave Mode or Sine-Wave Mode after the PLL is in lock *(refer to Section 3.2.3.)*

Table 5. PWM Engine Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
ANGDET (03h)	SIN_MAU	SIN_EA	N/A	Reserved					00h
DUTYAL (04h)	DUTY[2:0]			N/A	Reserved				00h
DUTYA (05h)	DUTY[10:3]								00h
PWMCFG (08h)	Reserved		DT[1:0]		Reserved	SYNCOFF	WMC	Reserved	00h
SAWCNTL (09h)	ASCAL	SAWMOD		PRESCAL		POSTCAL			00h
SPRDL (0Ah)	SPRD[2:0]			N/A					E0h
SPRDH (0Bh)	SPRD[10:3]								FFh

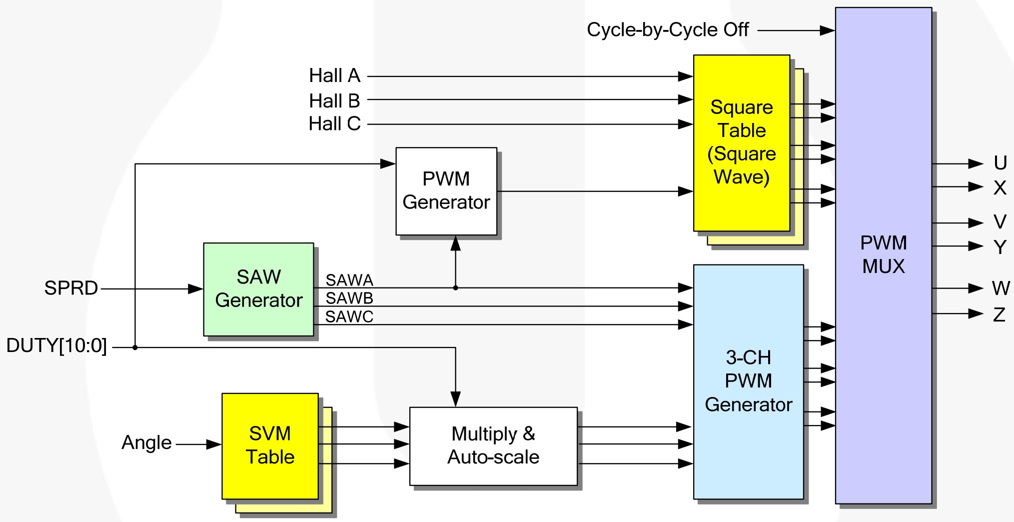

Figure 15. PWM Block Diagram

3.3.1 SAW Generator

The clock source of the SAW generator is provided from the result of the system clock passing through two frequency dividers: pre-scale module and post-scale module. It provides the pulses (SAW clock) for the 11-bit counter inside the SAW generator *(see Figure 16)*.

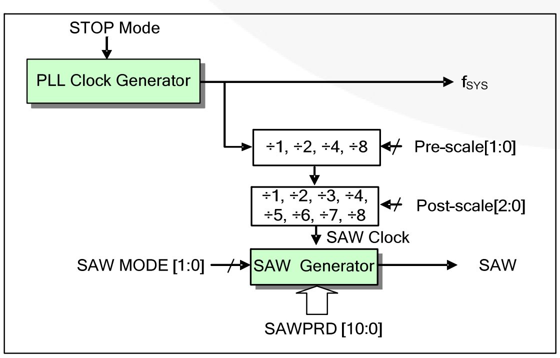

Figure 16. Pre-Scale and Post-Scale

There are three modes of carrier waveforms: Up Mode, Down Mode, and Up-Down Mode; selected by the SAWMOD bit in MSFR SAWCNTL (09h) *(see Figure 17)*.

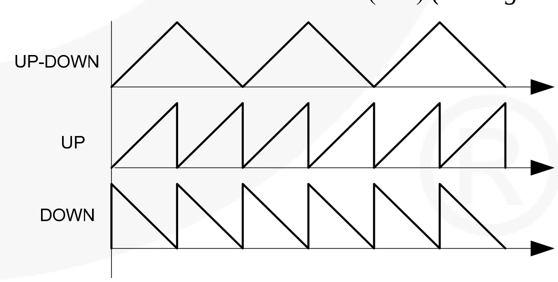

Figure 17. SAW Mode

In Up-Down Mode:

$$f_{PWM} = \text{SAW Clock} / (\text{SAW Period} \times 2) \quad (2)$$

In Up Mode or Down Mode:

$$f_{PWM} = \text{SAW Clock} / \text{SAW Period} \quad (3)$$

The SAW period is determined by MSFR SPRDH (0Bh) and MSFR SPRDL (0Ah) (11-bit, left aligned), as shown in Figure 18. Shift the actual SAW Period five bits left before writing it into the registers. The PWM duty ratio resolution is a ratio to SAW period. The resolution gets higher when SAW period increases.

SPRDH (0Bh) SPRDL(0Ah)

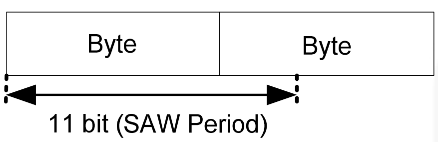

Figure 18. SAW Period Register

The pre-scale and the post-scale are set by MSFR SAWCNTL (09h)[4:0]. The formula and the description of SAWCNTL are:

$$\text{SAW Clock Frequency} = f_{SYS} / (\text{Post-Scale} \times \text{Pre-Scale}) \quad (4)$$

Example: To obtain an Up-Down Mode PWM frequency of 20 kHz when the system frequency is 30 MHz (from Equation (2)):

SAW Period = 30 MHz / (20 kHz × 2) = 750 = 2EEh

The SAW period corresponding to a 20 kHz PWM frequency, 750 (2EEh in hexadecimal), is determined.

Shift “2EEh” five bits left and the result is “5DC0h”. Write 5Dh and C0h into registers SPRDH (0Bh) and SPRDL (0Ah) to complete the setting.

3.3.2 Square-Wave Mode

The square-wave PWM generator generates square-wave PWM signals and its default pattern is based on the built-in default square-wave table.

In addition to generating default square-wave PWM output waveforms, a customizable user-define square-wave table is also provided so that users can define customized square-wave waveforms according to application requirements.

The motor starts in Square-Wave Mode and remains in Square-Wave mode after PLL is in lock if the highest two bits of ANGDET (03h)[7:6] are set to b’10.

The PWM on-time in a PWM duty is proportional to a ratio of the DUTY[10:0] to the SAW period. For example, when the DUTY[10:0] = 200h and the SAW period = 400h; the PWM on-time = 50%. Similarly, the PWM on-time = 25% when the SAW period = 800h.

The DUTY[10:0] in Square-Wave Mode is an 11-bit register, which is composed of DUTYA (05h) and the highest three bits of DUTYAL (04h). DUTYA is a high-order byte.

As shown in Figure 19, when a count value of the PWM on-time is the same as that of the SAW period, PWM has the largest on-time. The on-time setting should fall into the range of the SAW period.

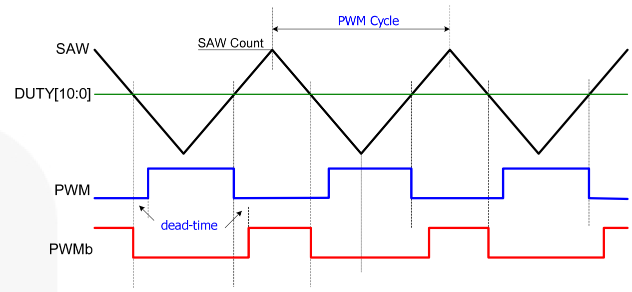

Figure 19. PWM Output

Appropriate PWM output signals are determined by the pattern of the Hall input signals or the Hall register, while direction is determined by the CW setting.

Table 6 shows PWM output signals in each Hall status regarding to CW.

Table 6. Defaulted Square-Wave PWM Output

CW	Hall Status (HA HB HC)	U-V-W	X-Y-Z
X	0 0 0	0 0 0	0 0 0
X	1 1 1	0 0 0	0 0 0
1	0 0 1	P 0 0	Pb 1 0
1	0 1 1	0 0 P	0 1 Pb
1	0 1 0	0 0 P	1 0 Pb
1	1 1 0	0 P 0	1 Pb 0
1	1 0 0	0 P 0	0 Pb 1
1	1 0 1	P 0 0	Pb 0 1
0	1 0 1	0 0 P	1 0 Pb
0	1 0 0	0 0 P	0 1 Pb
0	1 1 0	P 0 0	Pb 1 0
0	0 1 0	P 0 0	Pb 0 1
0	0 1 1	0 P 0	0 Pb 1
0	0 0 1	0 P 0	1 Pb 0

Notes:
1. X: Don’t care
2. P: PWM
3. Pb: PWM inverse

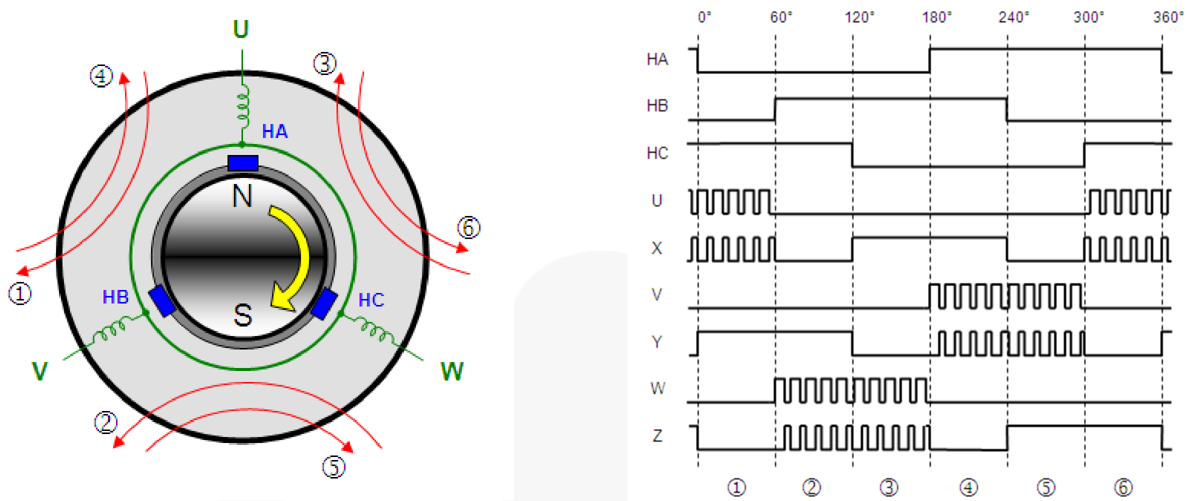

Figure 20. Square-Wave Mode (CW = 1)

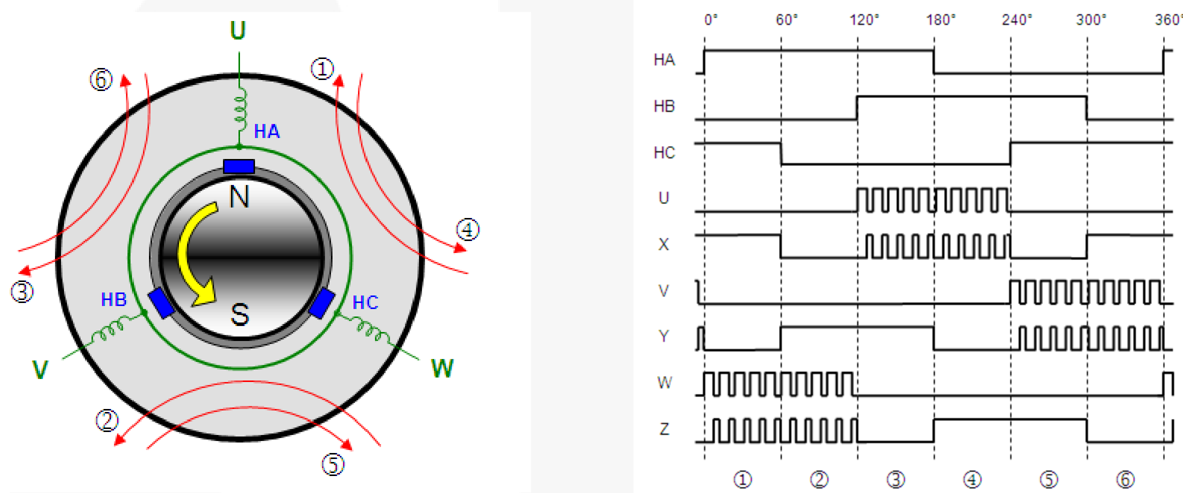

Figure 21. Square-Wave Mode (CW = 0)

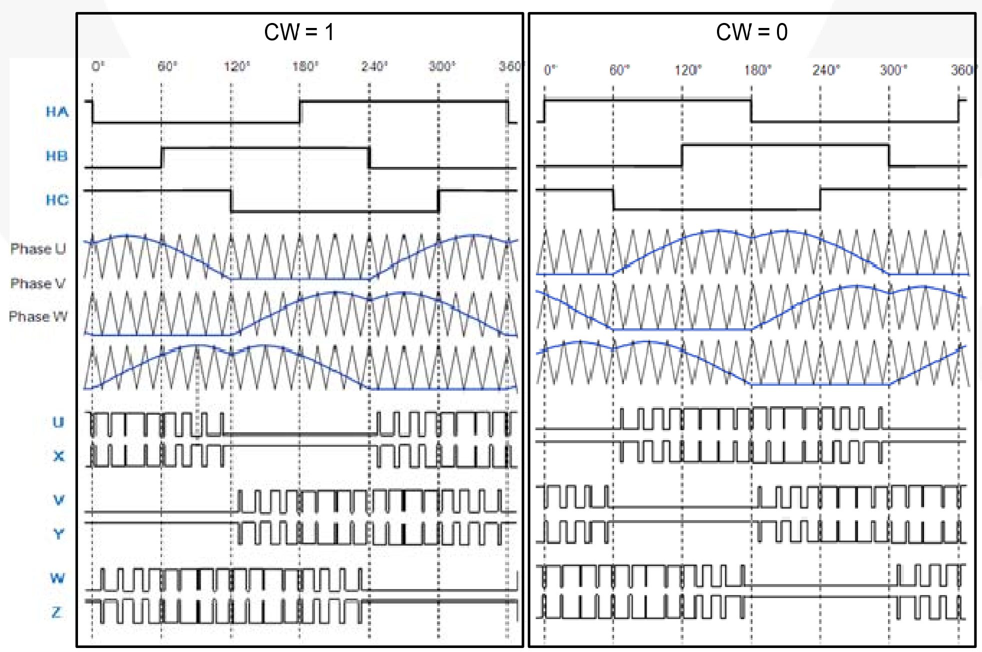

Figure 22. Sine-Wave Mode

In Table 6 above, the Pb (PWM inverse) can be turned off by disabling the Synchronous Rectification function. It is invoked by setting MSFR PWMCFG (08h)[2]. The default is enabled.

3.3.3 Sine-Wave Mode

Figure 22 shows that the modulation waveform (blue curve) is generated from the SVM table according to the predicted angle. The modulation waveform is compared with the SAW to produce a sine-wave PWM signal. The amplitude of the modulation waveform is determined by DUTY[10:2] register. Unlike the Square-Wave Mode, the DUTY[1:0] is neglected in the Sine-Wave Mode.

3.3.4 Auto SAW Alignment Function

If the auto SAW alignment feature is turned on in the MSFR SAWCNTL, DUTY's highest bit (bit 10) aligns with the valid highest bit of the SAW period. It is convenient for users to control the duty ratio through only a byte of register, DUTYA, without shifting.

Example:
The SAW period is an 11-bit register. For simplicity, it is left-shifted five bits. For example, when SAW period = 3FFh, it becomes 7FE0h. So does DUTY[10:0] and 5-bit shifted DUTY[10:0] is called DUTY.

When auto SAW alignment is turned off and the PWM mode is Square-Wave Mode; if the SAW period is 7FE0h, set DUTY= 7FE0h to get PWM output with the largest duty (*see Figure 23*).

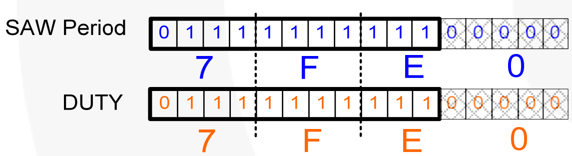

Figure 23. Auto SAW Alignment Disabled

When the Auto SAW Alignment is turned on, however, users should set DUTY = FFC0h for the largest duty because DUTY is aligned to the first valid bit of the SAW Period (*see Figure 24*).

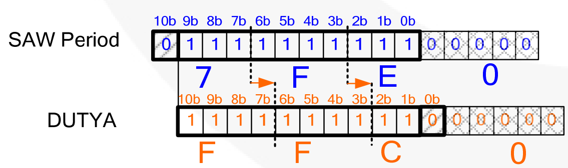

Figure 24. Auto SAW Alignment Enabled

When auto SAW alignment is on, the relationship between DUTY and the SAW is shown in Figure 25.

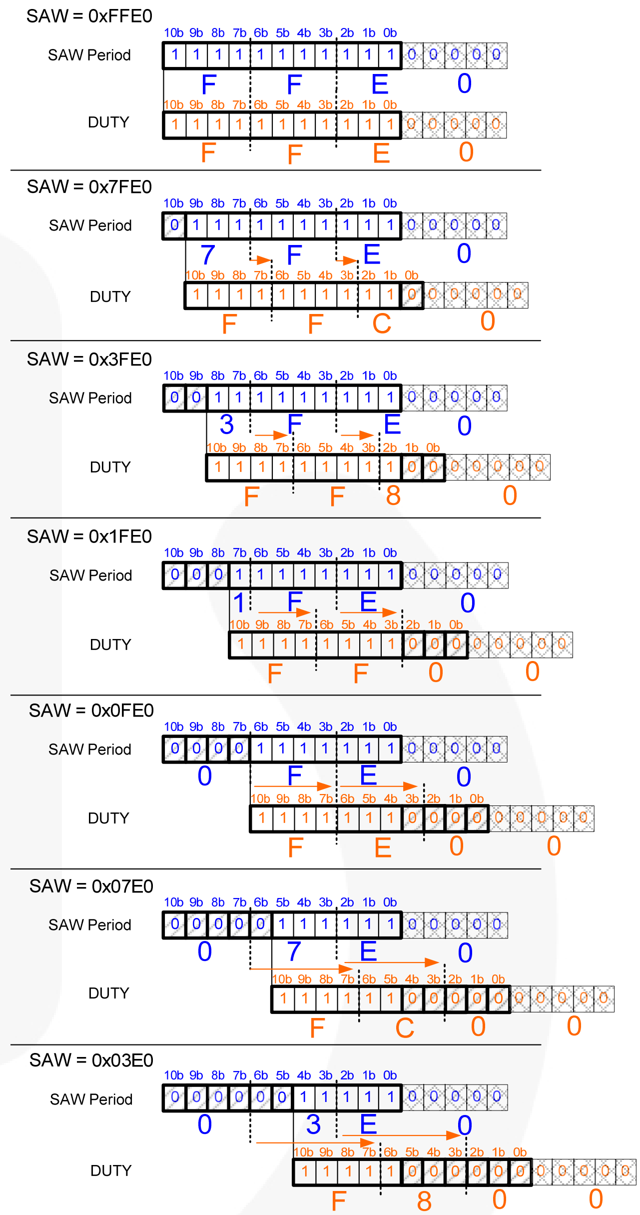

Figure 25. Auto SAW Alignment Function

3.3.5 Dead Time

Dead time is set in the MSFR PWMCFG (08h). This feature can prevent the inverter from burning out caused by cross conduction between high side and low side. The value of dead time is set according to rising/falling time of the inverter (FETs or IGBTs).

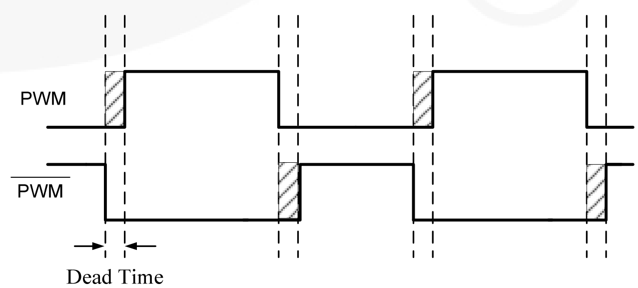

Figure 26. Dead Time

3.4. Hall Edge Interrupt

Through MSFR HALINT (1Bh), users can enable Hall edge interrupt and can choose three trigger types: rising/falling trigger, rising trigger, and falling trigger (*see* Figure 27).

An interrupt is triggered when the Hall signal's rising/falling matches the setting of HALL_INT. Set HALL_INT = b'00 to disable Hall Edge interrupt. Please note, to enable the interrupt, beside HALL_INT, EX10 should be enabled either.

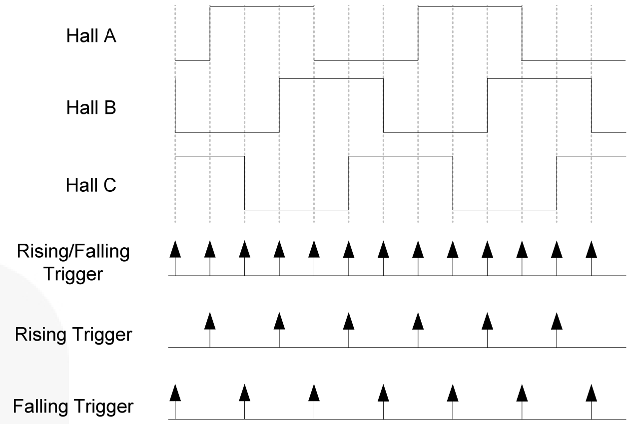

Figure 27. Hall Edge Interrupt Trigger Mode

Table 7. Hall Signal Control Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
HALINT (1Bh)	N/A				HTMR_OUT		HALL_INT		00h

Table 8. User-Defined Table Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
MCNTL (00h)	Reserved	AMC_RST	SIN_TBL	SQU_TBL	Reserved		CW	ST/FREE	00h

3.5. User-Defined Table

In addition to the default square-wave and sine-wave PWM output waveforms, two customizable user-defined square-wave and sine-wave PWM output waveforms can be achieved through the user-defined table *(see Table 8)*.

The user-defined table is located in a particular area of program memory, 2F00h - 2FFEh, which is set by MSFR MCNTL (00h)[5:4], as shown in Figure 29.

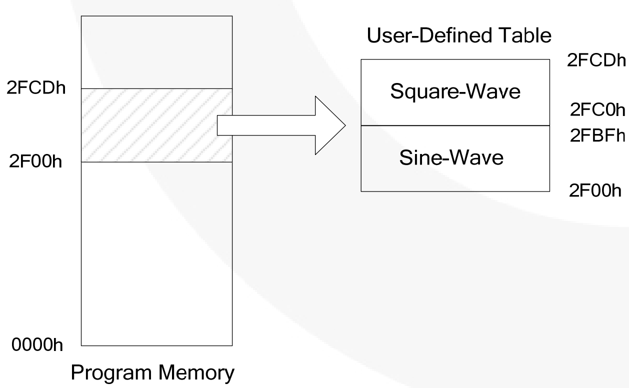

Figure 28. User-Defined Table

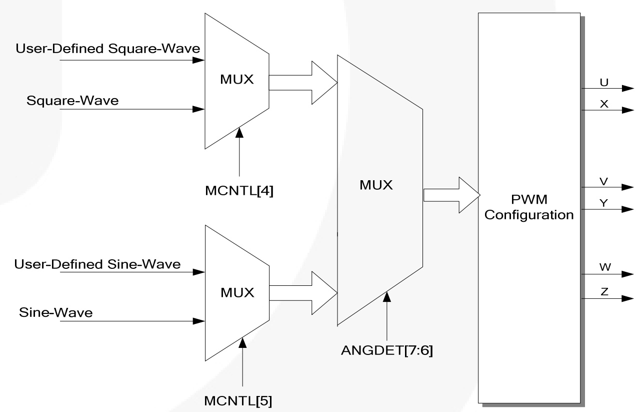

Figure 29. User-Defined Table Block Diagram

3.5.1 User-Defined Square-Wave Table

User-defined square-wave table is located in 2FC0h - 2FCDh, totally including 12 addresses. The first six addresses are corresponding to CW = 1 and the last six addresses are corresponding to CW = 0.

Each byte in the six bytes represents a particular 60-degree electrical angle corresponding to a Hall status, as shown in Table 9.

The stored codes are from 0 to 5, which represent different combinations of high/low-side signals. The table only defines phase U, but signals for phase V and phase W are automatically generated by shifting 120-degree and 240-degree electrical angle referring to phase U, respectively.

Table 9. User-Defined Square-Wave PWM

Address	CW	Hall Status (HA HB HC)	Code
2FC0h	1	0 0 1	
2FC1h	1	0 1 1	
2FC2h	1	0 1 0	
2FC3h	1	1 1 0	
2FC4h	1	1 0 0	
2FC5h	1	1 0 1	
2FC6h	0	1 0 1	
2FC7h	0	1 0 0	
2FC8h	0	1 1 0	
2FC9h	0	0 1 0	
2FCAh	0	0 1 1	
2FCBh	0	0 0 1	
2FCCh	X	0 0 0	
2FCDh	X	1 1 1	

Code	High Side	Low Side
0	OFF	OFF
1	OFF	ON
2	ON	OFF
4	PWM	/PWM
5	/PWM	PWM

Example: The required PWM is shown in Figure 30.

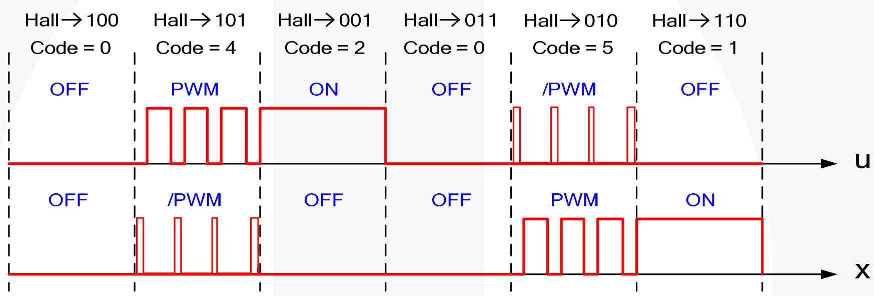

Figure 30. Required Waveforms

Users can fill fields in the high-side/low-side with the required waveform in Table 10 according to appropriate Hall signals and the CW. Users can find code values corresponding to the combination of high-side and low-side PWM signals and fill the code value up in Table 9. These codes must be stored in program memory 2FC0h to 2FCDh.

Table 10. User-Defined Square-Wave Table Address (Example)

Address	CW	Hall Status (HA HB HC)	Code	High-Side	Low-Side
2FC0h	1	0 0 1	2	ON	OFF
2FC1h	1	0 1 1	0	OFF	OFF
2FC2h	1	0 1 0	5	/PWM	PWM
2FC3h	1	1 1 0	1	OFF	ON
2FC4h	1	1 0 0	0	OFF	OFF
2FC5h	1	1 0 1	4	PWM	/PWM
2FC6h	0	1 0 1	1	OFF	ON
2FC7h	0	1 0 0	0	OFF	OFF
2FC8h	0	1 1 0	4	PWM	/PWM
2FC9h	0	0 1 0	2	ON	OFF
2FCAh	0	0 1 1	0	OFF	OFF
2FCBh	0	0 0 1	5	/PWM	PWM
2FCCh	X	0 0 0	0	OFF	OFF
2FCDh	X	1 1 1	0	OFF	OFF

3.5.2 User-Defined Sine-Wave Table

The user-defined sine-wave table is located in program memory 2F00h - 2FBFh and the 192 addresses are corresponding to the 360-degree electrical angles. The electrical angle 0º is located in 2F00h and aligned to the rising edge of Hall A.

Users can fill the addresses with the value 0 - 31 to describe the modulation waveform. The table only defines phase U, but signals for phase V and phase W are automatically generated by shifting 120-degrees and 240-degrees from phase U, respectively.

Example: To output a trapezoidal waveform, the required modulation waveform is similar to Figure 31.

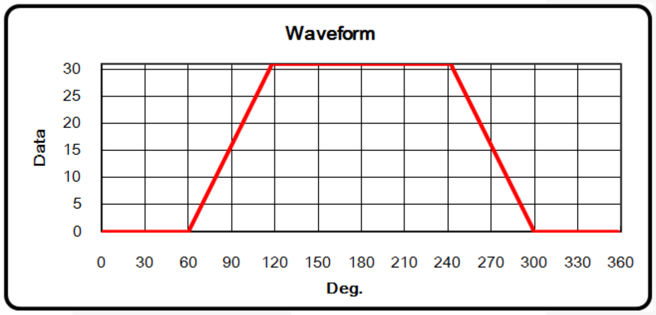

Figure 31. Required Modulation Waveform

Therefore, the users can fill in the "Entered Values" column in Table 11 to describe required modulation waveform according to appropriate electrical angles.

Table 11. User-Defined Sine-Wave Table Address (Example)

Address	Electrical Angle	Entered Values	Notes
2F00h - 2F1Fh	0 – 59°	0	No Amplitude
2F20h - 2F3Fh	60 – 119°	0 - 31	Increasing Step by Step
2F40h - 2F5Fh	120 – 179°	31	Maximum Amplitude
2F60h - 2F7Fh	180 - 239°	31	Maximum Amplitude
2F80h - 2F9Fh	240 - 299°	31 - 0	Decreasing Step by Step
2FA0h - 2FBFh	300 - 359°	0	No Amplitude

These codes must be stored in program memory 2F00h to 2FBFh.

4. Embedded MCU

The instruction sets of the embedded MCU of FCM8531 are fully compatible with MCS®51. Users can develop software with standard 805x assemblers and compilers. The embedded MCU uses Advanced Instruction Architecture (AIA) to significantly enhance performance. Compared with a traditional 8051, 63% of AIA's execution cycle are less than three (3) system clocks (3T).

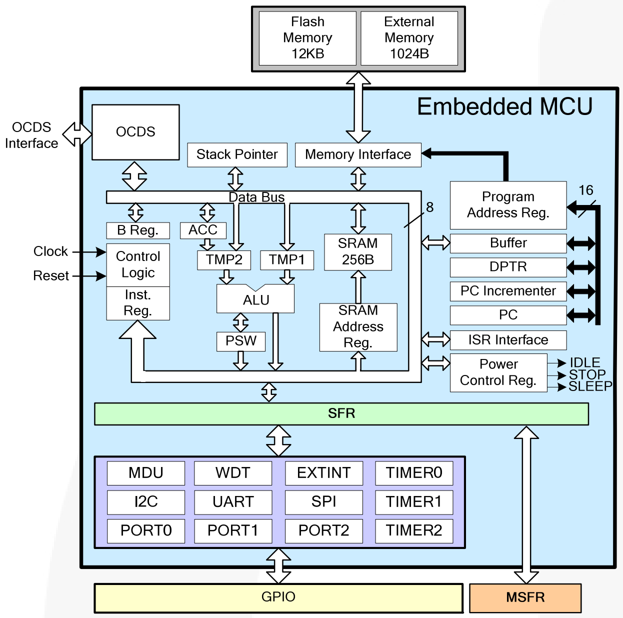

Figure 32. Embedded MCU Block Diagram

In addition to the existing 8051 MCU functions; such as GPIO, TIMER 0/1/2, ISR, and UART; other communication interfaces; such as SPI, I^{2}C, and WDT (Watchdog Timer); are also integrated into the embedded MCU. In addition, the On-Chip Debug Support (OCDS), In-System Programming (ISP), and Improved Multiply-Divide Unit (MDU) modules are provided for system debugging, program downloading, and faster computing.

The embedded MCU is capable of accessing data in MSFRs and transferring data to the AMC through the Special Function Registers (SFRs).

4.1. Memory Organization

Similar to the standard 8051, FCM8531 memory is divided into two parts: the program memory and the data memory.

The embedded MCU has 12 K-byte of flash memory as the program memory. Internal data memory and external data memory are composed of 256-byte and 1 K-byte high-speed Static Random-Access Memory (SRAM).

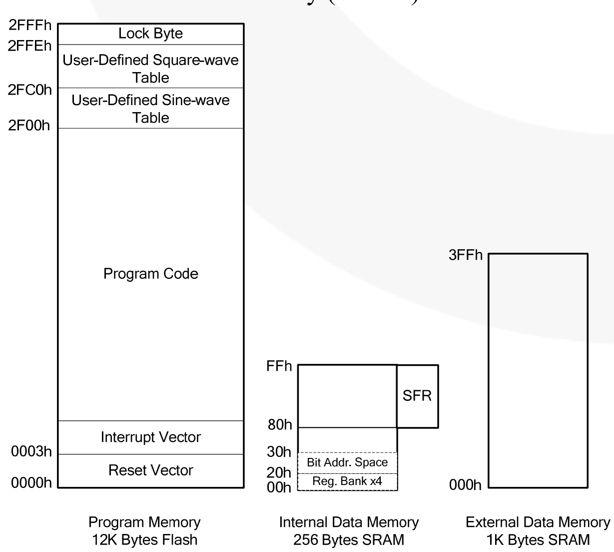

Figure 33. Memory Map of Embedded MCU

4.1.1 Program Memory

The 12 K-byte flash memory in the embedded MCU is with ISP functionality, which allows the program code to be updated online. The flash memory is divided into two parts, the program code area and special-purpose area. Addresses 0000h - 2EFFh define the program code area; addresses higher than 2EFFh define the special-purpose area, which includes the user-defined wave table and a lock byte. The OCDS function is disabled if the most significant bit of Lock byte is 0. The flash memory is encrypted when other bits in the Lock byte are 0.

The data in flash memory must first be erased to FFh before being overwritten.

Note: In the ISP mode, pins P12 and P13 become ISP functional pins. To assure running ISP properly, do not set the two pins as Direct Driver Mode. The capacitance on these two pins must be as small as possible.

Although the SFR CKCON register can adjust the Wait State for program memory and data memory, the recommendation is to set the highest speed (CKCON = 00h) for the best performance.

During power on or reset, the program starts at the program memory's address to 0000h. The embedded MCU provides

16 interrupts. The vectors of the interrupt service routines are distributed over the program memory at addresses 0003h - 00ABh. When an interrupt occurs, the program automatically jumps to the appropriate interrupt vector to execute the interrupt service subroutine. Interrupt vectors are shown in Table 12:

Table 12. Interrupt Vectors

Interrupt Source	Interrupt Vector	Symbol
External Interrupt 0	0003h	EX0
Timer 0 Overflow	000Bh	ET0
External Interrupt 1	0013h	EX1
Timer 1 Overflow	001Bh	ET1
Serial	0023h	ES0
Timer 2	002Bh	ET2
I^2C	0043h	EX7
SPI	004Bh	EX2
COM0	0053h	EX3
COM1	005Bh	EX4
COM2	0063h	EX5
FAULT	008Bh	EX8
ADC Ready	0093h	EX9
Hall Edge	009Bh	EX10
AMC	00A3h	EX11
External Interrupt 12	00ABh	EX12

4.1.2 Data Memory

The data memory of the embedded MCU is divided into two parts: 256-byte internal data memory and 1 K-byte external data memory. The first 128 bytes (00h - 7Fh) in internal data memory are permitted to directly access address, which include four register banks, Bit Map Address, and a general-purpose direct addressing area. The last 128 bytes (80h - FFh) in data memory are overlapped with SFR to access the SFR when direct addressing; whereas it reads and writes the SRAM when indirect addressing.

The size of the external data memory is 1 K-byte. Use the MOVX instruction to indirectly address through the Data Pointer (DPTR) or R0/R1 (Page Mode) so that more instruction cycles are required to access the data.

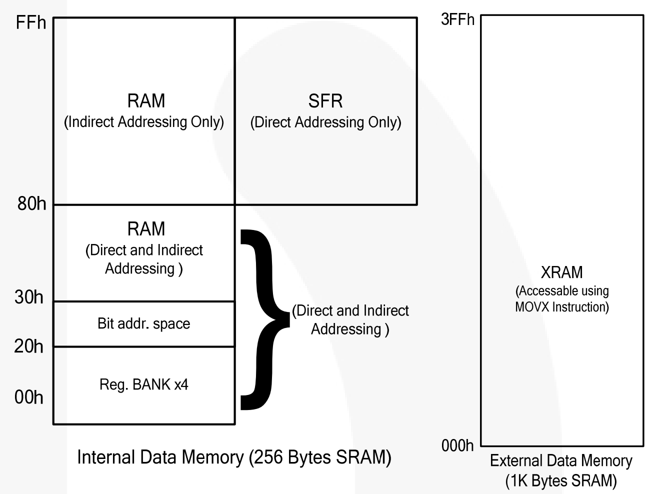

Figure 34. Data Memory

4.2. Reset

There are three reset methods: Power On Reset (POR), software reset, and Reset by a high-level input on RST pin. After reset, P0[7:2] is set as PWM outputs and are in low-level initially. P1[7:0] and P2[6:4] are set as open-drain outputs and is pulled HIGH initially. The program begins executing from the address 0000h stored in the SFR PC. The accumulator and flags are cleared and other registers are set to the initial state.

4.2.1 Power On Reset

When V_{DD} exceeds V_{DD_ON}, the operation of the voltage generator module begins to provide the required power to the internal circuitry of the FCM8531. Afterward, the Power On Reset (POR) functionality is enabled and the clock generator starts. About two milliseconds later, the reset status is removed and the MCU program begins executing.

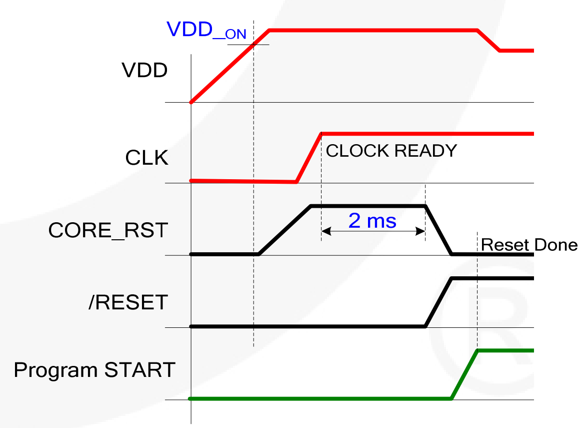

Figure 35. Power-On Reset Sequence

4.2.2 Hardware Reset

When the switch is pressed, the reset pin is set to HIGH and the FCM8531 enters Reset state, where the reset pin returns to LOW and the FCM8531 begins executing the program when the switch is released and the RC time has passed.

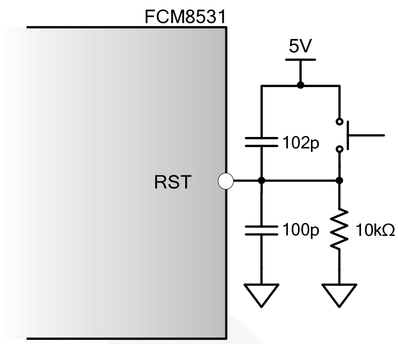

Figure 36. Hardware Reset

4.2.3 Software Reset

Internal software reset functionality is set through SFR SRST (F7h) to reset the embedded MCU.

4.3. SFRs (Special Function Registers)

The SFRs in the embedded MCU of the FCM8531use direct addressing access.

Table 13. Special Function Registers Map

Hex	X0h/X8h	X1h/X9h	X2h/XAh	X3h/XBh	X4h/XCh	X5h/XDh	X6h/XEh	X7h/XFh	Hex
F8	P0_CFG	IO_CFG	INT12_CFG	INT12_STA	DRV0	DRV1	DRV2		FF
F0	B							SRST	F7
E8		MD0	MD1	MD2	MD3	MD4	MD5	ARCON	EF
E0	ACC	SPSTA	SPCON	SPDAT	SPSSN				E7
D8	ADCON		I2CDAT	I2CADR	I2CCON	I2CSTA			DF
D0	PSW								D7
C8	T2CON		CRCL	CRCH	TL2	TH2			CF
C0	IRCON	CCEN	CCL1	CCH1	CCL2	CCH2			C7
B8	IEN1	IP1	SRELH					IRCON2	BF
B0	MTX0	MTX1	MTX2	MTX3	MRX0	MRX1	MRX2	MRX3	B7
A8	IEN0	IP0	SRELL						AF
A0	P2								A7
98	SCON	SBUF	IEN2						9F
90	P1		DPS	DPC			MSFRADR	MSFRDAT	97
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON		8F
80	P0	SP	DPL	DPH	DPL1	DPH1	WDTREL	PCON	87

Table 14. Special Function Register Description

Byte Name	Address	Reset	Bit	Type	Name	Description
P0	80h	FFh	Port 0			
			7:0	R/W	P0 [7:0]	Port 0
SP	81h	07h	Stack Point			
			7:0	R	SP	Stack Point
DPL	82h	00h	Data Pointer Low Byte			
			7:0	R/W	DPL	Data Pointer Low Byte
DPH	83h	00h	Data Pointer High Byte			
			7:0	R/W	DPH	Data Pointer High Byte
DPL1	84h	00h	Data Pointer 1 Low Byte			
			7:0	R/W	DPL1	Data Pointer 1 Low Byte
DPH1	85h	00h	Data Pointer 1 High Byte			
			7:0	R/W	DPH1	Data Pointer 1 High Byte
WDTREL	86h	00h	Watchdog Timer Reload Register			
			7	R/W	WDPS	Pre-scale Select 0: Normal Scale 1: 1/16 Scale When set, the watchdog is clocked through an additional pre-scale (divide by 16)
			6:0	R/W	WDTPER	Watchdog Reload Value Reload value for the highest seven bits of the watchdog timer. This value is loaded to the watchdog timer when a refresh is triggered by a consecutive setting of bits WDT (IEN 0.6) and SWDT (IEN 1.6)
PCON	87h	08h	Power Control			
			7	R/W	SMOD	Serial Port Baud-Rate Select (Baud-Rate Double) 0: $f_{SYS}/64$ 1: $f_{SYS}/32$
			6	R/W	WDT_TM	Watchdog Timer Test Mode Flag 0: Watchdog is clocked through a pre-scale ($f_{SYS}/12$) 1: Skip pre-scale (Test Mode Only)
			5	R/W	ISR_TM	Interrupt Service Routine Test Mode Flag
			4:2		Reserved	Must Be Set to 0
			1	R/W	STOP	STOP Mode Control
			0	R/W	IDLE	IDLE Mode Control
TCON	88h	00h	Timer/Counter Control Register			
			7	R/W	TF1	Timer 1 Overflow Flag TF1 is set by hardware when Timer 1 overflows It can be cleared by software and is automatically cleared when entering interrupt
			6	R/W	TR1	Timer 1 Run Control 0: Stop 1: Run
			5	R/W	TF0	Timer 0 Overflow Flag TF0 is set by hardware when Timer 0 overflows. It can be cleared by software and is automatically cleared when entering interrupt.
			4	R/W	TR0	Timer 0 Run Control 0: Stop 1: Run
			3	R/W	IE1	External Interrupt 1 Flag
			2	R/W	IT1	External Interrupt 1 Type Control

Byte Name	Address	Reset	Bit	Type	Name	Description
						0: Low-Level Trigger 1: Falling-Edge Trigger
			1	R/W	IE0	External Interrupt 0 Flag
			0	R/W	IT0	External Interrupt 0 Type Control 0: Low-Level Trigger 1: Falling-Edge Trigger
TMOD	89h	00h	Timer Mode Control Register			
			7	R/W	GATE1	Timer 1 Gate Control 0: Disabled External Gate Control 1: Enabled External Gate Control (pin INT1). When INT1 is HIGH and TR1 is set, the counter 1 is increased every falling edge of pin T1.
			6	R/W	C/T1	Timer 1 Counter / Timer Select 0: Timer Mode 1: Counter Mode (incremented every falling edge on T1 pin)
			5:4	R/W	T1MOD	Timer 1 Mode Control 00: 13-bit Counter / Timer, five lower bits in TL1, eight bits in TH1 01: 16-bit Counter / Timer 10: 8-bit Auto-Reload Counter / Timer. Reload value is TH1. 11: Timer 1 is stopped
			3	R/W	GATE0	Timer 0 Gate Control 0: Disabled External Gate Control. 1: Enabled External Gate Control (pin INT0). When INT0 is HIGH and TR0 is set, the counter 0 is increased every falling edge of pin T0.
			2	R/W	C/T0	Timer 0 Counter / Timer Select 0: Timer Mode 1: Counter Mode (incremented every falling edge on T0 pin)
			1:0	R/W	T0MOD	Timer 0 Mode Control 00: 13-bit Counter / Timer, with five lower bits in TL0 and eight bits in TH0 01: 16-bit Counter / Timer 10: 8-bit Auto-Reload Counter / Timer. The reload value is in TH0. 11: Timer 0 acts as two independent 8-bit Timer / Counter TL0,TH0
TL0	8Ah	00h	Timer 0, Low Byte			
			7:0	R/W	TL0	Timer 0, Low Byte
TL1	8Bh	00h	Timer 1, Low Byte			
			7:0	R/W	TL1	Timer 1, Low Byte
TH0	8Ch	00h	Timer 0, High Byte			
			7:0	R/W	TH0	Timer 0, High Byte
TH1	8Dh	00h	Timer 1, High Byte			
			7:0	R/W	TH1	Timer 1, High Byte
CKCON	8Eh	71h	Clock Control Register			
			7	N/A	N/A	N/A
			6:4	R/W	PMCYC	Program Memory Wait State Control
			3	N/A	N/A	N/A
			2:0	R/W	XRAMCYC	External Data Memory Stretch Cycle Control

Byte Name	Address	Reset	Bit	Type	Name	Description
P1	90h	FFh	Port 1			
			7:0	R/W	P1 [7:0]	Port 1
DPS	92h	00h	Data Pointer Select Register			
			7:4	N/A	N/A	N/A
			3	R/W	BSE	Bank Switch Enable (Enable RS0,RS1 of PSW)
			2:0	R/W	DPSEL2 DPSEL1 DPSEL0	Data Point Register Select
DPC	93h	00h	Data Point Control Register			
			7:6	N/A	N/A	N/A
			5:3	R/W	DPC[5:3]	Next Data Pointer Selection
			2	R/W	DPC[2]	Auto-Modification Size 0: The current DPTR is automatically modified by 1 after each MOVX@DPTR instruction when DPC[0] = 1. 1: The current DPTR is automatically modified by 2 after each MOVX@DPTR instruction when DPC[0] = 1.
			1	R/W	DPC[1]	Auto-Modification Direction 0: The current DPTR is automatically incremented after each MOVX@DPTR instruction when DPC[0] = 1. 1: The current DPTR is automatically decremented after each MOVX@DPTR instruction when DPC[0] = 1.
			0	R/W	DPC[0]	Auto-Modification Enable When set, the current DPTR is automatically incremented after each MOVX@DPTR instruction.
MSFRADR	96h	00h	MSFR Address (00h - 7Fh)			
			7:0	R/W	MSFRADR	MSFR Address (00h - 7Fh)
MSFRDAT	97h	00h	Access MSFR Data			
			7:0	R/W	MSFRDAT	MSFR Data
SCON	98h	00h	Serial Port, Control Register			
			7:6	R/W	SM0 and SM1	Serial Port Mode Select (SM0, SM1) 00: Shift Register, $f_{SYS}/12$ (Mode 0) 01: 8-bit UART, Variable (Mode 1) 10: 9-bit UART (Mode 2) SMOD=0 → $f_{SYS}/64$, SMOD=1 → $f_{SYS}/32$ 11: 9-bit UART, Variable (Mode 3)
			5	R/W	SM2	Multiprocessor Communication Enable
			4	R/W	REN	Serial Reception Enable 0: Disabled 1: Enabled
			3	R/W	TB8	Transmitter Bit 8 This bit is used while transmitting data through serial port in Mode 2 or Mode 3. The state of this bit corresponds with the state of the 9th transmitted bit, such as parity check or multiprocessor communication. It is controlled by software.
			2	R/W	RB8	Received Bit 8 This bit is used while receiving data through serial port in Mode 2 or Mode 3. It reflects the state of the 9th received bit. In Mode 1, if multi-processor communication is enabled (SM2=0), this bit is the Stop bit. In Mode 0, this bit is not used.

Byte Name	Address	Reset	Bit	Type	Name	Description
			1	R/W	TI	Transmit Interrupt Flag It indicates completion of a serial transmission at serial port. It is set by hardware at the end of bit 8 in Mode 0 or at the beginning of a Stop bit in other modes. It must be cleared by software.
			0	R/W	RI	Receive Interrupt Flag It is set by hardware after completion of a serial reception at serial port. It is set by hardware at the end of bit 8 in Mode 0 or in the middle of a Stop bit in other modes. It must be cleared by software.
SBUF	99h	00h	Serial Port, Data Buffer			
			7:0	R/W	SBUF [7:0]	Serial Port, Data Buffer
IEN2	9Ah	00h	Interrupt Enable Register 2			
			7:6		Reserved	Must Be Set to 0
			5	R/W	EX12	External Interrupt 12 0: Disabled 1: Enabled
			4	R/W	EX11	AMC Interrupt (Interrupt 11) 0: Disabled 1: Enabled
			3	R/W	EX10	Hall Edge Interrupt (Interrupt 10) 0: Disabled 1: Enabled
			2	R/W	EX9	ADC Interrupt (Interrupt 9) 0: Disabled 1: Enabled
			1	R/W	EX8	Fault Interrupt (Interrupt 8) 0: Disabled 1: Enabled
			0		Reserved	Must Be Set to 0
P2	A0h	FFh	Port 2			
			7:0	R/W	P2 [7:0]	Port 2
IEN0	A8h	00h	Interrupt Enable Register 0			
			7	R/W	EA	Interrupts Enable When set to 0, all interrupts are disabled. Otherwise, enable each interrupt by setting the corresponding Interrupt Enable bit.
			6	R/W	WDT	Watchdog Timer Refresh Flag Set to initiate / refresh the watchdog timer *(see Section 4.14)*
			5	R/W	ET2	Timer 2 Interrupt 0: Disabled 1: Enabled
			4	R/W	ES0	Serial Port Interrupt 0: Disabled 1: Enabled
			3	R/W	ET1	Timer 1 Overflow Interrupt 0: Disabled 1: Enabled
			2	R/W	EX1	External Interrupt 1 0: Disabled 1: Enabled
			1	R/W	ET0	Timer 0 Overflow Interrupt 0: Disabled

Byte Name	Address	Reset	Bit	Type	Name	Description
						1: Enabled
			0	R/W	EX0	External Interrupt 0 0: Disabled 1: Enabled
IP0	A9h	00h	Interrupt Priority Register 0			
			7		Reserved	Must Be Set to 0
			6	R/W	WDTS	Watchdog Timer Status Flag Set by hardware when the watchdog timer reset occurs
			5:0	R/W	IP0 [5:0]	Interrupt Priority See IP1
SRELL	AAh	D9h	Serial Port Reload Register Low Byte (Baud-Rate generator)			
			7:0	R/W	SREL[7:0]	Serial Port Reload Register [7:0]
MTX0	B0h	00h	Data Sent to AMC			
			7:0	R/W	MTX0	Data Sent to AMC
MTX1	B1h	00h	Data Sent to AMC			
			7:0	R/W	MTX1	Data Sent to AMC
MTX2	B2h	00h	Data Sent to AMC			
			7:0	R/W	MTX2	Data Sent to AMC
MTX3	B3h	00h	Data Sent to AMC			
			7:0	R/W	MTX3	Data Sent to AMC
MRX0	B4h	00h	Data Received from AMC			
			7:0	R	MRX0	Data Received from AMC
MRX1	B5h	00h	Data Received from AMC			
			7:0	R	MRX1	Data Received from AMC
MRX2	B6h	00h	Data Received from AMC			
			7:0	R	MRX2	Data Received from AMC
MRX3	B7h	00h	Data Received from AMC			
			7:0	R	MRX3	Data Received from AMC
IEN1	B8h	00h	Interrupt Enable Register 1			
			7	R/W	EXEN2	Timer 2 External Reload Interrupt 0: Disabled 1: Enabled
			6	R/W	SWDT	Watchdog Timer Start / Refresh Flag *(see Section 4.14)*
			5		Reserved	Must Be Set to 0
			4	R/W	EX5	CC2 Interrupt 0: Disabled 1: Enabled
			3	R/W	EX4	CC1 Interrupt 0: Disabled 1: Enabled
			2	R/W	EX3	CC0 Interrupt 0: Disabled 1: Enabled
			1	R/W	EX2	SPI Interrupt 0: Disabled 1: Enabled
			0	R/W	EX7	I^2C Interrupt 0: Disabled 1: Enabled

Byte Name	Address	Reset	Bit	Type	Name	Description
IP1	B9h	00h	Interrupt Priority Register 1			
			7:6		Reserved	Must Be Set to 0
			5	R/W		Timer 2 Interrupt / External Interrupt 12 Priority Setting. [IP1.5:IP0.5]= 00: Level 0, Lowest 01: Level 1 10: Level 2 11: Level 3, Highest
			4	R/W		Serial Port Interrupt / External Interrupt 5 / External Interrupt 11 Priority Setting. [IP1.4:IP0.4]= 00: Level 0, Lowest 01: Level 1 10: Level 2 11: Level 3, Highest
			3	R/W		Timer 1 Interrupt / External Interrupt 4 / External Interrupt 10 Priority Setting. [IP1.3:IP0.3]= 00: Level 0, Lowest 01: Level 1 10: Level 2 11: Level 3,Highest
			2	R/W		External Interrupt 1 / External Interrupt 3 / External Interrupt 9 Priority Setting. [IP1.2:IP0.2]= 00: Level 0, Lowest 01: Level 1 10: Level 2 11: Level 3, Highest
			1	R/W		Timer 0 Interrupt / External Interrupt 2 / External Interrupt 8 Priority Setting. [IP1.1:IP0.1]= 00: Level 0, Lowest 01: Level 1 10: Level 2 11: Level 3, Highest
			0	R/W		External Interrupt 0 / External Interrupt 7 Priority Setting. [IP1.0:IP0.0]= 00: Level 0, Lowest 01: Level 1 10: Level 2 11: Level 3, Highest
SRELH	BAh	03h	Serial Port Reload Register High Byte (Baud-Rate Generator)			
			7:2	N/A	N/A	N/A
			1:0	R/W	SREL [9:8]	Serial Port Reload Register [9:8]
IRCON2	BFh	00h	Interrupt Request Control 2 Register			
			7:5	N/A	N/A	N/A
			4	R/W	IEX12	External Interrupt 12 Flag
			3	R/W	IEX11	External Interrupt 11 Flag
			2	R/W	IEX10	External Interrupt 10 Flag
			1	R/W	IEX9	External Interrupt 9 Flag
			0	R/W	IEX8	External Interrupt 8 Flag

Byte Name	Address	Reset	Bit	Type	Name	Description
IRCON	C0h	00h	Interrupt Request Control Register			
			7	R/W	EXF2	Timer 2 External Reload Flag
			6	R/W	TF2	Timer 2 Overflow Flag
			5		Reserved	Must Be Set to 0
			4	R/W	IEX5	External Interrupt 5 Flag
			3	R/W	IEX4	External Interrupt 4 Flag
			2	R/W	IEX3	External Interrupt 3 Flag
			1	R/W	IEX2	External Interrupt 2 Flag
			0	R/W	IEX7	External Interrupt 7 Flag
CCEN	C1h	00h	Compare/Capture Enable Register			
			7:6		Reserved	Must Be Set to 0
			5:4	R/W	COCAH2 / COCAL2	Compare / Capture Mode for CC2 Register 00: Compare / capture disable 01: Capture on rising edge at pin CC2 10: Compare enabled 11: Capture on write operation into register CC2
			3:2	R/W	COCAH1 / COCAL1	Compare / Capture Mode for CC1 Register 00: Compare / capture disable 01: Capture on rising edge at pin CC1 10: Compare enabled 11: Capture on write operation into register CC1
			1:0	R/W	COCAH0 / COCAL0	Compare / Capture Mode for CRC Register 00: Compare / capture disable 01: Capture on rising edge at pin CC0 10: Compare enabled 11: Capture on write operation into register CC0
CCL1	C2h	00h	Compare / Capture Register 1, Low Byte			
			7:0	R/W	CCL1	Compare / Capture Register 1, LOW Byte
CCH1	C3h	00h	Compare / Capture Register 1, High Byte			
			7:0	R/W	CCH1	Compare / Capture Register 1, HIGH Byte
CCL2	C4h	00h	Compare / Capture Register 2, Low Byte			
			7:0	R/W	CCL2	Compare / Capture Register 2, LOW Byte
CCH2	C5h	00h	Compare / Capture Register 2, High Byte			
			7:0	R/W	CCH2	Compare / Capture Register 2, HIGH Byte
Reserved	C6 - C7h	00h			Reserved	Must Be Set to 0
T2CON	C8h	00h	Timer 2 Control Register			
			7	R/W	T2PS	Pre-Scale Select 0: Timer 2 is cocked by f_{SYS} /12 1: Timer 2 is clocked by f_{SYS} /24
			6	R/W	I3FR	Active Edge Selection for External Interrupt 3 0: Falling Edge 1: Rising Edge
			5	R/W	I2FR	Active Edge Selection for External Interrupt 2 0: Falling edge 1: Rise edge
			4:3	R/W	T2R[1:0]	Timer 2 Reload Mode Selection 0X: Reload disabled 10: Mode 0 11: Mode 1
			2		Reserved	Must Be Set to 0

Byte Name	Address	Reset	Bit	Type	Name	Description
			1:0	R/W	T2I[1:0]	Timer 2 Input Selection (T2I1,T2I0) 00: Timer 2 stopped 01: Input frequency = $f_{SYS}/12$ or $f_{SYS}/24$ 10: Timer 2 is increased by falling edge of pin T2 11: Input frequency ($f_{SYS}/12$ or $f_{SYS}/24$) gated by pin EXT2
CRCL	CAh	00h	Compare/Reload/Capture Register, Low Byte			
			7:0	R/W	CRCL	Compare / Reload / Capture Register, LOW Byte
CRCH	CBh	00h	Compare/Reload/Capture Register, High Byte			
			7:0	R/W	CRCH	Compare / Reload / Capture Register, HIGH Byte
TL2	CCh	00h	Timer 2, Low Byte			
			7:0	R/W	TL2	Timer 2, LOW Byte
TH2	CDh	00h	Timer 2, High byte			
			7:0	R/W	TH2	Timer 2, HIGH byte
PSW	D0h	00h	Program Status Word Register			
			7	R/W	CY	Carry Flag
			6	R/W	AC	Auxiliary Carry Flag
			5	R/W	F0	General-Purpose Flag 0
			4:3	R/W	RS1 RS0	[RS1,RS0] Selection Register Bank Locations 00: bank 0 (00h - 07h) 01: bank 1 (08h - 0Fh) 10: bank 2 (10h - 17h) 11: bank 3 (18h - 1Fh)
			2	R/W	OV	Overflow Flag
			1	R/W	F1	General-Purpose Flag 1
			0	R	P	Parity Flag
ADCON	D8h	00h	Serial Port Baud-Rate Select Register			
			7	R/W	BD	Serial Port Baud-Rate Selection (in Mode 1 and 3) When 1, additional internal baud-rate generator is used. Otherwise baud-rate is sourced by Timer 1.
			6:0		Reserved	Must Be Set to 0
I2CDAT	DAh	00h	I^2C Data Register			
			7:0	R/W	I2CDAT	I^2C Data
I2CADR	DBh	00h	I^2C Address			
			7:1	R/W	I2C address	I^2C Address in Slave Mode
			0	R/W	GC	Address Acknowledge
I2CCON	DCh	00h	I^2C Control Register			
			7	R/W	CR2	Clock Rate Bit 2
			6	R/W	ENS1	I^2C Activate 0: Disabled 1: Enabled
			5	R/W	STA	START Flag When STA = 1, the I^2C component checks the I^2C bus status and if the bus is free, a START condition is generated.
			4	R/W	STO	STOP Flag When STO = 1, the I^2C interface is in Master Mode, a STOP condition is transmitted to the I^2C bus.

Byte Name	Address	Reset	Bit	Type	Name	Description
			3	R/W	SI	Serial Interrupt Flag The SI is set by hardware when one of 25 out of 26 possible I²C states is entered. The only state that does not set the SI is F8h, which indicates that there is no available relevant state information. It must be cleared by software.
			2	R/W	AA	Assert Acknowledge Flag Define Acknowledge level 0: LOW level 1: HIGH level
			1	R/W	CR1	Clock Rate Bit 1
			0	R/W	CR0	Clock Rate Bit 0
I2CSTA	DDh	F8h	I²C Status Register			
			7:3	R	I2CSTA	I²C Status Register
			2:0	N/A	N/A	N/A
ACC	E0h	00h	Accumulator			
			7:0	R/W	ACC	Accumulator
SPSTA	E1h	00h	SPI Status Register			
			7	R	SPIF	Serial Peripheral Data Transfer Flag Set by hardware upon data transfer completion. Cleared by hardware when data transfer is in progress. Can be also cleared by reading the SPSTA register with the SPIF bit set, then reading the SPDAT register.
			6	R	WCOL	Write Collision Flag Set by hardware upon write collision to SPDAT. Cleared by hardware upon data transfer completion when no collision has occurred. Can be also cleared by an access to SPSTA register and an access to SPDAT register.
			5	R	SSERR	Synchronous Serial Slave Error Flag Set by hardware when SPSSN input is deserted before the end of receive sequence. Cleared by disabling the SPI module (clearing SPEN bit in SPCON register).
			4:0		Reserved	Must Be Set to 0
SPCON	E2h	34h	SPI Control Register			
			7	R/W	SPR2	SPI Clock Rate See SPR[1:0]
			6	R/W	SPEN	SPI Activate 0: Disabled 1: Enabled
			5		Reserved	Must Be Set to 0
			4	R/W	MSTR	SPI Mode 0: Slave Mode 1: Master Mode
			3	R/W	CPOL	Clock Polarity 0: The SCK is set to 0 in Idle state. 1: The SCK is set to 1 in Idle state.
			2	R/W	CPHA	Clock Phase 0: Data are sampled when the SCK leaves the Idle state 1: Data are sampled when the SCK returns to Idle state

Byte Name	Address	Reset	Bit	Type	Name	Description
			1:0	R/W	SPR[1:0]	SPI Clock Rate [SPR2,SPR1,SPR0]= 010: $f_{SYS}/8$ 011: $f_{SYS}/16$ 100: $f_{SYS}/32$ 101: $f_{SYS}/64$ 110: $f_{SYS}/128$ 111: Master clock is not generated.
SPDAT	E3h	00h	SPI Data Register			
			7:0	R/W	SPDAT	SPI Data Register
SPSSN	E4h	FFh	SPI Slave Select Register			
			7:1	N/A	N/A	N/A
			0	R/W	SSR	SPI Slave Select Register
MD0	E9h	00h	Multiplication / Division Register 0			
			7:0	R/W	MD0	Multiplication / Division Register 0
MD1	EAh	00h	Multiplication / Division Register 1			
			7:0	R/W	MD1	Multiplication / Division Register 1
MD2	EBh	00h	Multiplication / Division Register 2			
			7:0	R/W	MD2	Multiplication / Division Register 2
MD3	ECh	00h	Multiplication / Division Register 3			
			7:0	R/W	MD3	Multiplication / Division Register 3
MD4	EDh	00h	Multiplication / Division Register 4			
			7:0	R/W	MD4	Multiplication / Division Register 4
MD5	EEh	00h	Multiplication / Division Register 5			
			7:0	R/W	MD5	Multiplication / Division Register 5
ARCON	EFh	00h	Arithmetic Control			
			7	R	MDEF	MDU Error Flag Indicates an improperly performed operation (when one of the arithmetic operations has been restarted or interrupted by a new operation).
			6	R	MDOV	MDU Overflow Flag Overflow occurrence in the MDU operation
			5	R/W	SLR	Shift Direction 0: Left 1: Right
			4:0	R/W	SC[4:0]	Shift Counter (SC[4]: MSB, SC[0]: LSB) SC[4:0] = 0, Normalize function SC[4:0] ≠ 0, Shift function
B	F0h	00h	B Register			
			7:0	R/W	B	B Register
SRST	F7h	00h	Software Reset Register			
			7:1	N/A	N/A	N/A
			0	R/W	SRSTREG	Software Reset Request
P0_CFG	F8h	00h	P0 Configuration			
			7	R/W	P07_IO	P07 IO Type 0: PWM Z Channel 1: GPIO
			6	R/W	P06_IO	P06 IO Type 0: PWM W Channel 1: GPIO

Byte Name	Address	Reset	Bit	Type	Name	Description
			5	R/W	P05_IO	P05 IO Type 0: PWM Y Channel 1: GPIO
			4	R/W	P04_IO	P04 IO Type 0: PWM V Channel 1: GPIO
			3	R/W	P03_IO	P03 IO Type 0: PWM X Channel 1: GPIO
			2	R/W	P02_IO	P02 IO Type 0: PWM U Channel 1: GPIO
			1:0		Reserved	Must Be Set to 0
IO_CFG	F9h	00h	IO Configuration			
			7:6	R/W	EI_CFG[1:0]	INT0, INT1 Pin Assignment 00: Reserved 01: Reserved 10: P24→INT0, P25→INT1 11: P26→INT0
			5:4	R/W	I12_CFG[1:0]	INT12 Edge Trigger Type 00: Disable 01: Rising / Falling 10: Rising 11: Falling
			3:2	R/W	P2_CFG[1:0]	P2 Configuration *Refer to Table [P2_CFG1:P2CFG0]*
			1:0	R/W	P1_CFG[1:0]	P1 Configuration *Refer to Table [P1_CFG1:P1_CFG0]*
INT12_CFG	FAh	00h	INT12 Sourced Pin Assignment			
			7	R/W	ASI_OSC	INT12 Assign to OSC Check
			6	R/W	ASI_P16	INT12 Assign to P16
			5	R/W	ASI_P15	INT12 Assign to P15
			4	R/W	ASI_P14	INT12 Assign to P14
			3	R/W	ASI_P13	INT12 Assign to P13
			2	R/W	ASI_P12	INT12 Assign to P12
			1	R/W	ASI_P11	INT12 Assign to P11
			0	R/W	ASI_P10	INT12 Assign to P10
INT12_STA	FBh	00h	INT12 State, to identify INT12 trigger source			
			7	R	ST_OSC	INT12 is triggered by OSC Check
			6	R	ST_P16	INT12 is triggered by P16
			5	R	ST _P15	INT12 is triggered by P15
			4	R	ST _P14	INT12 is triggered by P14
			3	R	ST _P13	INT12 is triggered by P13
			2	R	ST _P12	INT12 is triggered by P12
			1	R	ST _P11	INT12 is triggered by P11
			0	R	ST _P10	INT12 is triggered by P10

Byte Name	Address	Reset	Bit	Type	Name	Description
DRV0	FCh	00h	GPIO 0 Driver Mode Select			
			7	R/W	P07_DRV	0: Open drain with internal pull-down resistor 1: Direct drive
			6	R/W	P06_DRV	0: Open drain with internal pull-down resistor 1: Direct drive
			5	R/W	P05_DRV	0: Open drain with internal pull-down resistor 1: Direct drive
			4	R/W	P04_DRV	0: Open drain with internal pull-down resistor 1: Direct drive
			3	R/W	P03_DRV	0: Open drain with internal pull-down resistor 1: Direct drive
			2	R/W	P02_DRV	0: Open drain with internal pull-down resistor 1: Direct drive
			1:0		Reserved	Must Be Set to 0
DRV1	FDh	00h	GPIO 1 Driver Mode Select			
			7	R/W	P17_ DRV	0: Open drain with internal pull-up resistor 1: Direct drive
			6	R/W	P16_ DRV	0: Open drain with internal pull-up resistor 1: Direct drive
			5	R/W	P15_ DRV	0: Open drain with internal pull-up resistor 1: Direct drive
			4	R/W	P14_ DRV	0: Open drain with internal pull-up resistor 1: Direct drive
			3	R/W	P13_ DRV	0: Open drain with internal pull-up resistor 1: Direct drive
			2	R/W	P12_ DRV	0: Open drain with internal pull-up resistor 1: Direct drive
			1	R/W	P11_ DRV	0: Open drain with internal pull-up resistor 1: Direct drive
			0	R/W	P10_ DRV	0: Open drain with internal pull-up resistor 1: Direct drive
DRV2	FEh	00h	GPIO 2 Driver Mode Select			
			7		Reserved	Must Be Set to 0
			6	R/W	P26_DRV	0: Open drain with internal pull-up resistor 1: Direct drive
			5	R/W	P25_DRV	0: Open drain with internal pull-up resistor 1: Direct drive
			4	R/W	P24_DRV	0: Open drain with internal pull-up resistor 1: Direct drive
			3:0		Reserved	Must Be Set to 0

4.4. GPIO

The FCM8531 has three GPIO ports: P0[7:2], P1[7:0], and P2[6:4], which can be set as direct drive or open drain through DRV0, DRV1, and DRV2 of the SFR. P0[7:2] are pulled down to GND by internal resistors and other digital IOs are pulled up to 5 V with internal resistors.

Table 15. GPIO Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
P0 (80h)	P07	P06	P05	P04	P03	P02	Reserved		FFh
P1 (90h)	P17	P16	P15	P14	P13	P12	P11	P10	FFh
P2 (A0h)	Reserved	P26	P25	P24	Reserved				FFh
P0_CFG (F8h)	P07_IO	P06_IO	P05_IO	P04_IO	P03_IO	P02_IO	Reserved		00h
IO_CFG (F9h)	EI_CFG1	EI_CFG0	I12_CFG1	I12_CFG0	P2_CFG1	P2_CFG0	P1_CFG1	P1_CFG0	00h
DRV0 (FCh)	P07_DRV	P06_DRV	P05_DRV	P04_DRV	P03_DRV	P02_DRV	Reserved		00h
DRV1 (FDh)	P17_DRV	P16_DRV	P15_DRV	P14_DRV	P13_DRV	P12_DRV	P11_DRV	P10_DRV	00h
DRV2 (FEh)	Reserved	P26_DRV	P25_DRV	P24_DRV	Reserved				00h

4.4.1 GPIO Schematic

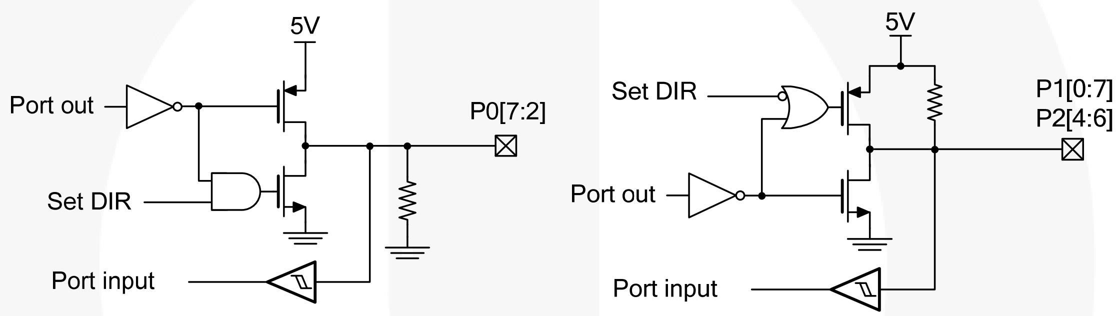

Figure 37. GPIO

4.4.2 Description

P0[7:2] can be defined as a GPIO or PWM output signal (U, V, W, X, Y, and Z) by using P0_CFG of the SFR. After reset, P0[7:2] is pre-set to a PWM output signal and other DIO pins are pre-set as the GPIO.

Multi-functional pins P1[7:0] and P2[6:4] can be set through IO_CFG (F9h) of the SFR *(see Table 16 and Table 17*).

Set SFR IO_CFG (F9h)[1:0] to configure P1[7:0] and distribute the serial bus (SPI Mode, I^2C Mode, UART Mode).

Table 16. P1_CFG[1:0]

CFG[1:0]	P17	P16	P15	P14	P13	P12	P11	P10
00 (Default)	SCK	MISO	MOSI	SPSSN / TDO	SDA	SCL	TX	RX
	SPI / OCDS				I2C		UART	
01	SCK	MISO	MOSI	SPSSN / TDO	TX	RX	SDA	SCL
	SPI / OCDS				UART		I2C	
10	SDA	SCL	TX	RX	SCK	MISO	MOSI	SPSSN / TDO
	I2C		UART		SPI / OCDS			
11	TX	RX	SDA	SCL	SCK	MISO	MOSI	SPSSN / TDO
	UART		I2C		SPI / OCDS			

P2[6:4] are set, by default, to be as GPIO pins. The DRV2 (FEh) register selects either open drain or direct driver. According to different purposes, the IO_CFG (F9h) register is set to distribute the timer input (Timer 0, Timer 1, Timer 2) pin assignment as shown in Table 17 below.

Table 17. P2_CFG[1:0]

CFG[1:0]	P26	P25	P24
00 (Default)	CC2	CC1	CC0
	Capture and Compare		
01	CC2	CC1	CC0
	Capture and Compare		
10	T2	T1	T0
	TMR2	TMR1	TMR0
11	T0	T2EX	T2
	TMR0	TMR2	

P1[6:0] can also be configured as an input pin of External Interrupt 12 (*see Table 18*).

Users can turn on INT12 and choose the Trigger Type by setting IO_CFG (F9h)[5:4].

Table 18. INT 12_CFG

		I12CFG[1:0] = 01, 10, 11 (Enable INT12)
INT12_CFG [7:0]	INT12_CFG [7]	OSC check assigned to INT12
	INT12_CFG [6]	P16 assigned to INT12
	INT12_CFG [5]	P15 assigned to INT12
	INT12_CFG [4]	P14 assigned to INT12
	INT12_CFG [3]	P13 assigned to INT12
	INT12_CFG [2]	P12 assigned to INT12
	INT12_CFG [1]	P11 assigned to INT12
	INT12_CFG [0]	P10 assigned to INT12

P2[6:4] can also be configured as an input pin of External Interrupt 0 or External Interrupt 1 by SFR IO_CFG (F9h)[7:6] as shown in Table 19.

Table 19. EI_CFG[1:0]

CFG[1:0]	P26	P25	P24
10		External Interrupt 1	External Interrupt 0
11	External Interrupt 0		

The GPIO pins include P0[7:2], P1[7:0], and P2[6:4], and P1 and P2 pins are set as shown in Table 20.

Table 20. All GPIO Configuration and Function

Pin	P1_CFG=00 P2_CFG=00	P1_CFG=01 P2_CFG=01	P1_CFG=10 P2_CFG=10	P1_CFG=11 P2_CFG=11	I12CFG[1:0]≠00 INT12_CFG=7Fh	EI_CFG [1:0]= 10	EI_CFG [1:0]= 11
P10	RX	SCL	SPSSN	SPSSN	INT12		
P11	TX	SDA	MOSI	MOSI	INT12		
P12	SCL	RX	MISO	MISO	INT12		
P13	SDA	TX	SCK	SCK	INT12		
P14	SPSSN	SPSSN	RX	SCL	INT12		
P15	MOSI	MISO	TX	SDA	INT12		
P16	MISO	MISO	SCL	RX	INT12		
P17	SCK	SCK	SDA	TX			

Pin	P1_CFG=00 P2_CFG=00	P1_CFG=01 P2_CFG=01	P1_CFG=10 P2_CFG=10	P1_CFG=11 P2_CFG=11	I12CFG[1:0]≠00 INT12_CFG=7Fh	EI_CFG [1:0]= 10	EI_CFG [1:0]= 11
P24	CC0	CC0	T0	T2		INT0	
P25	CC1	CC1	T1	T2EX		INT1	
P26	CC2	CC2	T2	T0			INT0

4.5. Timer 0

Timer 0 is a 16-bit timer/counter determined in Timer Mode or Counter Mode by SFR TMOD (89h). In Timer Mode, its counter value is increased by one for every 12 system cycles. In Counter Mode, a counter value is increased by one when each falling edge on the T0 pin. The maximum frequency on T0 cannot exceed $f_{SYS}/2$ because a falling edge (HIGH-to-LOW) of the signal needs to be confirmed in two clocks.

Table 21. Timer Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
IEN0 (A8h)	EA	WDT	ET2	ES0	ET1	EX1	ET0	EX0	00h
TCON (88h)	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
TMOD (89h)	GATE1	C/T1	T1MOD		GATE0	C/T0	T0MOD		00h
TL0 (8Ah)	Timer 0, LOW Byte								00h
TH0 (8Ch)	Timer 0, HIGH Byte								00h

4.5.1 Block Diagram

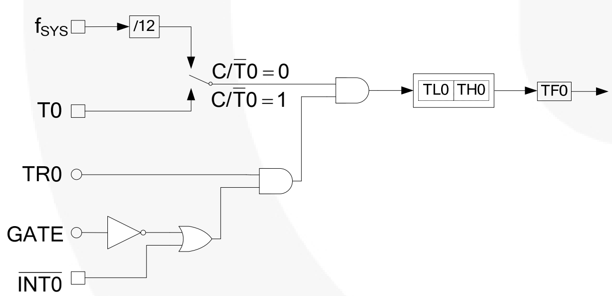

Figure 38. Timer 0 in Mode 0 and Mode 1

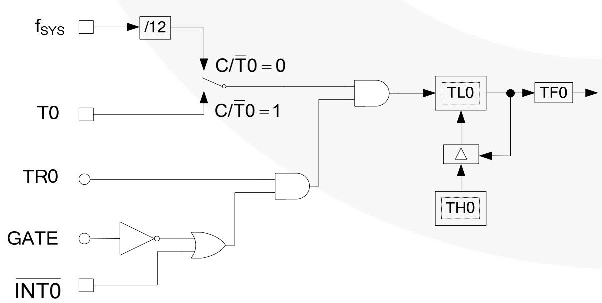

Figure 39. Timer 0 in Mode 2

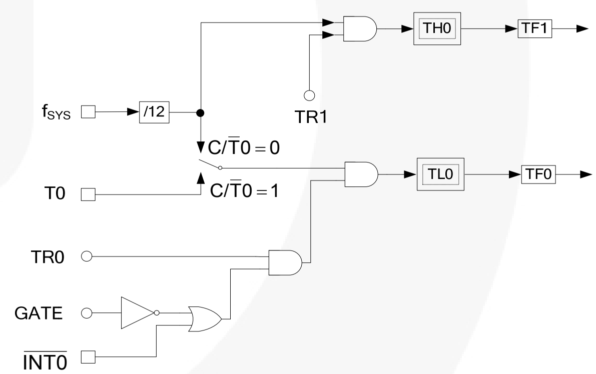

Figure 40. Timer 0 in Mode 3

4.5.2 Description

Timer 0 is set by SFR TMOD (89h) and SFR TCON (88h) in four modes.

Table 22. Timer 0 Mode

Mode	Description
0	13-bit timer/counter
1	16-bit timer/counter
2	8-bit auto-reload timer/counter
3	Timer 1 is disabled. Timer 0 handles two 8-bit timer/counter

Mode 0:
When SFR TMOD (89h)[1:0] = b'00, Timer 0 becomes a 13-bit timer or counter. SFR TMOD (89h)[2] determines whether it is a timer (TMOD[2] = 0) or a counter (TMOD[2] = 1).

When the Timer 0 is a timer, the counter frequency is equal to f_{SYS} divided by 12.

When the Timer 0 is a counter, the counter is counted when a falling edge (HIGH-to-LOW) is detected on the T0 pin.

In Mode 0, the 13 bits are composed of two registers: eight bits at TH0 and five bits at TL0. TL0 is divided into two blocks: three most significant bits and the other five bits. The three most significant bits are ignored and TL0's lower five bits and TH0's eight bits compose a 13-bit timer or counter.

Once Timer 0 / Counter 0 overflows, TCON[5] flag is set and a Timer 0 interrupt is triggered. The interrupt flag can be cleared by the hardware or software.

Mode 1:
When TMOD (89h)[1:0] = b'01, Timer 0 becomes a 16-bit counter or timer. TMOD (89h)[2] determines whether it is a timer or a counter.

When the Timer 0 is a timer, the counter frequency is equal to f_{SYS} divided by 12.

When the Timer 0 is a counter, the counter is counted when a falling edge (HIGH-to-LOW) is detected on the T0 pin.

In Mode 1, the 16 bits are composed of two 8-bit registers, TH0 and TL0. The TH0 is the HIGH byte, and TL0 is the LOW byte.

Mode 2:
When TMOD (89h)[1:0] = b'10, it automatically reloads an 8-bit interval value. It uses the lower byte TL0 as its counter register. Once TL0 overflows, TCON[5] flag is set and an interrupt is triggered. Upon overflow, TL0 loads data from TH0 and TL0 restarts its counting.

Mode 3:
When TMOD (89h)[1:0] = b'11, Timer 0 becomes an independent 8-bit counter or timer. In this mode, Timer 1 is inhibited because of occupation of the TF1 flag. Once TL0 overflows, the TCON[5] TF0 flag is set and Timer 0 interrupt is triggered. When TH0 overflows, the TCON[7] TF1 flag is set and Timer 1 interrupt is triggered. The TR0 bit in TCON controls the start/stop counting of TL0. The GATE0 bit sets whether to stop/continue counting when the External Interrupt 0 occurs. The TR1 bit in TCON controls the start/stop counting of TH0. In this mode, TH0 does not have the GATE function.

4.6. Timer 1

Timer 1 is a 16-bit timer / counter determined in Timer Mode or Counter Mode by SFR TMOD (89h). In Timer Mode, its counter value is increased by one for every 12 system cycles. In Counter Mode, the counter value is increased by one in each falling edge on T1 pin. The maximum frequency on T1 cannot exceed $f_{SYS}/2$ because a falling edge (HIGH-to-LOW) of signal needs to be confirmed in two clocks.

Table 23. Timer 1 Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
IEN0 (A8h)	EA	WDT	ET2	ES0	ET1	EX1	ET0	EX0	00h
TCON (88h)	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
TMOD (89h)	GATE1	C/T1	T1MOD		GATE0	C/T0	T0MOD		00h
TL1 (8Bh)	Timer 1, LOW Byte								00h
TH1 (8Dh)	Timer 1, HIGH Byte								00h

4.6.1 Block Diagrams

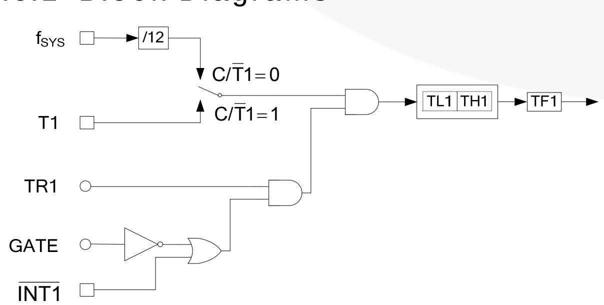

Figure 41. Timer 1 in Mode 0 and Mode 1

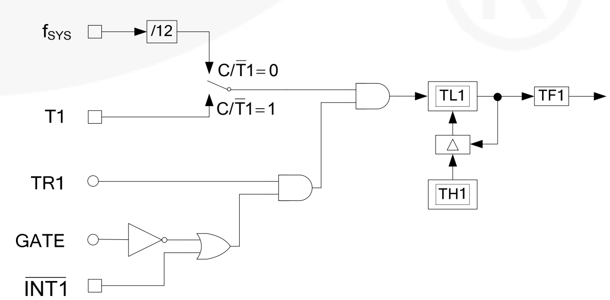

Figure 42. Timer 1 in Mode 2

4.6.2 Description

Timer 1 is set by SFR TMOD (89h) and SFR TCON (88h) in three modes.

Table 24. Timer 1 Mode

Mode	Description
0	13-bit timer/counter
1	16-bit timer/counter
2	8-bit auto-reload timer/counter
3	Timer 1 is stopped

Mode 0:
When SFR TMOD (89h)[5:4] = b'00, Timer 1 becomes a 13-bit timer or counter. TMOD (89h)[6] determines whether it is a timer (TMOD[6] = 0) or a counter (TMOD[6] = 1).

When the Timer 1 is a timer, the counter frequency is equal to f_{SYS} divided by 12.

When the Timer 1 is a counter, the counter is counted when a falling edge (HIGH-to-LOW) is detected on the T1 pin.

In Mode 0, the 13 bits are composed of two registers: eight bits at TH1 and five bits at TL1. TL1 is divided into two blocks: three most significant bits and five other bits. The three most significant bits are ignored and TL1's lower five bits and TH1's eight bits compose a 13-bit timer or counter.

Once Timer 1 / Counter 1 overflows, TCON[7] flag is set and a Timer 1 interrupt is triggered. The interrupt flag can be cleared by the hardware or software.

Mode 1:
When TMOD (89h)[5:4] = b'01, Timer 1 becomes a 16-bit timer or counter. TMOD (89h)[6] determines whether it is a timer or a counter.

When the Timer 1 is a timer, the counter frequency is equal to f_{SYS} divided by 12.

When the Timer 1 is a counter, the counter is counted when a falling edge (HIGH-to-LOW) is detected on the T1 pin.

In Mode 1, the 16 bits are composed of two 8-bit registers, TH1 and TL1. The TH1 is the HIGH byte and TL1 is the LOW byte.

Mode 2:
When TMOD (89h)[5:4] = b'10, Timer 1 becomes an 8-bit auto-reload timer or counter. It automatically reloads the 8-bit timer or counter interval value. It uses the lower bytes' TL1 as its counter register. Once TL1 overflows, TCON[7] flag is set and an interrupt is triggered. Upon overflow, TL1 loads data from TH1 and TL0, then restarts counting.

Mode 3:
In Timer 1 Mode 3, Timer 1 is stopped.

4.7. Timer 2

Timer 2 is a 16-bit timer/counter can be configured in three modes: Timer Mode, Event Counter Mode, and Gated Timer Mode. Additionally, two reload modes are selectable in reload functions: Auto-Reload or External Reload.

Table 25. Timer 2 Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
IEN0 (A8h)	EA	WDT	ET2	ES0	ET1	EX1	ET0	EX0	00h
IEN1 (B8h)	EXEN2	SWDT	Reserved	EX5	EX4	EX3	EX2	EX7	00h
IRCON (C0h)	EXF2	TF2	Reserved	IEX5	IEX4	IEX3	IEX2	IEX7	00h
CCEN (C1h)	Reserved		COCA H2	COCA L2	COCA H1	COCA L1	COCA H0	COCA L0	00h
CCL1 (C2h)	Compare / Capture Register 1, LOW Byte								00h
CCH1 (C3h)	Compare / Capture Register 1, HIGH Byte								00h
CCL2 (C4h)	Compare / Capture Register 2, LOW Byte								00h
CCH2 (C5h)	Compare / Capture Register 2, HIGH Byte								00h
T2CON (C8h)	T2PS	I3FR	I2FR	T2R1	T2R0	Reserved	T2I1	T2I0	00h
CRCL (CAh)	Compare / Capture Register, LOW Byte								00h
CRCH (CBh)	Compare / Capture Register, HIGH Byte								00h
TL2 (CCh)	Timer 2, LOW Byte								00h
TH2 (CDh)	Timer 2, HIGH Byte								00h

4.7.1 Block Diagram

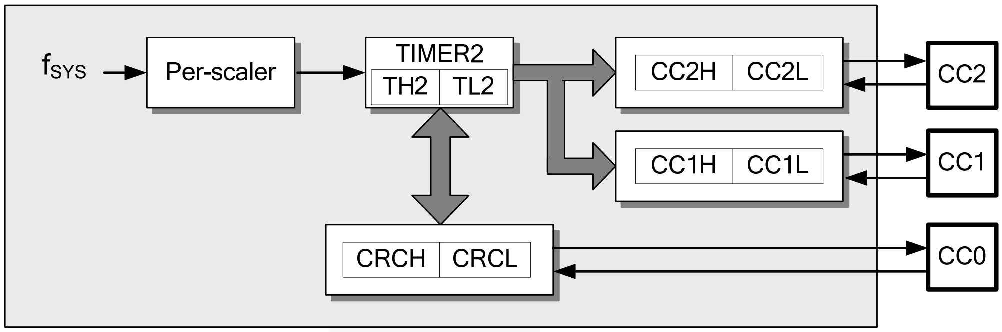

Figure 43. Timer 2 Block Diagram

4.7.2 Description

Timer 2 can be configured in Timer Mode, Event Counter Mode, and Gate Timer Mode, as shown in Figure 44.

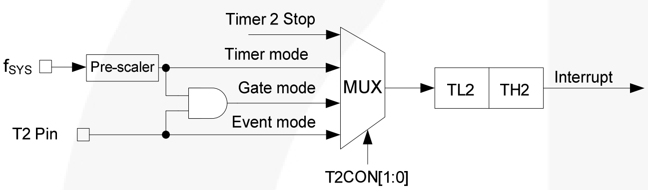

Figure 44. Timer 2 Clock Source

Timer Mode:
This mode is invoked by setting SFR T2CON[1:0] = b'01. In this mode, the count rate is derived from f_{SYS}, then passed through the pre-scale. The pre-scale is selectable between $f_{SYS}/12$ and $f_{SYS}/24$; the Timer 2 is incremented every 12 or 24 clock cycles, depending on pre-scale selection. When T2CON (C8h)[7] = 0 (T2PS), Timer 2 is incremented every 12 clock cycles; otherwise every 24 cycles.

Event Counter Mode:
This mode is invoked by setting T2CON[1:0] = b'10. In this mode, the count rate is derived from the pin T2. It is incremented when the signal on the pin T2 changes its state from 1 to 0 (HIGH to LOW). The maximum frequency on the T2 pin cannot exceed $f_{SYS}/2$.

Gate Timer Mode:
This mode is invoked by setting T2CON[1:0] = b'11. In this mode, the Timer 2 is incremented every 12 or 24 clock cycles, depending on T2PS, but it is additionally gated by the pin T2. When T2 = 0, the Timer 2 is stopped; otherwise, the Timer 2 starts its increment.

Timer 2 Reload Mode can be executed in Auto-Reload Mode or External Reload Mode, as shown in Figure 45.

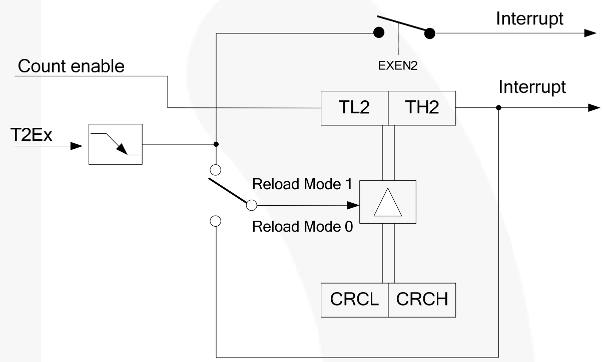

Figure 45. Timer 2 Reload Mode

Auto-Reload:
When TH2 and TL2 of Timer 2 overflow, values from CRCH and CRCL are automatically reloaded into the TH2 and TL2 registers.

External Reload:
Reload occurs when a negative signal transition (HIGH-to-LOW) occurs at the T2 pin. Values from CRCH and CRCL are reloaded into the TH2 and TL2 registers. SFR IEN1 (B8h)[7], the EXEN2 bit have to be set. Timer 2 external reload flag (IRCON (C0h)[7]) EXF2 is cleared by software.

There are three compare functions for Timer 2: CRC, CC1, and CC2. CRC is enabled by setting CCEN (C1h)[1:0] = b'10 and enabling interrupt EX3. CC1 is enabled by setting CCEN[3:2] = b'10 and enabling interrupt EX4. CC2 is enabled by setting CCEN[5:4] = b'10 and enabling interrupt EX5. Once the value of the Timer 2 (composed of TH2 and TL2) equals to the value of compare register CRC, CC1, or CC2; a corresponding interrupt EX3, EX4, or EX5 is triggered and the corresponding pin CC0, CC1, or CC2 (P24 / P25 / P26) outputs HIGH level. The pin is driven back to LOW on Timer 2 overflow.

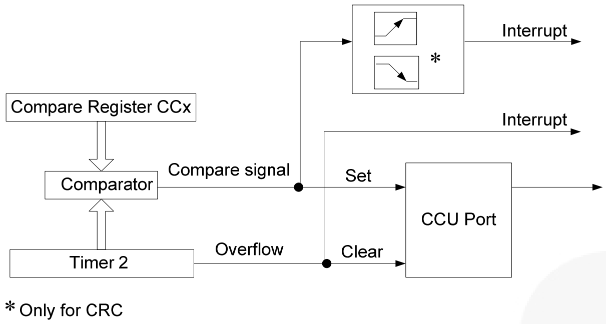

Figure 46. Timer 2 Compare Mode

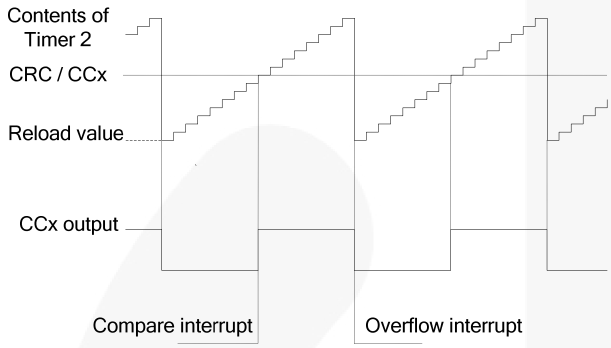

Figure 47. Compare Mode Operation

Timer 2 has three capture functions enabled by the SFR CCEN (C1h), very similar to the compare functions, besides setting the CCEN register. There are two capture modes:

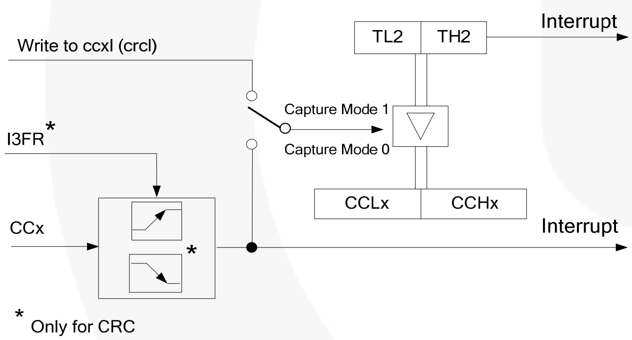

Figure 48. Timer 2 Capture Mode

Capture Mode 0:

SFR CCEN[5:4] = b'01, CCEN[3:2] = b'01, or CCEN[1:0] = b'01 are correspondingly set to CC2, CC1, or CRC. In Mode 0, once a rising edge on input pin CC2, CC1, or CC0 is detected; the capture function is executed and the counter of Timer 2 begins counting until next the rising edge occurs. Values in TH2 and TL2 are then latched into appropriate capture registers. Those registers are CCHx, CCLx, CRCL, and CRCH. This function is useful for calculating a pulse width. In this mode, no interrupt request is generated.

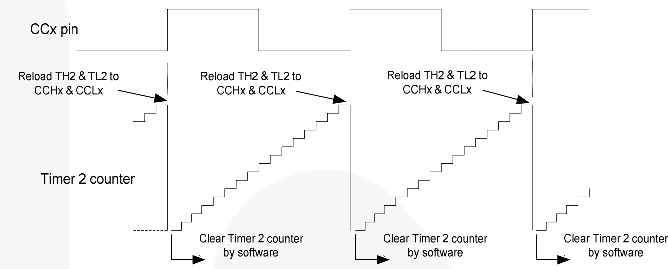

Figure 49. Capture Mode 0 Operation

Capture Mode 1:

This mode is invoked by setting appropriate register CCEN[5:4] = b'11, CCEN[3:2] = b'11, or CCEN[1:0] = b'11. Captured operation is executed by any writing into the low-order byte of the dedicated capture register. The written value to the capture register is irrelevant for this function. Values in TH2 and TL2 are then latched into appropriate capture registers once the written operation occurs. In this mode, no interrupt request is generated.

4.8. Interrupt

16 interrupt sources are available in the FCM8531 and they are divided into six groups. One of four priority levels can be assigned to each of the groups. SFR IP0 (A9h) and SFR IP1 (B9h) are used to prioritize the interrupt level. Each of the interrupt sources can be individually enabled or disabled by corresponding enable flag in SFR IEN0 (A8h), IEN1 (B8h), or IEN2 (9Ah). Additionally, all interrupts can be globally enabled or disabled by the EA bit in SFR IEN0. Each interrupt has its own interrupt request flag that can be read at SFR IRCON (C0h) or SFR IRCON2 (BFh).

Some of interrupt sources are triggered by the detection of FCM8531 itself or motor status. For instance: ADC ready, Hall signal changing, Hall signal timeout, Hall signal error, and short-circuit detection.

Table 26. Interrupt Vector

Interrupt Source	Interrupt Vector	Symbol	Trigger	Interrupt No. *(Keil C)
External Interrupt 0 (INT0)	0003h	EX0	Falling / LOW	0
Timer 0 Overflow	000Bh	ET0		1
External Interrupt 1 (INT1)	0013h	EX1	Falling / LOW	2
Timer 1 Overflow	001Bh	ET1		3
Serial	0023h	ES0		4
Timer 2	002Bh	ET2		5
I^2C	0043h	EX7		8
SPI (INT2)	004Bh	EX2		9
COM0 (INT3)	0053h	EX3	Rising / Falling	10
COM1	005Bh	EX4	Rising	11
COM2	0063h	EX5	Rising	12
FAULT	008Bh	EX8	Rising	17
ADC Ready	0093h	EX9		18
Hall Edge	009Bh	EX10	Rising / Falling / Rising and Falling	19
AMC	00A3h	EX11	Rising	20
External Interrupt 12 (INT12)	00ABh	EX12	Rising / Falling / Rising and Falling	21

Table 27. Interrupt Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
IEN2 (9Ah)	Reserved		EX12	EX11	EX10	EX9	EX8	Reserved	00h
IEN0 (A8h)	EA	WDT	ET2	ES0	ET1	EX1	ET0	EX0	00h
IEN1 (B8h)	EXEN2	SWDT	Reserved	EX5	EX4	EX3	EX2	EX7	00h
IP0 (A9h)	Reserved	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	00h
IP1 (B9h)	Reserved		IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	00h
IRCON2 (BFh)	Reserved			IEX12	IEX11	IEX10	IEX9	IEX8	00h
IRCON (C0h)	EXF2	TF2	Reserved	IEX5	IEX4	IEX3	IEX2	IEX7	00h

Table 28. IO Configuration

IO_CFG	Bit	Type	Name	IO Configuration
Address F9h 00h after reset	7:6	R/W	EI_CFG1 EI_CFG0	INT0, INT1 Pin Assignment 00: Reserved 01: Reserved 10: P24→INT0, P25→INT1 11: P26→INT0
	5:4	R/W	I12_CFG1 I12_CFG0	INT12 Edge Trigger Type 00: Disable 01: Rising / Falling 10: Rising 11: Falling
	3:2	R/W	P2_CFG1 P2_CFG0	P2 (TMR assignment) Refer to Table[P2_CFG1:P2CFG0]
	1:0	R/W	P1_CFG1 P1_CFG0	P1 (Serial bus assignment) Refer to Table[P1_CFG1:P1_CFG0]

4.8.1 Description

SFR IEN0 (A8h), IEN1 (B8h), and IEN2 (9Ah) are used to enable or disable 16 interrupts. Each interrupt has its own interrupt request flag and these interrupt request flags can be read at SFR IRCON (C0h) and SFR IRCON2 (BFh). Interrupt priorities are prioritized by SFR IP0 and IP1. Additionally, users may assign signal inputs of interrupt sources through SFR IO_CFG (F9h). Besides IO_CFG as shown in Table 28, the related P2_CFG and P1_CFG are as shown in Table 16 and Table 17.

P24 or P26 pin may be assigned to be the source trigger input of the external interrupt 0 by setting the SFR IO_CFG (F9h). P25 pin may only be assigned to be the source trigger input of the external interrupt 1. These two interrupts are triggered by low level active or falling transaction with setting of SFR TCON (88h) bit 2 and bit 0.

When Timer 0 or Timer 1 is in Timer Mode or Counter Mode, the TF0 or TF1 interrupt flag is set once it overflows. These flags can be cleared by software.

For Timer 2, the TF2 or EXF2 may be set once it overflows or external reload is triggered. In the interrupt service routine, users must identify the set flag and clearing the flag must be accomplished in the interrupt service routine.

The FCM8531 has three COMx interrupts. COMx is comprised of the Compare Mode interrupt and the Capture Mode interrupt. Enable Compare Mode or Capture Mode through the CCEN (C1h) register. Both modes use the same interrupt source and the same external trigger pins.

The serial port interrupt yields two flags: RI and TI. Users must identify RI or TI in the interrupt service routine. These two flags must be cleared in the interrupt service routine.

Once data is received / transmitted in SPI Mode, an external interrupt EX2 is generated. The data from the slave device can be correctly read in SFR SPDAT (E3h).

In I^2C Mode, an external interrupt, EX7, is generated after completing the following: start, address and data transfer. This flag must be cleared in the interrupt service routine to avoid an external interrupt EX7 mistakenly triggering every time I^2C's status changes.

The ADC-ready interrupt is triggered by the SAW or by the Timer 0 overflow. It is set at SFR ADCCFG (1Fh). After sampling and conversion, the interrupt is triggered and the data in those ADC registers is available to be read. The highest ADC sampling frequency is about 30 kHz. The ADC triggering is synchronized with the SAW if the ADC ready interrupt is set according to the SAW.

Hall interrupt is invoked by choosing a Hall edge type at the SFR HALINT (1Bh)[1:0]. The AMC detects GPIOs to obtain the Hall signals. At this time, a Hall signal transaction triggers an interrupt according to the selected Hall edge type.

A fault interrupt is triggered by any one of following conditions: the detection of Hall Slow, Hall Error, and any SHORT Circuit on the IA, IB, or IC pin. Reading SFR MSTAT (3Fh) in the interrupt service routine identifies the fault cause. The Hall Slow is the circumstance the Hall signal status has not changed for exceeding setting time and this causes an overflow in the counter of the Hall period. The SHORT protection mechanism senses the motor's three-phase current by voltages on the IA, IB, and IC pins exceeding SHORT voltage. Hall Error detects abnormal combination of the Hall signals.

Through the AMC interrupt, MCU is informed that AMC completes its data transmitting.

To distribute the interrupt 12 input signal, set SFR IO_CFG (F9h)[5:4] to choose INT12 trigger type. Then set the SFR INT12_CFG (FAh) to choose P1[6:0] pin(s) to be the interrupt source pin(s). Examine INT12_STA (F8h) to identify the trigger source pin.

Interrupt Prioritization:

Once an interrupt occurs, the interrupt service jumps to the specified address per the interrupt vector and executes the interrupt service routine. The currently running interrupt service routine can only be interrupted by an interrupt with a higher priority level. No interrupt with the same or lower priority level may interrupt the currently running interrupt service routine.

The four interrupt priority levels run from level 3, the highest priority level, to Level 0, the lowest priority level. These are set in SFR IP0 (A9h) and SFR IP1 (B9h) and the setting of priority level is shown in Table 29.

Table 29. Interrupt Priority Level

Level	Priority	IP1.x	IP0.x
Level 0	Lowest	0	0
Level 1		0	1
Level 2		1	0
Level 3	Highest	1	1

The 16 interrupts fall into six groups and the definitions of the six groups are shown in Table 30.

Table 30. Interrupt Priority Groups

Interrupt Group	Highest Priority	Middle Priority	Lowest Priority	Set Register Flag	Priority within Same Priority Level
Group 0	External Interrupt 0		I2C	IP1[0], IP0[0]	Highest
Group 1	Timer 0 Overflow	FAULT	SPI	IP1[1], IP0[1]	
Group 2	External Interrupt 1	ADC Ready	COM0	IP1[2], IP0[2]	
Group 3	Timer 1 Overflow	Hall Edge	COM1	IP1[3], IP0[3]	
Group 4	Serial	AMC	COM2	IP1[4], IP0[4]	
Group 5	Timer 2	External Interrupt 12		IP1[5], IP0[5]	Lowest

Inside Table 30, interrupts sources from the second column have the highest priority in the group (row); sources from the third column have middle priority; and sources from the fourth column have the lowest priority. Inside the same group, the priority structure is fixed by hardware and there is no ability to change interrupt priority.

There is another priority level structure between groups. Group 0 has the highest priority level and Group 5 has the lowest. The priority level of interrupt groups can be set from 0 to 3 by changing SFR IP0 and IP1 in the fifth column.

All priority types are taken into account when more than one interrupt is requested: the most important is the priority level set by IP0 and IP1 SFR, then the natural priority between groups (for the same priority level between groups), and last the priority inside each group.

4.9. INT12

The input signal(s) of external interrupt 12 can be assigned by SFR INT12_CFG (FAh) register to the P1[6:0] pin(s). INT12_STA (FBh) register may identify the pin that triggers the interrupt. Additionally, the IO_CFG (F9h) register determines the interrupt edge type.

Table 31. INT12 Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
IEN2 (9Ah)	Reserved		EX12	EX11	EX10	EX9	EX8	Reserved	00h
IEN0 (A8h)	EA	WDT	ET2	ES0	ET1	EX1	ET0	EX0	00h
IRCON2 (BFh)	Reserved			IEX12	IEX11	IEX10	IEX9	IEX8	00h
IO_CFG (F9h)	EI_CFG1	EI_CFG0	I12_CFG1	I12_CFG0	P2_CFG1	P2_CFG0	P1_CFG1	P1_CFG0	00h
INT12_CFG (FAh)	ASI_OSC	ASI_P16	ASI_P15	ASI_P14	ASI_P13	ASI_P12	ASI_P11	ASI_P10	00h
INT12_STA (FBh)	ST_OSC	ST_P16	ST_P15	ST_P14	ST_P13	ST_P12	ST_P11	ST_P10	00h

4.9.1 Block Diagram

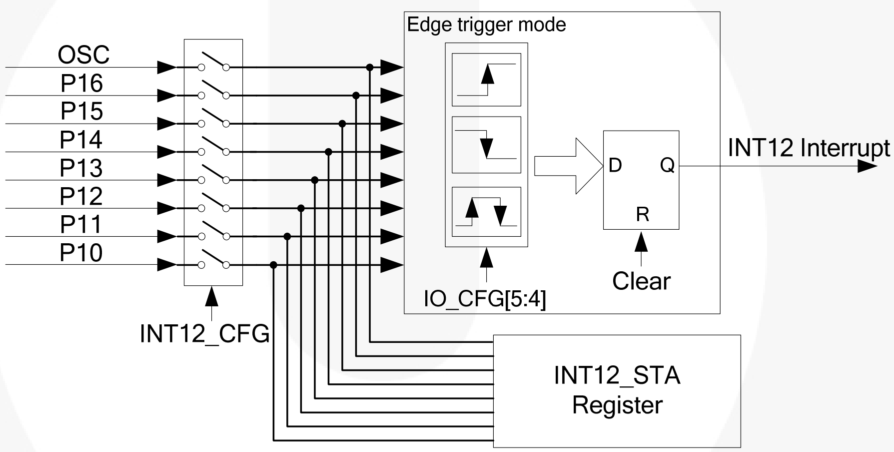

Figure 50. INT12 Block Diagram

4.9.2 Description

As a special interrupt, all pins of P1[6:0] can be the input signal source(s) of external interrupt 12. It is determined by setting the SFR INT12_CFG (FAh). In this circumstance, pin(s) defined by SFR INT12_CFG may trigger INT12 and identification is accomplished by reading SFR INT12_STA (FBh) and checking the triggering source.

External interrupt 12 provides three trigger types set by SFR IO_CFG (F9h)[5:4]. The three types are: Rising Trigger, Falling Trigger, and Rising/Falling Trigger.

4.10. UART

The Universal Asynchronous Receiver/Transmitter (UART) is a flexible full-duplex synchronous / asynchronous receiver / transmitter. It is fully compatible with the MCS®51 serial port.

Table 32. UART Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
PCON (87h)	SMOD	WDT_TM	ISR_TM	Reserved			STOP	IDLE	08h
SCON (98h)	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00h
SBUF (99h)	Serial Port, Data Buffer								00h
IEN0 (A8h)	EA	WDT	ET2	ES0	ET1	EX1	ET0	EX0	00h
SRELL (AAh)	Reload Register Low Byte (Baud-Rate Generator)								D9h
SRELH (BAh)	Reserved						Reload Register HIGH Byte (Baud-Rate Generator)		03h
ADCON (D8h)	BD	Reserved							00h

4.10.1 Block Diagram

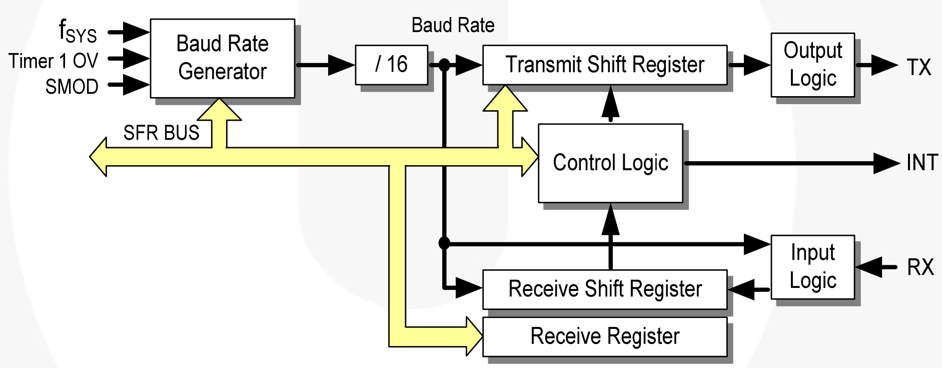

Figure 51. Serial Port Block Diagram

4.10.2 Description

UART includes one synchronous mode and three asynchronous modes set by bits SM0 and SM1 in SFR SCON (98h). *Please refer to Table 33 for more details of the transmission format.*

There are two options to generate the baud rate: by Timer 1 and by the internal baud rate generator. The internal baud rate generator is set by SFR SRELH (BAh) and SFR SRELL (AAh).

Table 33. Serial Port Mode vs. Baud-Rate

SM0	SM1	Mode	Description	Baud Rate
0	0	Mode 0	Shift Register	$f_{SYS}/12$
0	1	Mode 1	8-Bit UART	Variable (Timer 1 or Internal Baud-Rate Generator)
1	0	Mode 2	9-Bit UART	$f_{SYS}/64$ (SMOD=0), $f_{SYS}/32$ (SMOD=1)
1	1	Mode 3	9-Bit UART	Variable (Timer 1 or Internal Baud-Rate Generator)

Equations for baud-rate calculation (Mode 1 and Mode 3):

From Timer 1:

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times f_{\text{SYS}}}{32} \times (\text{Timer 1 reload frequency}) \quad (5)$$

From internal baud rate generator:

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times f_{\text{SYS}}}{64 \times (2^{10} - \text{SREL})} \quad (6)$$

Mode 0:

Mode 0 is for synchronous 8-bit serial reception / transmission. TxD outputs the shift clock and RxD is for data input / output. The baud rate is fixed at $f_{SYS}/12$. Before receiving, REN should be set and RI should be cleared in SFR SCON (98h) register. After receiving, RI is set and triggers a serial interrupt.

Data is sent by writing the SBUF (99h) register. After sending data, the TI of SFR SCON (98h) register is set and triggers an interrupt.

Mode 1:

Mode 1 is for asynchronous 8-bit serial reception / transmission. The baud rate should be set in the software. The BD bit of SFR ADCON (D8h) chooses the baud rate type. When set, the additional internal baud-rate generator is used; otherwise, Timer 1 overflow is used. The frequency of the internal baud-rate generator is set by SFR SRELL (AAh) and SFR SRELH (BAh). Additionally, the baud rate can be doubled by setting the SMOD bit of SFR PCON (87h).

By writing to SFR SBUF (99h), transmission is started and data is output through the TxD pin. Transmitted data starts with a Start bit (always 0), then eight bits of data, then it ends in a Stop bit (always 1).

Data is input from the RxD pin. Starting data reception is triggered by a falling edge detected at the RxD pin and the data transmission synchronizes with the first falling edge. Input data is available after completion of the reception in SFR SBUF (99h) and the value of the Stop bit is available as the RB8 bit in SFR SCON (98h). During reception, the SBUF and RB8 is not changed until reception is complete.

Mode 2:

In Mode 2, the serial port is operated as a 9-bit UART with fixed baud rate of $f_{SYS}/32$ or $f_{SYS}/64$, determined by bit SMOD of SFR PCON.

By writing to the SFR SBUF (99h), transmission is started and data is output though the TxD pin. Transmitted data starts with a Start bit (always 0), then nine bits of data proceed, where the 9th bit is taken from bit TD8 of the SFR SCON (98h), after which it ends in a Stop bit (always 1).

Data is input from the RxD pin. Starting data reception is triggered by a falling edge detected at the RxD pin and the data transmission synchronizes with the falling edge. Input data is available after completion of the reception in the SFR SBUF (99h) and the value of the 9th bit is available as the RB8 flag in SFR SCON (98h). During the reception, the SBUF and RB8 is not changed until reception is complete.

Mode 3:

There is only one difference between Mode 2 and Mode 3: in Mode 3, the baud rate is sourced by either the internal baud rate generator or Timer 1 overflows.

The serial port is operated as a 9-bit the UART with programmable baud rate in Mode 3.

The baud rate's setting in Mode 3 is the same as Mode 1. Bit BD (ADCON[7]), SFR SRELH (BAh), and SFR SRELL (AAh) determine the baud rate source (Timer 0 overflow / internal baud rate generator) and frequency (internal baud rate generator only). The baud rate can be doubled by setting the SMOD bit of SFR PCON (87h).

By writing to the SFR SBUF (99h), transmission is started and data is output through the TxD pin. Transmitted data starts with a Start bit (always 0), then nine bits of data proceed, where the 9th bit is taken from bit TD8 of the SFR SCON (98h), after which it ends in a Stop bit (always 1).

Data is input from the RxD pin. Starting data reception is triggered by a falling edge detected at the RxD pin and the data transmission synchronizes with the first falling edge. Input data is available after completion of the reception in the SFR SBUF (99h) and the value of the 9th bit is available as the RB8 bit in SFR SCON (98h). During reception, the SBUF and RB8 is not changed until reception is complete.

4.11. SPI

The FCM8531 provides a Serial Peripheral Interface (SPI) module, with full duplex and synchronous communicating protocol, for communication and it is able to work as a host in the Master Mode or as a slave in the Slave Mode.

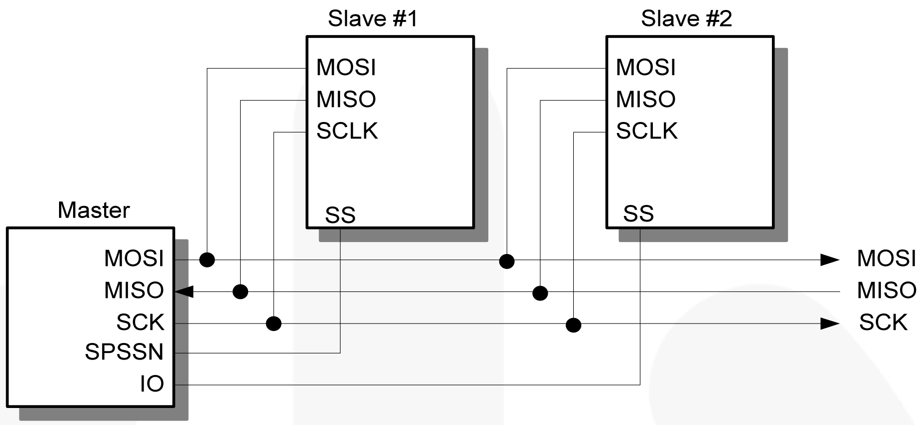

Figure 52. SPI Interface

Table 34. SPI Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
IEN0 (A8h)	EA	WDT	ET2	ES0	ET1	EX1	ET0	EX0	00h
IEN1 (B8h)	EXEN2	SWDT	Reserved	EX5	EX4	EX3	EX2	EX7	00h
IRCON (C0h)	EXF2	TF2	Reserved	IEX5	IEX4	IEX3	IEX2	IEX7	00h
SPSTA (E1h)	SPIF	WCOL	SSERR	Reserved					00h
SPCON (E2h)	SPR2	SPEN	Reserved	MSTR	CPOL	CPHA	SPR1	SPR0	34h
SPDAT (E3h)	SPI Data Register								00h
SPSSN (E4h)	Reserved							SSR	FFh

4.11.1 Block Diagram

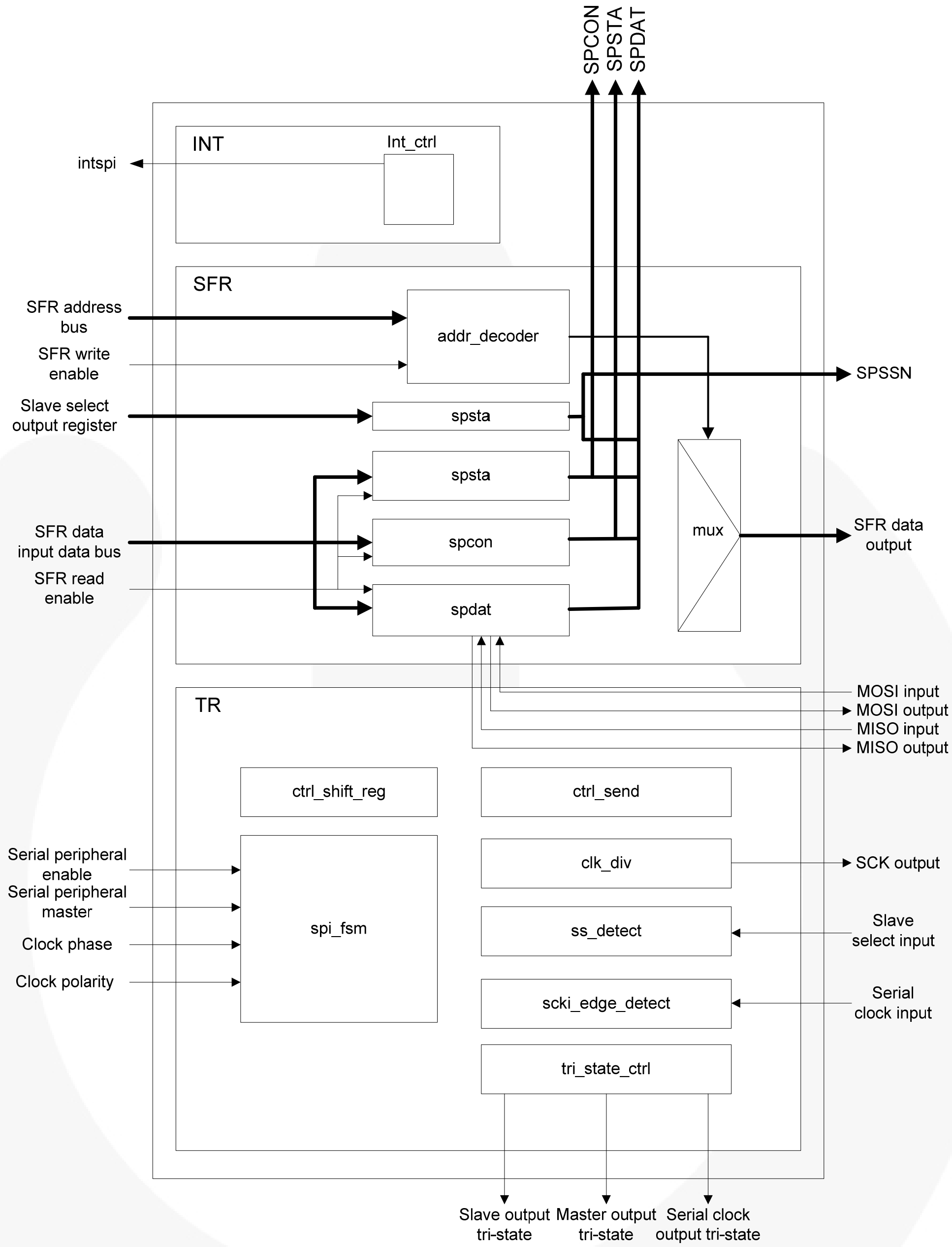

Figure 53. SPI Block Diagram

4.11.2 Description

The SPI operating mode is determined by setting bit MSTR of SFR SPCON (E2h): when 1, Master Mode is enabled; otherwise, Slave Mode is enabled.

In Master Mode, users can determine the SPI clock output rate by setting bits SPR2, SPR1, and SPR0. The clock polarity (CPOL) and clock phase (CPHA) bits are used to define the transmission format of Master Mode. The SPEN bit can enable or disable the SPI module.

Bit SSR of SFR SPSSN (E4h) directly maps to the SPSSN pin in Master Mode to notify the slave that SPI transmission / reception is starting. If there is more than one slave, users should use digital IO pins to notify and enable the slave device with which users want to communicate.

Transmission of the SPI in Master Mode is started by writing the data to SFR SPDAT (E3h). The data shifts out to the MOSI pin according to the serial clock pin on SCK. Simultaneously, a byte shifts in through the MISO pin. Once transmission is complete, flag SPIF (peripheral data transfer flag) is set and interrupt EX2 is triggered; after which, received data can be read from SFR SPDAT (E3h).

The SPIF flag must be cleared by reading SFR SPSTA (E1h) in software.

In Slave Mode, SPSSN and SCK are set as input pins and receive data from the master device.

Reception of SPI in Slave Mode is started once the SPSSN pin is LOW level. The data shift into the MOSI pin is synchronized to the serial clock on the SCK pin. Once reception is complete, the SPIF flag is set and interrupt EX2 is triggered; after which, the received data can be read from SFR SPDAT (E3h).

Transmission of SPI in Slave Mode is started by detecting SPSSN signal LOW. The data shifts out to the MISO pin according to the serial clock on SCK pin.

The SPI send / receive status can be read at SFR SPSTA (E1h). By default, the SPSSN pin is assigned to P14; MOSI pin to P15; MISO pin to P16; and SCK pin to P17.

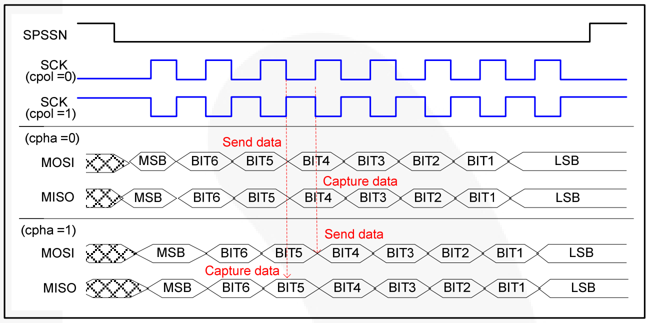

Figure 54. SPI Transmitter Frame Format

4.12. I^{2}C

With I^{2}C, the MCU is able to communicate with two or more devices by two wires: SCL and SDA. The maximum speed of SCL is 400 kbps. SCL is assigned to P12 by default; SDA is assigned to P13 by default.

The I^{2}C can operate in Master Mode or Slave Mode. START, Re-START, and STOP signals are generated automatically by hardware according to SFR I2CCON (DCh) setting in Master Mode to communicate with a slave device. In Slave Mode; START, Re-START, and STOP are also detected by hardware.

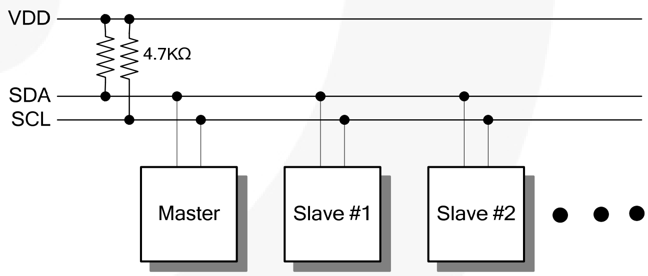

Figure 55. I^{2}C Interface

Table 35. I^{2}C Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
IEN0 (A8h)	EA	WDT	ET2	ES0	ET1	EX1	ET0	EX0	00h
IEN1 (B8h)	EXEN2	SWDT	Reserved	EX5	EX4	EX3	EX2	EX7	00h
IRCON (C0h)	EXF2	TF2	Reserved	IEX5	IEX4	IEX3	IEX2	IEX7	00h
I2CDAT (DAh)	I^{2}C Data Register								00h
I2CSTA (DDh)	I^{2}C Status Register								00h
I2CCON (DCh)	CR2	ENS1	STA	STO	SI	AA	CR1	CR0	00h
I2CADR (DBh)	I^{2}C Address							GC	00h

4.12.1 Block Diagram

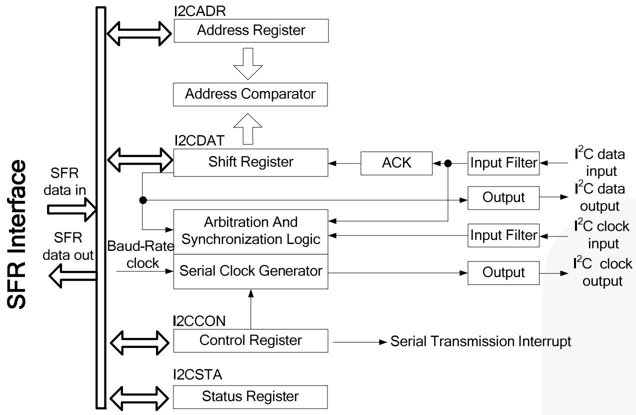

Figure 56. I²C Block Diagram

4.12.2 Description

The I²C Bus uses two signal lines, SCL and SDA, for data transferring and its protocol consists of device address and data. SCL is for clock output and SDA is for data transmission and reception. The data is read and stored in SFR I2CDAT (DAh). The value of SFR I2CADR (DBh) is used to select the slave device. SFR I2CSTA (DDh) indicates information of the transmission state of the I²C. I2CCON (DCh) is for choosing the work mode of I²C. There are four modes:

- In Master Transmitter Mode, the SCL pin outputs the serial clock and the SDA pin transfers serial data.
- In Master Receiver Mode, the SCL pin outputs the serial clock and the SDA pin receives serial data then shifts it into SFR I2CDAT (DAh).
- In Slave Transmitter Mode, the SCL pin receives the serial clock and the SDA pin transfer serial data.
- In Slave Receiver Mode, the SCL pin receives the serial clock and the SDA pin receives serial data then shifts it into SFR I2CDAT.

In Master Mode, set bit STA of SFR I2CCON (DCh) to start I²C transmission. The clock frequency divider is set by bits CR2, CR1, and CR0 of SFR I2CCON (DCh). When CR2=1, CR1=1, and CR0=1; the baud rate clock is generated as Timer 1 overflows; so the I²C Baud-Rate is controlled by Timer 1. In Slave Mode, the clock is sourced by host.

The data flow on the SDA pin of I²C includes the start signal (START), device address (ADDRESS), read/write signal (R/W), two acknowledge signals (ACK), data (DATA), and stop signal (STOP). The SCL pin sources a synchronous clock *(refer to Figure 57)*.

The synchronous clock is sourced by the master device.

START/STOP informs the slave devices of starting / ending transmission sent by the master device.

7-bit ADDRESS sent by the master device is used to compare with each own address of slave devices to access the chosen device. The ADDRESS is set in SFR I2CDAT (DAh)[7:1] in Master Mode. In Slave Mode, ADDRESS is set in I2CADR (DBh)[7:1] and hardware automatically compares whether input corresponds to the ADDRESS the user set or not. If yes, EX7 interrupt is triggered.

R/W determines whether the master device is reading data from slave devices or writing data to them. R/W is set in the last bit of SFR I2CDAT (DAh) in Master Mode and automatically detected by hardware in Slave Mode.

DATA frame is as the data of the protocol and is able to be read from or written into SFR I2CDAT (DAh).

Flag SI of SFR I2CCON (DCh) is set by interrupt EX7 and must be cleared by software.

Table 36. I²C Clock Rate Bit Settings

I2CCON [7]	I2CCON [1:0]		SCL Frequency (f_{SYS} = 30 MHz)	CLK Divided By
cr2	cr1	cr0		
0	0	0	117.18 kHz	256
0	0	1	133.9 kHz	224
0	1	0	156.2 kHz	192
0	1	1	187.5 kHz	160
1	0	0	31.25 kHz	960
1	0	1	250 kHz	120
1	1	0	500 kHz (exceeds high-speed mode 400 kbps)	60
1	1	1	Clock input divided by 8	

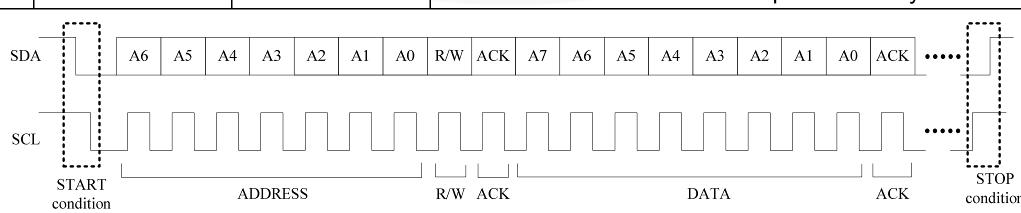

Figure 57. I²C Frame

4.13. MDU (Multiplication-Division Unit)

The MDU is an arithmetical co-processor embedded in the FCM8531 to provide 32-bit division, 16-bit division, 16-bit multiplication, and 32-bit shift and normalization.

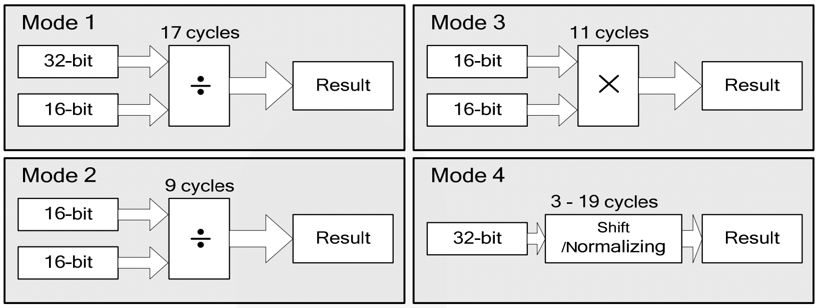

Figure 58. MDU (Multiplication-Division Unit)

Table 37. MDU Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
MD0 (E9h)	Multiplication / Division Register 0								00h
MD1 (EAh)	Multiplication / Division Register 1								00h
MD2 (EBh)	Multiplication / Division Register 2								00h
MD3 (ECh)	Multiplication / Division Register 3								00h
MD4 (EDh)	Multiplication / Division Register 4								00h
MD5 (EEh)	Multiplication / Division Register 5								00h
ARCON (EFh)	MDEF	MDOV	SLR	Shift Count [4:0]					00h

4.13.1 Block Diagram

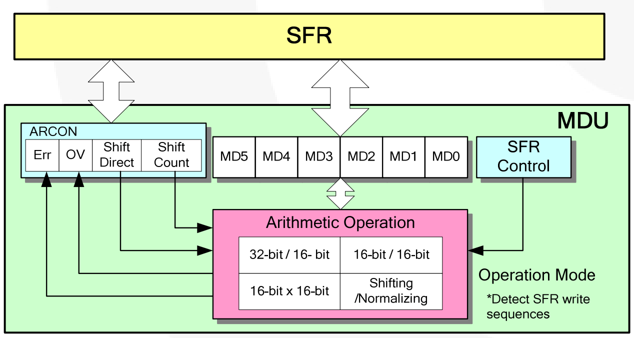

Figure 59. MDU Block Diagram

4.13.2 Description

The MDU provides high-speed arithmetic of division computation (32-bit / 16-bit and 16-bit / 16- bit), multiplication computation (16-bit × 16-bit), shift functionality (32-bit shifting), and normalization functionality (32-bit normalizing). The type of executed arithmetic is determined by the writing sequences of MD0 - MD5 and the executing duration depends on the type of the arithmetic. Please note: calculating result is valid until exceeding executing cycles (*see Figure 58*).

There are three steps to execute a complete computation with the MDU.

Loading

Fill SFR MD0 - MD5 with operands in specific sequences of arithmetic types.

Calculating

Users need to wait for a certain time to execute the calculation, and it depends on the type of the arithmetic.

Reading

While the calculation is completed, the result is stored in MD0 - MD5 and needs to be read in sequence.

Operating instructions of the five computation types are shown below:

32bit/16bit:

(MD3 MD2 MD1 MD0) / (MD5 MD4) = (MD3 MD2 MD1 MD0).(MD5 MD4)

- Loading: Writing order is MD0→MD1→MD2→MD3→MD4→MD5; MD3 - MD0 is the dividend; MD5 - MD4 is the divisor.
- Calculating: Executing time is 17 system clocks.
- Reading: Reading sequence is MD0 → MD1 → MD2 → MD3 → MD4 → MD5; MD3-MD0 is the quotient; MD5 - MD4 is the remainder.

16bit / 16bit:

(MD1 MD0) / (MD5 MD4) = (MD1 MD0).(MD5 MD4)

- Loading: Writing order is MD0 → MD1 → MD4 → MD5; MD1 - MD0 is the dividend; MD5 - MD4 is the divisor.
- Calculating: Executing time is nine system clocks.
- Reading: Reading sequence is MD0 → MD1 → MD4 → MD5; MD1 - MD0 is the quotient; MD5 - MD4 is the remainder.

16bit ×16bit:

(MD5 MD4) × (MD1 MD0) = (MD3 MD2 MD1 MD0)

- Loading: Writing order is MD0 → MD4 → MD1 → MD5; MD5 - MD4 is the multiplicand; MD1 - MD0 are the multipliers.
- Calculating: Executing time is 11 system clocks.
- Reading: Reading sequence is MD0 → MD1 → MD2 → MD3; MD3 - MD0 is the product.

Normalizing:

(MD3 MD2 MD1 MD0) → MD3 MD2 MD1 MD0

- Loading: Writing order is MD0 → MD1 → MD2 → MD3 → ARCON = 00h; SFR ARCON (EFh) should be 00h to enable the normalization function.
- Calculating: Executing time is 4 - 19 system clocks, determined by shift bits *(see Table 38).*
- Reading: Reading sequence is MD0 → MD1 → MD2 → MD3, where MD3 is the highest byte of the result, and MD0 is the lowest.

Shifting:

(MD3 MD2 MD1 MD0) → MD3 MD2 MD1 MD0

- Loading: Writing order is MD0 → MD1 → MD2 → MD3 → ARCON. Left or right shift and the shift count are determined by ARCON (EFh). ARCON (EFh)[5] = 1, shifts to the right; ARCON (EFh)[5] = 0, shifts to the left; ARCON (EFh)[4:0] determines the shift counts.
- Calculating: Executing time is 3 - 18 system clocks, determined by shift bits.
- Reading: Reading sequence is MD0 → MD1 → MD2 → MD3, where MD3 is the highest byte of the result and MD0 is the lowest.

In the normalization and shifting functions, the number of shifting bits determines the necessary executing cycles. The number of shifting bits vs. the required time is shown in Table 38. Figure 60 below is a scheme of the sequence and executing cycles for the five modes in the MDU.

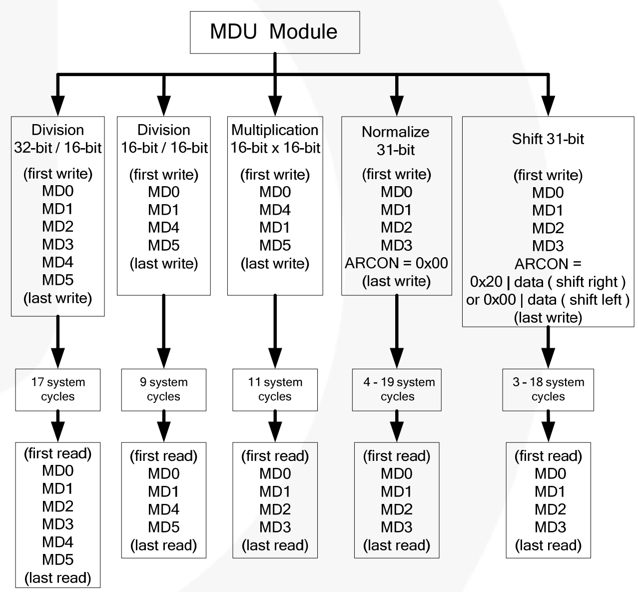

Figure 60. Execution Flow of MDU

Table 38. Executing Cycles

	Number of Shift Bits															
	1, 2	3, 4	5, 6	7, 8	9,10	11, 12	13, 14	15, 16	17, 18	19, 20	21, 22	23, 24	25, 26	27, 28	29, 30	31
Shift (System Cycles)	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Normalize (System Cycles)	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

An error flag or overflow flag of SFR ARCON is set if any MDU fault occurs. *For a detailed description, refer toTable 39.*

Table 39. MDU Fault Flag

ARCON	Condition
Error = 1	write data to MD0 - MD5 and ARCON during computation
	read data from MD0 - MD5 during computation
Overflow = 1	divided by zero
	product is greater than FFFF0000h in multiplication
	input's MSB is 1 in normalizing

SFR ARCON (EFh)[7] is set as an error flag if writing or reading the MDx register before the MDU finishes calculating. The error flag is cleared automatically after reading.

4.14. Watchdog

Watchdog Timer is a 15-bit counter increasing every 384 or 6144 system cycles progressively, which can be used to monitor the system to avoid software or hardware errors.

Table 40. Watchdog Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
IEN0 (A8h)	EA	WDT	ET2	ES0	ET1	EX1	ET0	EX0	00h
IP0 (A9h)	Reserved	WDTS	IP0[5:0]						00h
IEN1 (B8h)	EXEN2	SWDT	Reserved	EX5	EX4	EX3	EX2	EX7	00h
WDTREL (86h)	WDPS	WDTPER							00h
PCON (87h)	SMOD	WDT_TM	ISR_TM	Reserved			STOP	IDLE	08h

4.14.1 Block Diagram

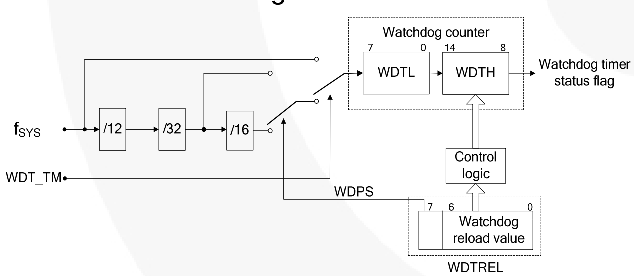

Figure 61. Watchdog Block Diagram

4.14.2 Description

Bit WDT of SFR IEN1 (B8h) is set to activate / refresh the Watchdog Timer. Once WDT is set (the watchdog function enabled), set WDT again to refresh the Watchdog Timer and this bit is cleared by hardware immediately.

Bit WDT_TM of SFR PCON (87h) determines whether the clock feeding to counter is through pre-scale or not, as shown in Figure 61. Please note: if WDT_TM is set, the period of the watchdog is very short and it might cause unexpected problems.

Bit WDPS of SFR WDTREL (86h) sets the pre-scale. If WDPS is set, pre-scale divides the system frequency by 12 $\times$ 32 $\times$ 16 or by 12 $\times$ 32 otherwise.

The Watchdog Timer is a 15-bit counter mapping to WDTL and WDTH registers. Bits WDTPER[6:0] of SFR WDTREL, the reload value, are written to WDTH when the Watchdog Timer is refreshed by WDT.

Watchdog Timer Clock is enabled when bit SWDT of SFR IEN1 is set. The Watchdog Timer should be refreshed periodically or Watchdog resets the MCU when the counter overflows and sets bit WDTS of SFR IP0 (A9h). However, WDTS is not cleared by Watchdog reset and users can check this bit to identify if the system has had an error in the initial of software after reset.

Care should be taken with the sequence of setting WDT and SWDT; WDT should be set before SWDT.

4.15. Mail Box

Table 41. Mail Box Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
IEN2 (9Ah)	Reserved		EX12	EX11	EX10	EX9	EX8	Reserved	00h
IEN0 (A8h)	EA	WDT	ET2	ES0	ET1	EX1	ET0	EX0	00h
IRCON2 (BFh)	N/A			IEX12	IEX11	IEX10	IEX9	IEX8	00h
MTX0 (B0h)	Data Sent to AMC								00h
MTX1 (B1h)	Data Sent to AMC								00h
MTX2 (B2h)	Data Sent to AMC								00h
MTX3 (B3h)	Data Sent to AMC								00h
MRX0 (B4h)	Data Received from AMC								00h
MRX1 (B5h)	Data Received from AMC								00h
MRX2 (B6h)	Data Received from AMC								00h
MRX3 (B7h)	Data Received from AMC								00h

4.15.1 Block Diagram

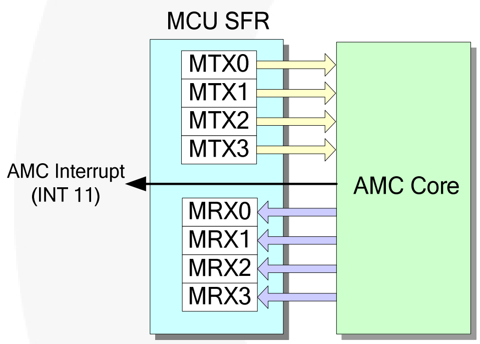

Figure 62. Mail Box Block Diagram

4.15.2 Description

The FCM8531 provides eight registers, MTX0 (B0h) - MTX3 (B3h) and MRX0 (B4h) - MRX3 (B7h) in SFR, for communicating between the MCU and AMC; MTX0 - MTX3 for transmitting data to the AMC; and MRX0 - MRX3 for receiving.

Through the AMC interrupt, the MCU is acknowledged for the data from AMC is available.

4.16. Access MSFR

Table 42. Access MSFR Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
MSFRADR (96h)	MSFR Address (00h - 7Fh)								00h
MSFRDAT (97h)	MSFR Data								00h

4.16.1 Description

MSFR (Motor Special Function Registers) is for accessing special function blocks of motor control, i.e. PWM setting, ADC reading, etc.

To access MSFR, users should fill MSFRADR (96h) with the address first, then write/read the data to/from the MSFRDAT (97h).

5. Analog Input / Output

There are eight channels of 10-bit ADC (Analog-to-Digital Converter) and one 8-bit DAC (Digital-to-Analog Converter) in the FCM8531.

5.1. ADC

The analog signal input pins (IA, IB, IC, VA, VB, VC, ADC0, and ADC3 / AOUT) can be programmed for different purposes, such as current sensing, voltage feedback, speed control, over-temperature protection, or other analog signal inputs (depending on the application). The ADC3 / AOUT pin location can be used as a 0 – 4 V analog output. Output voltage is set via MSFR DACO (47h).

Table 43. ADC Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
ADCCFG (1Fh)	ADC_ST	N/A	DAC_EA	AD_CK	FS_DIV		ADC_TR		00h
IAL (20h)	IA[1:0]		N/A		Reserved	Bias_A0	GIA		0Ch
IAH (21h)	IA[10:2]								00h
IBL (22h)	IB[1:0]		N/A		Reserved	Bias_B0	GIB		0Ch
IBH (23h)	IB[10:2]								00h
ICL (24h)	IC[1:0]		N/A		Reserved	Bias_C0	GIC		0Ch
ICH (25h)	IC[10:2]								00h
VAL (28h)	VA[1:0]		N/A				GVA		00h
VAH (29h)	VA[10:2]								00h
VBL (2Ah)	VB[1:0]		N/A				GVB		00h
VBH (2Bh)	VB[10:2]								00h
VCL (2Ch)	VC[1:0]		N/A				GVC		00h
VCH (2Dh)	VC[10:2]								00h
ADC0L (30h)	ADC0[1:0]		N/A				GADC0		00h
ADC0H (31h)	ADC0[10:2]								00h
ADC3L (36h)	ADC3[1:0]		N/A				GADC3		00h
ADC3H (37h)	ADC3[10:2]								00h

5.1.1 Block Diagram

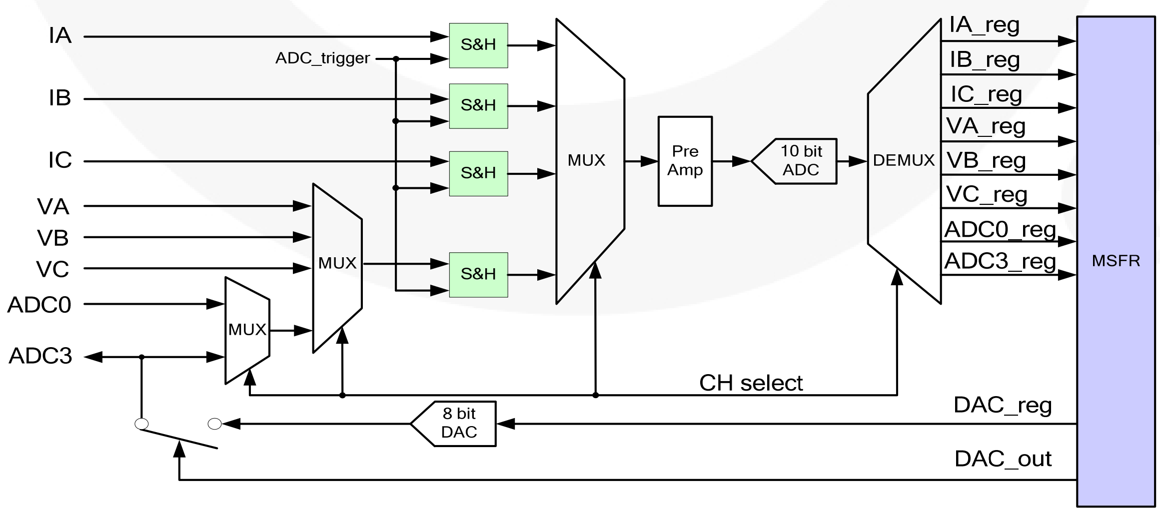

Figure 63. ADC Block Diagram

5.1.2 Description

When ADC trigger signals occur, the sample-and-hold circuits retrieve the voltage to be converted. Then it goes through a pre-amplifier to a 10-bit Analog-to-Digital Converter (ADC). After conversion, it is stored in MSFR and an ADC-Ready interrupt is generated.

ADC Trigger Mode has four sub-modes: SAW Peak, SAW Valley, Timer 0, and Manual Trigger.

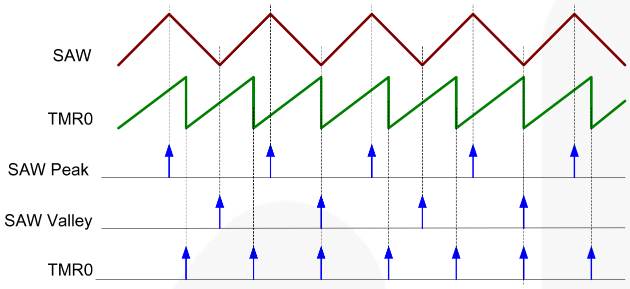

Figure 64. ADC Trigger Mode

SAW Generator must be activated first if SAW Peak or SAW Valley Trigger Mode is selected.

The sampling rate of ADC must be less than 30 kHz, i.e. SAW frequency must be under 30 kHz in SAW Mode with ADCCFG (1Fh)[3:2] = b'00. If SAW frequency is higher than threshold frequency, 30 kHz, a sampling rate divider must be considered. Through setting MSFR ADCCFG [3:2], the sampling rate divider is activated (*see Figure 65*).

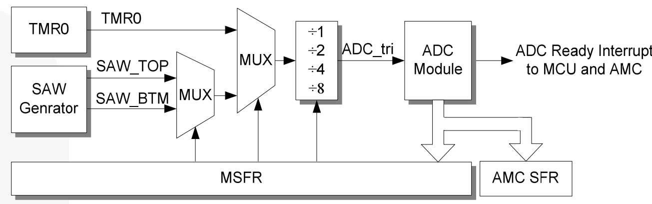

Figure 65. ADC Sample Mode

The internal ADC is divided into three groups according to the speed of the sampling rate: IA, IB, and IC are the highest; VA, VB, and VC are the middle; ADC0 and ADC3 are the lowest. MSFR ADCINX (2Eh)[3:0] indicated the index of the latest updated ADC channel (*see Table 44*).

Table 44. ADC Sampling Rate

Sampling Rate	Channel	Convert Trigger
High Speed	IA, IB, IC	Every 1 ADC Trigger
Mid Speed	VA, VB, VC	Every 4 ADC Triggers
Low Speed	ADC0, ADC3	Every 16 ADC Triggers

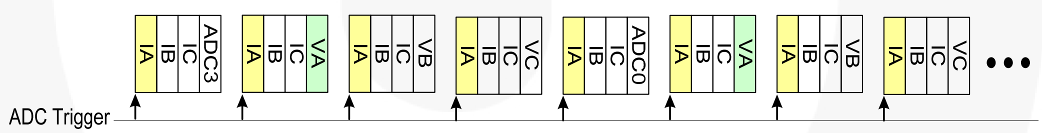

Figure 66. ADC Sampling Sequence

The internal pre-amplifiers are able to amplify ADC input signals by ×1, ×2, and ×4 (*see Figure 67*).

The magnification is set individually in the gain bits of each channel. For example: the gain bits of ADC channel IA are the GIA bits of MSFR IAL (20h)[1:0] *(see Table 43 for other channels).*

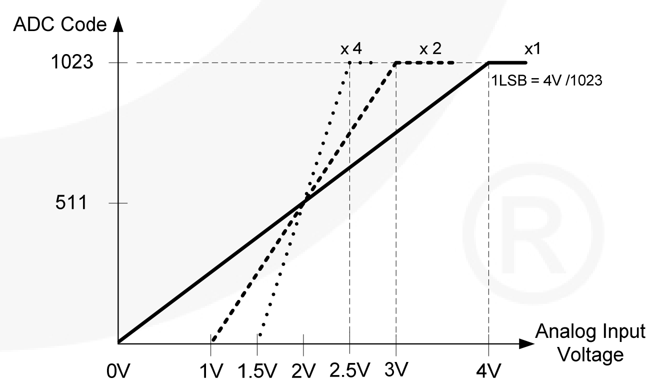

Figure 67. ADC Pre-Amplifier

5.2. DAC

ADC3 / AOUT pin location can be used as 0 – 4 V analog output. The output voltage is set via MSFR DACO (47h).

Table 45. DAC Output Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
ADCCFG (1Fh)	ADC_ST	N/A	DAC_EA	AD_CK	FS_DIV		ADC_TR		00h
DACO (47h)	DACO								00h

5.2.1 Block Diagram

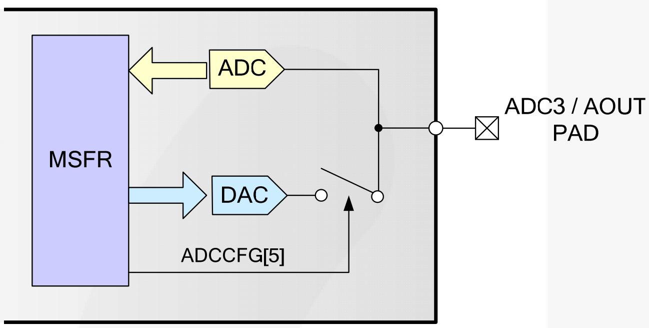

Figure 68. ADC3 / DAC Diagram

5.2.2 Description

Setting bit DAC_EA of MSFR ADCCFG (1Fh) switches the DAC onto pin ADC3 / AOUT *(see Figure 68)*.

Fill an 8-bit value of 00h - FFh into MSFR DACO (47h) to output voltage level of 0 – 4 V *(see Figure 69)*.

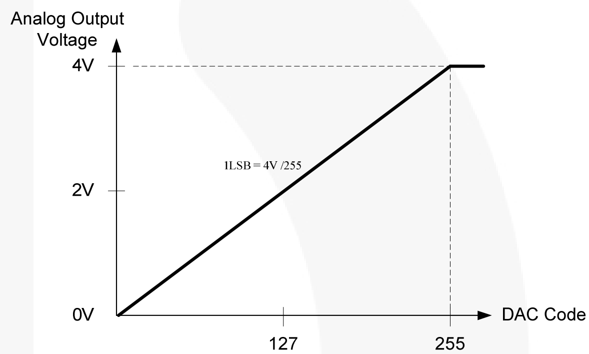

Figure 69. Filled Code vs. DAC Output

6. Protection

6.1. Fault Function

A fault protection occurs when any one of following conditions occur: the detection of Hall Slow, Hall Error, and any SHORT circuit on the IA, IB or IC pin.

Once a short circuit occurs (any input voltage of current-sense pins is higher than the SHORT voltage), PWM is immediately turned off until the next cycle (cycle-by-cycle) and an interrupt EX8 is generated. With this interrupt, appropriate action can be taken to protect systems by software.

When a Hall signal error occurs, PWM is turned off automatically until the error status is all clear.

Table 46. Fault and Protection

Type	Condition	Action
Hall Slow	Hall Period Overflow	Fault Interrupt
SHORT A	IA > I_{SHORT}	Fault Interrupt
SHORT B	IB > I_{SHORT}	Fault Interrupt
SHORT C	IC > I_{SHORT}	Fault Interrupt
Hall Error	Hall Sensor = 111 or 000	Fault Interrupt (PWM Off)
OC High	IA / IB / IC > I_{OCH}	PWM Cycle by Cycle Off
OC LOW	IA / IB / IC < I_{OCL}	PWM Cycle by Cycle Off

Table 47. Protection Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
HALINT (1Bh)	N/A				HTMR_OUT		HALL_INT		00h
MSTAT (3Fh)	VDD_TEST	H_SLOW	SHORT_A	SHORT_B	SHORT_C	H_ERR	S_ACT	DIR	00h
SHORT (46h)	SHORT								FFh
IEN2 (9Ah)	Reserved		EX12	EX11	EX10	EX9	EX8	Reserved	00h
IEN0 (A8h)	EA	WDT	ET2	ES0	ET1	EX1	ET0	EX0	00h
IRCON2 (BFh)	Reserved			IEX12	IEX11	IEX10	IEX9	IEX8	00h

6.1.1 Block Diagram

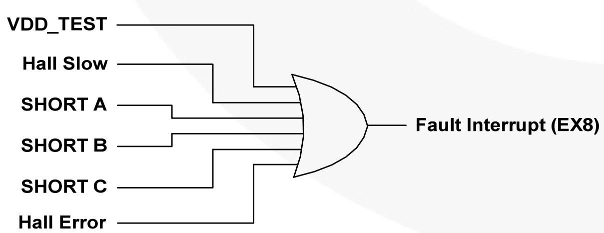

Figure 70. Fault Protection

6.1.2 Description

Three conditions: Hall Slow, SHORT, and Hall Error; normally trigger a fault interrupt of EX8 by hardware in the FCM8531 and the fault information is stored in MSFR MSTAT (3Fh) to identify the fault cause.

Note: interrupt EX8 must be turned on for fault detection.

The conditions are described below:

VDD_TEST
For internal testing only. Please ignore when detected.

Hall Slow
The Hall Slow is the circumstance when the Hall signal status does not change within a specific setting time and this causes an overflow in the counter of the Hall period.

Hall Slow functionality is activated by HTMR_OUT of MSFR HALINT (1Bh). The setting of HTMR_OUT is described below:

HTMR_OUT = b'00: Functionality Disable

HTMR_OUT = b'01: Interrupt EX8 if Hall Counter [17] = 1

HTMR_OUT = b'10: Interrupt EX8 if Hall Counter [18] = 1

HTMR_OUT = b'11: Interrupt EX8 if Hall Counter [19] = 1

Please see PLL section for reference.

SHORT

The protection mechanism is started if the phase current (IA, IB, IC) of the motor surges up to the OCH protection level. The hardware promptly detects and stops the PWM immediately within each cycle. Exceeding the short level set at MSFR SHORT (46h) triggers a fault interrupt. With this interrupt, appropriate actions can be taken to protect systems by software (shown in Figure 71).

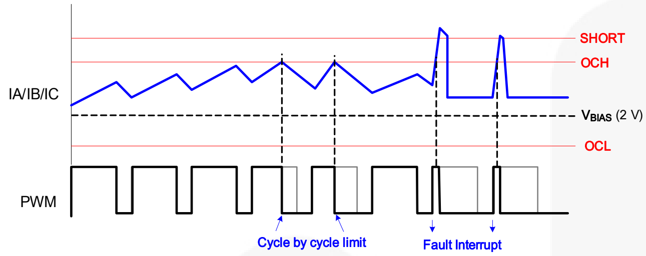

Figure 71. Current Protection

Hall Error

Hall signal status of 111 or 000 is treated as abnormal input and indicates there could be a hardware issue. The error generates a Hall signal error interrupt and turns off the PWM output. However, output is automatically resumed once the error status disengaged.

6.2. Current Protection

The FCM8531 has three types of current protection mechanisms. The protection level is set at the MSFR OCH (44h), OCL (45h), and SHORT (46h). These setting voltages are compared with the voltages on the current feedback input pins (IA, IB, IC). When voltage is over OCH or under OCL, the PWM is immediately turned off and turned on in next cycle start if the situation is disengaged (cycle-by-cycle). If the voltage exceeds the SHORT level, a fault interrupt is triggered (*see Figure 71 and Figure 72*).

Table 48. Current-Sensing Registers

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
OCCNTL (26h)	OC_DEB		OCCH_EA	OCBH_EA	OCAH_EA	OCCL_EA	OCBL_EA	OCAL_EA	00h
OCSTA (27h)	N/A		OCCH	OCBH	OCAH	OCCL	OCBL	OCAL	00h
OCH (44h)	OCH								FFh
OCL (45h)	OCL								10h
SHORT (46h)	SHORT								FFh

6.2.1 Block Diagram

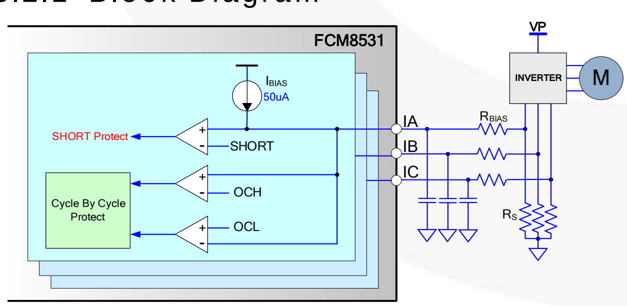

Figure 72. Current Feedback

6.2.2 Description

The current-sensing pin provides current feedback and over-current protection for a motor system. Each current-sensing pin (IA, IB, and IC) has an output of 50 µA of bias current. The recommended setting for the bias voltage is 2.0 V (R_{BIAS} = 40 kΩ).

$$V_{BIAS} = I_{BIAS} \times R_{BIAS} \quad (7)$$

The levels for positive and negative over-current protection and short-circuit detection are set at MSFR OCH (44h), MSFR OCL (45h), and MSFR SHORT (46h). The level range is 0 – 4 V.

When voltage of a current-sensing pin is over OCH or under OCL, the PWM is immediately turned off and turned on in next cycle start if the situation is disengaged (cycle-by-cycle).

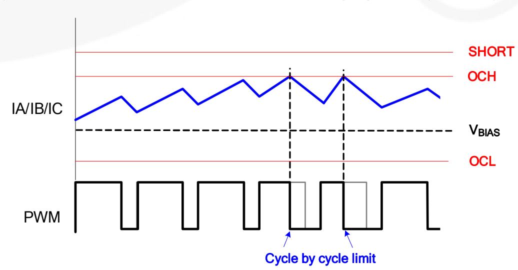

Figure 73. Over-Current Protection

Each protection mechanism is listed in Table 49.

Over-current protection raises a corresponding flag that can be read at MSFR OCSTA (27h) and is automatically cleared after read.

Set OC_DEB of MSFR OCCNTL (26h) to select the debounce time (600 – 1800 ns).

Table 49. Over-Current Protection

	Square-Wave	Sine-Wave	EN/DIS	Flag
OCAH	Cycle by Cycle PWM Duty Limit (High Gate Off)	Cycle by Cycle Free (All Gate Off)	Yes	Yes
OCAL	Cycle by Cycle Free (All Gate Off)	Cycle by Cycle Free (All Gate Off)	Yes	Yes
OCBH	Cycle by Cycle PWM Duty Limit (High Gate Off)	Cycle by Cycle Free (All Gate Off)	Yes	Yes
OCBL	Cycle by Cycle Free (All Gate Off)	Cycle by Cycle Free (All Gate Off)	Yes	Yes
OCCH	Cycle by Cycle PWM Duty Limit (High Gate Off)	Cycle by Cycle Free (All Gate Off)	Yes	Yes
OCCL	Cycle by Cycle Free (All Gate Off)	Cycle by Cycle Free (All Gate Off)	Yes	Yes

7. Power Management

7.1. Power On and Power Off

Power On

When V_{DD} exceeds VDD_{ON}, the voltage generator module begins operating and provides the required power to the internal circuitry of the FCM8531. Then the Power-On Reset (POR) is set and the clock generator begins. After about 2 ms, the reset status is removed and the MCU's program begins executing.

Power Off

When V_{DD} is under VDD_{OFF}, the FCM8531 is completely shut down.

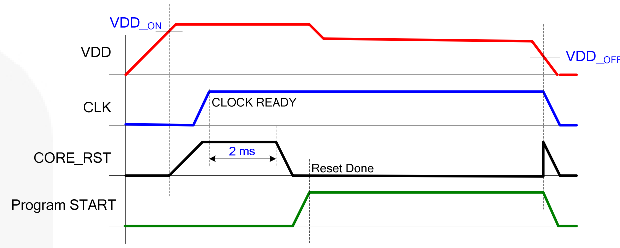

Figure 74. Power On and Off Sequence

7.2. Power Saving

The FCM8531 has three power-saving modes: IDLE Mode, STOP Mode, and SLEEP Mode. The IDLE and STOP modes are set at SFR PCON (87h). SLEEP Mode is set at MSFR SLEEP (43h).

IDLE Mode

Execution of MCU programs pauses, but the peripheral I/O circuits; such as PWM, external interrupt, timing, and serial output: continue to work until there is an external interrupt (EX0/EX1) or a system reset.

STOP Mode

Execution of programs, digital I/O interfaces, and all digital circuits pause. This mode continues until the occurrence of an EX0/EX1 external interrupt or a system reset.

Note: the external interrupt level must be set to LOW to have an interrupt.

SLEEP Mode

To enter SLEEP Mode, MSFR SLEEP (43h)[0] must be set. Figure 75 illustrates Sleep Mode operation. In SLEEP Mode, the MCU and AMC are both turned off. At that moment, the alarm timer begins to count. After a timeout (T_ALM), the MCU and AMC are turned on again.

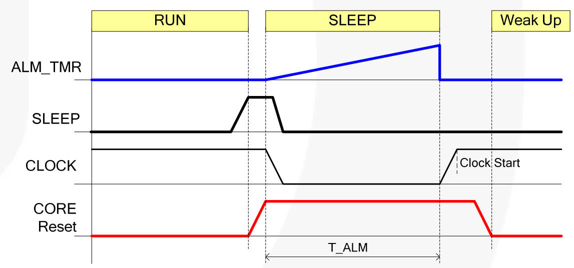

Figure 75. SLEEP Mode

8. Development Supports

8.1. MCDS (Motor Control Development System)

Fairchild provides the Motor Control Development System (MCDS) Integrated Development Environments (IDE) for the FCM8531. On Microsoft® Windows platforms, functions such as project building, program code generation, compilation, In System Programming (ISP), and On-Chip Debug Support (OCDS) are supported. This facilitates software development and debugging.

For detailed information about MCDS, please see: *AN-8207— User Guide for MCDS IDE of FCM8531*.

8.2. AMC Library

Advanced Motor Control (AMC) is used for motor driving. Depending on applications, the configurable processing core can be configured with a suitable AMC library to perform different motor control algorithms, such as Field-Oriented Control (FOC) or Sensorless.

For more information about AMC Library, please see:

AN-8204 — AMC Library User Guide - Speed Integral for FCM8531

AN-8206 — AMC Library User Guide - Sliding Mode for FCM8531

AN-8205 — AMC Library User Guide - Hall Interface for FCM8531

8.3. On-Chip Debug Support (OCDS)

OCDS is for software program debugging and must be executed with the Keil µVision® software environment. It can overwrite and monitor the memory and registers of the FCM8531. It has functions such as start, stop, step execution, break point, etc.

8.3.1 Description

OCDS operates through the JTAG interface (IEEE 1149.1 port). It is enabled by the last byte of program memory. When it is set to 0, the OCDS is disabled *(see Table 50)*. When OCDS is enabled, pins P14, P15, P16, and P17 are configured to JTAG function pins *(see Table 51)*.

Note: DO NOT set these pins as direct driver when OCDS is enabled.

Table 50. Program Memory Last Byte

Byte Name (Address)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Erase
OCDS (2FFFh)	OCDS_EN	Lock Address							FFh

Table 51. JTAG Interface Configuration

JTAG	Pin	Description
TCK	P17	Test clock input
TMS	P16	Test mode select input
TDI	P15	Test data input
TDO	P14	Test data output

Related Datasheets

FCM8531 — MCU Embedded and Configurable 3-Phase PMSM / BLDC Motor Controller

AN-8203 — FCM8531 User Manual Instruction Set

AN-8204 — FCM8531 AMC Library_Speed Integral

AN-8205 — FCM8531 AMC Library: Hall-Interface

AN-8206 — FCM8531 AMC Library: Sliding Mode

AN-8207 — FCM8531 User Guide for MCDS IDE