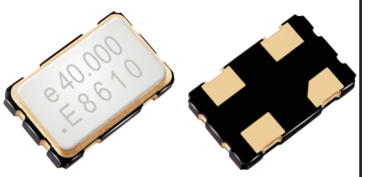
saRonix-eCera™

1.8~3.3V CMOS Low Jitter
FD Series Seam Sealed Crystal Clock Oscillator



Product Description

The FD Series could working with 1.8~3.3V that achieves superb jitter and stability over a broad range of operating conditions and frequencies. The output clock signal, generated internally with a non-PLL oscillator design, is compatible with LVCMOS/LVTTL logic levels. The device, available on tape and reel, is contained in a 5.0x3.2mm surface-mount ceramic package.

Product Features

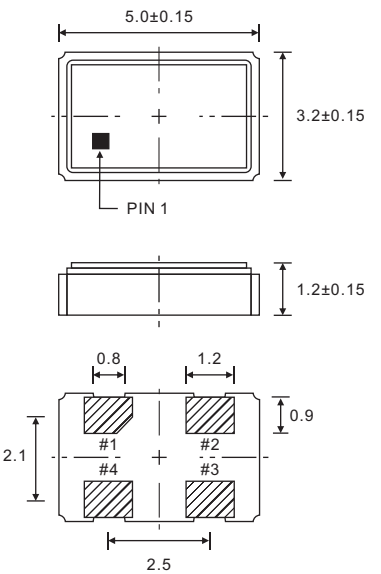
- Less than 1.5ps RMS jitter with fundamental or overtone design
- 1.8~3.3V CMOS compatible logic levels
- Pin-compatible with standard 5.0x3.2mm packages
- Designed for standard reflow and washing techniques
- Low power standby mode
- Available on tape & reel; 1000pcs/reel
- Pb-free and RoHS/Green compliant

Applications

The FD Series is an ideal reference clock for compact, high-density applications requiring low jitter or tight stability, including:

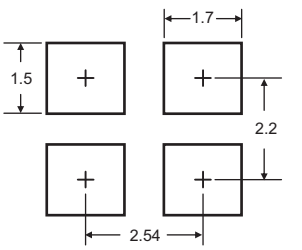
- Ethernet
- Fiber Channel
- Serial Attached SCSI (SAS)
- Server & Storage platforms
- SONET/SDH line cards
- T1/E1, T3/E3 line cards
- DSLAM
- 802.11a/b/g WiFi

Dimensions (UNIT: mm)



(Bottom View)

Footprint (UNIT: mm)



External high-frequency power decoupling is recommended. (See test circuit for minimum recommendation). To ensure optimal performance, do not route traces beneath the package.

Scale: None. Dimensions ar in mm

Pin Functions

Pin	Function
#1	OE Function
#2	Ground
#3	Clock Output
#4	V_{CC}

Part Number Example

F D 2 5 0 0 0 0 1

A B C

A: Product series
B: Digit of frequency
C: Internal specification

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Electrical Performance

Parameter		Min.	Typ.	Max.	Units	Notes
Output frequency		1		125	MHz	As specified
Supply voltage		1.8		3.3	V	
Supply current, output enabled				10	mA	1 to <40 MHz
				20		40 to 75 MHz
				30		>75 to <125 MHz
Supply current, standby mode				10	µA	Output Hi-Z
Frequency stability		±20		±50	ppm	See Note 1 below
Operating temperature		-40		+85	°C	As specified
Output logic 0, V_{OL}				10% V_{DD}	V	
Output logic 1, V_{OH}		90% V_{DD}			V	
Output load			15	30	pF	
Duty cycle		45		55	%	
Rise and fall time	1 to 40 MHz			5	ns	0.1V_{DD} to 0.9V_{DD} or 0.9V_{DD} to 0.1V_{DD}
	40 to <80 MHz			3		
	80 to 125 MHz			2		
Jitter, Phase	up to <80 MHz			1.5	ps RMS (1-σ)	10 kHz to 20 MHz frequency band
	80 to 125 MHz			1		
Jitter, Accumulated	up to <80 MHz			5	ps RMS (1-σ)	20.000 adjacent periods
	80 to 125 MHz			3		
Jitter, Total	up to <80 MHz			50	ps pk-pk	100.000 random periods
	80 to 125 MHz			30		

Notes:
1. As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (1 year at 25°C average effective ambient temperature), shock and vibration.

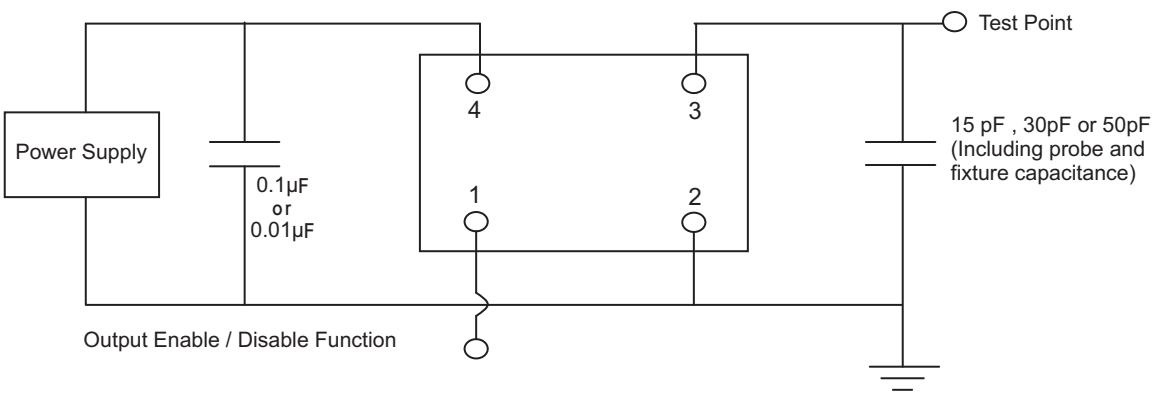
Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (pin 1), Output Enable	0.7V_{DD}			V	or open
Input voltage (pin 1), Output Disable (low power standby)			0.3V_{DD}	V	Output is Hi-Z
Internal pullup resistance	50			k ohm	
Output disable delay			100	ns	
Output enable delay			10	ms	

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage temperature	-55		+125	°C	

Test Circuit

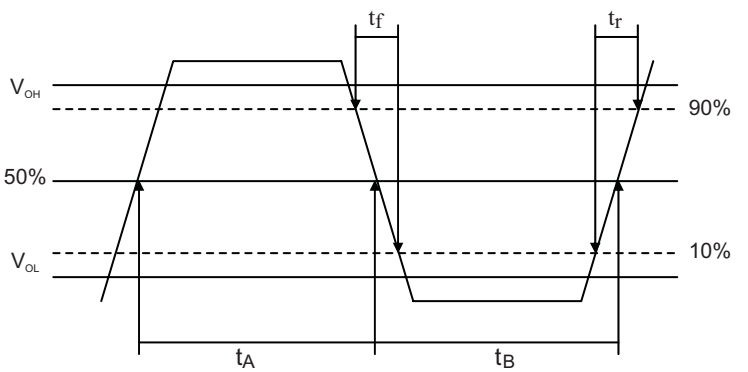


Reliability Test Ratings

This product is rated to meet the following test conditions:

Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 (R_1= $2x10^{-8}$atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

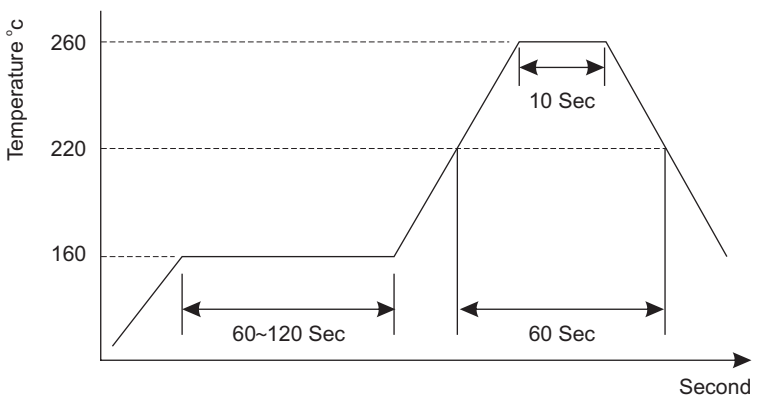
Output Waveform



Duty cycle=100% x (t_A) / (t_A+t_B)

Refow Soldering Profle

As per IPC/JEDEC J-STD-020C



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