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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

April 2015

FDC5614P

## 60V P-Channel Logic Level PowerTrench® MOSFET

General Description

This 60V P-Channel MOSFET uses Fairchild's high voltage PowerTrench process. It has been optimized for power management applications.

Applications

- DC-DC converters
- Load switch
- Power management

Features

- −3 A, −60 V. $R_{DS(ON)} = 0.105\ \Omega$ @ $V_{GS} = -10$ V
  $R_{DS(ON)} = 0.135\ \Omega$ @ $V_{GS} = -4.5$ V

- Fast switching speed

- High performance trench technology for extremely low $R_{DS(ON)}$

SuperSOT ™-6
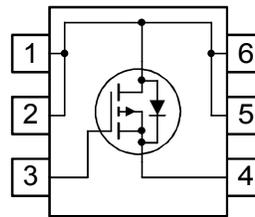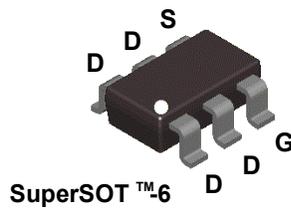
Absolute Maximum Ratings

$T_A = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		−60	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1a)	−3	A
	– Pulsed		−20	
P_D	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.564	FDC5614P	7''	8mm	3000 units

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C		–49		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –48 V, V_{GS} = 0 V			–1	μA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 20V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –20 V V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–1	–1.6	–3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 μA,Referenced to 25°C		4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –10 V, I_D = –3 A V_{GS} = –4.5 V, I_D = –2.7 A V_{GS} = –10 V, I_D = –3 A T_J=125°C		82 105 130	105 135 190	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = –10 V, V_{DS} = –5 V	–20			A
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –3 A		8		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –30 V, V_{GS} = 0 V,		759		pF
C_{oss}	Output Capacitance	f = 1.0 MHz		90		pF
C_{rss}	Reverse Transfer Capacitance			39		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –30 V, I_D = –1 A,		7	14	ns
t_r	Turn–On Rise Time	V_{GS} = –10 V, R_{GEN} = 6 Ω		10	20	ns
$t_{d(off)}$	Turn–Off Delay Time			19	34	ns
t_f	Turn–Off Fall Time			12	22	ns
Q_g	Total Gate Charge	V_{DS} = –30V, I_D = –3.0 A,		15	24	nC
Q_{gs}	Gate–Source Charge	V_{GS} = –10 V		2.5		nC
Q_{gd}	Gate–Drain Charge			3.0		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–1.3	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –1.3 A (Note 2)		–0.8	–1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

   a.   78°C/W when mounted on a 1in^2 pad of 2oz copper on FR-4 board.

   b.   156°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
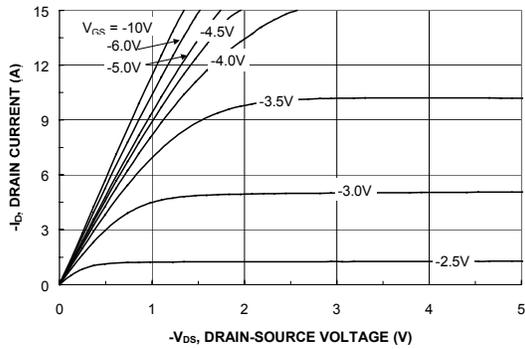
Typical Characteristics

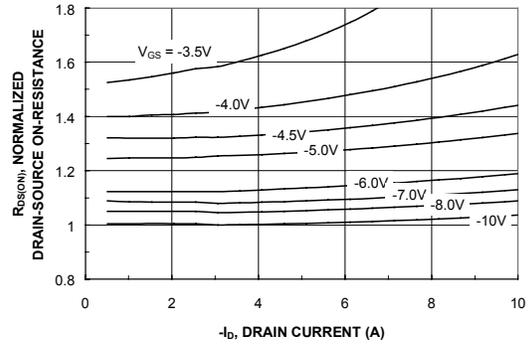Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with
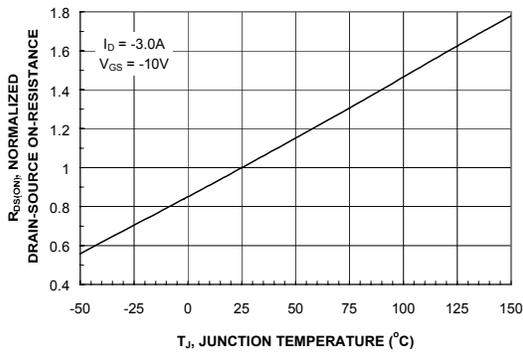Drain Current and Gate Voltage.

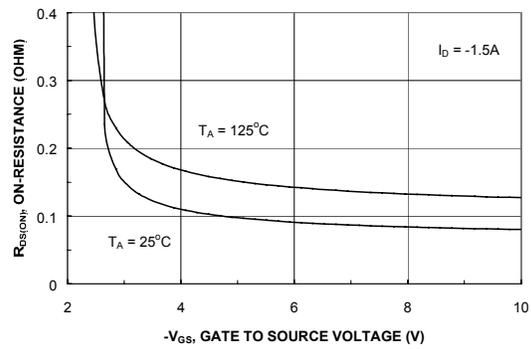Figure 3. On-Resistance Variation with
Temperature.

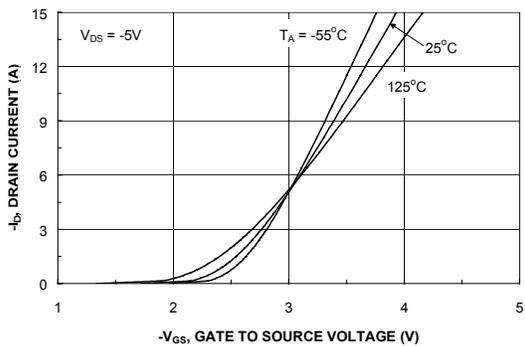Figure 4. On-Resistance Variation with
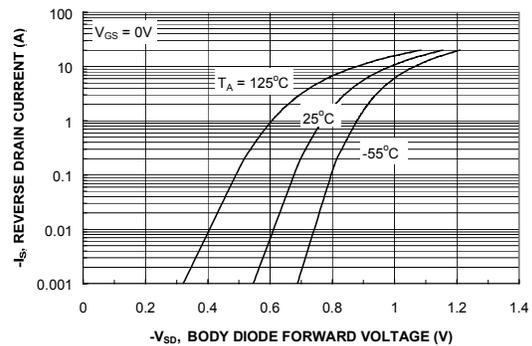Gate-to-Source Voltage.

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation
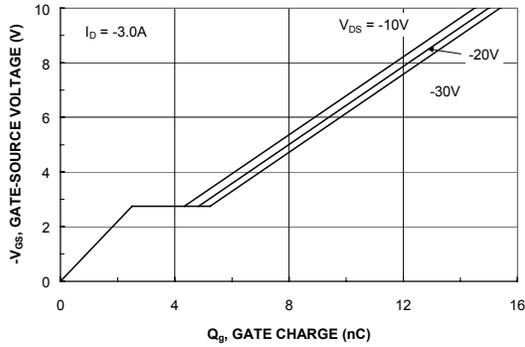with Source Current and Temperature.

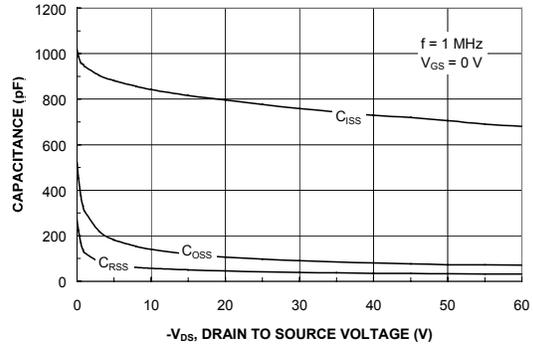## Typical Characteristics

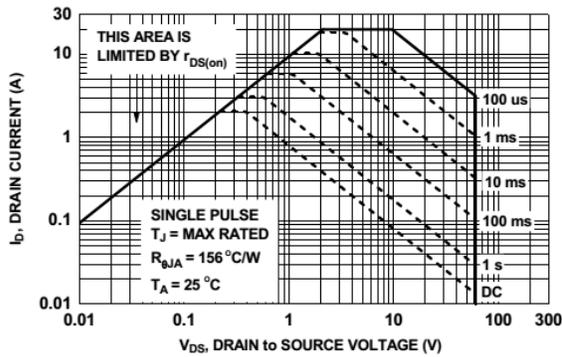Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.

Figure 9. Maximum Safe Operating Area.
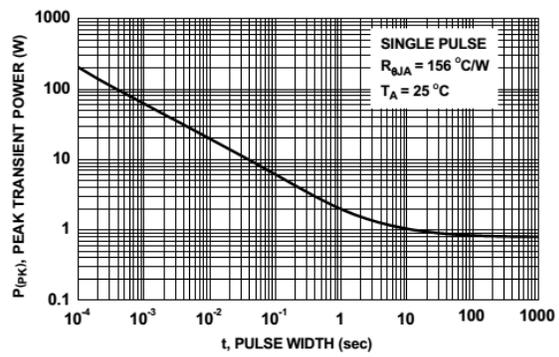
Figure 10. Single Pulse Maximum
Power Dissipation.

NOTES:
$Z_{\theta JA}(t) = r(t) \times R_{\theta JA}$
$R_{\theta JA} = 156°C/W$
Peak $T_J = P_{DM} \times Z_{\theta JA}(t) + T_A$
Duty Cycle, $D = t_1 / t_2$
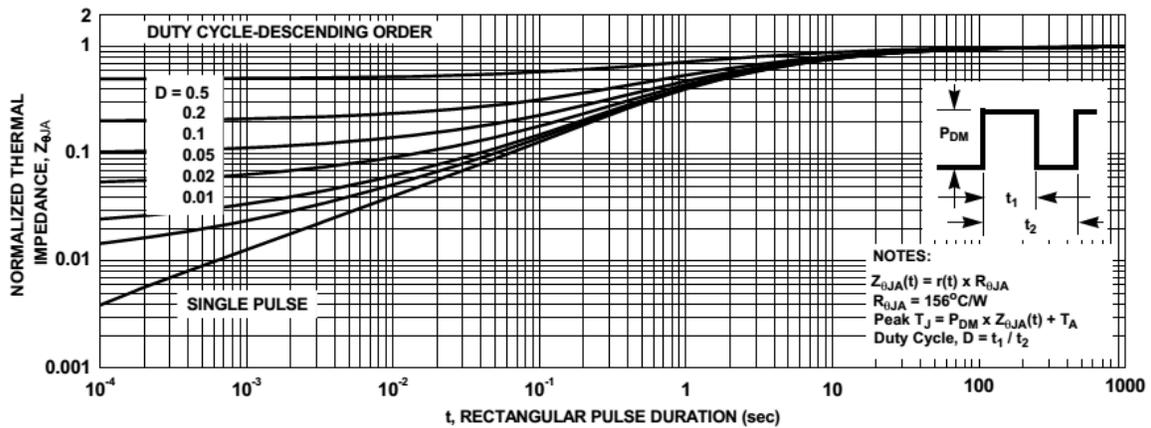
Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

C
3.00
2.80
A

6   4

B

3.00
2.60

1.70
1.50 C

1

3

0.95

0.50
0.30

1.90

⊕ 0.20 Ⓜ A B

(0.30)

SYMM
CL

0.95   0.95

1.00 MIN

2.60

0.70 MIN
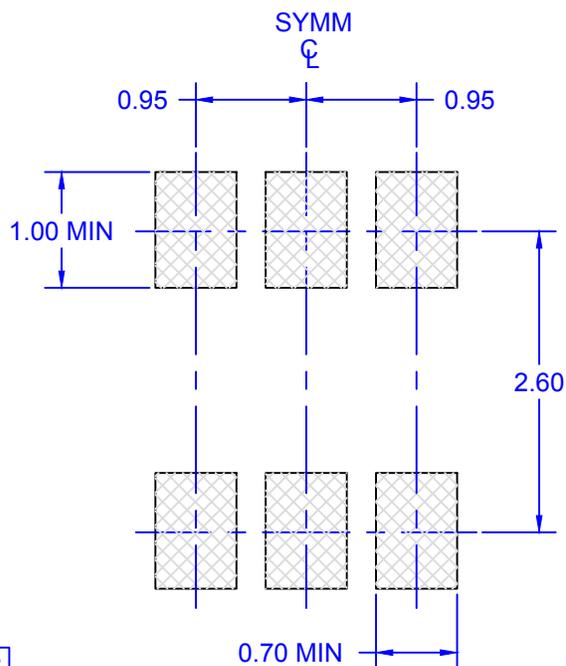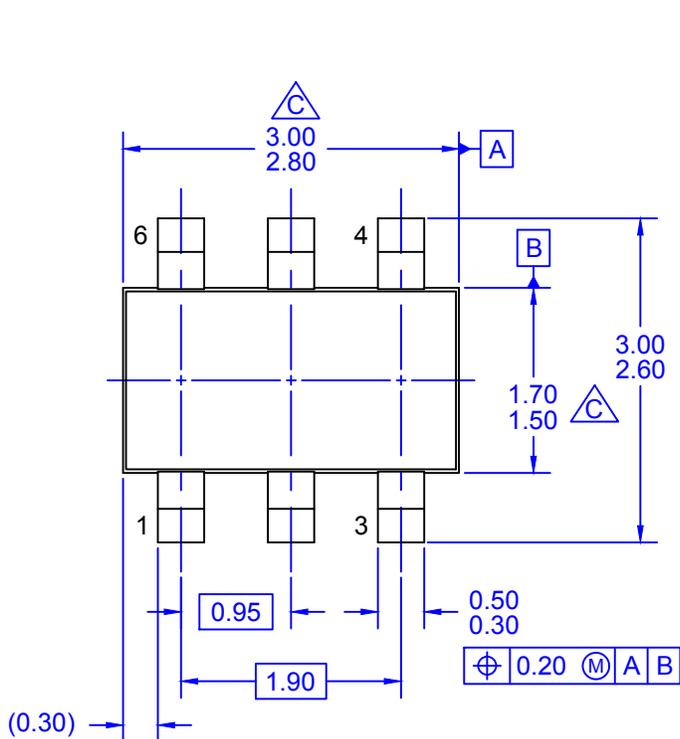
LAND PATTERN RECOMMENDATION

1.10 MAX

1.00
0.70

0.10
0.00

C

⌒ 0.10 C

SEE DETAIL A

H

0.20
0.08
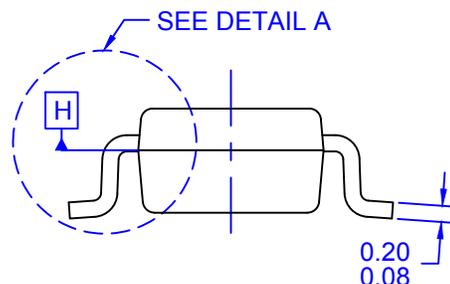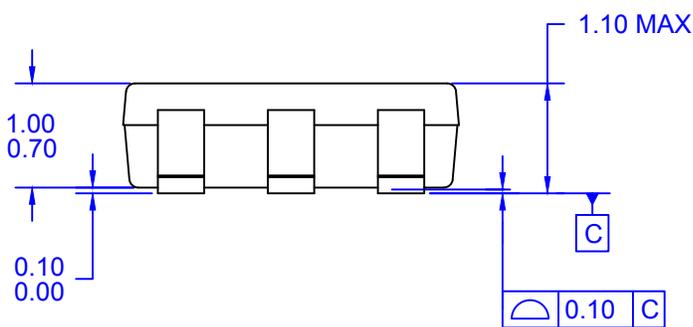
NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC MO-193.
VAR. AA, ISSUE E.
B) ALL DIMENSIONS ARE IN MILLIMETERS.

C PACKAGE LENGTH DOES NOT INCLUDE MOLD
FLASH, PROTRUSIONS OR GATE BURRS. MOLD
FLASH, PROTRUSIONS OR GATE BURRS SHALL
NOT EXCEED 0.25mm PER END. PACKAGE WIDTH
DOES NOT INCLUDE INTERLEAD FLASH OR
PROTRUSION. INTERLEAD FLASH OR
PROTRUSION SHALL NOT EXCEED 0.25mm PER
SIDE. PACKAGE LENGTH AND WIDTH DIMENSIONS
ARE DETERMINED AT DATUM H.
D) DRAWING FILE NAME: MKT-MA06AREVF

GAGE PLANE

0.25

8°
0°

0.55
0.35

SEATING PLANE

0.60 REF
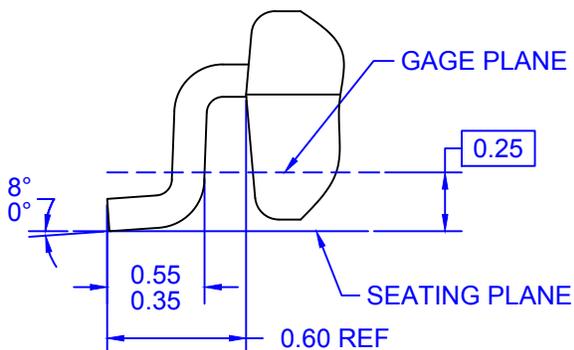
DETAIL A
SCALE: 50X

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