

FDD18N20LZ

N-Channel UniFET™ MOSFET

200 V, 16 A, 125 mΩ

Features

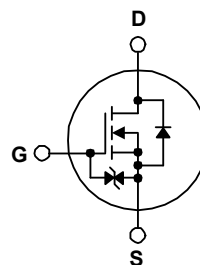
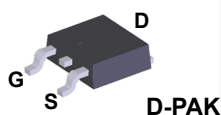
- $R_{DS(on)} = 125 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 8 \text{ A}$
- Low Gate Charge (Typ. 30 nC)
- Low C_{RSS} (Typ. 25 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Applications

- LED TV
- Consumer Appliances
- Uninterruptible Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDD18N20LZ	Unit
V_{DSS}	Drain to Source Voltage	200	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	A
		- Continuous ($T_C = 100^\circ\text{C}$)	
I_{DM}	Drain Current	- Pulsed (Note 1)	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	mJ
I_{AR}	Avalanche Current	(Note 1)	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	W
		- Derate above 25°C	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.	300	°C

Thermal Characteristics

Symbol	Parameter	FDD18N20LZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	83	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD18N20LZ	FDD18N20LZ	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$, $T_J = 25^\circ\text{C}$	200	-	-	V
$\Delta BV_{DSS} / \Delta$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	0.2	-	$\text{V}/^\circ\text{C}$
T_J I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200\ \text{V}$, $V_{GS} = 0\ \text{V}$	-	-	1	μA
		$V_{DS} = 160\ \text{V}$, $T_C = 125^\circ\text{C}$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 16\ \text{V}$, $V_{DS} = 0\ \text{V}$	-	-	± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	1.0	-	2.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 8\ \text{A}$	-	0.10	0.125	Ω
		$V_{GS} = 5\ \text{V}$, $I_D = 8\ \text{A}$	-	0.11	0.13	
g_{FS}	Forward Transconductance	$V_{DS} = 20\ \text{V}$, $I_D = 2\ \text{A}$	-	11	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}$, $V_{GS} = 0\ \text{V}$ $f = 1\ \text{MHz}$	-	1185	1575	pF
C_{oss}	Output Capacitance		-	190	255	pF
C_{rss}	Reverse Transfer Capacitance		-	25	40	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 200\ \text{V}$, $I_D = 16\ \text{A}$ $V_{GS} = 10\ \text{V}$ (Note 4)	-	30	40	nC
Q_{gs}	Gate to Source Gate Charge		-	3.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	8.5	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\ \text{V}$, $I_D = 16\ \text{A}$ $V_{GS} = 10\ \text{V}$, $R_G = 25\ \Omega$ (Note 4)	-	15	40	ns
t_r	Turn-On Rise Time		-	20	50	ns
$t_{d(off)}$	Turn-Off Delay Time		-	135	280	ns
t_f	Turn-Off Fall Time		-	50	110	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	16	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	64	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 4 A	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 4 A	-	105	-	ns
Q _{rr}	Reverse Recovery Charge	di _F /dt = 100 A/μs	-	0.4	-	μC

Notes:

- 1: Repetitive rating; pulse-width limited by maximum junction temperature.
- 2: $L = 2.5\ \text{mH}$, $I_{AS} = 16\ \text{A}$, $V_{DD} = 50\ \text{V}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
- 3: $I_{SD} \leq 16\ \text{A}$, $di/dt \leq 200\ \text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
- 4: Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

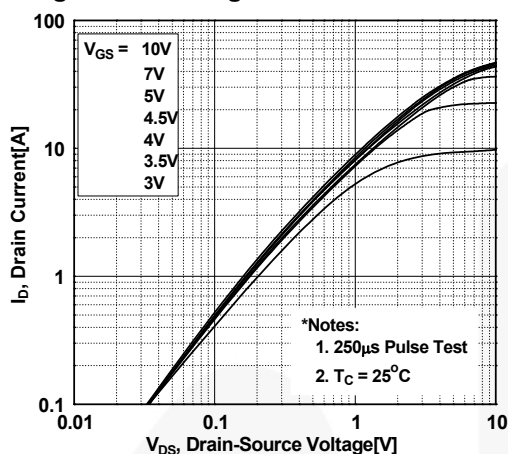


Figure 2. Transfer Characteristics

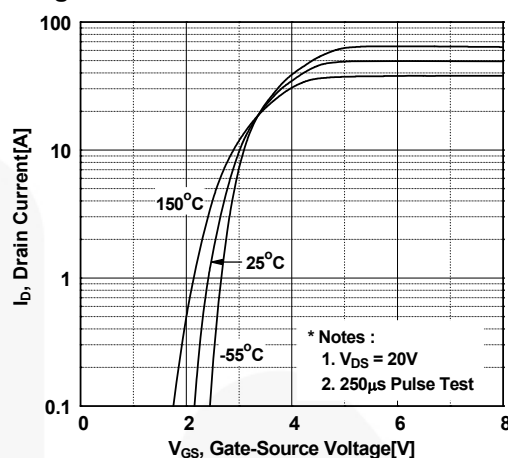


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

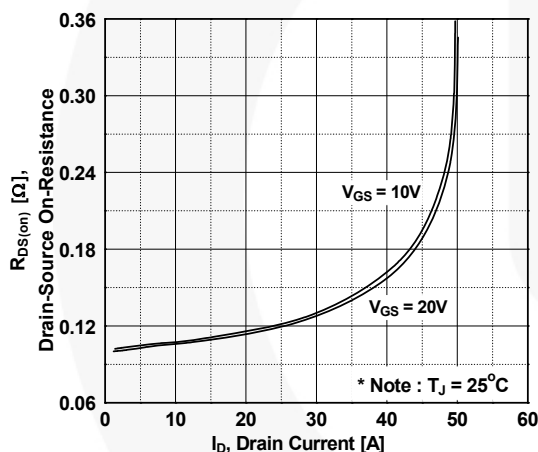


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

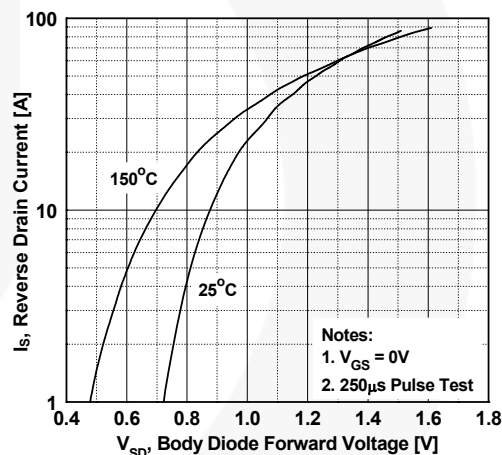


Figure 5. Capacitance Characteristics

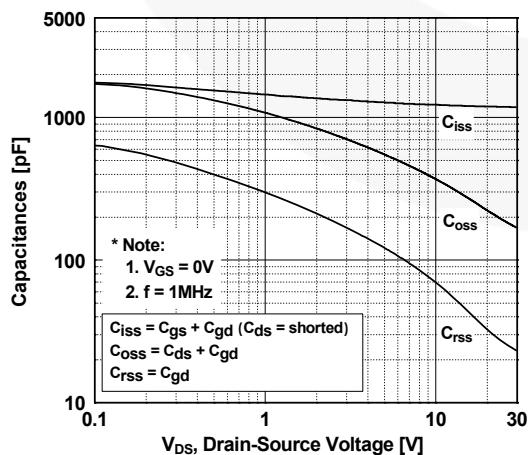
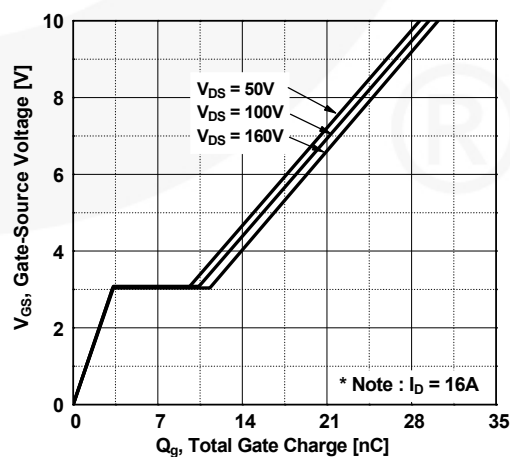


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

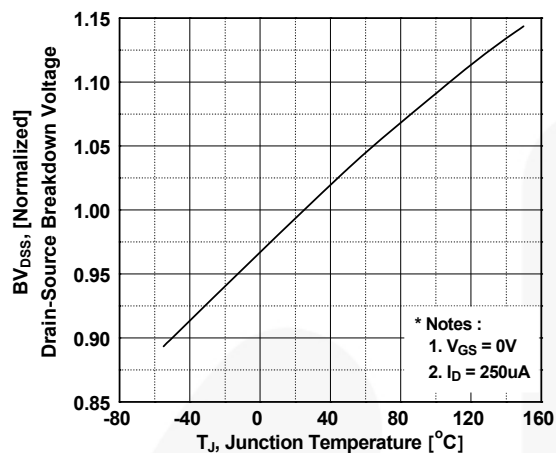


Figure 8. On-Resistance Variation vs. Temperature

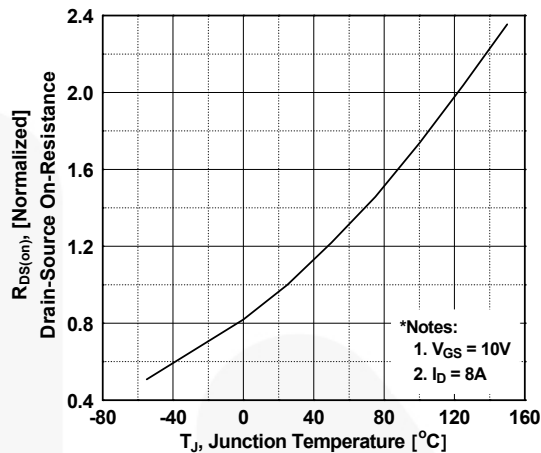


Figure 9. Maximum Safe Operating Area

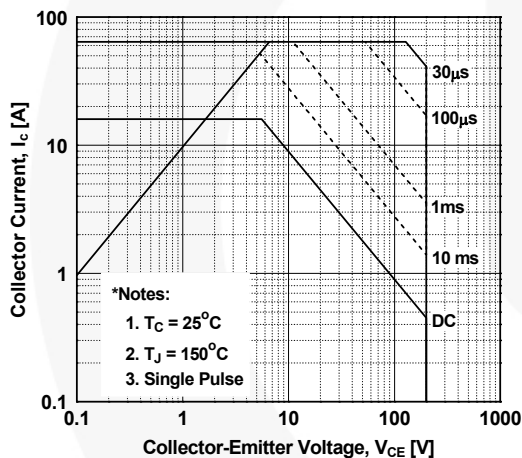


Figure 10. Maximum Drain Current vs. Case Temperature

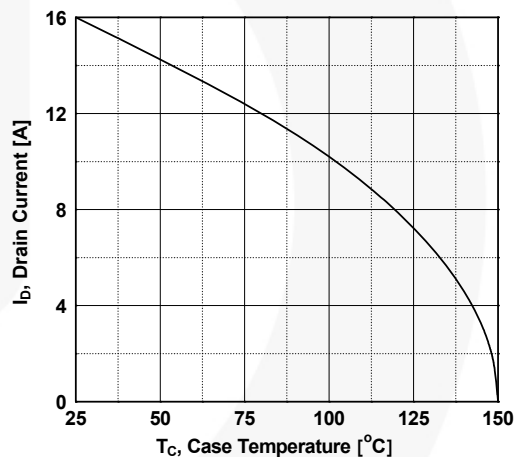
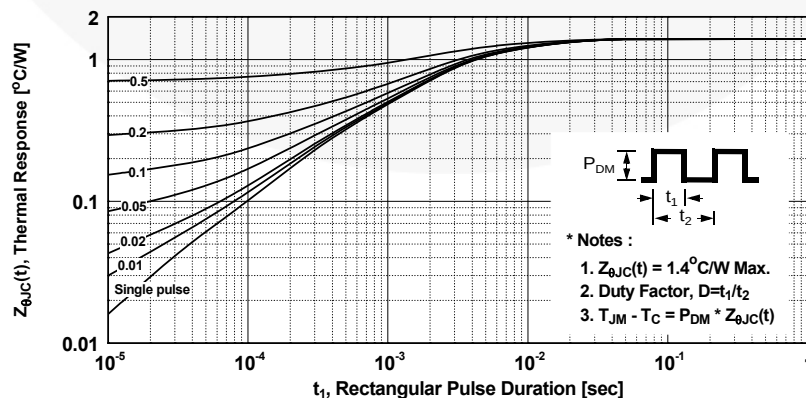


Figure 11. Transient Thermal Response Curve



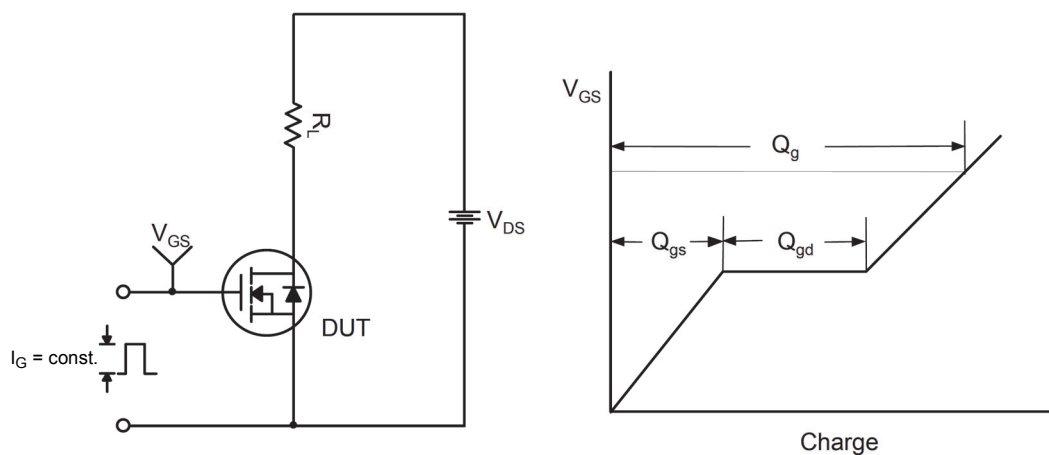


Figure 12. Gate Charge Test Circuit & Waveform

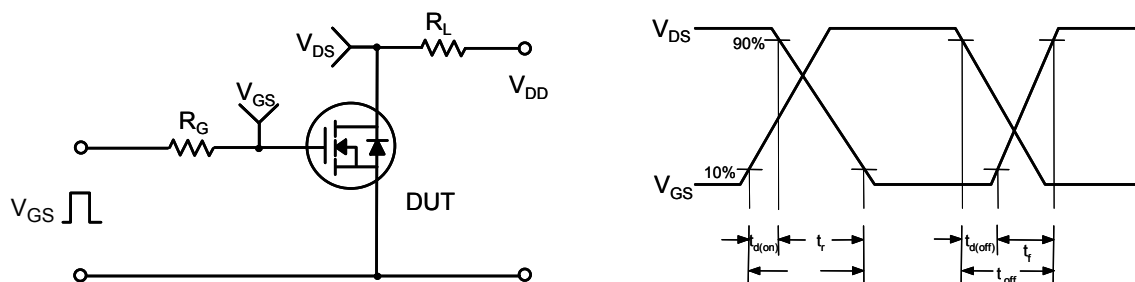


Figure 13. Resistive Switching Test Circuit & Waveforms

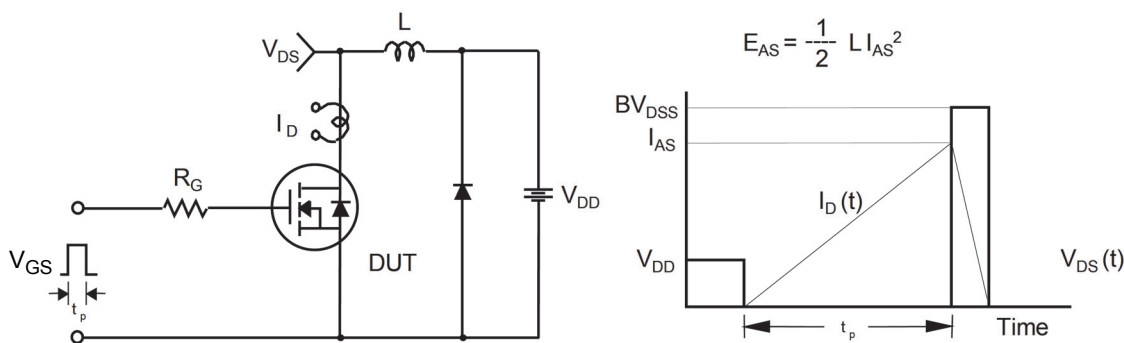
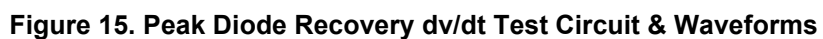


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions

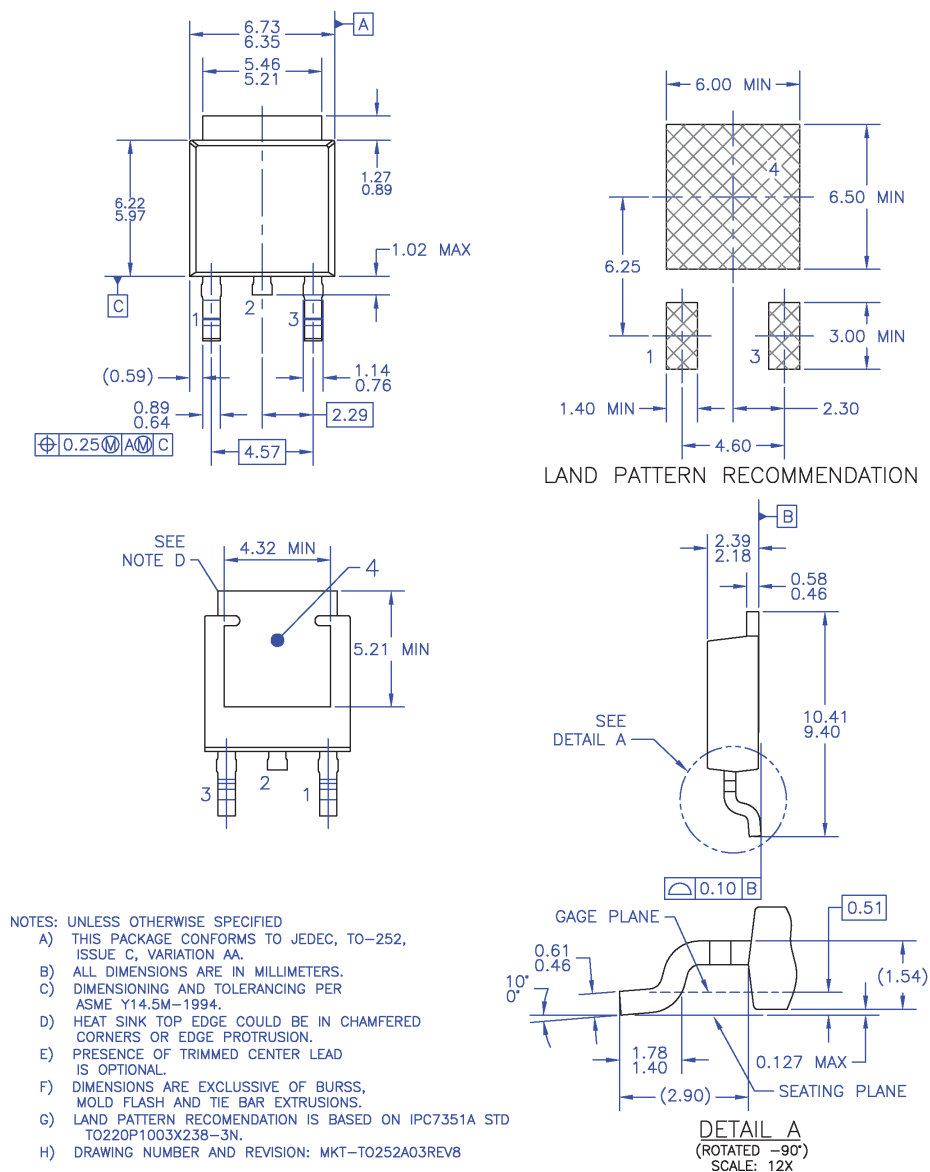


Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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