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September 2015

# FDMC8360LET40

## N-Channel Shielded Gate Power Trench® MOSFET

**40 V, 141 A, 2.1 mΩ**

### Features

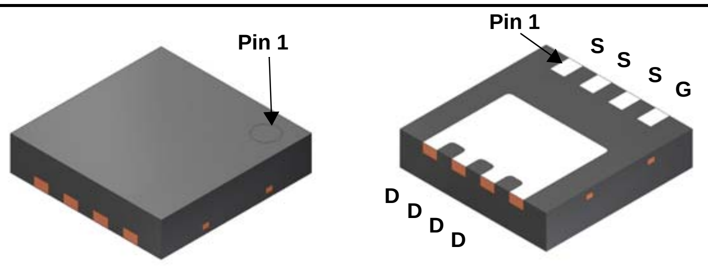
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 2.1 mΩ at $V_{GS}$ = 10 V, $I_D$ = 27 A
- Max $r_{DS(on)}$ = 3.1 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 22 A
- High Performance Technology for Extremely Low $r_{DS(on)}$
- Termination is Lead-free
- 100% UIL Tested
- RoHS Compliant

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates shielded gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

### Application

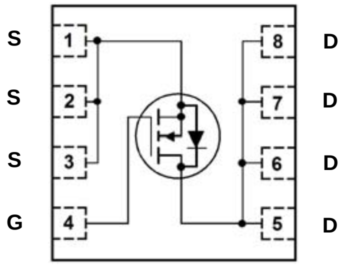
- DC-DC Conversion



Top

Power33

Bottom



## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted.

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | 40 | V |
| $V_{GS}$ | Gate to Source Voltage | ±20 | V |
| $I_D$ | Drain Current -Continuous $T_C$ = 25 °C (Note 5) | 141 | A |
| | -Continuous $T_C$ = 100 °C (Note 5) | 100 | |
| | -Continuous $T_A$ = 25 °C (Note 1a) | 27 | |
| | -Pulsed (Note 4) | 658 | |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 3) | 253 | mJ |
| $P_D$ | Power Dissipation $T_C$ = 25 °C | 75 | W |
| | Power Dissipation $T_A$ = 25 °C (Note 1a) | 2.8 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | -55 to +175 | °C |

### Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case (Note 1) | 2.0 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 53 | |

### Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMC8360LET | FDMC8360LET40 | Power33 | 13 ” | 12 mm | 3000 units |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|

### Off Characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 40 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | 20 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 32 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |

### On Characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1.0 | 1.7 | 3.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | -6 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 27 A | | 1.4 | 2.1 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 22 A | | 2.1 | 3.1 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 27 A, $T_J$ = 150 °C | | 2.3 | 3.5 | |
| $g_{FS}$ | Forward Transconductance | $V_{DD}$ = 5 V, $I_D$ = 27 A | | 138 | | S |

### Dynamic Characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, f = 1 MHz | | 3785 | 5300 | pF |
| $C_{oss}$ | Output Capacitance | | | 1220 | 1710 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 57 | 80 | pF |
| $R_g$ | Gate Resistance | | 0.1 | 0.8 | 1.6 | Ω |

### Switching Characteristics

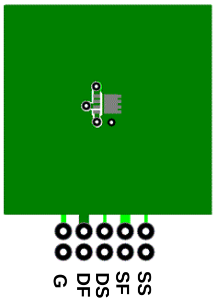
| | | | | | | |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 20 V, $I_D$ = 27 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 14 | 26 | ns |
| $t_r$ | Rise Time | | | 8 | 16 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 35 | 57 | ns |
| $t_f$ | Fall Time | | | 7 | 14 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V<br>$V_{DD}$ = 20 V, $I_D$ = 27 A | | 57 | 80 | nC |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 4.5 V | | 27 | 38 | nC |
| $Q_{gs}$ | Gate to Source Charge | | | 9.9 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | | 8.1 | | nC |

### Drain-Source Diode Characteristics

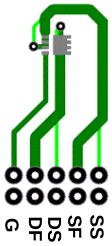
| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 27 A (Note 2) | | 0.8 | 1.3 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 1.9 A (Note 2) | | 0.7 | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 27 A, di/dt = 100 A/μs | | 47 | 76 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 30 | 48 | nC |

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in$^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 53°C/W when mounted on a 1 in$^2$ pad of 2 oz copper



b) 125°C/W when mounted on a minimum pad

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. $E_{AS}$ of 253 mJ is based on starting $T_J$ = 25 °C, L = 3 mH, $I_{AS}$ = 13 A, $V_{DD}$ = 40 V, $V_{GS}$ = 10 V. 100% test at L = 0.1 mH, $I_{AS}$ = 42 A.
4. Pulsed Id please refer to Fig 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

## Typical Characteristics $T_J$ = 25°C unless otherwise noted.

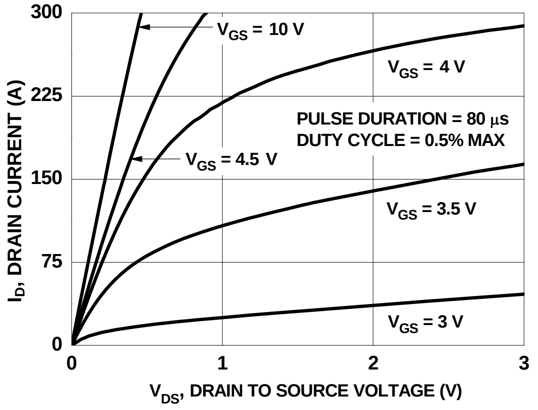


Figure 1. On Region Characteristics

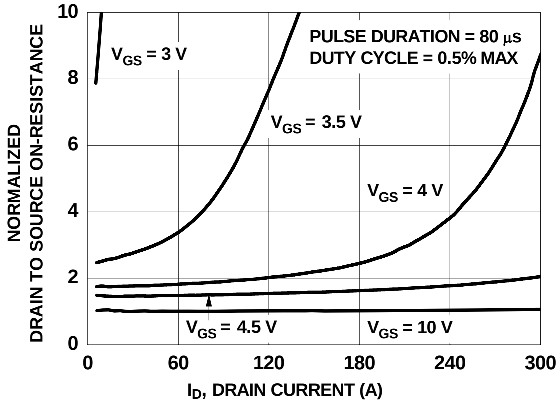


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

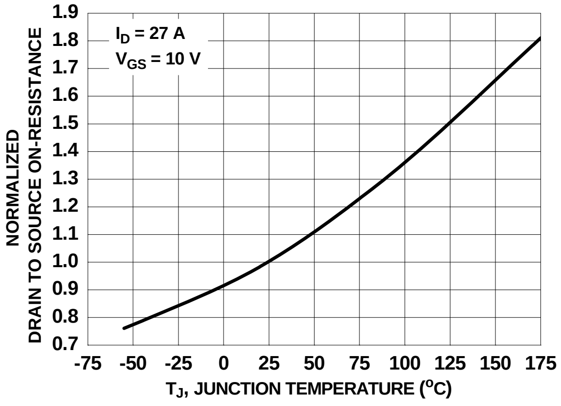


Figure 3. Normalized On Resistance vs. Junction Temperature

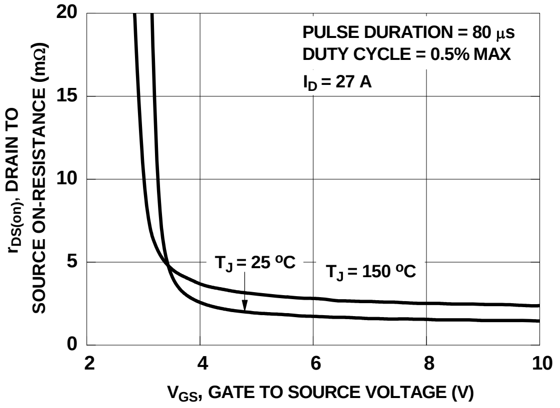


Figure 4. On-Resistance vs. Gate to Source Voltage

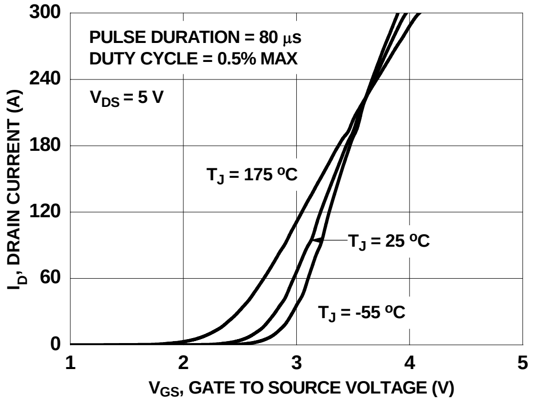


Figure 5. Transfer Characteristics

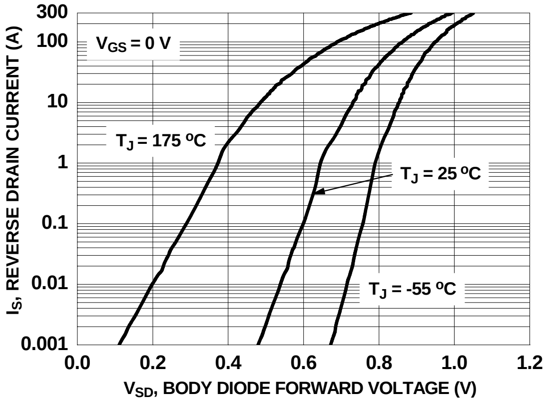


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

## Typical Characteristics $T_J$ = 25°C unless otherwise noted.

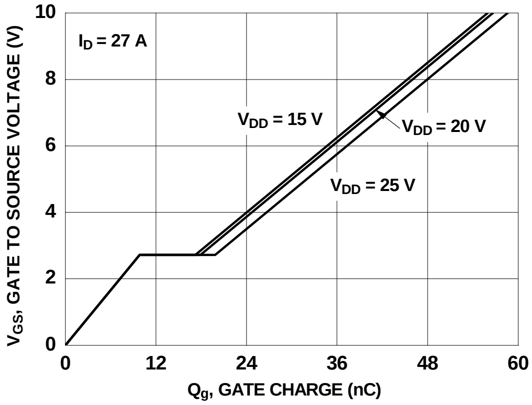


Figure 7. Gate Charge Characteristics

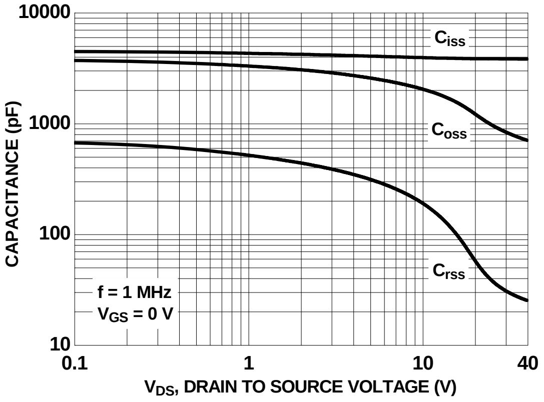


Figure 8. Capacitance vs. Drain to Source Voltage

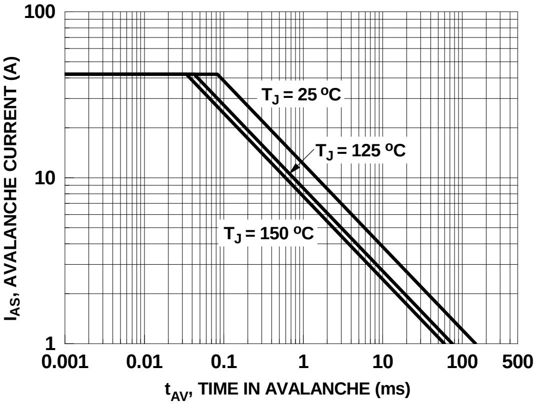


Figure 9. Unclamped Inductive Switching Capability

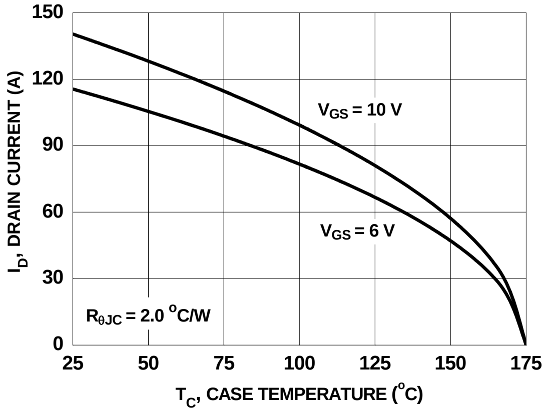


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

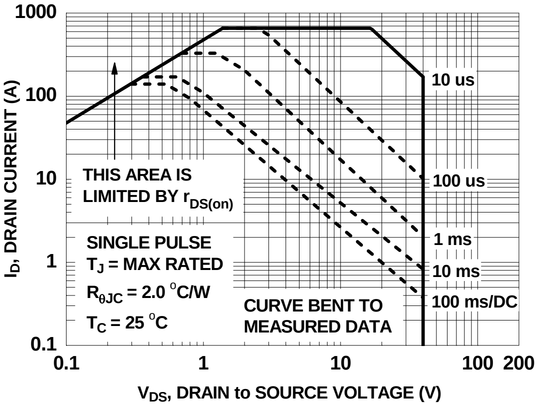


Figure 11. Forward Bias Safe Operating Area

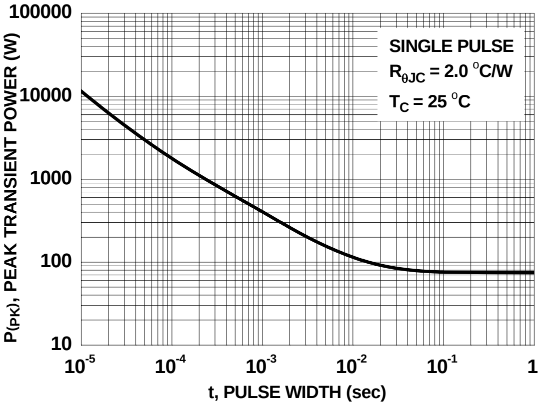


Figure 12. Single Pulse Maximum Power Dissipation

## Typical Characteristics $T_J$ = 25°C unless otherwise noted.

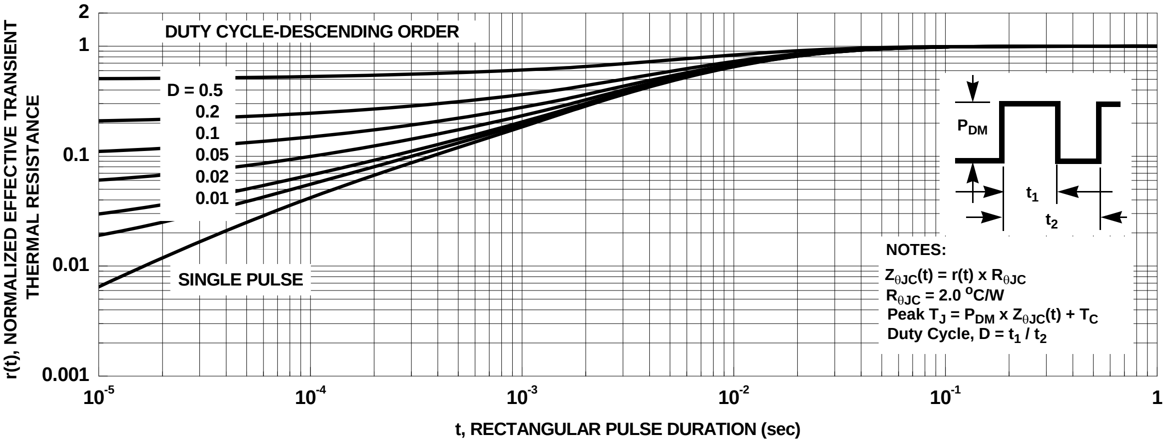
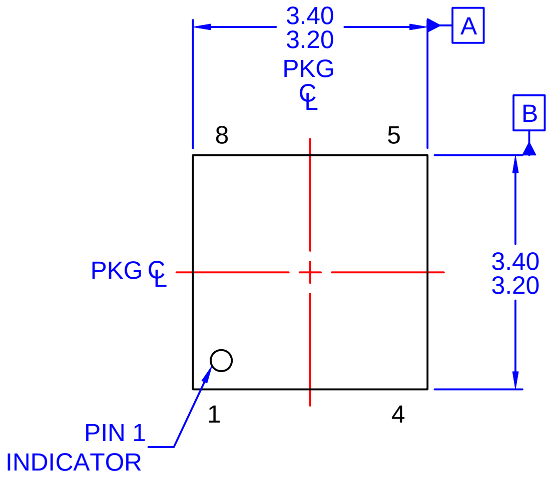
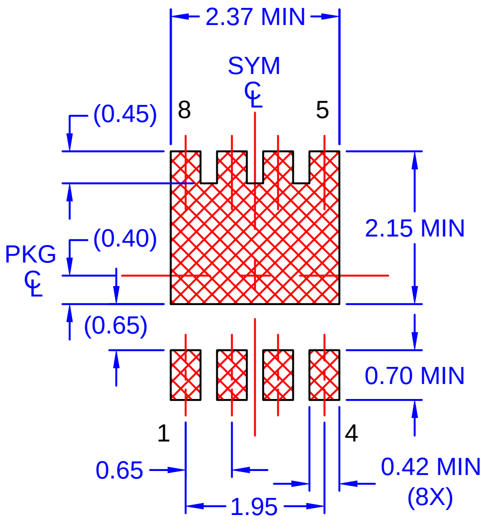


**Figure 13. Junction-to-Case Transient Thermal Response Curve**





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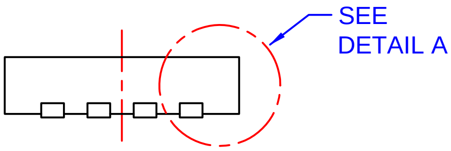

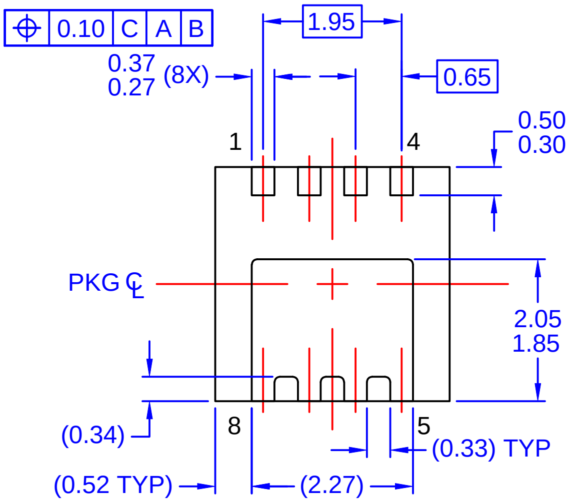

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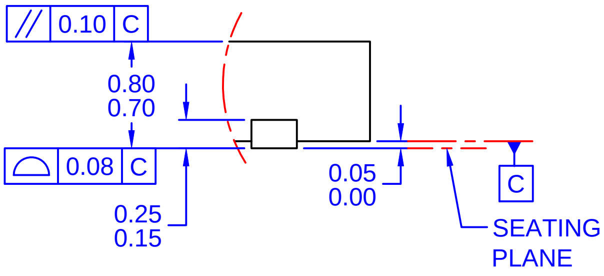

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