



February 2015

FDMD86100

Dual N-Channel Shielded Gate PowerTrench[®] MOSFET 100 V, 39 A, 10.5 mΩ

Features

- Common source configuration to eliminate PCB routing
- Large source pad on bottom of package for enhanced thermals
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 10.5 mΩ at $V_{GS} = 10$ V, $I_D = 10$ A
- Max $r_{DS(on)}$ = 17.3 mΩ at $V_{GS} = 6$ V, $I_D = 7.8$ A
- Ideal for flexible layout in secondary side synchronous rectification
- Termination is Lead-free and RoHS Compliant
- 100% UIL tested

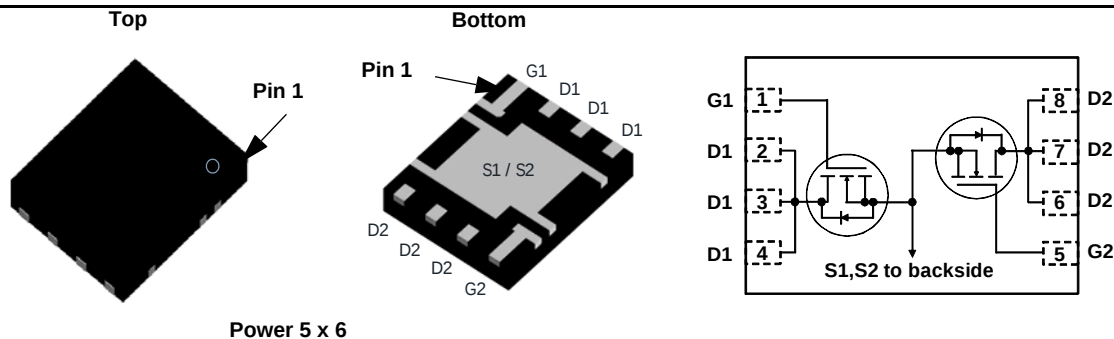


General Description

This package integrates two N-Channel devices connected internally in common-source configuration and incorporates Shielded Gate technology. This enables very low package parasitics and optimized thermal path to the common source pad on the bottom. Provides a very small footprint (5 x 6 mm) for higher power density.

Applications

- Isolated DC-DC Synchronous Rectifiers
- Common Ground Load Switches



Power 5 x 6

MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous $T_C = 25^\circ\text{C}$ (Note 5)	39	A
	-Continuous $T_C = 100^\circ\text{C}$ (Note 5)	24	
	Drain Current -Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	10	
	-Pulsed (Note 4)	299	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	337	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	33	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMD86100	FDMD86100	Power 5 x 6	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		7		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		-10		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 10\ \text{A}$		7.8	10.5	m Ω
		$V_{GS} = 6\ \text{V}$, $I_D = 7.8\ \text{A}$		12	17.3	
		$V_{GS} = 10\ \text{V}$, $I_D = 10\ \text{A}$, $T_J = 125^\circ\text{C}$		14.5	19.5	
g_{FS}	Forward Transconductance	$V_{DD} = 5\ \text{V}$, $I_D = 10\ \text{A}$		26		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}$, $V_{GS} = 0\ \text{V}$ $f = 1\ \text{MHz}$		1469	2060	pF
C_{oss}	Output Capacitance			321	450	pF
C_{rss}	Reverse Transfer Capacitance			12	20	pF
R_g	Gate Resistance		0.1	1.3	3.3	Ω

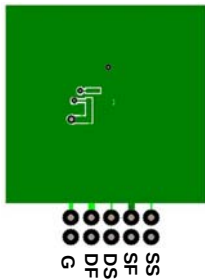
Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}$, $I_D = 10\ \text{A}$ $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$		13	23	ns
t_r	Rise Time			4.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			18	32	ns
t_f	Fall Time			4.1	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 50\ \text{V}$ $I_D = 10\ \text{A}$	21	30	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $6\ \text{V}$		13	18	nC
Q_{gs}	Gate to Source Charge			6.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			4.1		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 10\ \text{A}$ (Note 2)		0.8	1.3	V
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 2\ \text{A}$ (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 10\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		46	74	ns
Q_{rr}	Reverse Recovery Charge			46	74	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.a. 55 $^\circ\text{C}/\text{W}$ when mounted on
a 1 in² pad of 2 oz copperb. 125 $^\circ\text{C}/\text{W}$ when mounted on
a minimum pad of 2 oz copper2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0 %.3. E_{AS} of 337 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3\ \text{mH}$, $I_{AS} = 15\ \text{A}$, $V_{DD} = 100\ \text{V}$, $V_{GS} = 10\ \text{V}$. 100% tested at $L = 0.1\ \text{mH}$, $I_{AS} = 47\ \text{A}$.4. Pulsed I_D please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

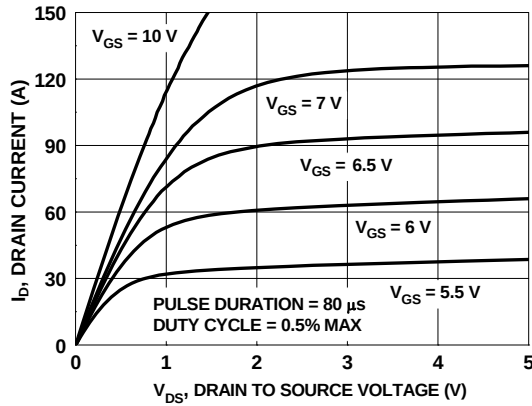


Figure 1. On-Region Characteristics

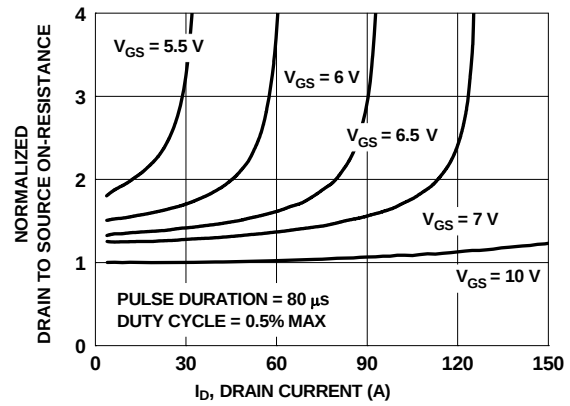


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

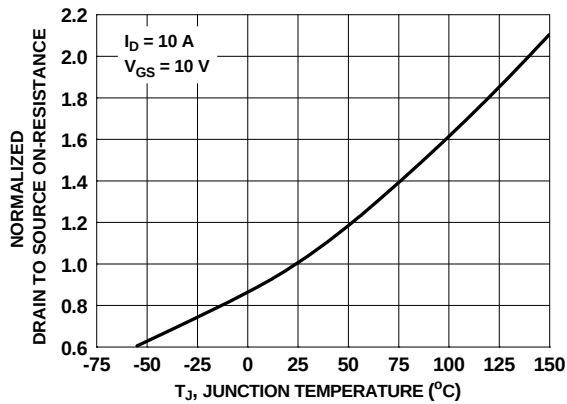


Figure 3. Normalized On-Resistance vs Junction Temperature

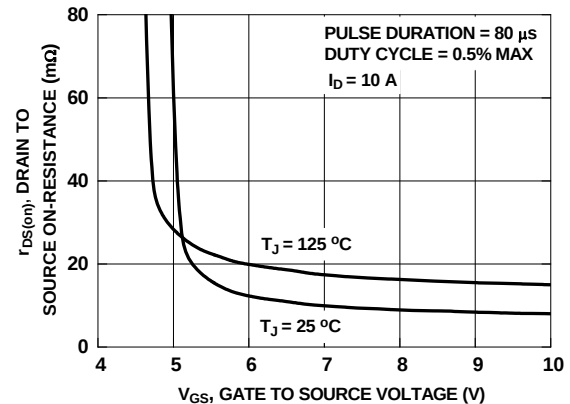


Figure 4. On-Resistance vs Gate to Source Voltage

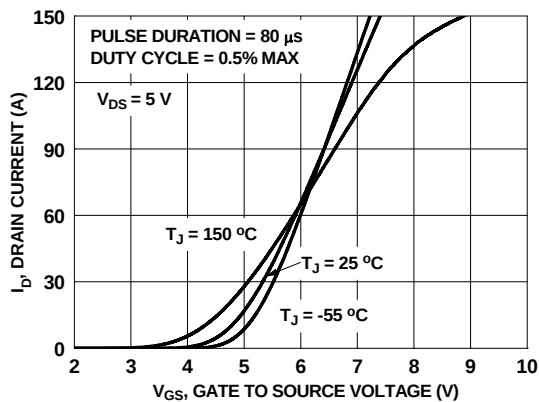


Figure 5. Transfer Characteristics

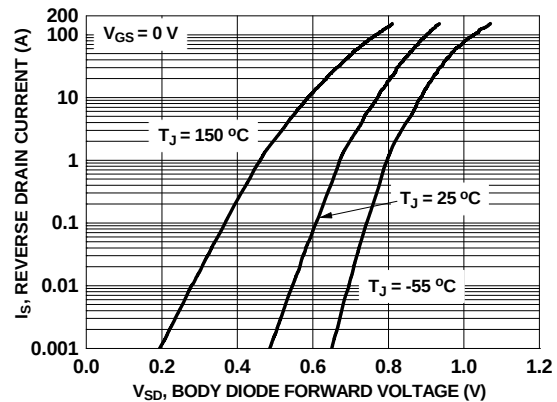


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

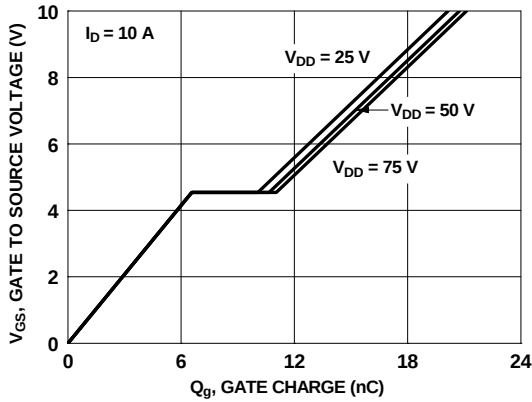


Figure 7. Gate Charge Characteristics

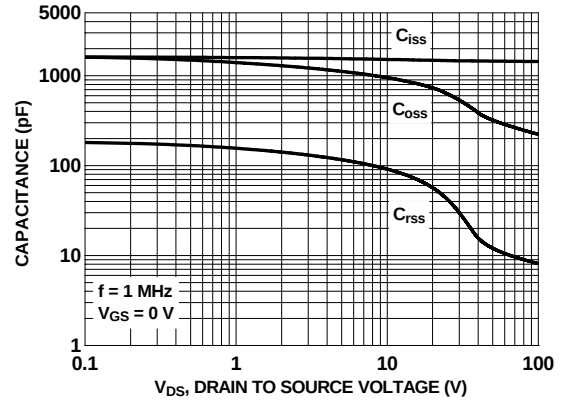


Figure 8. Capacitance vs Drain to Source Voltage

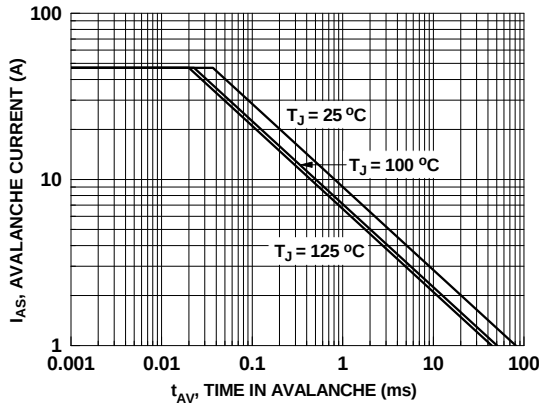


Figure 9. Unclamped Inductive Switching Capability

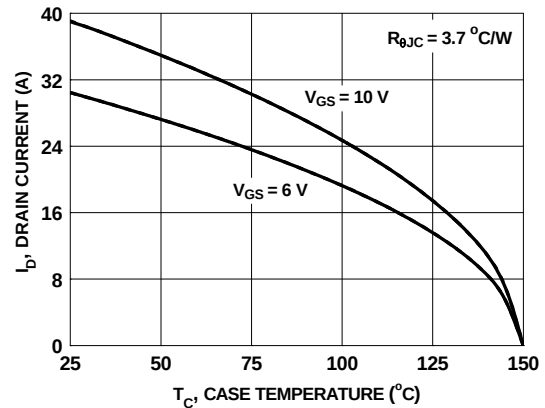


Figure 10. Maximum Continuous Drain Current vs Case Temperature

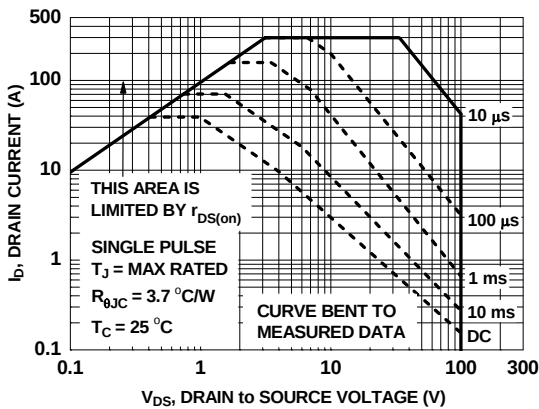


Figure 11. Forward Bias Safe Operating Area

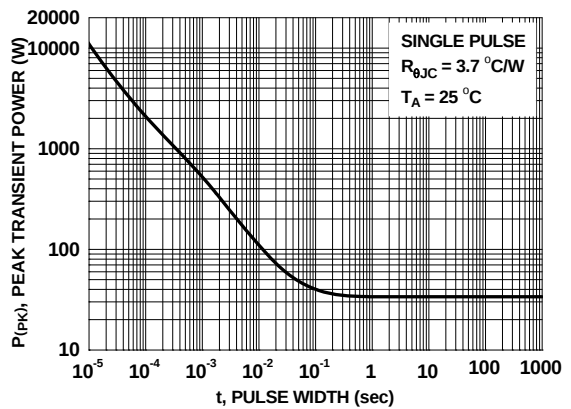


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted

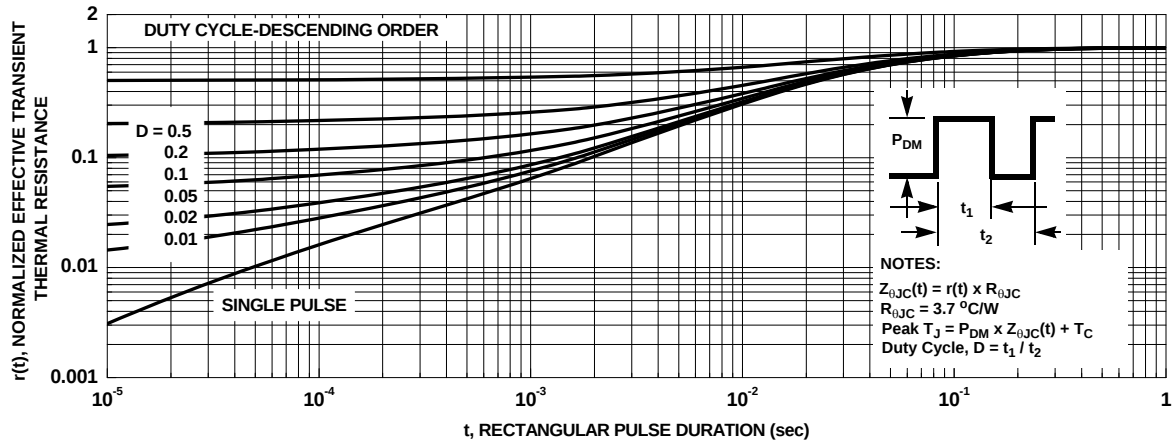
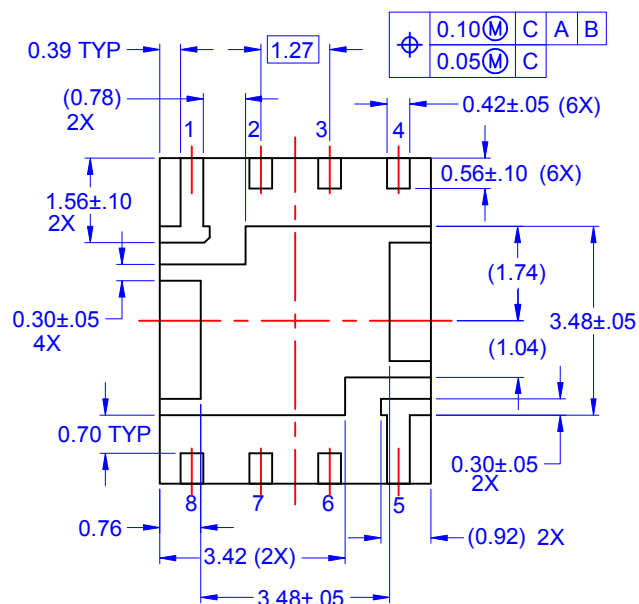
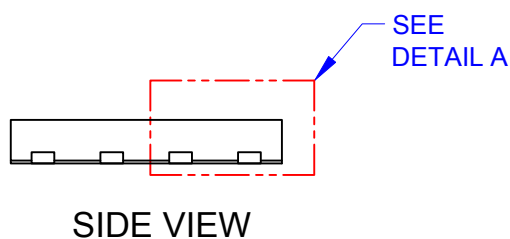
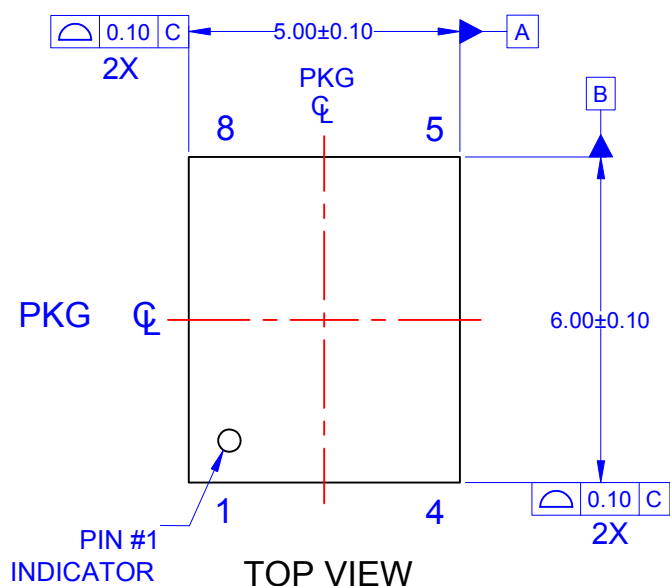
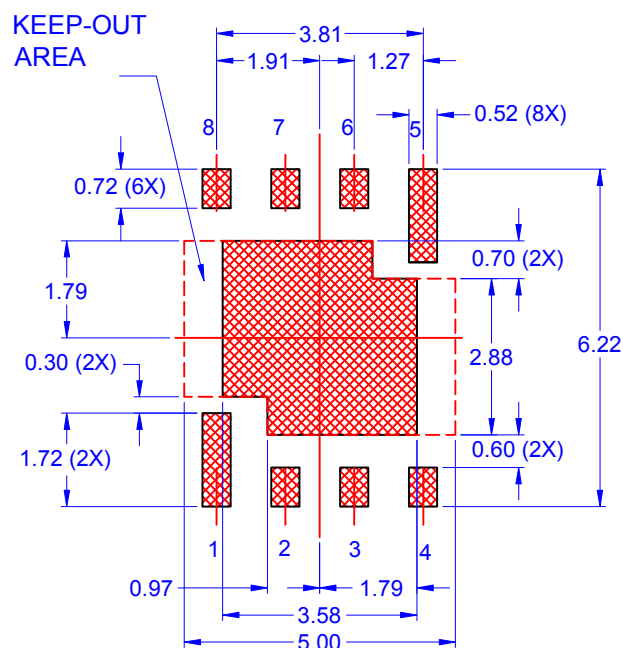


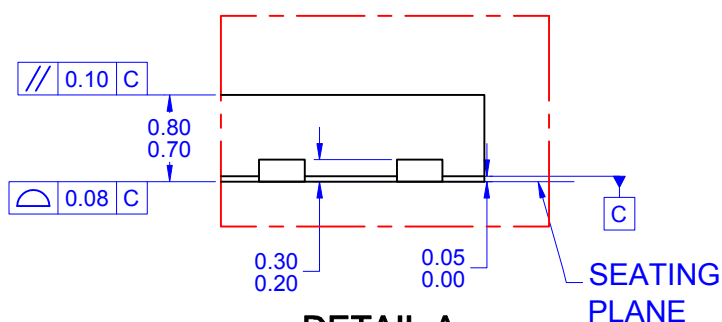
Figure 13. Junction-to-Case Transient Thermal Response Curve



BOTTOM VIEW



RECOMMENDED LAND PATTERN



DETAIL A
(SCALE: 2X)

NOTES:

- A) PACKAGE REFERENCE :
TO JEDEC REGISTRATION, MO-240B, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009
- E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP-OUT AREA
- F) DRAWING FILE NAME: PQFN08OREV1



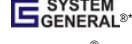


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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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