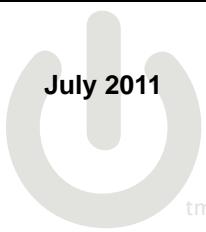




July 2011



FDP150N10A_F102

N-Channel PowerTrench® MOSFET

100V, 50A, 15mΩ

Features

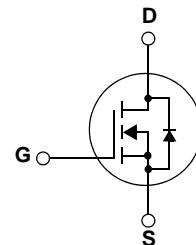
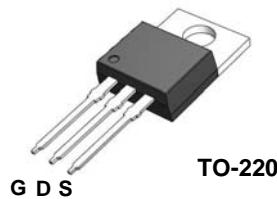
- $R_{DS(on)} = 12.5\text{m}\Omega$ (Typ.) @ $V_{GS} = 10\text{V}$, $I_D = 50\text{A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- DC to DC Converters
- Synchronous Rectification for Telecommunication PSU
- Battery Charger
- AC motor drives and Uninterruptible Power Supplies
- Off-line UPS



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter		FDP150N10A_F102	Units
V_{DSS}	Drain to Source Voltage		100	V
V_{GSS}	Gate to Source Voltage		± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	50	A
		- Continuous ($T_C = 100^\circ\text{C}$)	36	
I_{DM}	Drain Current	- Pulsed	(Note 1)	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	91	W
		- Derate above 25°C	0.61	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP150N10A	FDP150N10A_F102	TO-220	-	-	50

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	100	-	-	V
$\Delta \text{BV}_{\text{DSS}}$ ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.08	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 80\text{V}, T_C = 150^\circ\text{C}$	-	-	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 50\text{A}$	-	12.5	15.0	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 50\text{A}$	(Note 4)	-	40	-

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	1080	1440	pF
C_{oss}	Output Capacitance		-	267	355	pF
C_{rss}	Reverse Transfer Capacitance		-	11	-	pF
$C_{\text{oss(er)}}$	Engry Related Output Capacitance	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$	-	436	-	pF
$Q_{g(\text{tot})}$	Total Gate Charge at 10V		-	16.2	21.0	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DS} = 50\text{V}, V_{GS} = 10\text{V}$ $I_D = 50\text{A}$	-	5.3	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	2.6	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4, 5)	-	3.7	nC
ESR	Equivalent Series Resistance (G-S)	Drain Open, $f = 1\text{MHz}$	-	1.3	-	Ω

Switching Characteristics

$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = 50\text{V}, I_D = 50\text{A}$ $V_{GS} = 10\text{V}, R_{\text{GEN}} = 4.7\Omega$	-	13	36	ns
t_r	Turn-On Rise Time		-	16	42	ns
$t_{d(\text{off})}$	Turn-Off Delay Time		-	21	52	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	-	5	20

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	50	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	200	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 50\text{A}$	-	-	1.3
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, V_{DD} = 50\text{V}, I_{SD} = 50\text{A}$ $dI_F/dt = 100\text{A}/\mu\text{s}$	-	50	-
Q_{rr}	Reverse Recovery Charge		(Note 4)	-	55

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 2\text{mH}, I_{AS} = 9.2\text{A}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 100\text{A}, dI/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq \text{BV}_{\text{DSS}}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Dual Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

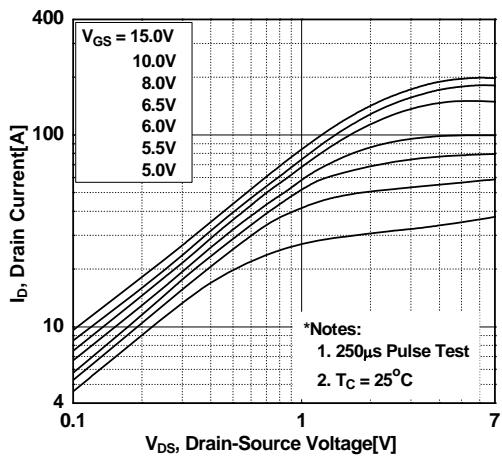


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

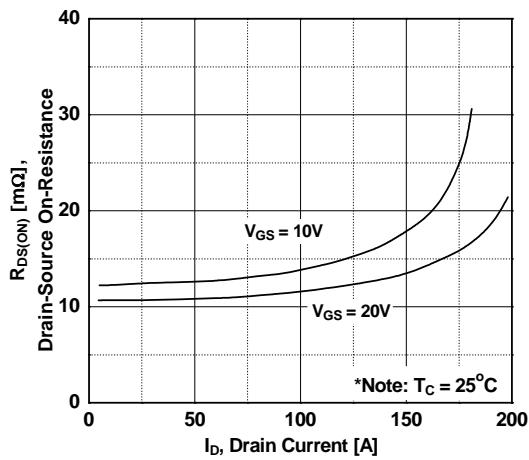


Figure 5. Capacitance Characteristics

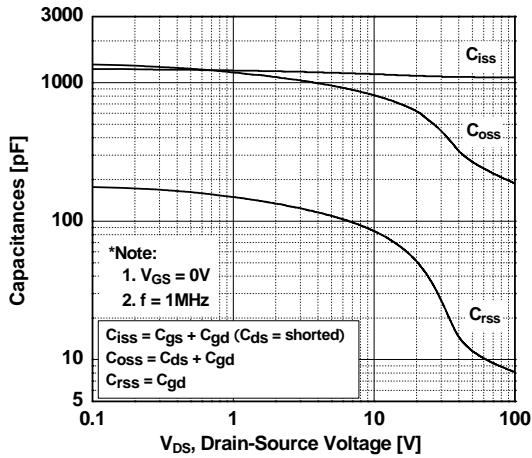


Figure 2. Transfer Characteristics

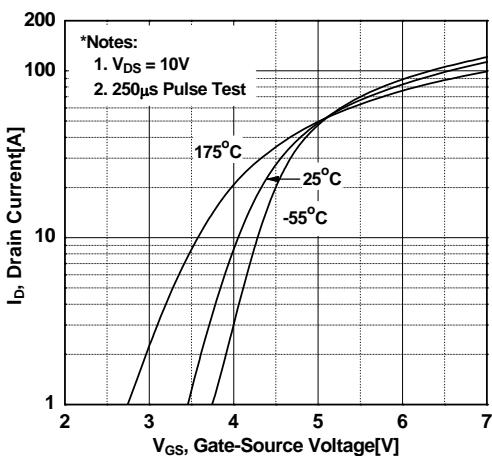


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

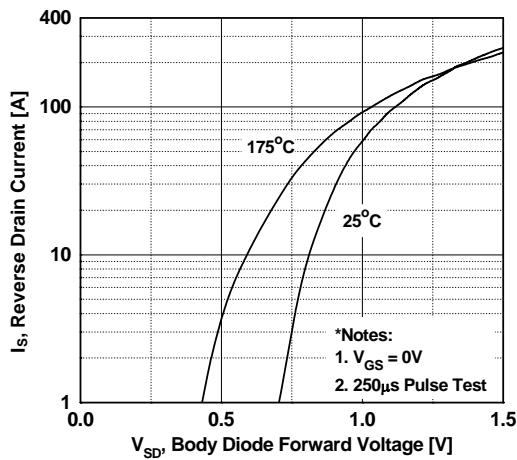
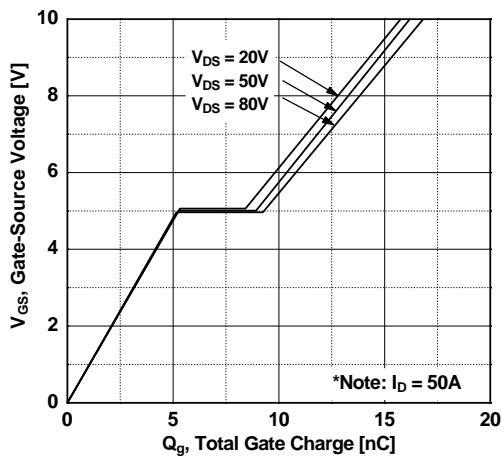


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

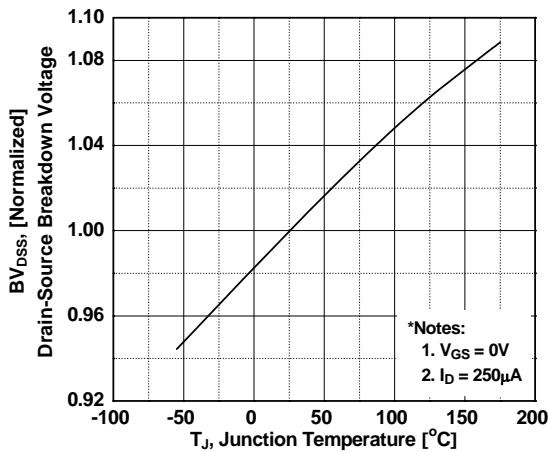


Figure 8. On-Resistance Variation vs. Temperature

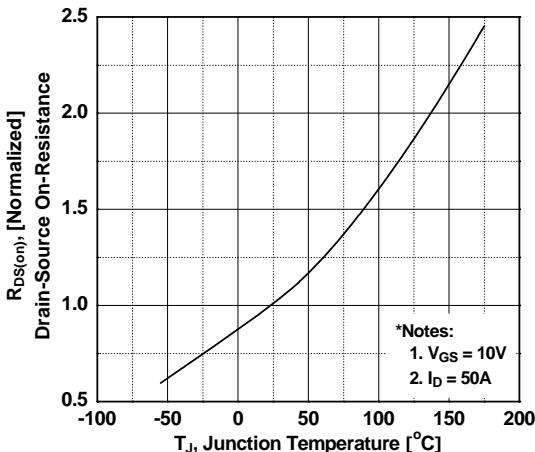


Figure 9. Maximum Safe Operating Area vs. Case Temperature

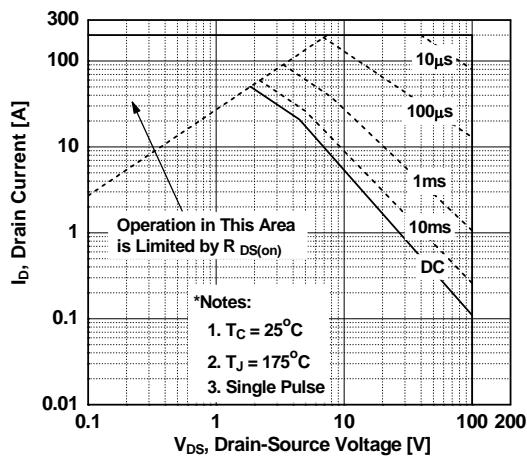


Figure 10. Maximum Drain Current

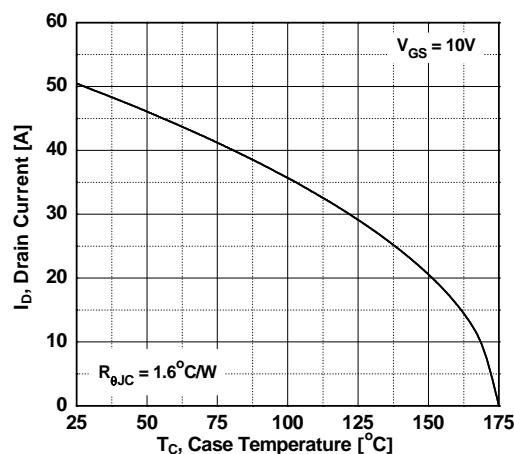


Figure 11. Eoss vs. Drain to Source Voltage

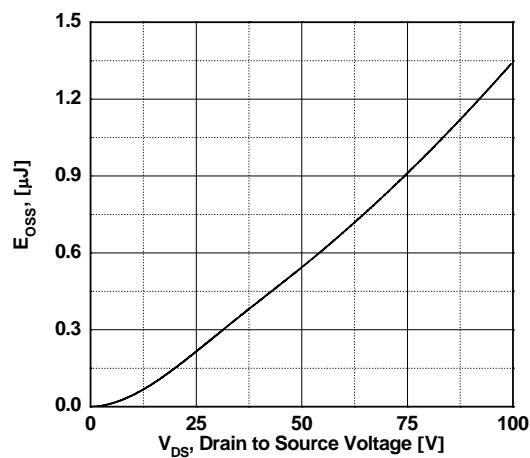
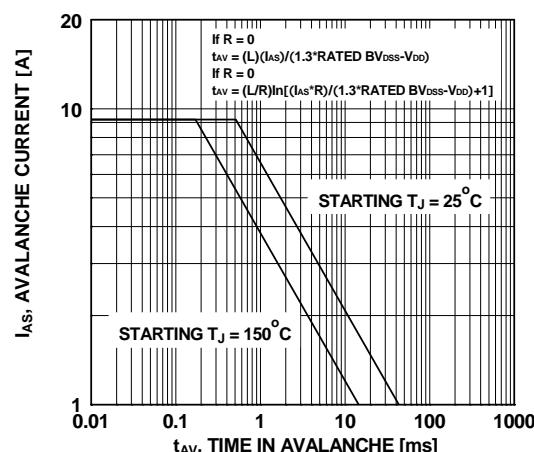
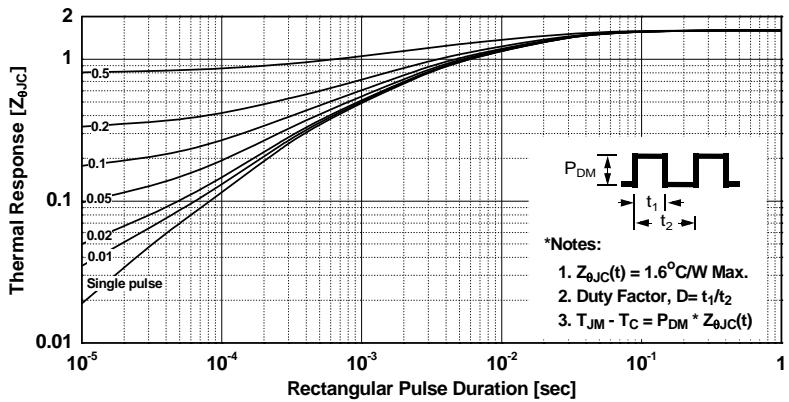


Figure 12. Unclamped Inductive Switching Capability

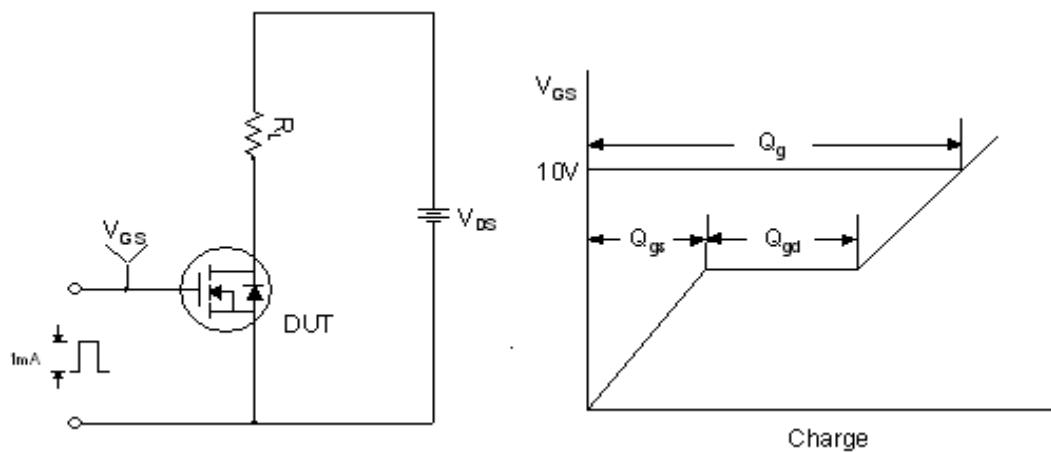


Typical Performance Characteristics (Continued)

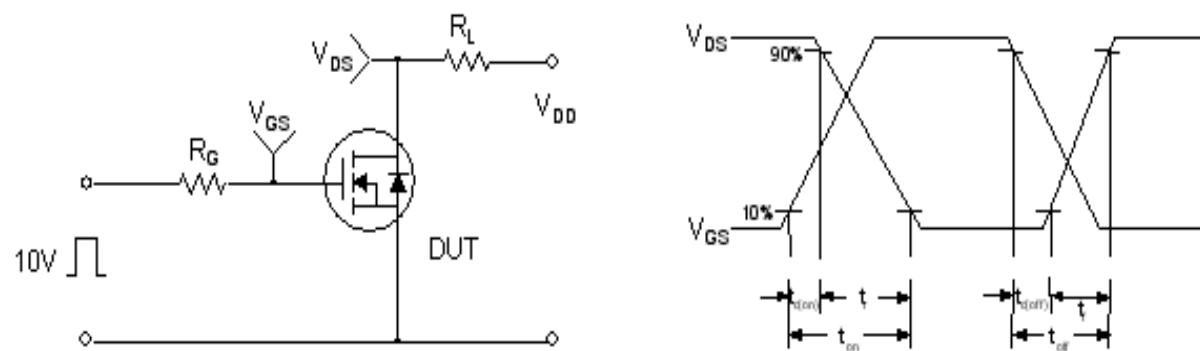
Figure 13. Transient Thermal Response Curve



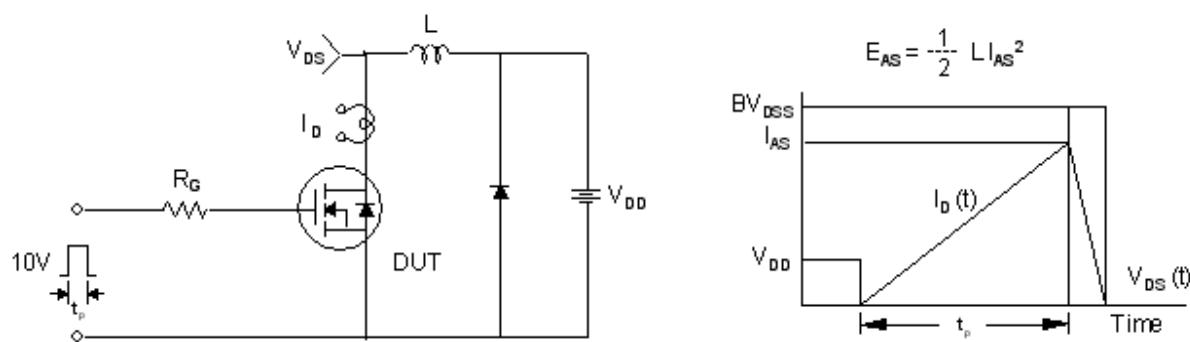
Gate Charge Test Circuit & Waveform



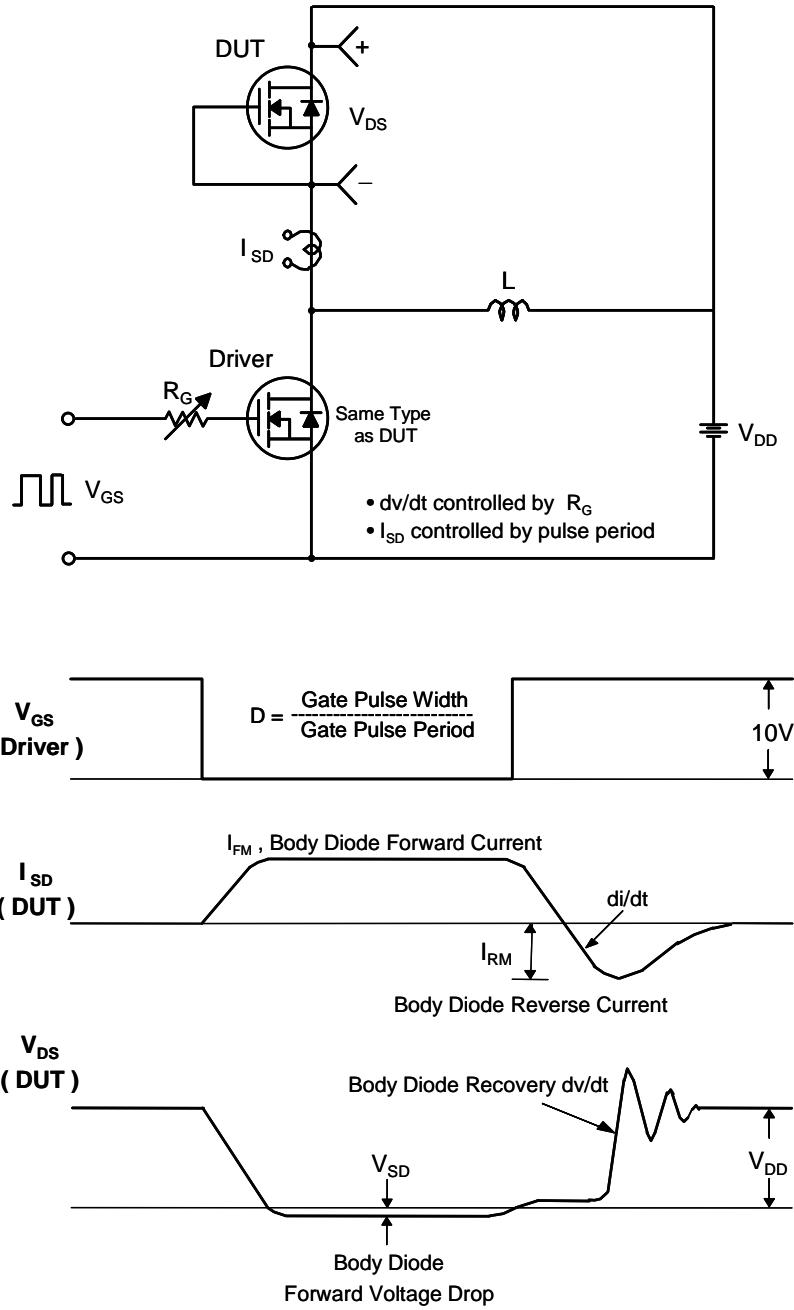
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

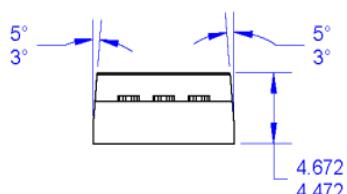
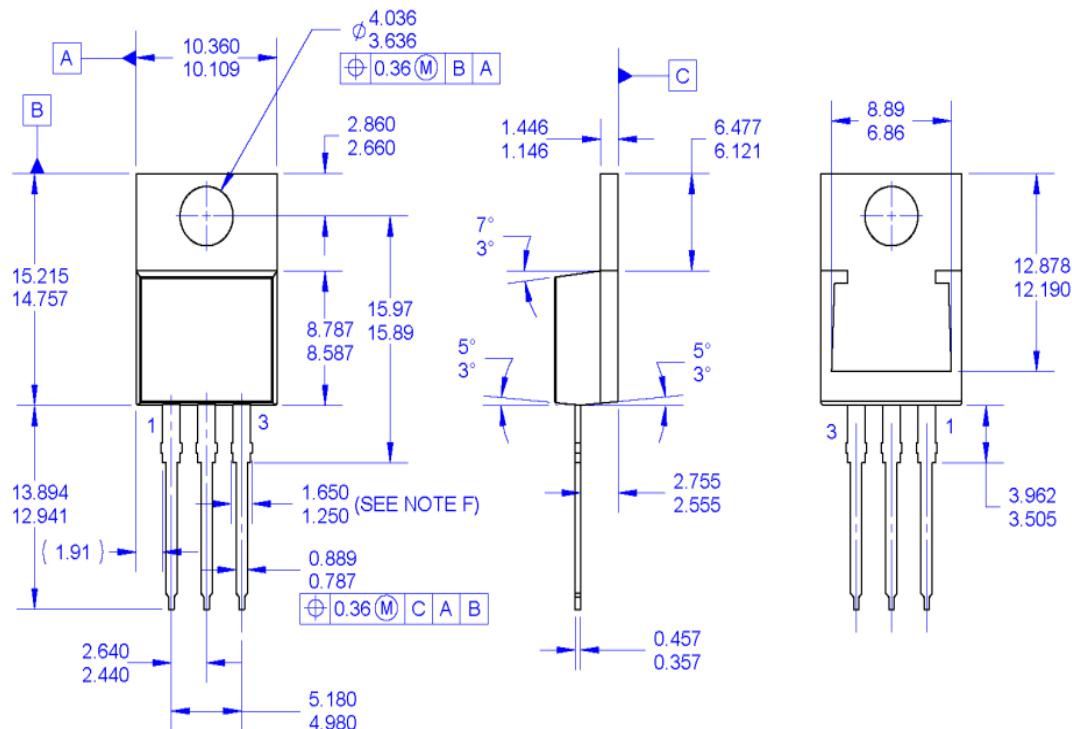


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

TO-220



NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 VARIATION AB
 - B. ALL DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
 - D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
 - E. THIS PACKAGE IS FSZ2 INTERNAL PRODUCTION AND INTENDED FOR DELTA CUSTOMER ONLY.
 - F. MAX WIDTH FOR F102 DEVICE = 1.35mm.
 - G. DRAWING FILE NAME: TO220T03REV2



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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