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FAIRCHILD

October 2014

FDPC8013S

PowerTrench® Power Clip
30 V Asymmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 9.6 mΩ at V_{GS} = 4.5 V, I_D = 10 A

Q2: N-Channel

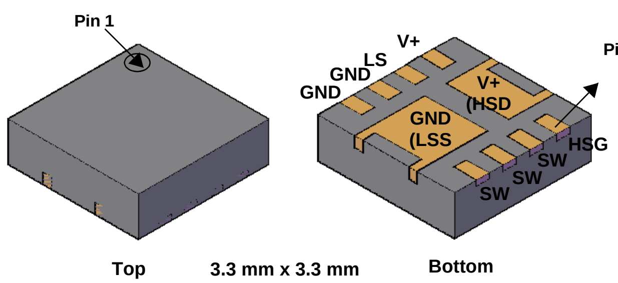
- Max $r_{DS(on)}$ = 2.7 mΩ at V_{GS} = 4.5 V, I_D = 22 A
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- RoHS Compliant

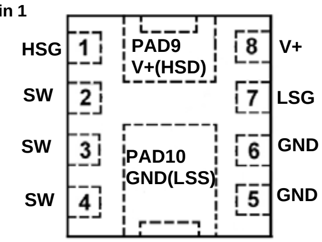
General Description

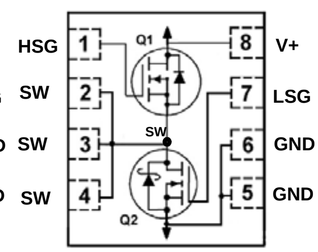
This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET^{TM} (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load







MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		30	30	V
V_{GS}	Gate to Source Voltage	(Note 4)	±20	±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25 °C	20	55	A
	-Continuous	T_A = 25 °C	13[1a]	26[1b]	
	-Pulsed		40	100	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	21	97	mJ
P_D	Power Dissipation for Single Operation	T_A = 25 °C	1.6[1a]	2.0[1b]	W
	Power Dissipation for Single Operation	T_A = 25 °C	0.8[1c]	0.9[1d]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	77[1a]	63[1b]	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	151[1c]	135[1d]	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.0	3.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
13CF/15CF	FDPC8013S	Power Clip 33	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

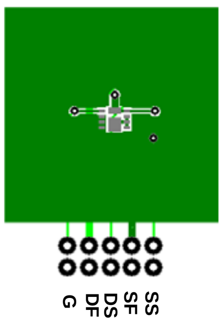
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		16 20		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2			1 500	μA μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS}= 0 V V_{GS} = 20 V, V_{DS}= 0 V	Q1 Q2			100 100	nA nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = 1 mA	Q1 Q2	1.2 1.2	1.5 1.7	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		-5 -6		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 13 A V_{GS} = 4.5 V, I_D = 10 A V_{GS} = 10 V, I_D = 13 A, T_J =125 °C	Q1		4.6 6.7 6.6	6.4 9.6 9.2	mΩ
		V_{GS} = 10 V, I_D = 26 A V_{GS} = 4.5 V, I_D = 22 A V_{GS} = 10 V, I_D = 26 A , T_J =125 °C	Q2		1.4 2.0 1.9	1.9 2.7 2.6	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 13 A V_{DS} = 5 V, I_D = 26 A	Q1 Q2		53 168		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ Q2: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		827 2785		pF
C_{oss}	Output Capacitance		Q1 Q2		333 997		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		44 128		pF
R_g	Gate Resistance		Q1 Q2		0.5 0.5		Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 15 V, I_D = 13 A, R_{GEN} = 6 Ω Q2: V_{DD} = 15 V, I_D = 26 A, R_{GEN} = 6 Ω	Q1 Q2		6 11		ns
t_r	Rise Time		Q1 Q2		2 5		ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		16 30		ns
t_f	Fall Time		Q1 Q2		2 4		ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; Q1 V_{DD} = 15 V, I_D = 13 A; Q2 V_{DD} = 15 V, I_D = 26 A	Q1 Q2		13 44		nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V	Q1 Q2		6 21		nC
Q_{gs}	Gate to Source Gate Charge		Q1 Q2		2.2 7.2		nC
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2		1.9 6.6		nC

Electrical Characteristics T_J = 25 °C unless otherwise noted

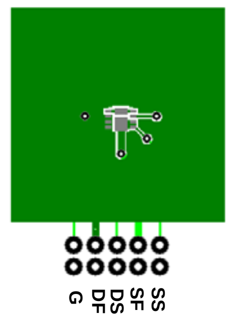
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 13 A (Note 2) V_{GS} = 0 V, I_S = 26 A (Note 2)	Q1 Q2		0.80 0.77	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 13 A, di/dt = 100 A/µs Q2 I_F = 26 A, di/dt = 300 A/µs	Q1 Q2		22 29		ns
Q_{rr}	Reverse Recovery Charge		Q1 Q2		7 30		nC

Notes:

1.$R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

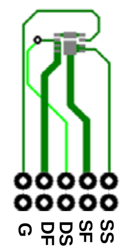


a. 77 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 63 °C/W when mounted on a 1 in^2 pad of 2 oz copper

c. 151 °C/W when mounted on a minimum pad of 2 oz copper



d. 135 °C/W when mounted on a minimum pad of 2 oz copper

2 Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.

3. Q1 :E_{AS} of 21 mJ is based on starting T_J = 25 ^oC; N-ch: L = 1.2 mH, I_{AS} = 6 A, V_{DD} = 23 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 14.5 A.
Q2: E_{AS} of 97 mJ is based on starting T_J = 25 ^oC; N-ch: L = 0.6 mH, I_{AS} = 18 A, V_{DD} = 23 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 32.9 A.

4. As an N-ch device, the negative V_{gs} rating is for low duty cycle pulse occurence only. No continuous rating is implied.

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

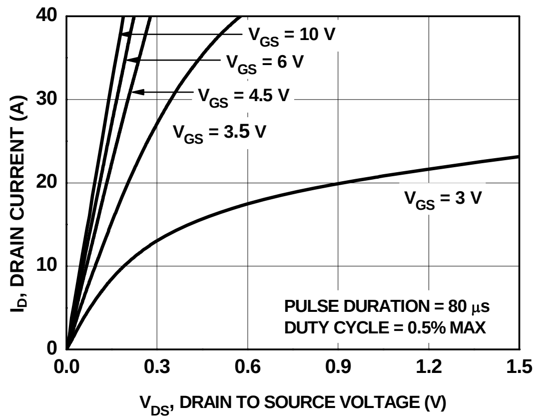


Figure 1. On Region Characteristics

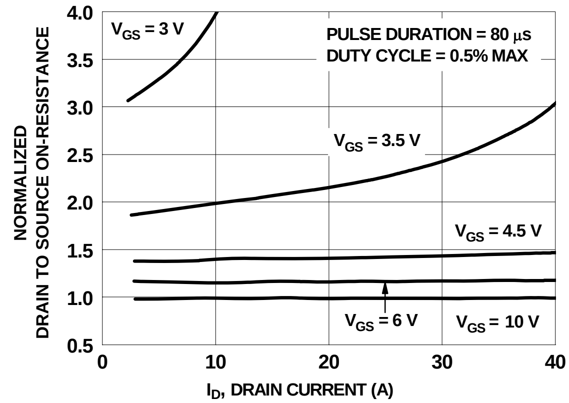


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

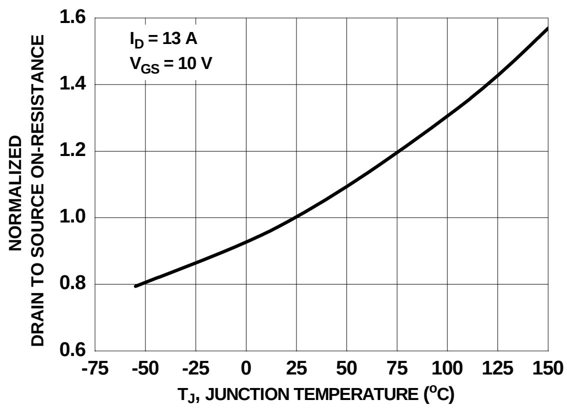


Figure 3. Normalized On Resistance vs Junction Temperature

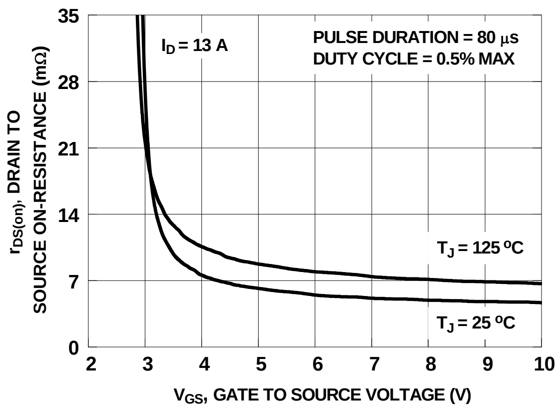


Figure 4. On-Resistance vs Gate to Source Voltage

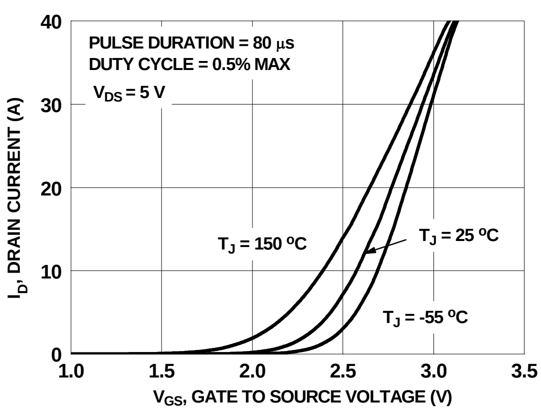


Figure 5. Transfer Characteristics

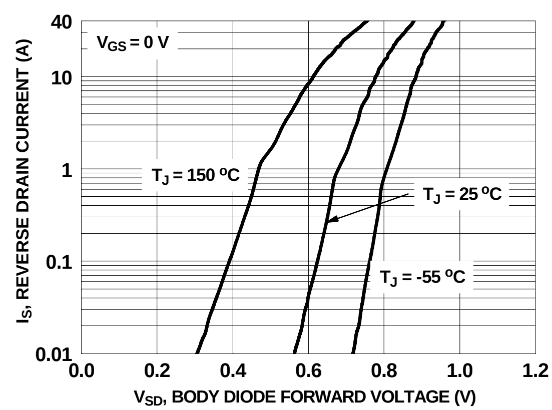


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

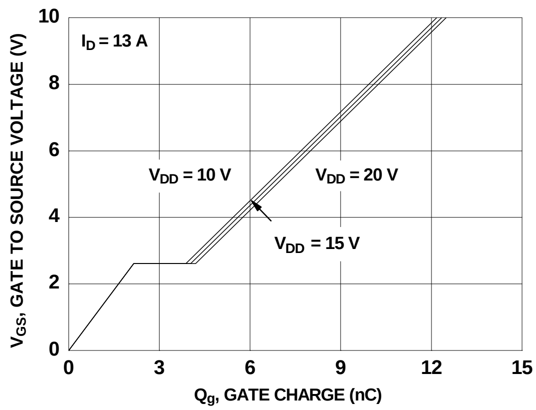


Figure 7. Gate Charge Characteristics

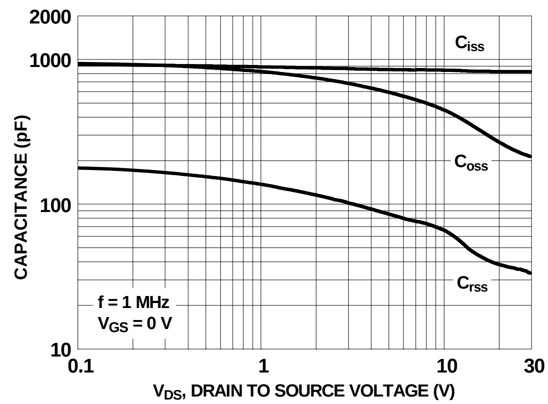


Figure 8. Capacitance vs Drain to Source Voltage

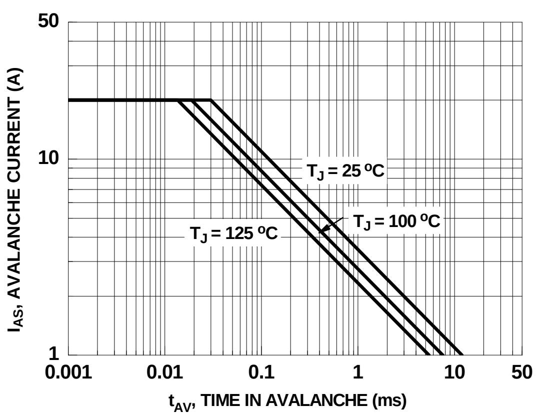


Figure 9. Unclamped Inductive Switching Capability

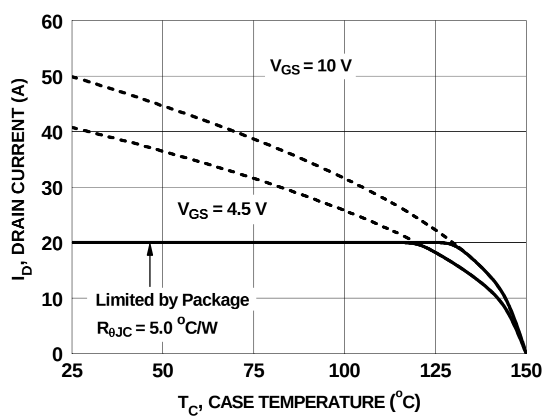


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

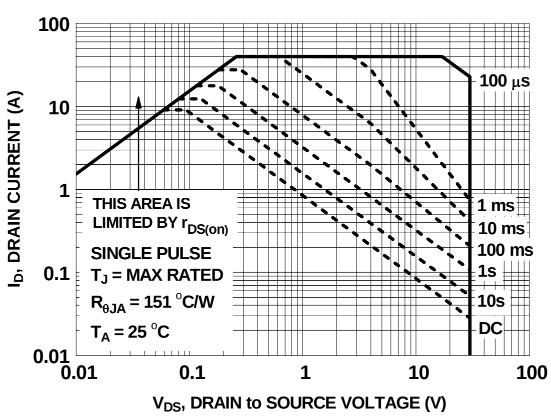


Figure 11. Forward Bias Safe Operating Area

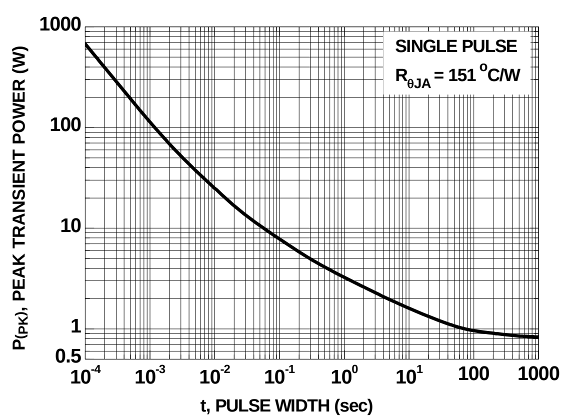


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25 °C unless otherwise noted

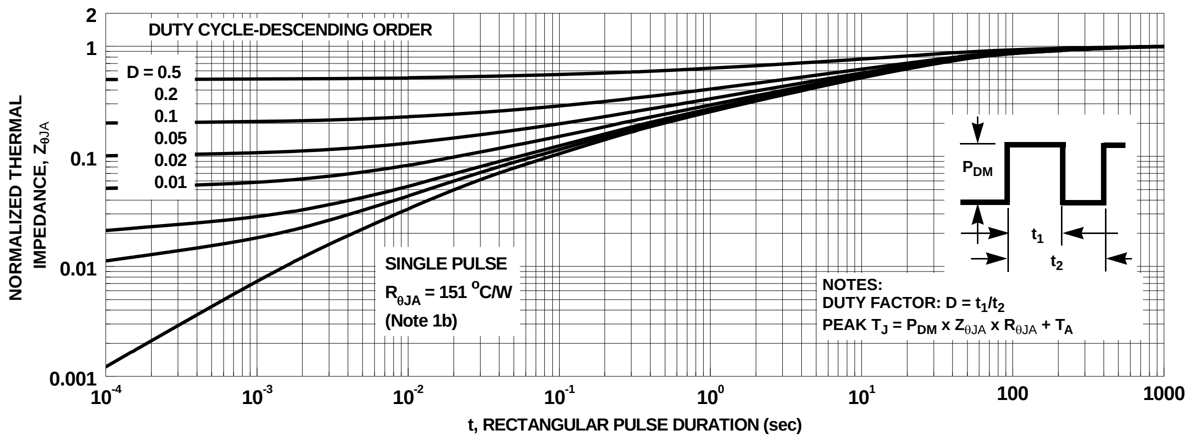


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unlenss otherwise noted

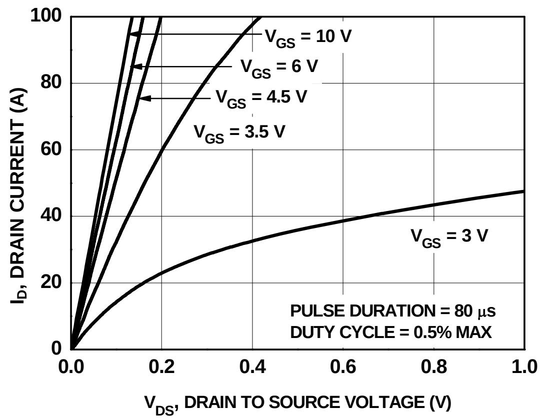


Figure 14. On-Region Characteristics

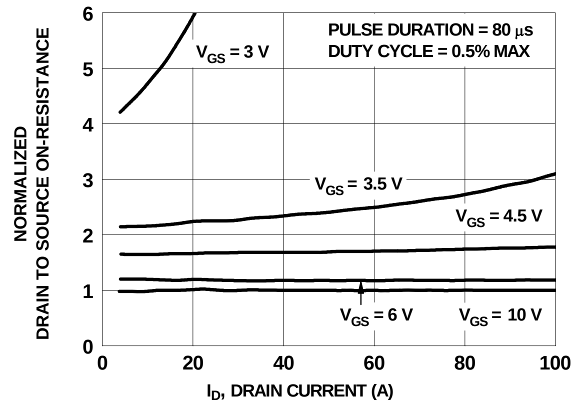


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

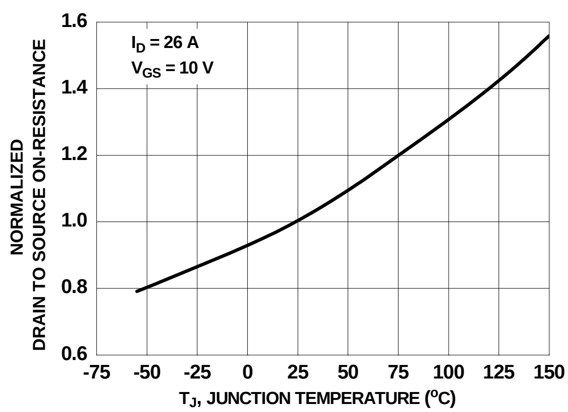


Figure 16. Normalized On-Resistance vs Junction Temperature

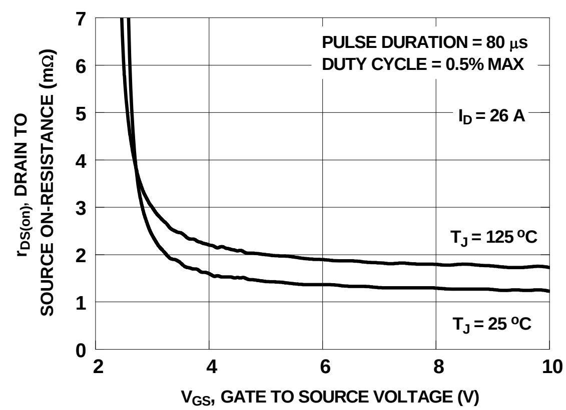


Figure 17. On-Resistance vs Gate to Source Voltage

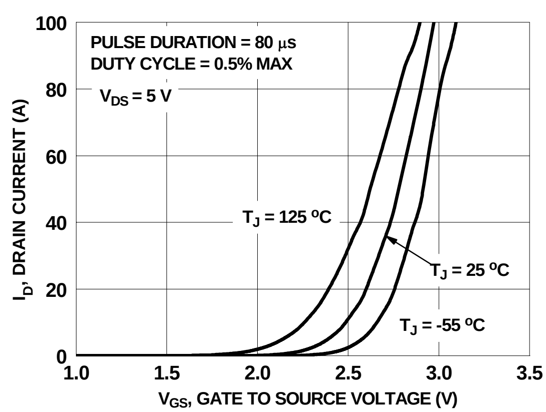


Figure 18. Transfer Characteristics

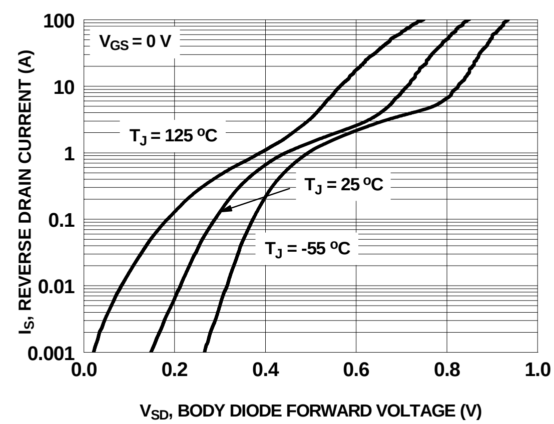


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unlenss otherwise noted

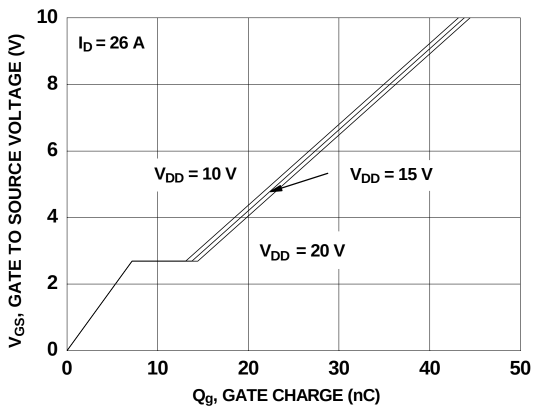


Figure 20. Gate Charge Characteristics

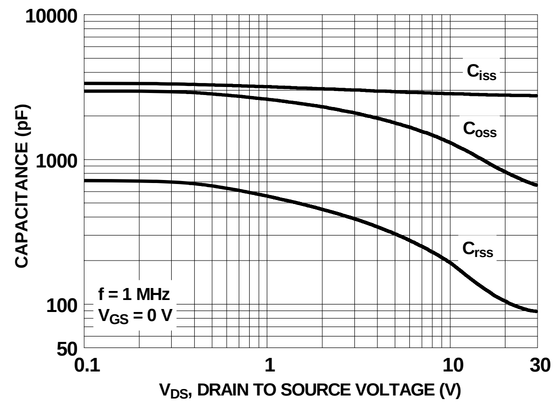


Figure 21. Capacitance vs Drain to Source Voltage

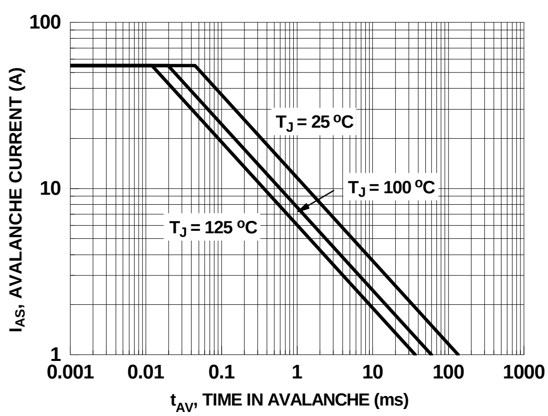


Figure 22. Unclamped Inductive Switching Capability

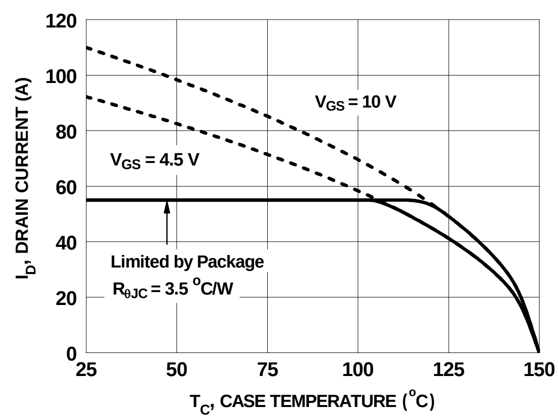


Figure 23. Maximum Continouns Drain Current vs Ambient Temperature

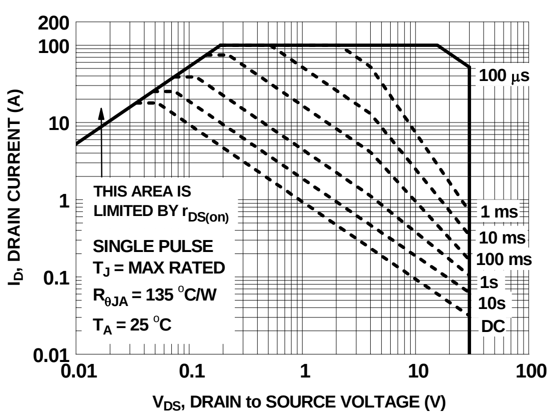


Figure 24. Forward Bias Safe Operating Area

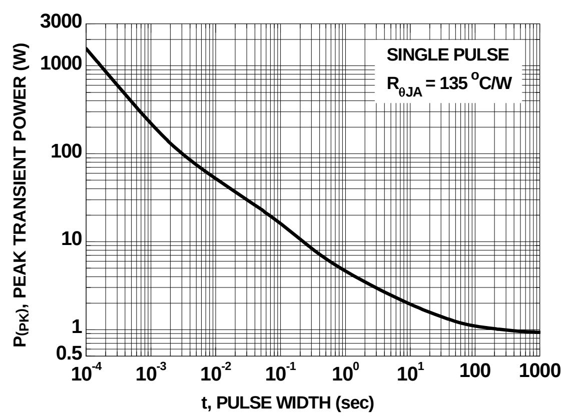


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unlenss otherwise noted

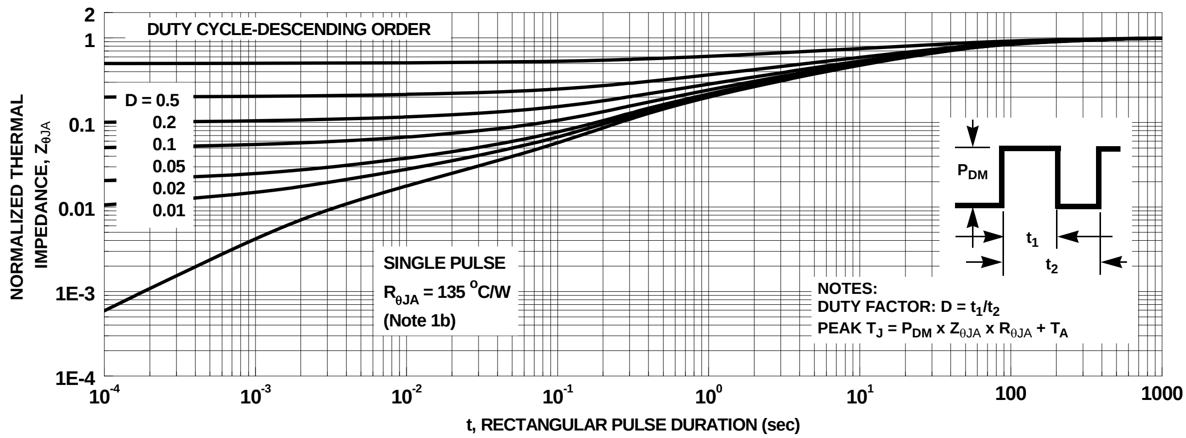


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET™ Schottky body diode Characteristics

Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC8013S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

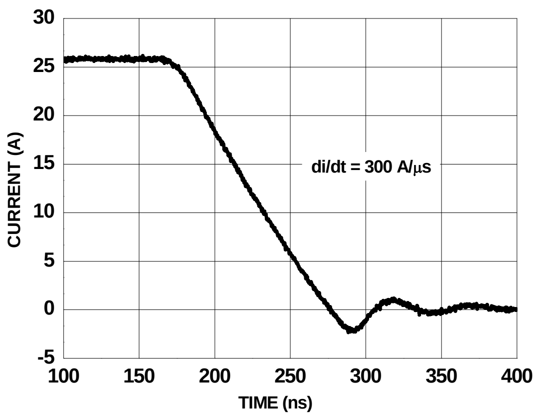


Figure 27. FDPC8013S SyncFET™ body diode reverse recovery characteristic

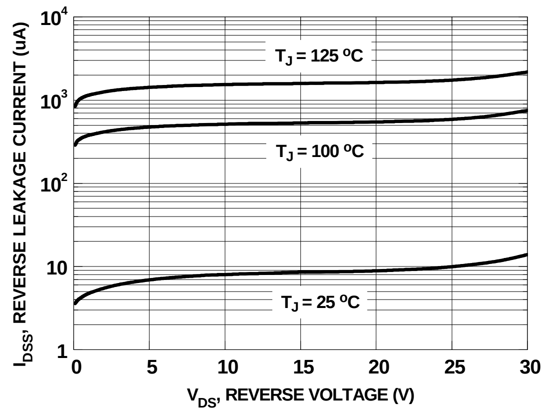
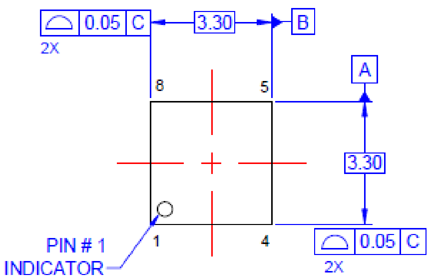
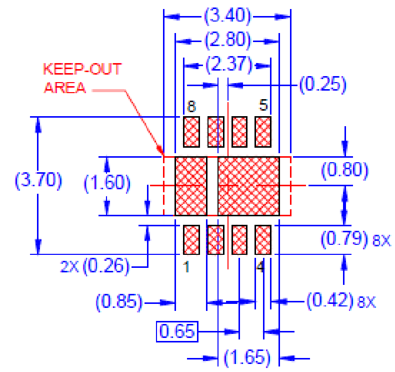


Figure 28. SyncFET™ body diode reverse leakage versus drain-source voltage

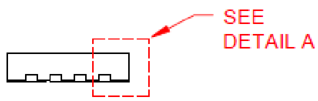
Dimensional Outline and Pad Layout



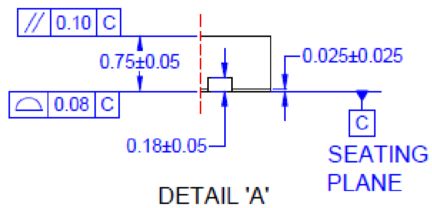
TOP VIEW



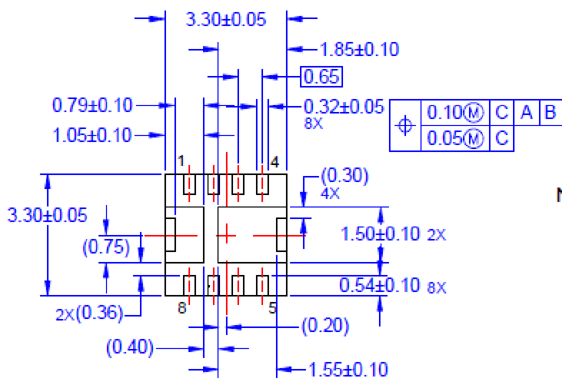
LAND PATTERN RECOMMENDATION



FRONT VIEW



DETAIL 'A'
SCALE 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE IS REFERENCED FROM JEDEC MO-240, VARIATION BA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME: MKT-PQFN08GREV4

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MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
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SuperSOT™-6
SuperSOT™-8
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TINYOPTO™
TinyPower™
TinyPWM™
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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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