FAIRCHILD™

FDZ1323NZ

Common Drain N-Channel 2.5 V PowerTrench® WL-CSP MOSFET

20 V, 10 A, 13 mΩ

Features

- Max $r_{S1S2(on)}$ = 13 mΩ at V_{GS} = 4.5 V, I_{S1S2} = 1 A
- Max $r_{S1S2(on)}$ = 13 mΩ at V_{GS} = 3.8 V, I_{S1S2} = 1 A
- Max $r_{S1S2(on)}$ = 16 mΩ at V_{GS} = 3.1 V, I_{S1S2} = 1 A
- Max $r_{S1S2(on)}$ = 18 mΩ at V_{GS} = 2.5 V, I_{S1S2} = 1 A
- Occupies only 3 mm^2 of PCB area
- Ultra-thin package: less than 0.35 mm height when mounted to PCB
- High power and current handling capability
- HBM ESD protection level > 3.6 kV (Note 3)
- RoHS Compliant

General Description

This device is designed specifically as a single package solution for Li-Ion battery pack protection circuit and other ultra-portable applications. It features two common drain N-channel MOSFETs, which enables bidirectional current flow, on Fairchild's advanced PowerTrench® process with state of the art "low pitch" WLCSP packaging process, the FDZ1323NZ minimizes both PCB space and $r_{S1S2(on)}$. This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge and low $r_{S1S2(on)}$.

Applications
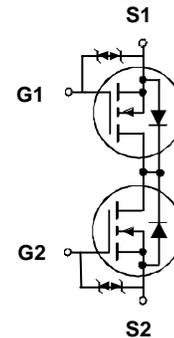
- Battery management
- Load switch
- Battery protection
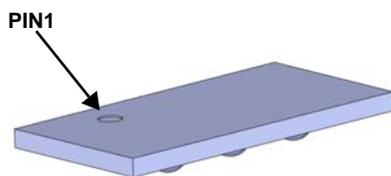
TOP
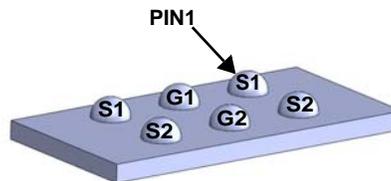
BOTTOM

WL-CSP 1.3X2.3

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{S1S2}	Source1 to Source2 Voltage			20	V
V_{GS}	Gate to Source Voltage			±12	V
I_{S1S2}	Source1 to Source2 Current -Continuous T_A = 25°C	(Note 1a)	10	A
	-Pulsed			40	
P_D	Power Dissipation T_A = 25°C	(Note 1a)		2	W
	Power Dissipation T_A = 25°C	(Note 1b)		0.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

			Ratings	Units
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	62	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	257	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
EC	FDZ1323NZ	WL-CSP 1.3X2.3	7 "	8 mm	5000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

| Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
I_{S1S2}	Zero Gate Voltage Source1 to Source2 Current	V_{S1S2} = 16 V, V_{GS} = 0 V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±12 V, V_{S1S2} = 0 V			±10	µA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{S1S2}, I_{S1S2} = 250 µA	0.4	0.9	1.2	V
$r_{S1S2(on)}$	Static Source1 to Source2 On Resistance	V_{GS} = 4.5 V, I_{S1S2} = 1 A	4.5	9.7	13	mΩ
		V_{GS} = 3.8 V, I_{S1S2} = 1 A	5.5	10	13	
		V_{GS} = 3.1 V, I_{S1S2} = 1 A	7	11	16	
		V_{GS} = 2.5 V, I_{S1S2} = 1 A	8	13	18	
		V_{GS} = 4.5 V, I_{S1S2} = 1 A, T_J = 125 °C		13	20	
g_{FS}	Forward Transconductance	V_{S1S2} = 5 V, I_{S1S2} = 1 A		9		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{S1S2} = 10 V, V_{GS} = 0 V, f = 1 MHz		1545	2055	pF
C_{oss}	Output Capacitance			269	405	pF
C_{rss}	Reverse Transfer Capacitance			252	380	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{S1S2} = 10 V, I_{S1S2} = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		12	22	ns
t_r	Rise Time			13	23	ns
$t_{d(off)}$	Turn-Off Delay Time			34	54	ns
t_f	Fall Time			13	23	ns
Q_g	Total Gate Charge	V_{S1S2} = 10 V, I_{S1S2} = 1 A, V_{G1S1} = 4.5 V, V_{G2S2} = 0 V		17	24	nC
Q_{gs}	Gate to Source1 Gate Charge			1.9		nC
Q_{gd}	Gate to Source2 "Miller" Charge			5.4		nC
Source1 to Source2 Diode Characteristics						
I_{fss}	Maximum Continuous Source1 to Source2 Diode Forward Current				1	A
V_{fss}	Source1 to Source2 Diode Forward Voltage	V_{G1S1} = 0 V, V_{G2S2} = 4.5 V, I_{fss} = 1 A (Note 2)		0.6	1.2	V

Notes:

1. $R_{θJA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{θJC}$ is guaranteed by design while $R_{θCA}$ is determined by the user's board design.
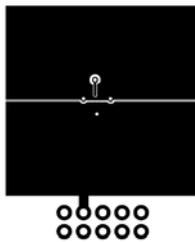
a. 62 °C/W when mounted on a 1 in² pad of 2 oz copper.
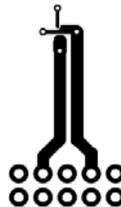
b. 257 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 us, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only protection against ESD. No gate overvoltage rating is implied.

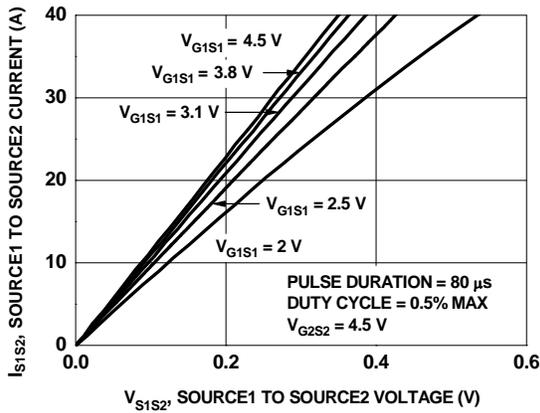## Typical Characteristics $T_J = 25°C$ unless otherwise noted

Figure 1. On-Region Characteristics
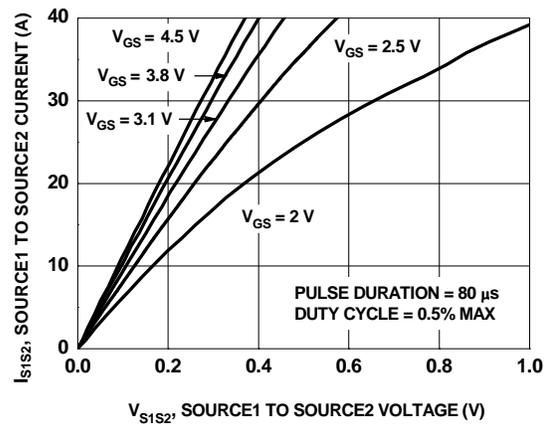

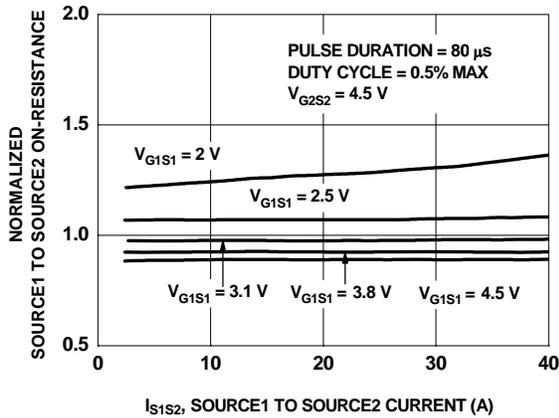**Figure 2. On-Region Characteristics**

Figure 3. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage
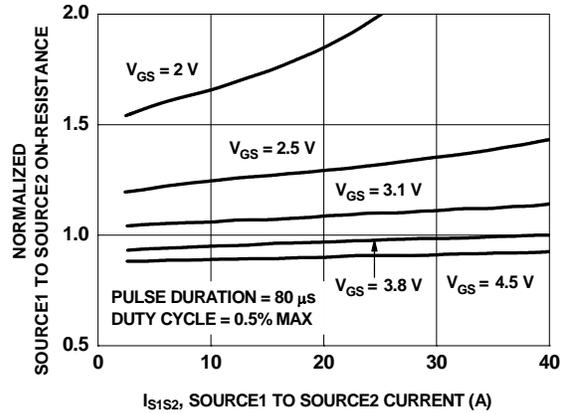

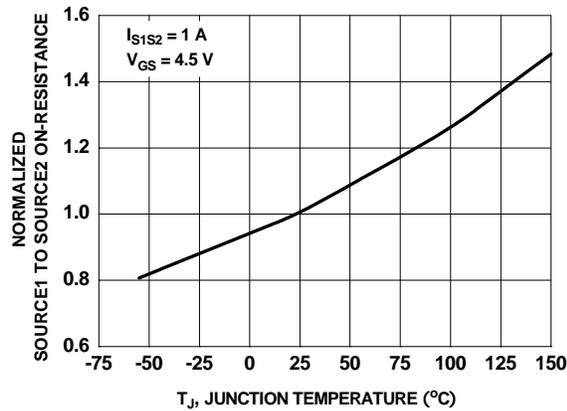**Figure 4. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage**
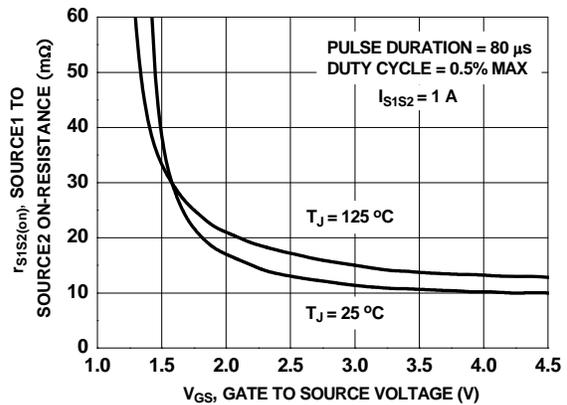

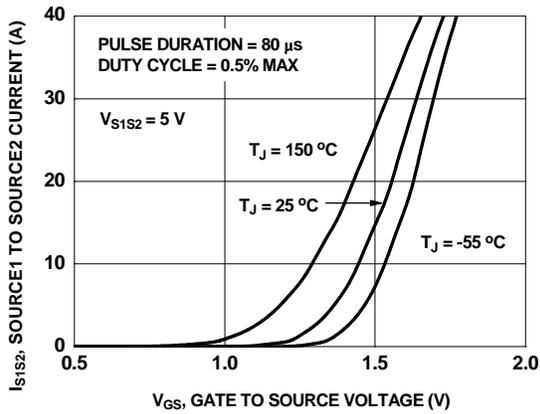**Figure 5. Normalized On Resistance vs Junction Temperature**

Figure 6. On Resistance vs Gate to Source Voltage

Typical Characteristics T_J = 25°C unless otherwise noted

Figure 7. Transfer Characteristics
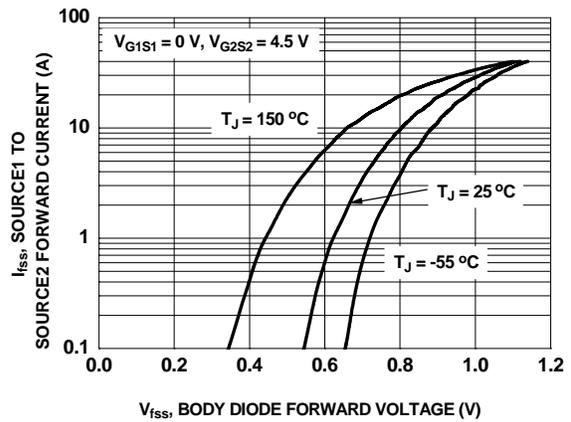
Figure 8. Source1 to Source2 Diode Forward Voltage vs Source Current
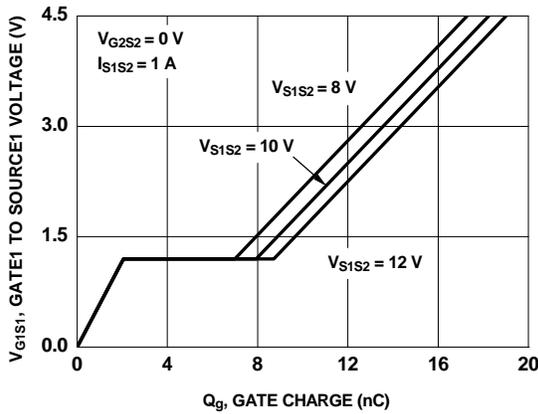
Figure 9. Gate Charge Characteristics
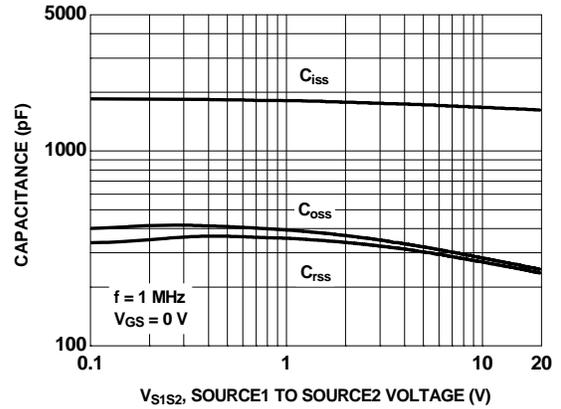
Figure 10. Capacitance vs Source1 to Source2 Voltage
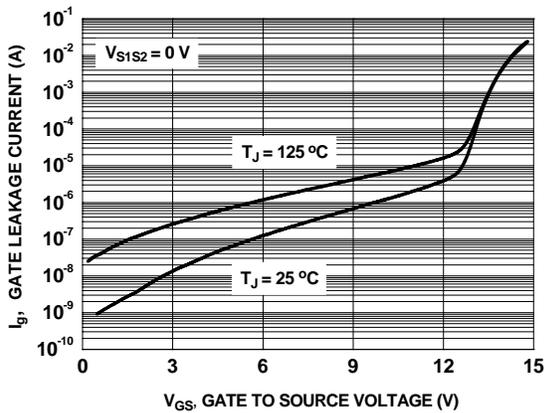
Figure 11. Gate Leakage Current vs Gate to Source Voltage
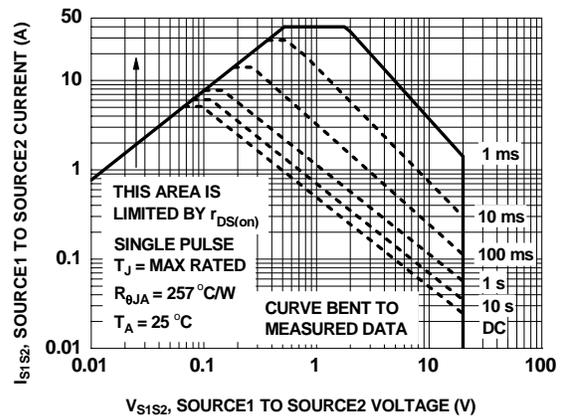
Figure 12. Forward Bias Safe Operating Area

Typical Characteristics T_J = 25°C unless otherwise noted

P$_{(PK)}$, PEAK TRANSIENT POWER (W)

SINGLE PULSE
$R_{\theta JA}$ = 257 °C/W
T_A = 25 °C

t, PULSE WIDTH (sec)
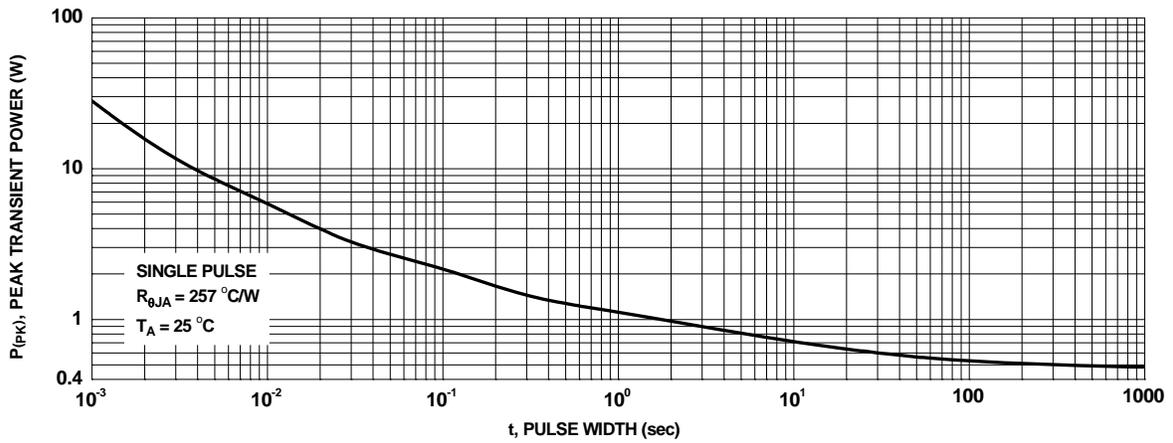
Figure 13. Single Pulse Maximum Power Dissipation

NORMALIZED THERMAL IMPEDANCE, $Z_{\theta JA}$

DUTY CYCLE-DESCENDING ORDER

D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE
$R_{\theta JA}$ = 257 °C/W
(Note 1b)

P_{DM}

t_1

t_2

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK T_J = P_{DM} x $Z_{\theta JA}$ x $R_{\theta JA}$ + T_A

t, RECTANGULAR PULSE DURATION (sec)
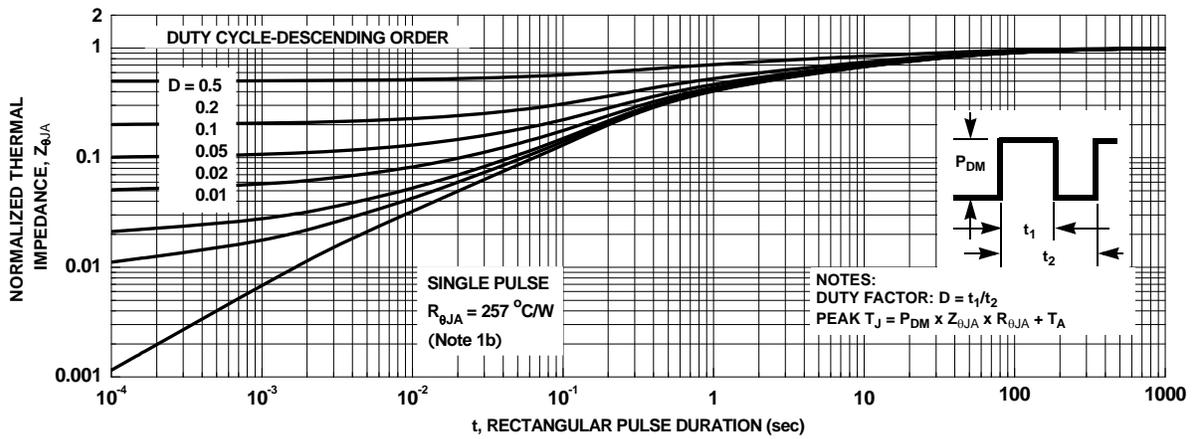
Figure 14. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout

TOP VIEW

0.03 C
2X
E ±0.05
C
D ±0.05
PIN A1 INDEX AREA
A
1   2

LAND PATTERN RECOMMENDATION

0.65
Ø0.250
C
0.65
B
1.30
A
1   2

0.05 C
// 0.06 C
0.350 MAX
C
SEATING PLANE

0.150 +0.015 -0.025
0.160±0.025

⊕ Ø0.005 M C A B
SOLDER BALL
0.300±0.025 (6X)
0.65
1   2
A
B
E
C
Y±0.020
0.65
E
X±0.020

BOTTOM VIEW
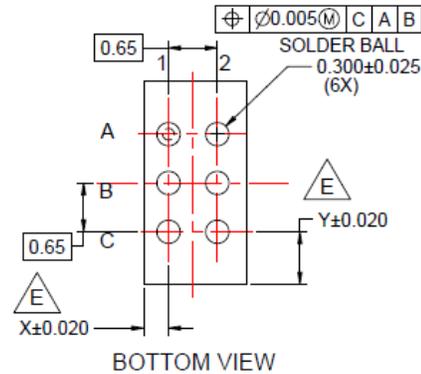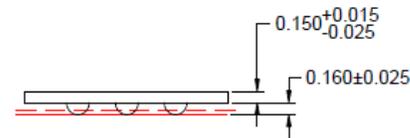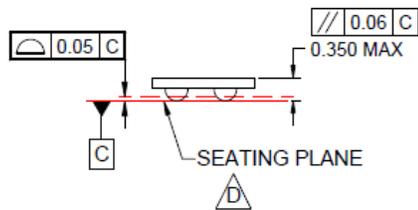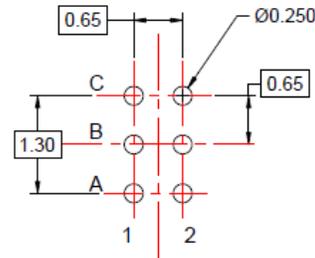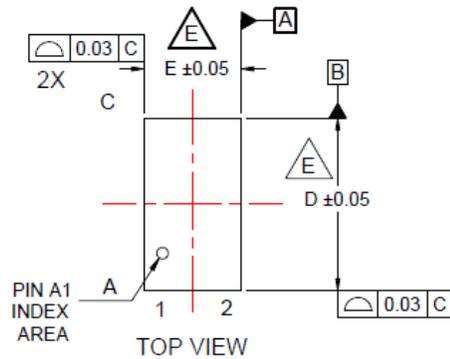
NOTES:
A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 2009.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. FOR DIMENSIONS D,E,X, AND Y SEE PRODUCT DATA SHEET.
F. MKT-UC006ABREV2
G. FOR PIN-OUT ASSIGNMENT, REFER TO DATA SHEET.

FAIRCHILD.

Pin Definations:

Gate	Source1	Source2
B1, B2	A1, C1	A2, C2

Product Specific Dimensions:

D	E	X	Y
2.3 mm	1.3 mm	0.315 mm	0.49 mm

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/package/packageDetails.html?id=PN_UCBEA-006

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
Awinda®
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficentMax™
ESBC™

F®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™

F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
Marking Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
MotionGrid®
MTi®
MTx®
MVN®
mWSaver®
OptoHiT™

®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™

™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™

SYSTEM GENERAL ®*
TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
µSerDes™

µSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™
Xsens™
仙童 ™

*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I71