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FDZ197PZ

P-Channel 1.5 V Specified PowerTrench[®] Thin WL-CSP MOSFET -20 V, -3.8 A, 64 mΩ

Features

- Max $r_{DS(on)}$ = 64 mΩ at $V_{GS} = -4.5$ V, $I_D = -2.0$ A
- Max $r_{DS(on)}$ = 71 mΩ at $V_{GS} = -2.5$ V, $I_D = -2.0$ A
- Max $r_{DS(on)}$ = 79 mΩ at $V_{GS} = -1.8$ V, $I_D = -1.0$ A
- Max $r_{DS(on)}$ = 95 mΩ at $V_{GS} = -1.5$ V, $I_D = -1.0$ A
- Occupies only 1.5 mm² of PCB area. Less than 50% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.65 mm height when mounted to PCB
- HBM ESD protection level > 4400V (Note3)
- RoHS Compliant

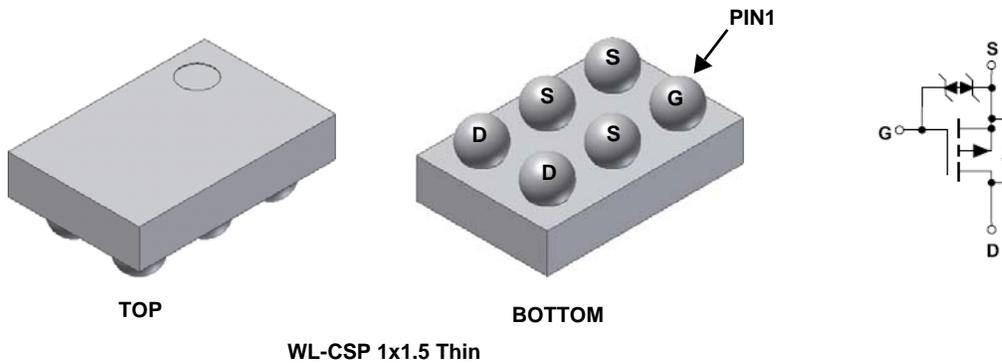


General Description

Designed on Fairchild's advanced 1.5 V PowerTrench[®] process with state of the art "fine pitch" WLCSP packaging process, the FDZ197PZ minimizes both PCB space and $r_{DS(on)}$. This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low $r_{DS(on)}$.

Applications

- Battery management
- Load switch
- Battery protection



WL-CSP 1x1.5 Thin

MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	-3.8
	-Pulsed		-15
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	1.9
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1b)	0.9
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	65	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	133	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
7	FDZ197PZ	WL-CSP 1x1.5 Thin	7"	8 mm	5000 units

FDZ197PZ P-Channel 1.5 V Specified PowerTrench[®] Thin WL-CSP MOSFET

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-10		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\text{ }\mu\text{A}$	-0.4	-0.5	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		2.7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\text{ V}$, $I_D = -2.0\text{ A}$		46	64	m Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -2.0\text{ A}$		53	71	
		$V_{GS} = -1.8\text{ V}$, $I_D = -1.0\text{ A}$		59	79	
		$V_{GS} = -1.5\text{ V}$, $I_D = -1.0\text{ A}$		68	95	
		$V_{GS} = -4.5\text{ V}$, $I_D = -2.0\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		54	84	
g_{FS}	Forward Transconductance	$V_{DD} = -5\text{ V}$, $I_D = -3.8\text{ A}$		21		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		1180	1570	pF
C_{oss}	Output Capacitance			190	255	pF
C_{rss}	Reverse Transfer Capacitance			160	225	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{ V}$, $I_D = -3.8\text{ A}$, $V_{GS} = -4.5\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		5.8	12	ns
t_r	Rise Time			5.9	12	ns
$t_{d(off)}$	Turn-Off Delay Time			311	498	ns
t_f	Fall Time			280	448	ns
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V}$ to -4.5 V		18	25
Q_{gs}	Gate to Source Charge	$V_{DD} = -10\text{ V}$, $I_D = -3.8\text{ A}$		1.5		nC
Q_{gd}	Gate to Drain "Miller" Charge			4.7		nC

Drain-Source Diode Characteristics

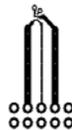
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = -1.1\text{ A}$ (Note 2)		-0.6	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -3.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		194	310	ns
Q_{rr}	Reverse Recovery Charge			344	550	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $65\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $133\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

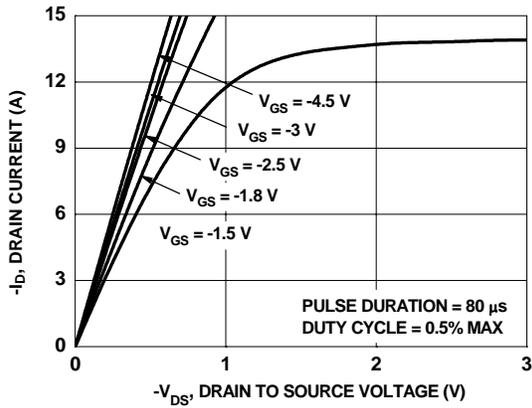


Figure 1. On-Region Characteristics

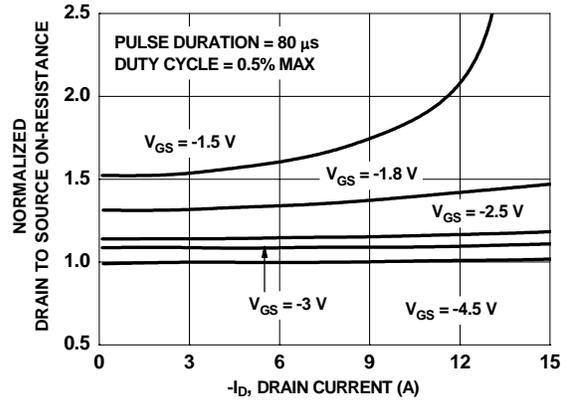


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

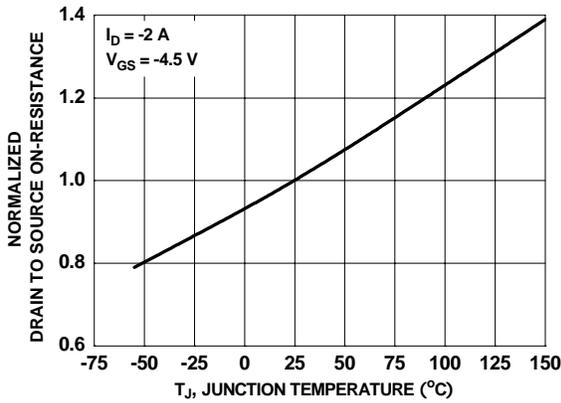


Figure 3. Normalized On-Resistance vs Junction Temperature

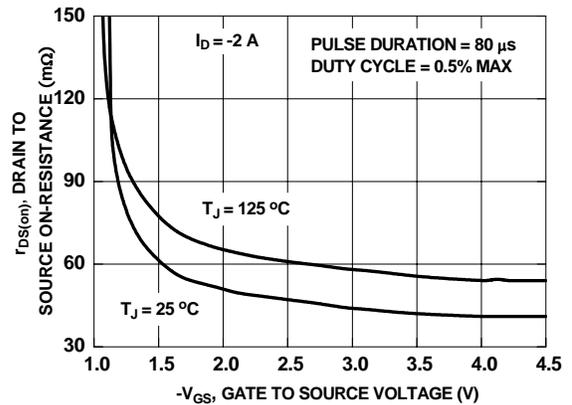


Figure 4. On-Resistance vs Gate to Source Voltage

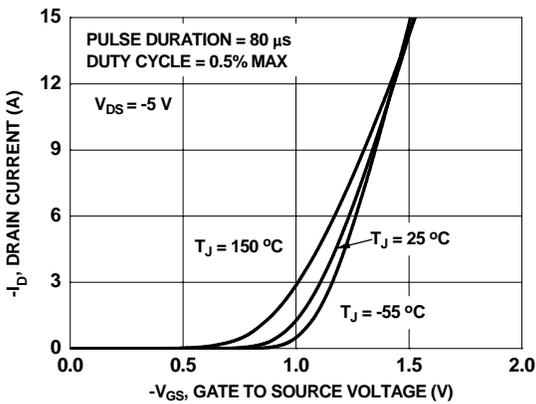


Figure 5. Transfer Characteristics

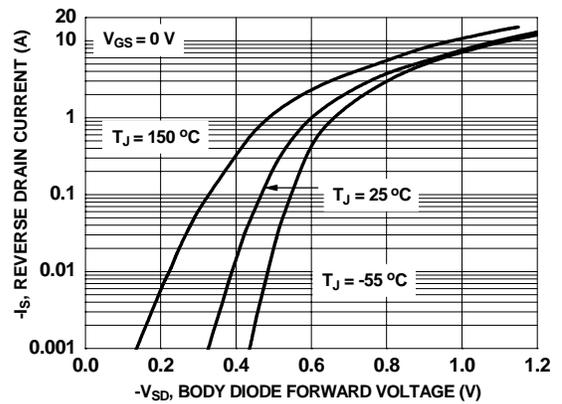


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

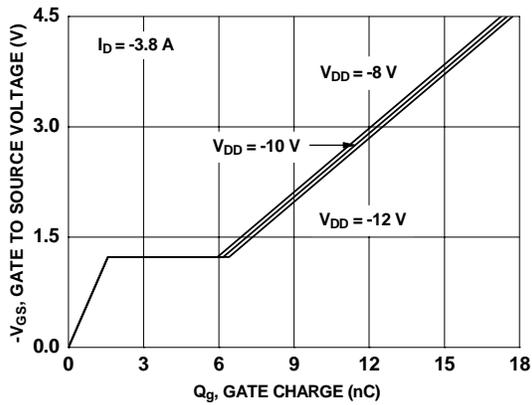


Figure 7. Gate Charge Characteristics

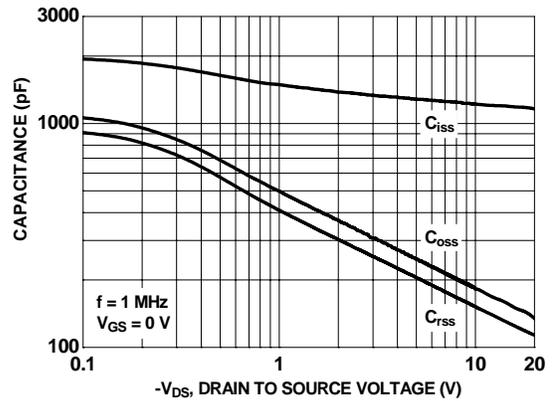


Figure 8. Capacitance vs Drain to Source Voltage

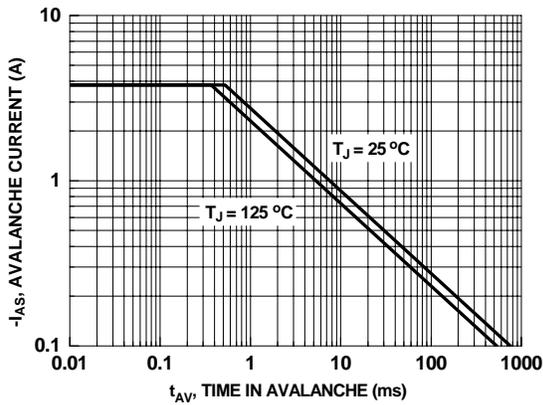


Figure 9. Unclamped Inductive Switching Capability

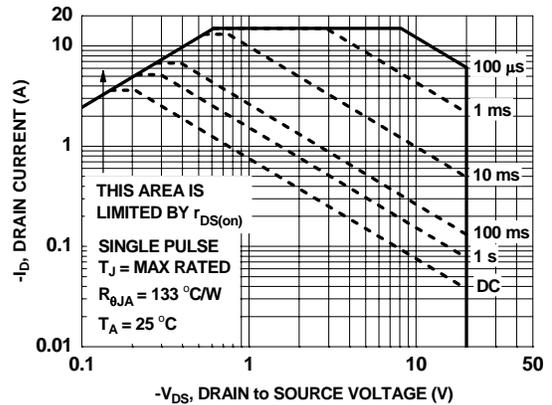


Figure 10. Forward Bias Safe Operating Area

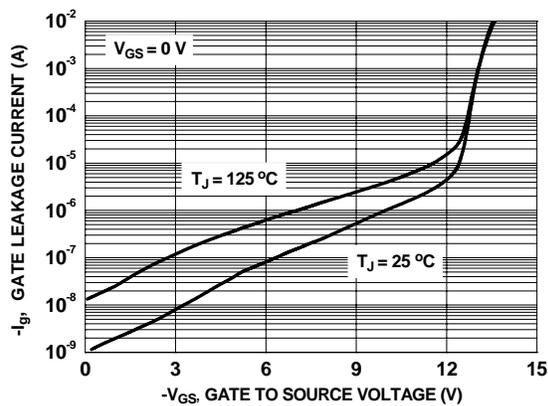


Figure 11. Gate Leakage Current vs Gate to Source Voltage

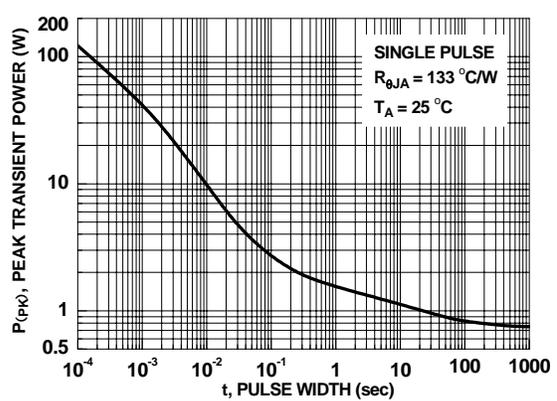


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

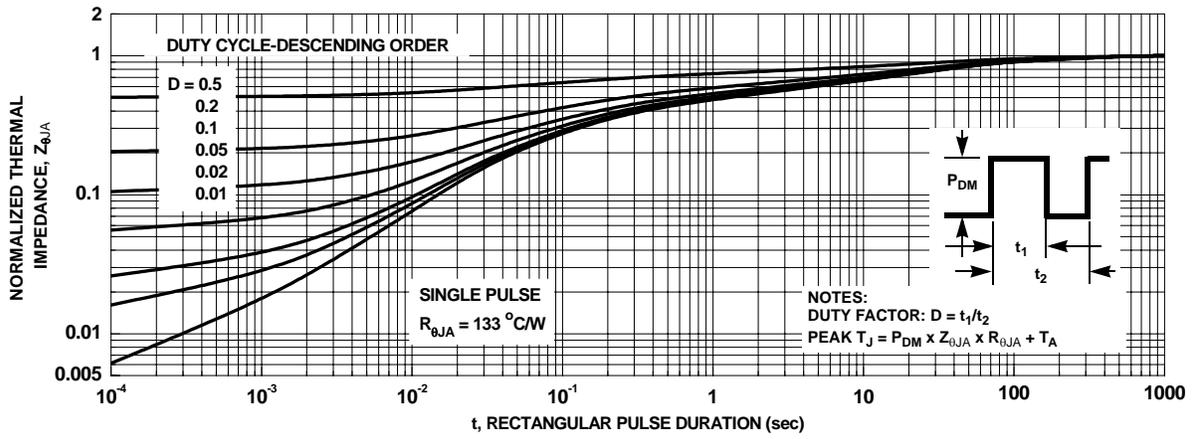
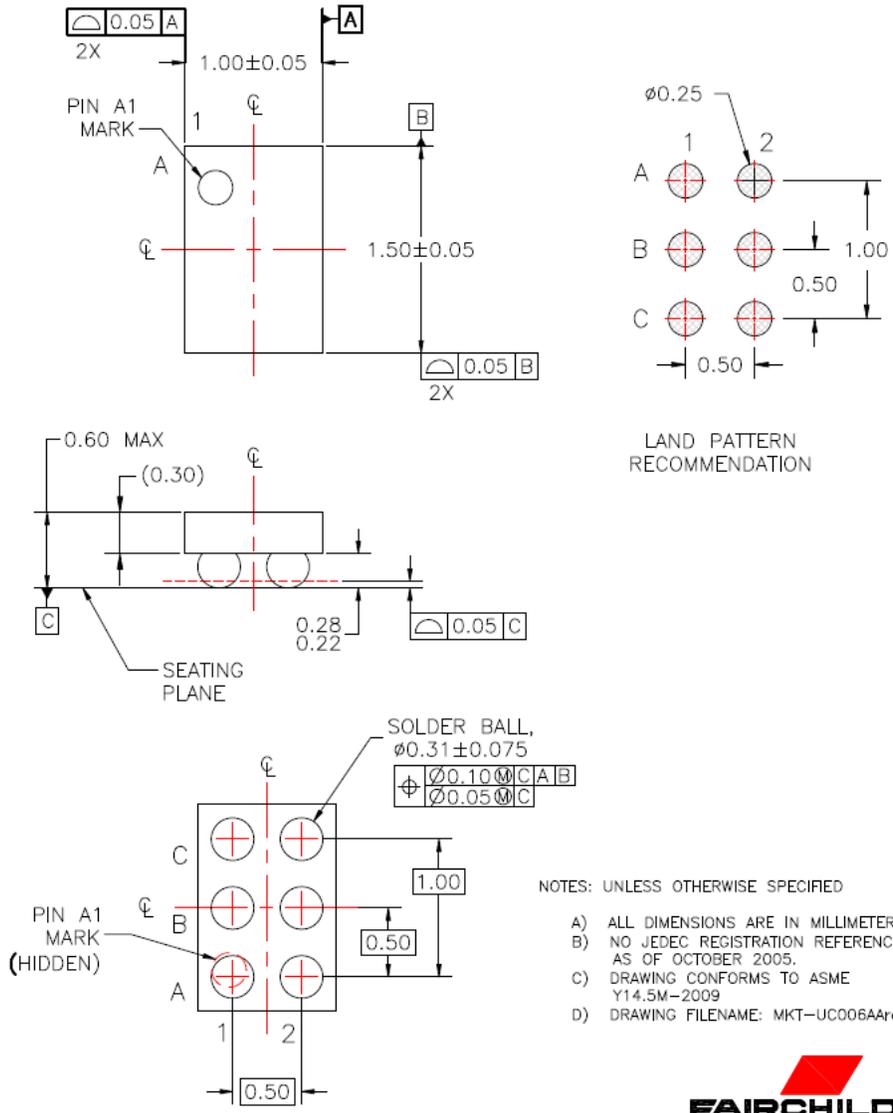


Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout



Pin Definations:

Gate	Drain	Source
A1	C1, C2	A2, B1, B2

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